



# High Speed CMOS 8-Bit Universal Shift Register

QS54/74FCT299T

## FEATURES/BENEFITS

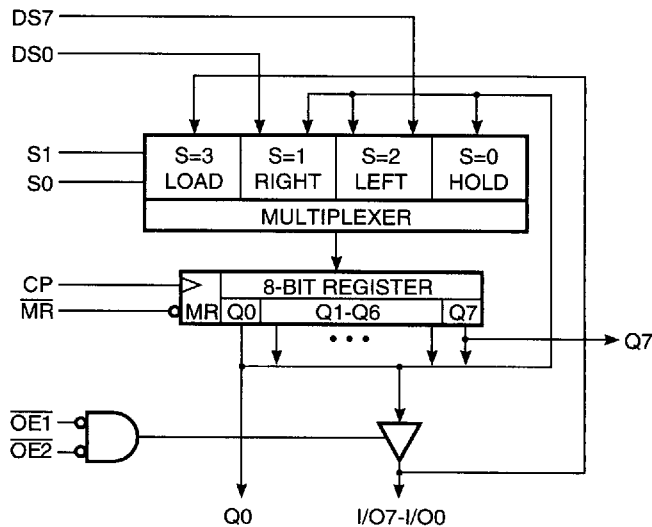
- Pin and function compatible to the 74F299, 74FCT299 and 74ALS299
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883
- I<sub>OL</sub> = 48 mA Com., 32 mA Mil.
- Standard and A speed grades with 7.2 ns t<sub>PD</sub> for A

## DESCRIPTION

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The QSFCT299T is a high-speed CMOS 8-bit universal shift register. The contents of the 8-bit register may be loaded from a bus, shifted left or right, or gated to the bus. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

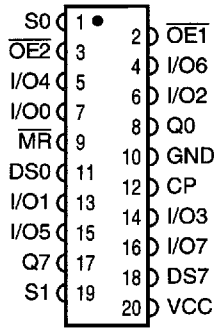
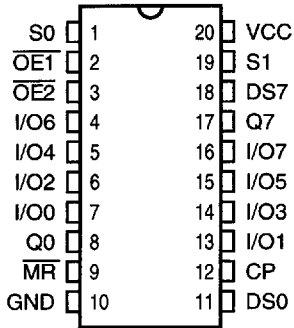
## FUNCTIONAL BLOCK DIAGRAM



**PIN CONFIGURATIONS (All Pins Top View)**

DIP, SOIC, QSOP, HQSOP

ZIP



**PIN DESCRIPTION**

Name	I/O	Description
I/O7-I/O0	I/O	Data I/O Bus
S1, S0	I	Function Select
CP	I	Clock
Q7, Q0	O	Shift Out
DS7, DS0	I	Shift In
OE1, OE2	I	Output Enables
MR	I	Master Reset

**FUNCTION TABLE**

Inputs				Outputs			Function
MR	S1	S0	CP	Q7	Q6-Q1	Q0	
L	X	X	X	L	LLLLLL	L	Reset
H	L	L	↑	Q7	Q6-Q1	Q0	Hold Data
H	L	H	↑	DS7	Q7-Q2	Q1	Shift Right
H	H	L	↑	Q6	Q5-Q0	DS0	Shift Left
H	H	H	↑	I/O7	I/O6-1	I/O0	Load

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-3, 9, 11, 12, 18, 19	4	4	5	7	pF
8, 17	6	6	7	9	pF
4-7, 13-16	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0$ <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

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**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5.0V ± 5%

Military T<sub>A</sub> = -55°C to 125°C, V<sub>CC</sub> = 5.0V ± 10%

C<sub>LOAD</sub> = 50 pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Description <sup>(1)</sup>		299		299A		Unit
			Min	Max	Min	Max	
t <sub>CPQ</sub>	Propagation Delay CP to Q <sub>i</sub>	COM	2	10	2	7.2	ns
		MIL	2	14	2	9.5	
t <sub>CPi</sub>	Propagation Delay CP to I/O	COM	2	12	2	7.2	ns
		MIL	2	12	2	9.5	
t <sub>MRQ</sub>	Propagation Delay $\overline{MR}$ to Q <sub>i</sub>	COM	2	10	2	7.2	ns
		MIL	2	10.5	2	9.5	
t <sub>MRI</sub>	Propagation Delay $\overline{MR}$ to I/O	COM	2	15	2	8.7	ns
		MIL	2	15	2	11.5	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to I/O	COM	1.5	11	1.5	6.5	ns
		MIL	1.5	15	1.5	7.5	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to I/O	COM <sup>(2)</sup>	1.5	7	1.5	5.5	ns
		MIL <sup>(2)</sup>	1.5	9	1.5	6.5	
t <sub>S0,1</sub>	Setup Time S <sub>0</sub> , S <sub>1</sub> to CP	COM	7.5		3.5		ns
		MIL	7.5		4.0		
t <sub>H0,1</sub>	Hold Time S <sub>0</sub> , S <sub>1</sub> to CP	COM	1		1		ns
		MIL	1		1		
t <sub>S</sub>	Setup Time I/O or DS <sub>n</sub> to CP	COM	5.5		4.0		ns
		MIL	5.5		4.5		
t <sub>H</sub>	Hold Time I/O or DS <sub>n</sub> to CP	COM	1.5		1.5		ns
		MIL	1.5		1.5		
t <sub>WCP</sub>	CP Pulse Width HIGH or LOW	COM <sup>(2)</sup>	7		5		ns
		MIL <sup>(2)</sup>	7		6		
t <sub>WMR</sub>	$\overline{MR}$ Pulse Width LOW	COM <sup>(2)</sup>	7		5		ns
		MIL <sup>(2)</sup>	7		6		
t <sub>REM</sub>	Recovery Time $\overline{MR}$ to CP	COM	7		5		ns
		MIL	7		6		

**Notes:**

1. Minimums guaranteed but not tested. For all parameters except t<sub>S</sub>, t<sub>H</sub>, and t<sub>REM</sub>.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

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