1.1 Scope.

This specification covers the detail requirements for an octal CMOS digital-to-analog converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD7228T(X)/883B
−2	AD7228U(X)/883B

NOTE
[1]To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3" Width
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... −0.3 V to +17 V
V_{DD} to V_{SS} ..... +0.3 V to +24 V
Digital Input Voltage ..... −0.3 V, V_{DD}
V_{REF} to GND ..... −0.3 V, V_{DD}
V_{OUT} to GND[1] ..... V_{SS}, V_{DD}
Power Dissipation
  Up to +75°C ..... 1000 mW
  Derates above +75°C ..... 2.0 mW/°C
Operating Temperature Range ..... −55°C to +125°C
Thermal Resistance (θ_{JC}):
  Case 1 (Q-24) ..... See MIL-M-38510, Appendix C
  Case 3 (E-28A) ..... See MIL-M-38510, Appendix C
Storage Temperature ..... −65°C to +125°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C

NOTE
[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit for a short to V_{SS} is 50 mA.

AD7228—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Min	Design Max	Sub Group	Test Condition[1]	Units
Total Unadjusted Error[2]	TUE	−1, 2	−2	+2	1	V_{DD} = 15 V ±10%, V_{REF} = +10 V (Single Supply Only)	LSB
		−1	−2	+2	2, 3		
		−2	−1	+1	2, 3		
		−2	−1	+1	4		
Total Unadjusted Error	TUE	−1	−2	+2	13, 14, 15	Dual Supply Only	LSB
		−2	−1	+1			
Relative Accuracy	RA	−1, 2	−1	+1	1		LSB
		−1	−1	+1	2, 3		
		−2	−0.5	+0.5	2, 3		
		−2	−0.5	+0.5	12		
Differential Nonlinearity	DNL	−1, 2	−1	+1	1, 2, 3	Guaranteed Monotonic (Single Supply Only)	LSB
Differential Nonlinearity	DNL	−1, 2	−1	+1	13, 14, 15	Dual Supply Only	LSB
Full-Scale Error[3]	A_E	−1, 2	−1	+1	1		mV
		−1	−1	+1	2, 3		
		−2	−0.5	+0.5	2, 3		
		−2	−0.5	+0.5	12		
Zero Code Error	A_{ZCE}	−1, 2	−25	+25	1		mV
		−1	−30	+30	2, 3		
		−2	−20	+20	2, 3		
		−2	−15	+15	12		
Load Resistance	R_L	−1, 2	2		1, 2, 3	V_{OUT} = ±10 V (Dual Supply & Single Supply)	kΩ
Reference Input Voltage Range	V_{REF}	−1, 2	2	10	1, 2, 3		V
Reference Input Resistance	R_{IN}	−1, 2	2		1, 2, 3	Dual Supply Only	kΩ
Reference Input Capacitance[4]	C_{IN} (REF)	−1, 2		500	13, 14, 15	Dual and Single Supply	pF
Digital Input High Voltage	V_{INH}	−1, 2	2.4		1, 2, 3	Dual Supply Only	V
Digital Input Low Voltage	V_{INL}	−1, 2		0.8	1, 2, 3	Input Coding Is Binary	V
Digital Input Leakage Current	I_{ILC}	−1, 2	−1	+1	1, 2, 3		μA
Digital Input Capacitance	C_{IN}	−1, 2		8	13, 14, 15		pF
Voltage Output Slew Rate	SR	−1, 2	2		13, 14, 15	Dual and Single Supply	V/μs
Voltage Output Settling Time[5] Positive Full-Scale Change	t_{SL}	−1, 2		5	13, 14, 15	Dual and Single Supply	μs
Negative Full-Scale Change		−1, 2		5		Dual Supply	
				7		Single Supply	
Power Supply Current	I_{DD}	−1, 2		16	1	Dual Supply Only	mA
				22	2, 3		
	I_{SS}	−1, 2		14	1		
				20	2, 3		
Function Tests[6]		−1, 2			7		
Address to $\overline{WR}$ Setup Time	t_1	−1, 2	0		9, 10, 11	Dual and Single Supply See Figure 2 and Note 7	ns
Address to $\overline{WR}$ Hold Time	t_2	−1, 2	0		9, 10, 11		
Data Valid to $\overline{WR}$ Setup Time	t_3	−1, 2	70		9		
			100		10, 11		
Data Valid to $\overline{WR}$ Hold Time	t_4	−1, 2	10		9, 10, 11		ns

Test	Symbol	Device	Design Min	Design Max	Sub Group	Test Condition[1]	Units
Write Pulse Width	t_5	−1, 2	95		9		ns
			150		10, 11		

NOTES
[1] $-55°C<T_A<+125°C$, Dual Supply unless otherwise specified. R_L = 2k, C_L = 100 pF unless otherwise stated. Parameters in subgroups 13, 14, 15 are characterized at initial design and after any subsequent redesigns.
[2] Includes zero code error, relative accuracy and full-scale error.
[3] Calculated after zero code error has been adjusted out.
[4] Occurs when each DAC is loaded with all 1s.
[5] V_{REF} = +10 V; settling time to ± 1/2 LSB.
[6] Subgroup 7 tests are for the purpose of verifying the truth table.
[7] All input rise and fall times measured from 10% to 90% of +5 V, $t_R = t_F$ = 5 ns.
Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$.

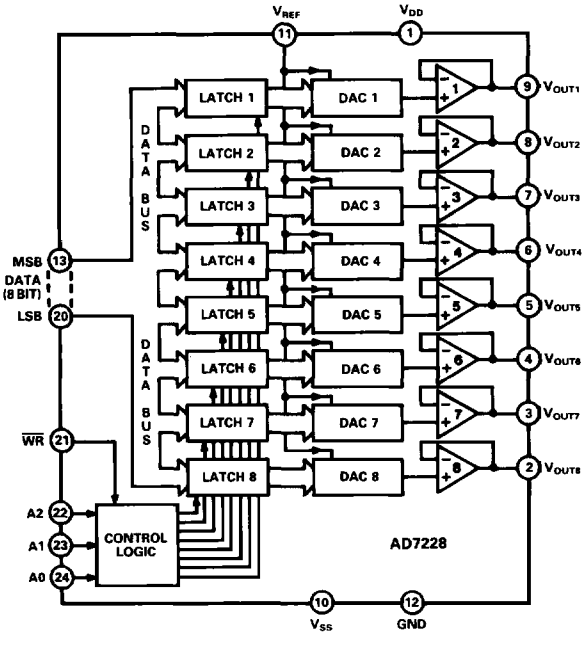
1.3.1 Recommended Operating Conditions.

Operating Voltage Range for Dual Supply
- Positive Supply (V_{DD}) ..... +10.8 V to +16.5 V
- Negative Supply (V_{SS}) ..... −4.5 V to −5.5 V
- Reference Voltage (V_{REF})[1] ..... +2.0 V to +10.0 V

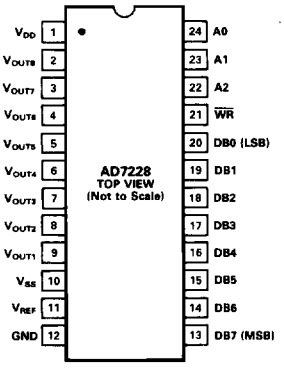
Operating Voltage Range for Single Supply
- Positive Supply (V_{DD}) ..... +13.5 V to +16.5 V
- Negative Supply (V_{SS}) ..... 0 V
- Reference Voltage (V_{REF})[1] ..... +10 V

NOTE
[1] V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.

3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)

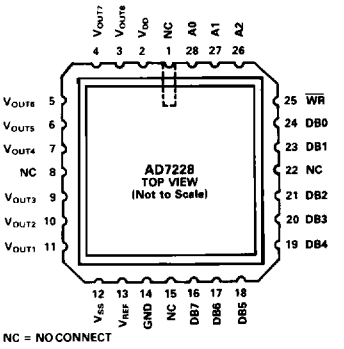


Table 2. Truth Table

AD7228 Control Inputs

$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State L = Low State X = Don't Care

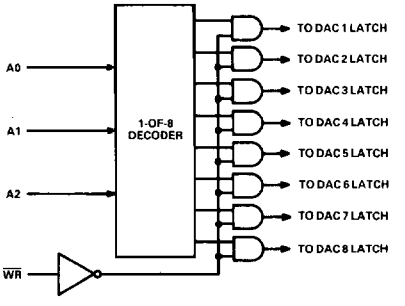
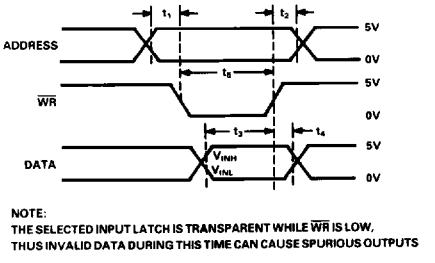


Figure 1. Input Control Logic



NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

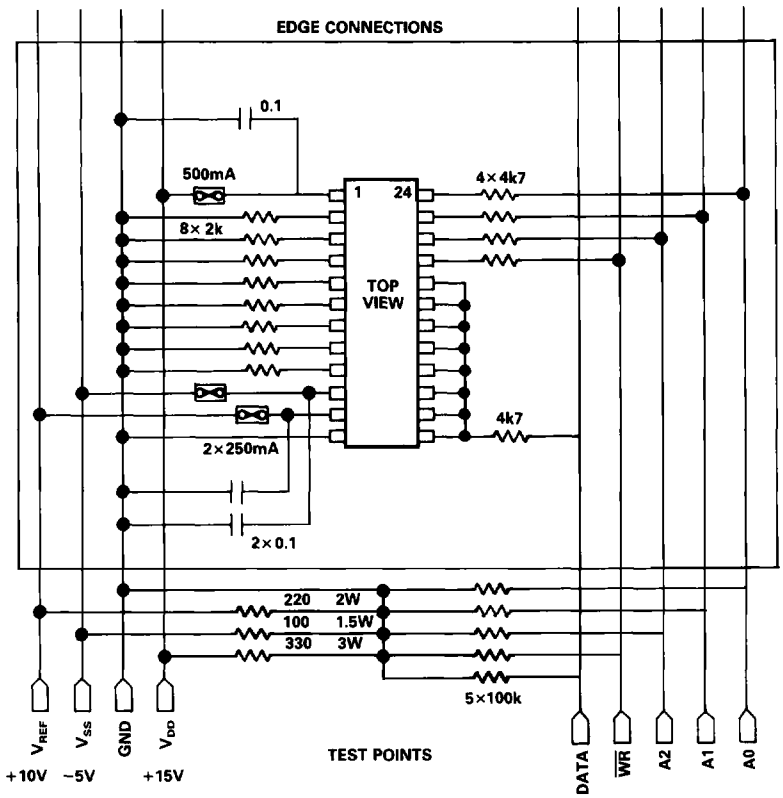
Figure 2. Write Cycle Timing Diagram

3.2.4 Microcircuit Technology Group.

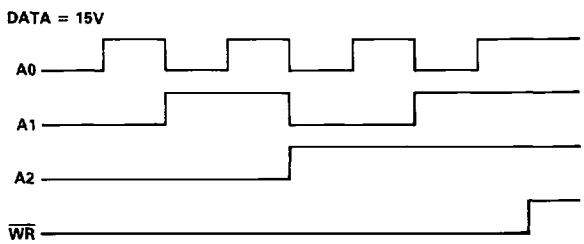
This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



TO INITIALIZE, APPLY THE FOLLOWING WAVEFORMS:
EACH PULSE OF A0 SHOULD BE AT LEAST 50μs.



THIS SEQUENCE ENSURES ALL DACS ARE LOADED.

Burn-In Conditions