

# CSD18511KTT 40-V N-Channel NexFET™ Power MOSFET

## 1 Features

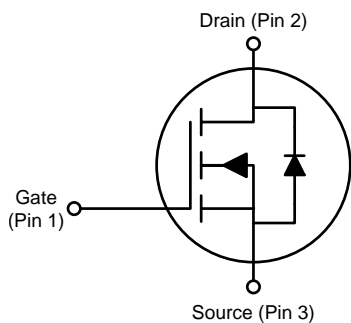
- Low  $Q_g$  and  $Q_{gd}$
- Low  $R_{DS(on)}$
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- D<sup>2</sup>PAK Plastic Package

## 2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

## 3 Description

This 40-V, 2.1-m $\Omega$ , D<sup>2</sup>PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	40		V
$Q_g$	Gate Charge Total (10 V)	63.9		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	9.7		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	3.2	m $\Omega$
		$V_{GS} = 10\text{ V}$	2.1	
$V_{GS(th)}$	Threshold Voltage	1.8		V

## Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18511KTT	500	13-Inch Reel	D <sup>2</sup> PAK Plastic Package	Tape and Reel
CSD18511KTTT	50			

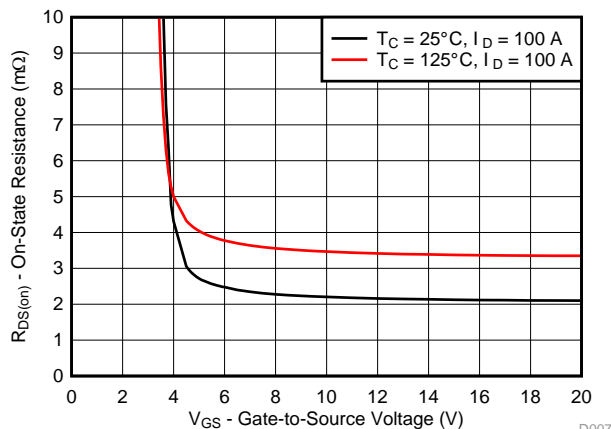
(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package Limited)	110	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	194	
	Continuous Drain Current (Silicon Limited), $T_C = 100^\circ\text{C}$	137	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	400	A
$P_D$	Power Dissipation	188	W
$T_J, T_{stg}$	Operating Junction, Storage Temperature	-55 to 175	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 56\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	156	mJ

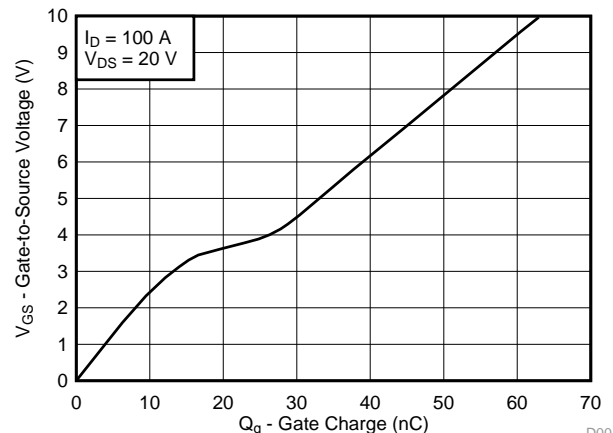
(1) Max  $R_{\theta JC} = 0.8^\circ\text{C}/\text{W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

### $R_{DS(on)}$ vs $V_{GS}$



D007

### Gate Charge



D004



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## 4 Revision History

DATE	REVISION	NOTES
July 2017	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5	1.8	2.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 100\text{ A}$		3.2	4.2	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		2.1	2.6	
$g_{fs}$	Transconductance	$V_{DS} = 4\text{ V}, I_D = 100\text{ A}$		249		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		4570	5940	pF
$C_{oss}$	Output capacitance			454	591	pF
$C_{rss}$	Reverse transfer capacitance			235	306	pF
$R_G$	Series gate resistance		0.9	1.8		$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 20\text{ V}, I_D = 100\text{ A}$		31		nC
$Q_g$	Gate charge total (10 V)			64		nC
$Q_{gd}$	Gate charge gate-to-drain			9.7		nC
$Q_{gs}$	Gate charge gate-to-source			17.9		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			7.4		nC
$Q_{oss}$	Output charge		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		20.7	
$t_{d(on)}$	Turnon delay time	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$		8		ns
$t_r$	Rise time			6		ns
$t_{d(off)}$	Turnoff delay time			17		ns
$t_f$	Fall time			3		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.0	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 20\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		62		nC
$t_{rr}$	Reverse recovery time			31		ns

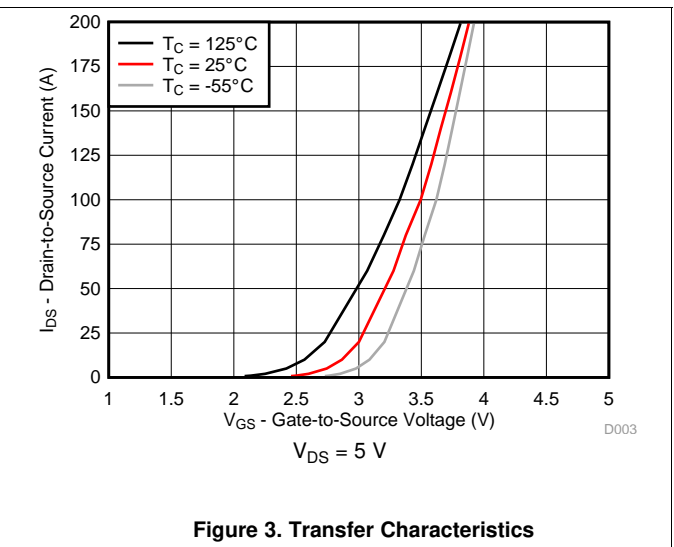
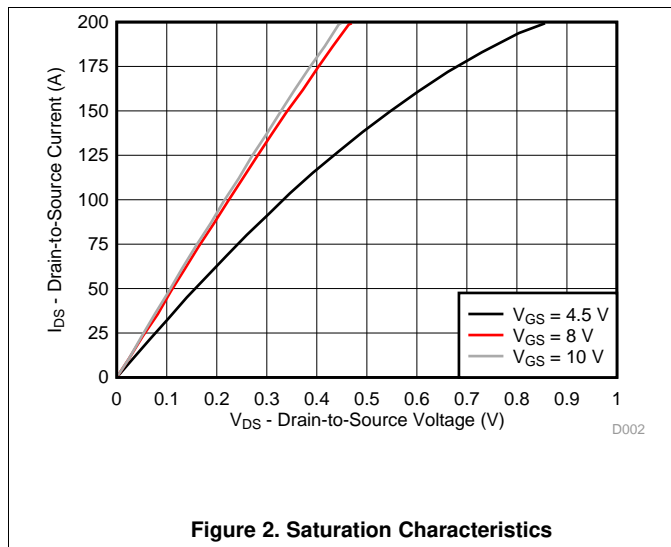
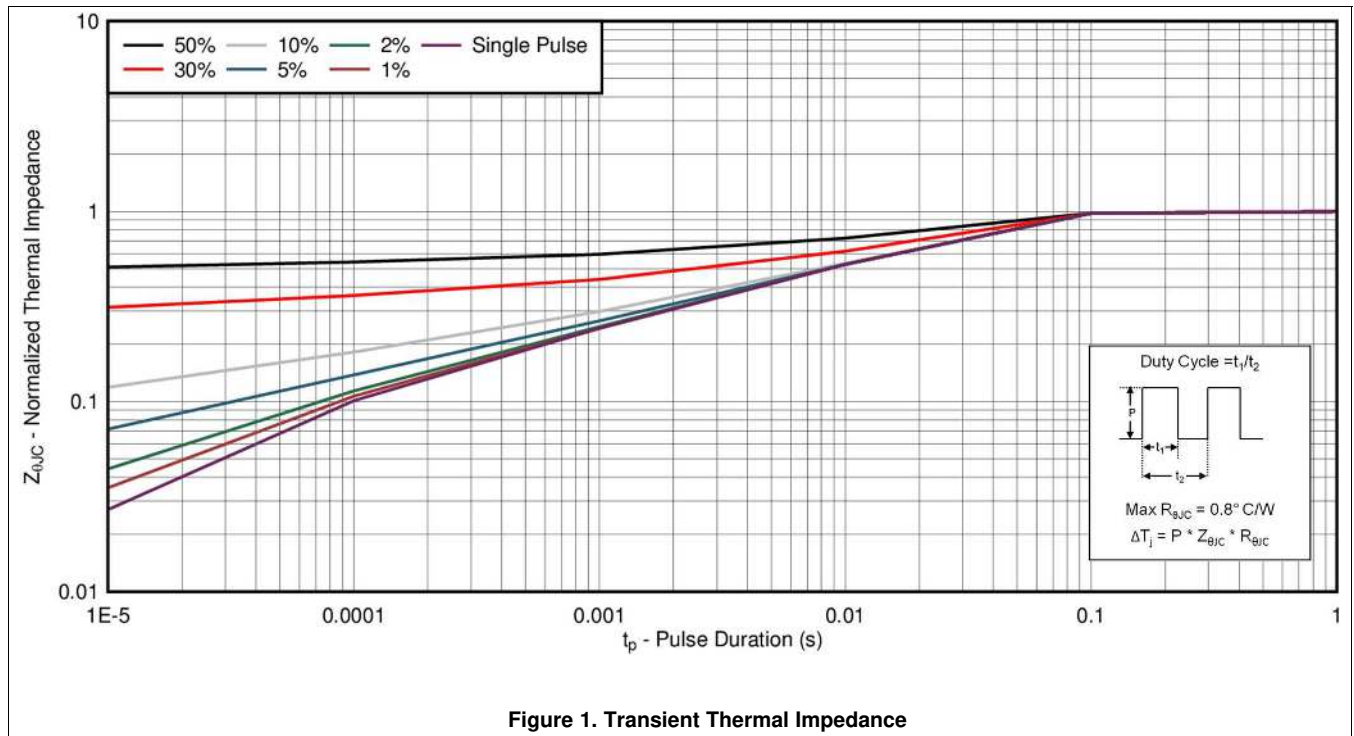
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

### 5.3 Typical MOSFET Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)

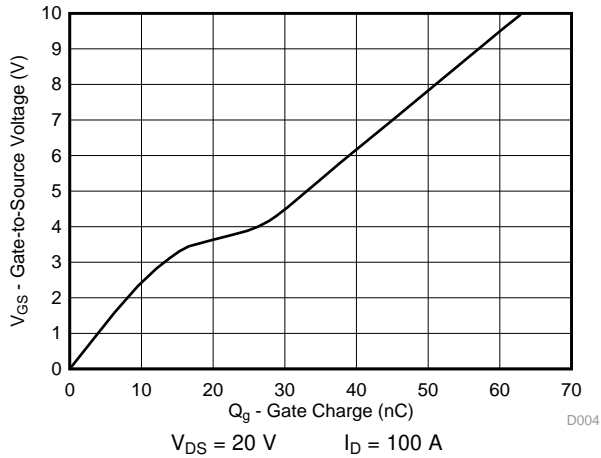


Figure 4. Gate Charge

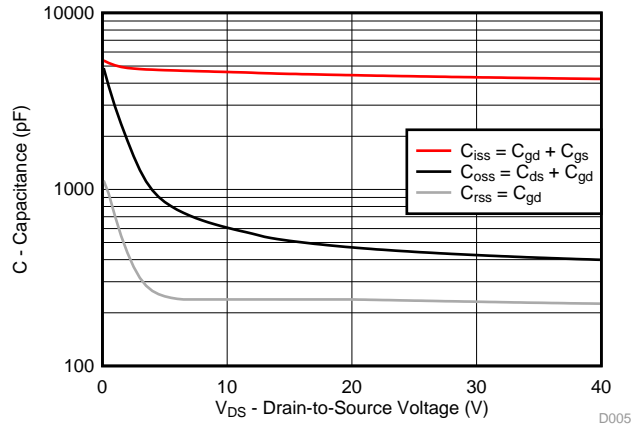


Figure 5. Capacitance

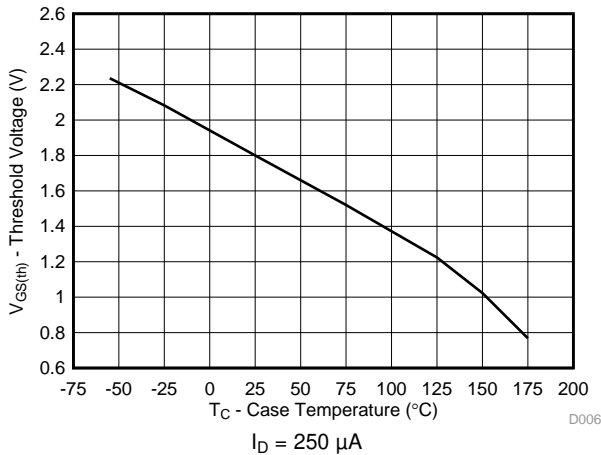


Figure 6. Threshold Voltage vs Temperature

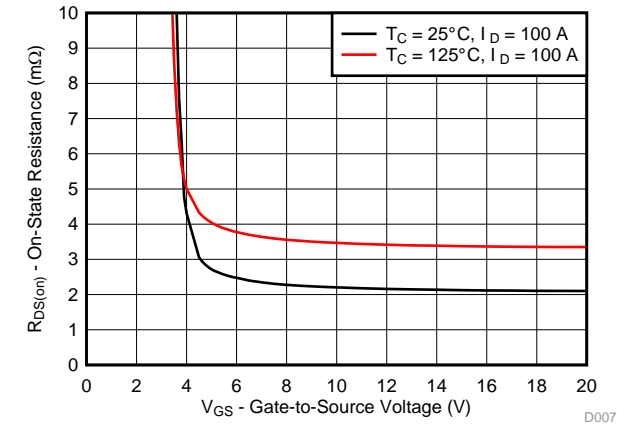


Figure 7. On-State Resistance vs Gate-to-Source Voltage

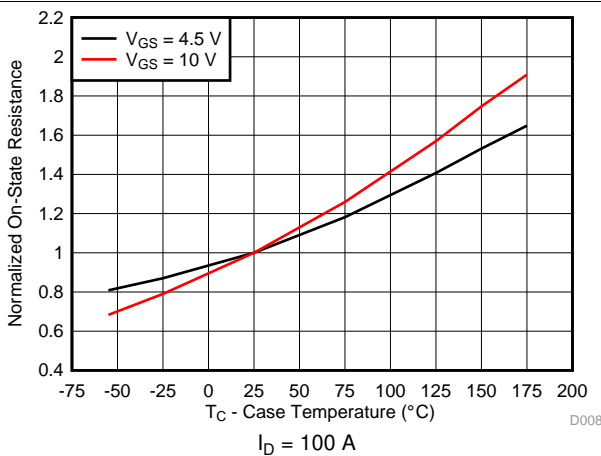


Figure 8. Normalized On-State Resistance vs Temperature

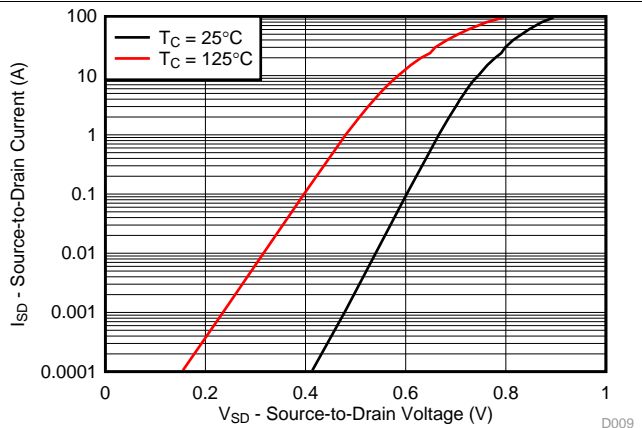
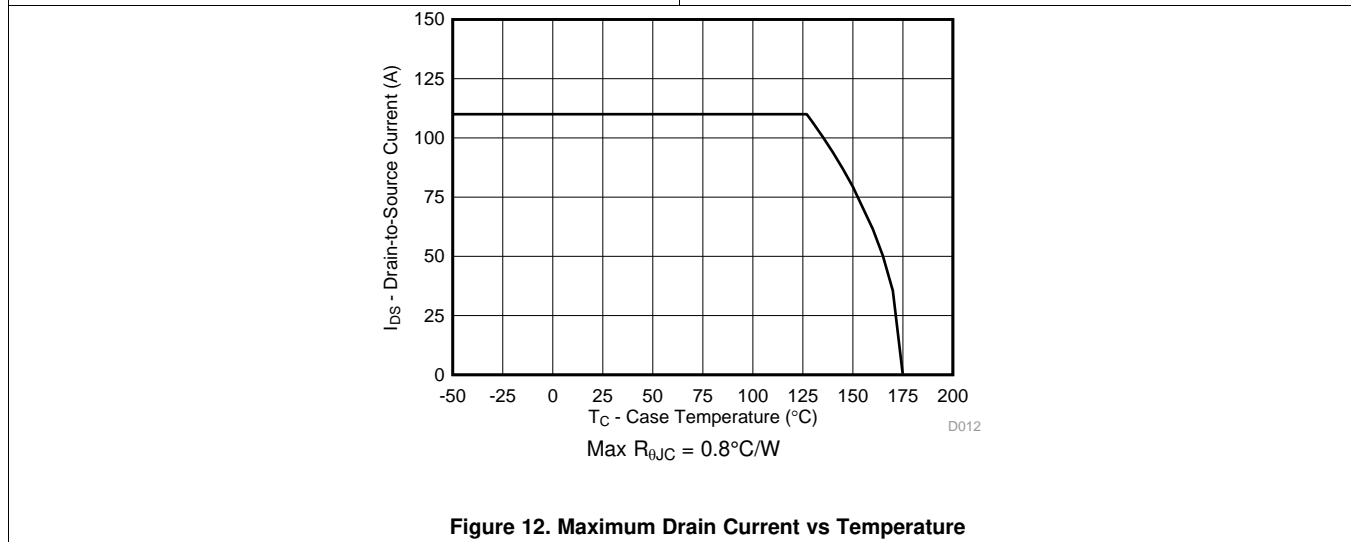
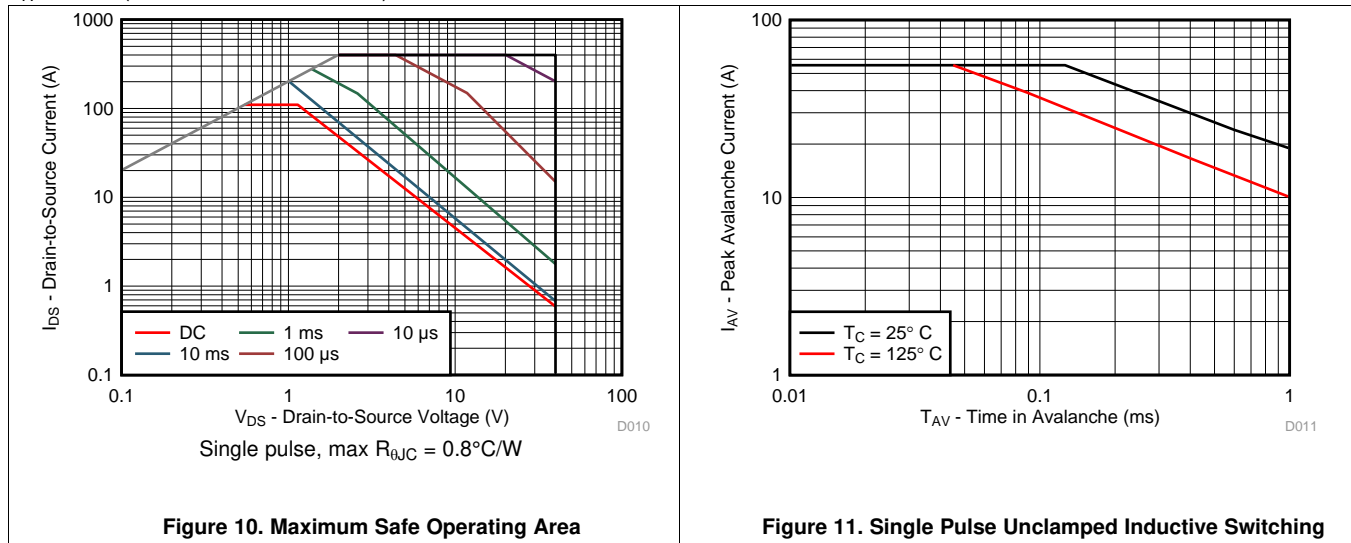


Figure 9. Typical Diode Forward Voltage

**Typical MOSFET Characteristics (continued)**

$T_A = 25^\circ\text{C}$  (unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E, PowerPAD are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

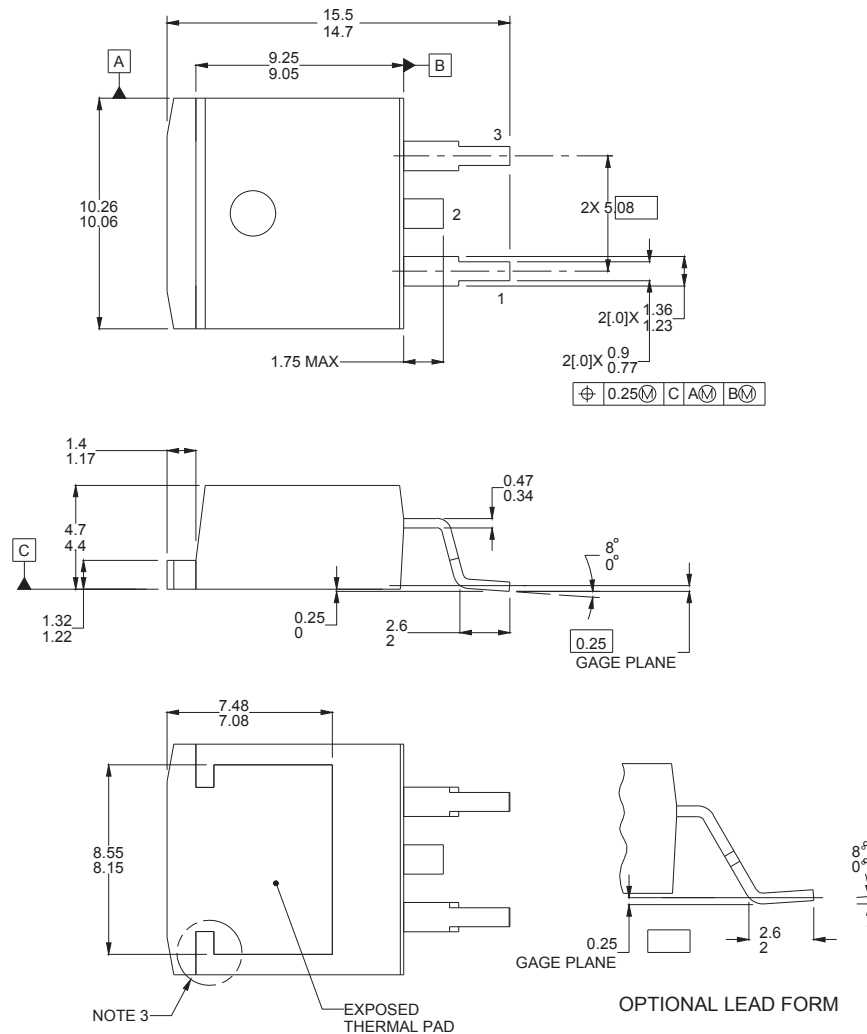
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 KTT Package Dimensions



#### Notes:

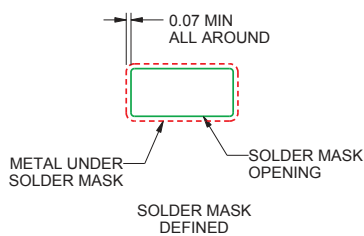
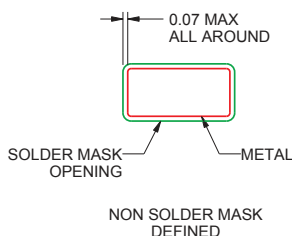
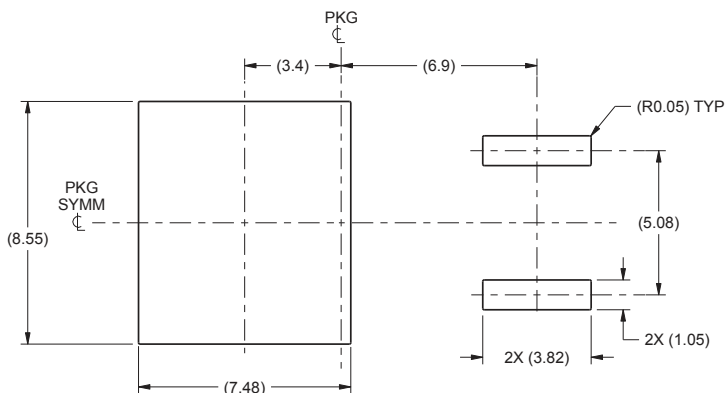
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.

**Table 1. Pin Configuration**

POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

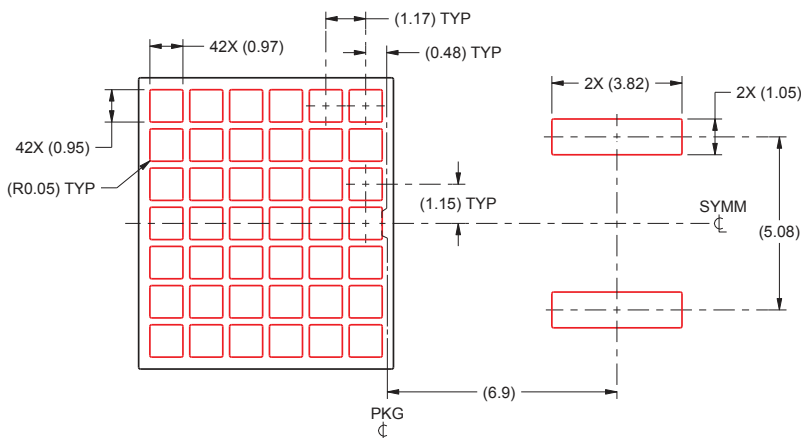


## 7.2 Recommended PCB Pattern



For recommended circuit layout for PCB designs, see [Reducing Ringing Through PCB Layout Techniques \(SLPA005\)](#).

## 7.3 Recommended Stencil Opening (0.125 mm Stencil Thickness)



### Notes:

1. This package is designed to be soldered to a thermal pad on the board. See [PowerPAD™ Thermally Enhanced Package \(SLMA002\)](#) and [PowerPAD™ Made Easy \(SLMA004\)](#) for more information.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
3. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18511KTT	ACTIVE	DDPAK/ TO-263	KTT	2	500	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18511KTT	<a href="#">Samples</a>
CSD18511KTTT	ACTIVE	DDPAK/ TO-263	KTT	2	50	RoHS-Exempt & Green	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18511KTT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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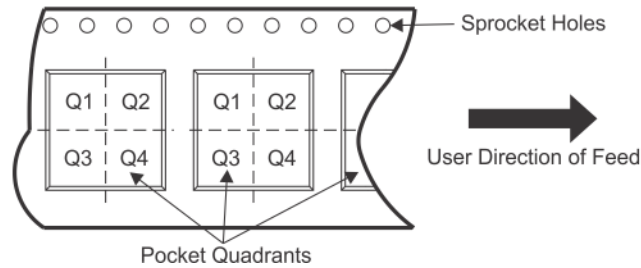
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18511KTT	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD18511KTTT	DDPAK/ TO-263	KTT	3	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

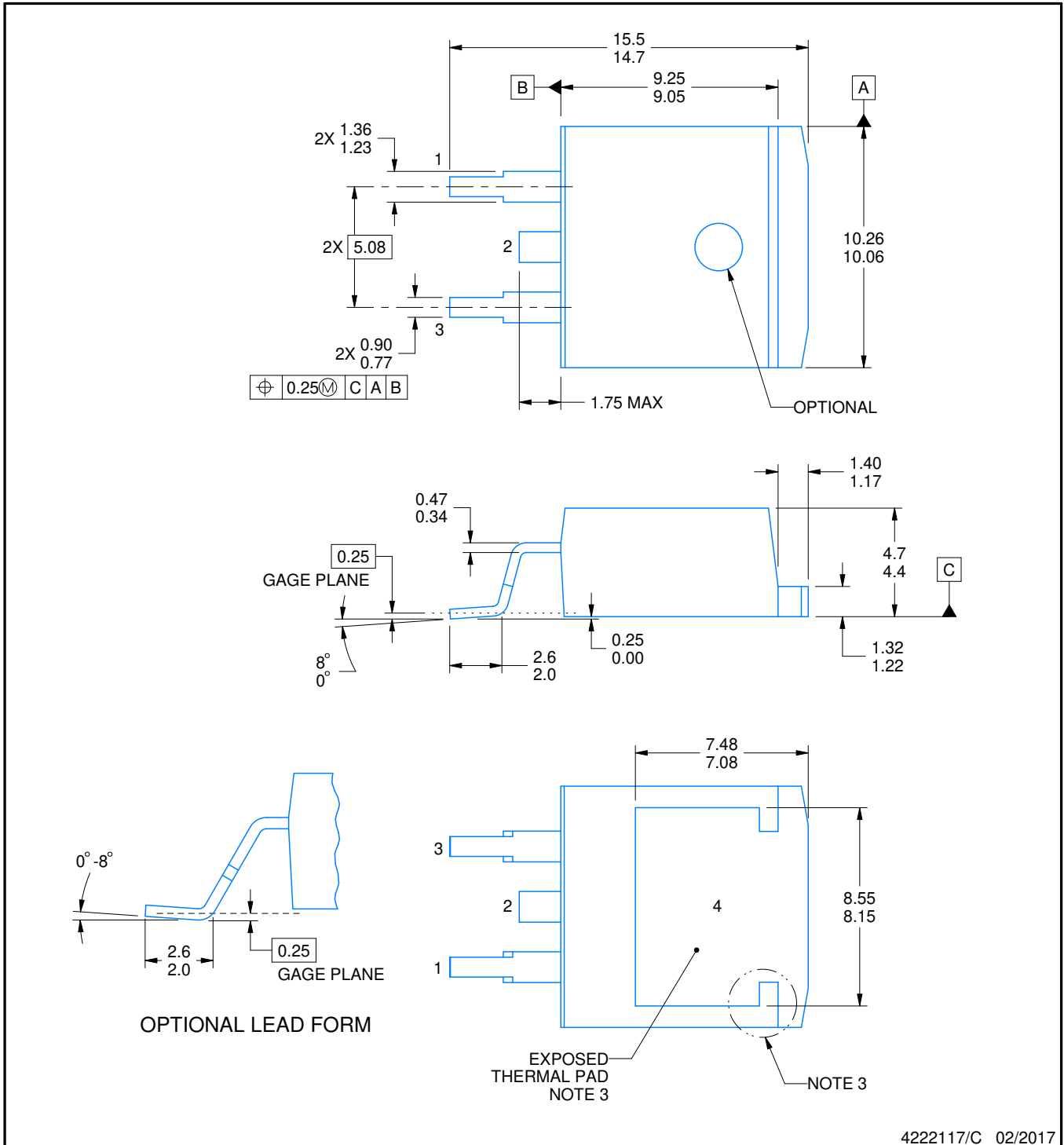
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18511KTT	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
CSD18511KTTT	DDPAK/TO-263	KTT	3	50	340.0	340.0	38.0

KTT0002A



**PACKAGE OUTLINE**  
**TO-263 - 4.7 mm max height**

TO-263



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**NOTES:**

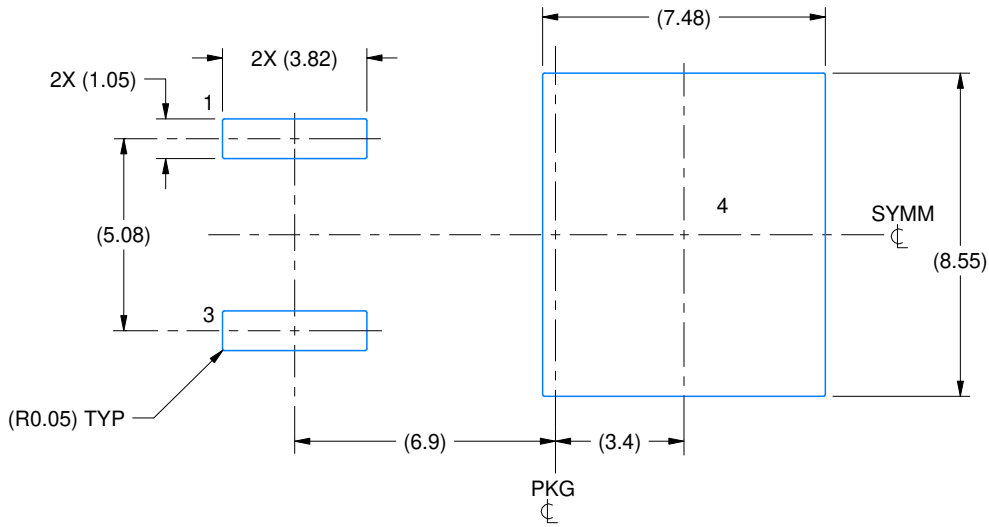
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263.

# EXAMPLE BOARD LAYOUT

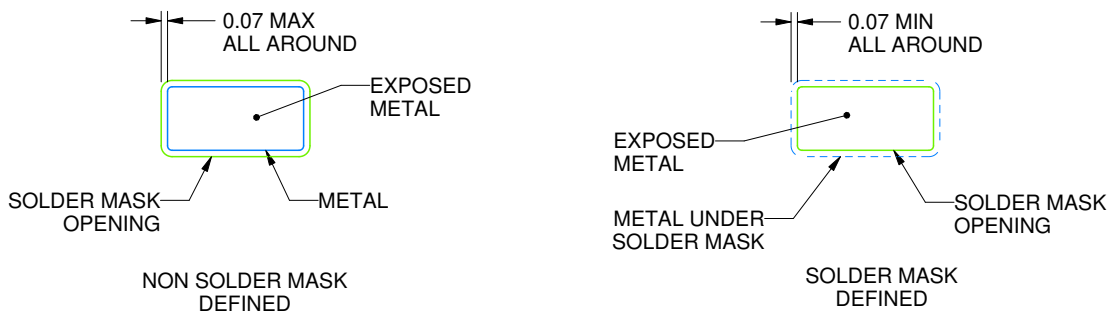
KTT0002A

TO-263 - 4.7 mm max height

TO-263



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:5X



SOLDER MASK DETAILS

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NOTES: (continued)

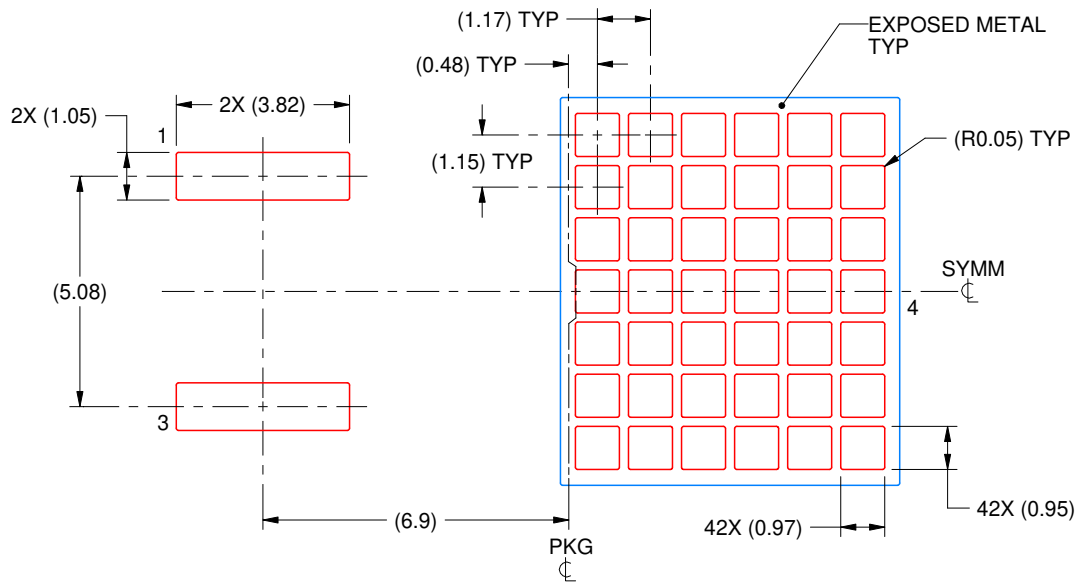
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slm002](http://www.ti.com/lit/slm002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TO-263



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
60.5% PRINTED SOLDER COVERAGE BY AREA  
SCALE:6X

4222117/C 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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