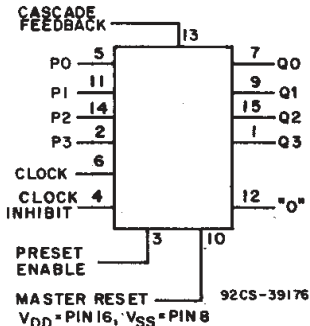


NOT RECOMMENDED FOR NEW DESIGNS

# CD4522B Types

Advance Information/  
Preliminary Data



**FUNCTIONAL DIAGRAM**

## CMOS Programmable BCD Divide-by-“N” Counter

High-Voltage Types (20-Volt Rating)

**Features:**

- Internally synchronous for high internal and external speeds.
- Logic edge-clocked design — increments on positive Clock transition or on negative Clock Inhibit transition.
- 100% tested for quiescent current at 20-V.
- 5-V, 10-V, and 15-V parametric ratings.

- Standard symmetrical output characteristics.
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range: 100 nA at 18 V and 25° C.
- Meets all requirements of JEDEC Standard No. 13B, “Standard Specifications for Description of ‘B’ Series CMOS Devices.”

■ CD4522B programmable BCD counter has a decoded “0” state output for divide-by-N applications. In single stage operation the “0” output is tied to the Preset Enable input. The Cascade Feedback allows multiple stage divide-by-N operation without the need for external gating. A HIGH on the Clock Inhibit disables the pulse-counting function. A HIGH on the Master Reset asynchronously resets the divide-by-N operation. The output is presented in BCD format.

**Applications:**

- Frequency synthesizers
- Phase-locked loops
- Programmable down counters
- Programmable frequency dividers

The CD4522B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

**DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)**

Voltages referenced to V<sub>SS</sub> Terminal) ..... -0.5V to +20V

**INPUT VOLTAGE RANGE, ALL INPUTS** ..... -0.5V to V<sub>DD</sub> +0.5V

**DC INPUT CURRENT, ANY ONE INPUT** .....  $\pm$ 10mA

**POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):**

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

**DEVICE DISSIPATION PER OUTPUT TRANSISTOR**

FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

**OPERATING-TEMPERATURE RANGE (T<sub>A</sub>)** ..... -55°C to +125°C

**STORAGE TEMPERATURE RANGE (T<sub>stg</sub>)** ..... -65°C to +150°C

**LEAD TEMPERATURE (DURING SOLDERING):**

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max ..... +265°C

3  
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HIGH VOLTAGE ICs

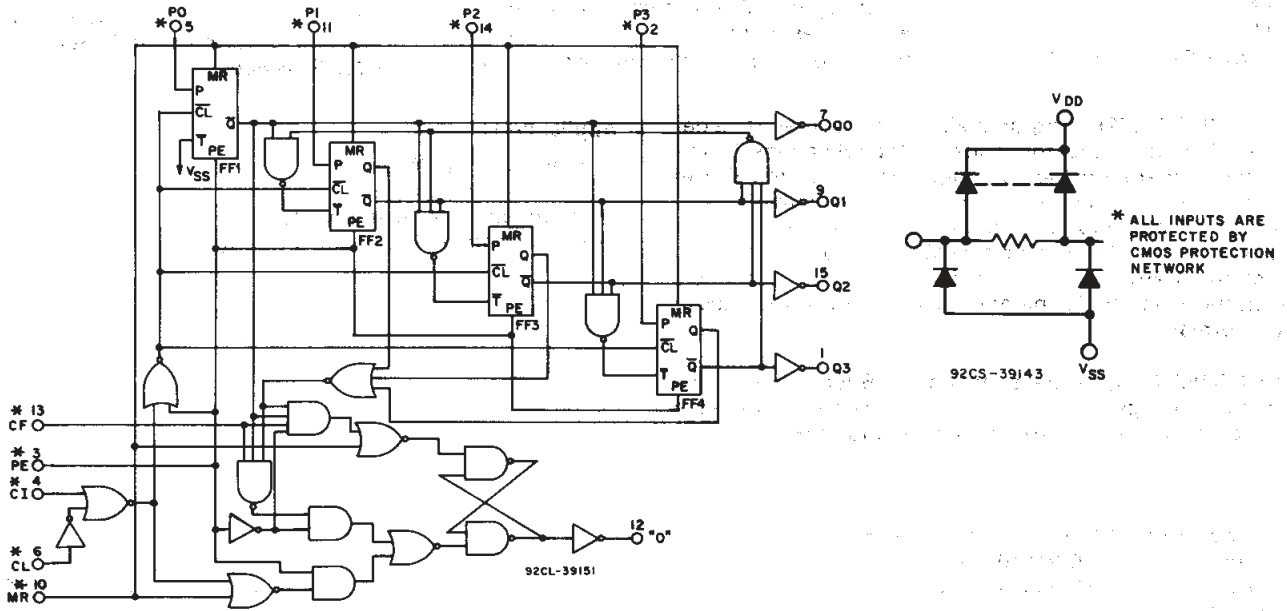
# CD4522B Types

## TRUTH TABLES

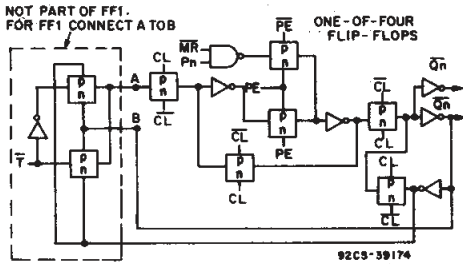
| CLOCK | CLOCK INHIBIT | PRESET ENABLE | MASTER RESET | ACTION     |
|-------|---------------|---------------|--------------|------------|
| 0     | 0             | 0             | 0            | No Count   |
| 0     | 0             | 0             | 0            | Count Down |
| X     | 1             | 0             | 0            | No Count   |
| 1     | 0             | 0             | 0            | Count Down |
| X     | X             | 1             | 0            | Preset     |
| X     | X             | X             | 1            | Reset      |

X = Don't Care

| Count | OUTPUTS        |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | 0              | 0              | 0              | 0              |
| 1     | 1              | 0              | 0              | 0              |
| 2     | 0              | 1              | 0              | 0              |
| 3     | 1              | 1              | 0              | 0              |
| 4     | 0              | 0              | 1              | 0              |
| 5     | 1              | 0              | 1              | 0              |
| 6     | 0              | 1              | 1              | 0              |
| 7     | 1              | 1              | 1              | 0              |
| 8     | 0              | 0              | 0              | 1              |
| 9     | 1              | 0              | 0              | 1              |



a. Basic diagram.



b. Flip-flop detail.

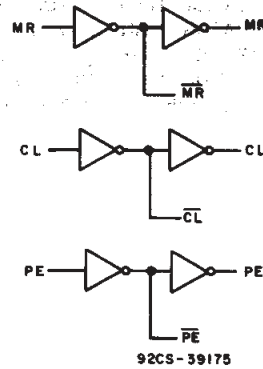


Fig. 1 - Logic diagram for the CD4522B.

## CD4522B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , except as noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTICS   | $V_{DD}$<br>(V) | LIMITS |      | UNITS         |
|---|-----------------|--------|------|---------------|
|   |                 | Min.   | Max. |               |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) |                 | 3      | 18   | V             |
| Pulse Width:  | 5               | 250    | —    | ns            |
| Clock, $t_w(cc)$  | 10              | 100    | —    |               |
| Preset Enable, $t_w(cc)$  | 15              | 80     | —    |               |
|   | 5               | 250    | —    | ns            |
| Preset Enable, $t_w(cc)$  | 10              | 100    | —    |               |
| Master Reset, $t_w(MR)$   | 15              | 80     | —    |               |
|   | 5               | 350    | —    | ns            |
| Master Reset, $t_w(MR)$   | 10              | 250    | —    |               |
| Master Reset, $t_w(MR)$   | 15              | 200    | —    |               |
| Clock Frequency, $f_{CL}$   | 5               | —      | 1.5  | MHz           |
|   | 10              | —      | 3.0  |               |
|   | 15              | —      | 4.0  |               |
| Clock Rise and Fall Time $t_{rCL}, t_{fCL}$                       | 5               | —      | 15   | $\mu\text{s}$ |
|   | 10              | —      | 15   |               |
|   | 15              | —      | 15   |               |
| Preset Enable Set-up Time, $t_{su}$                               | 5               | 0      | —    | ns            |
|   | 10              | 0      | —    |               |
|   | 15              | 0      | —    |               |
| Preset Enable Hold Time, $t_h$                                    | 5               | 75     | —    | ns            |
|   | 10              | 25     | —    |               |
|   | 15              | 20     | —    |               |
| Master Reset Removal Time, $t_{rem}$                              | 5               | 130    | —    | ns            |
|   | 10              | 50     | —    |               |
|   | 15              | 30     | —    |               |

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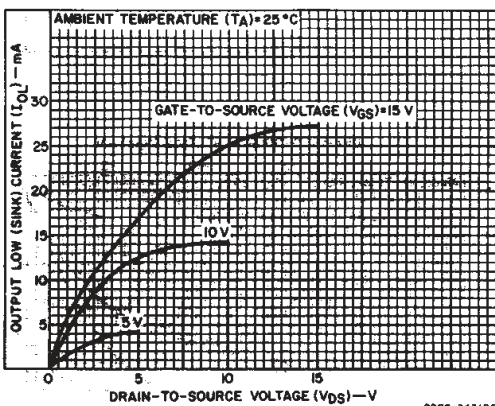


Fig. 2 — Typical output low (sink) current characteristics.

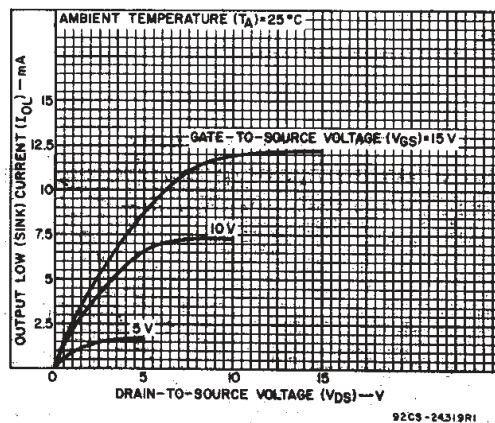
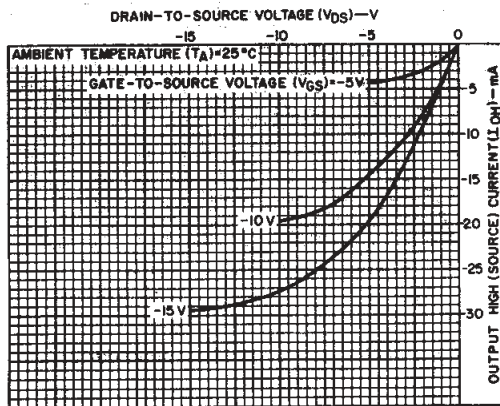


Fig. 3 — Minimum output low (sink) current characteristics.

# CD4522B Types

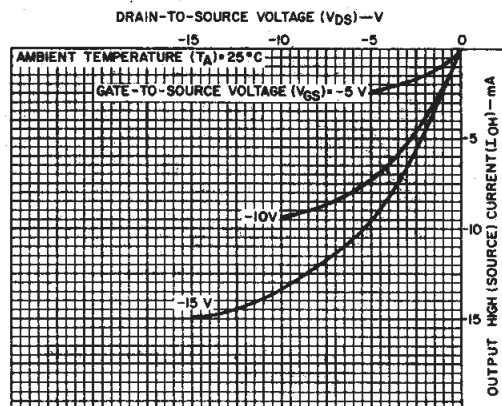
## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC   | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|---|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|   | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) |                                       |       |       |       | +25   |                   |      |       |
|   |                       |                        |                        | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device<br>Current, I <sub>DD</sub> Max.           | —                     | 0, 5                   | 5                      | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA    |
|   | —                     | 0, 10                  | 10                     | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |       |
|   | —                     | 0, 15                  | 15                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
|   | —                     | 0, 20                  | 20                     | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0, 5                   | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|   | 0.5                   | 0, 10                  | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|   | 1.5                   | 0, 15                  | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
|   | 4.6                   | 0, 5                   | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 2.5                   | 0, 5                   | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    | mA    |
|   | 9.5                   | 0, 10                  | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|   | 13.5                  | 0, 15                  | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
|   | —                     | 0, 5                   | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0, 10                  | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|   | —                     | 0, 15                  | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|   | —                     | 0, 5                   | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    |       |
| Output Voltage:<br>High-Level<br>V <sub>OH</sub> Min.       | —                     | 0, 10                  | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    | V     |
|   | —                     | 0, 15                  | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
|   | 0.5, 4.5              | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  |       |
| Input low<br>Voltage, V <sub>IL</sub> Max.                  | 1, 9                  | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    | V     |
|   | 1.5, 13.5             | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
|   | 0.5, 4.5              | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    |       |
| Input High<br>Voltage, V <sub>IH</sub> Min.                 | 1, 9                  | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    | V     |
|   | 1.5, 13.5             | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
|   | —                     | 0, 18                  | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 |       |



92CS-24520R3

Fig. 4 — Typical output high (source) current characteristics.



92CS-24321R2

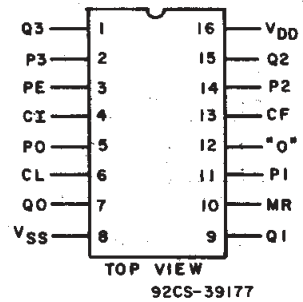
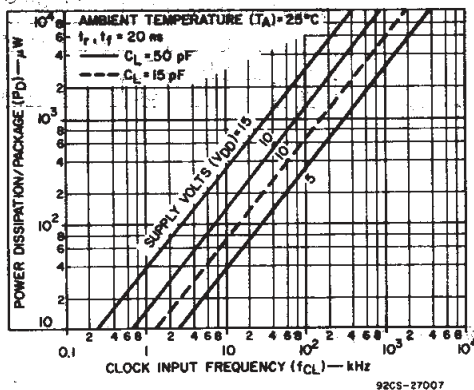
Fig. 5 — Minimum output high (source) current characteristics.

## CD4522B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_i = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$**

| CHARACTERISTIC   | TEST CONDITIONS | LIMITS       |      |      | UNITS |      |
|--|-----------------|--------------|------|------|-------|------|
|  |                 | $V_{DD}$ (V) | Min. | Typ. |       | Max. |
| Propagation Delay Time; $t_{PHL}, t_{PLH}$<br>Clock to "Q" outputs |                 | 5            | —    | 550  | 1100  | ns   |
|  |                 | 10           | —    | 225  | 450   |      |
|  |                 | 15           | —    | 160  | 320   |      |
| Clock to "0" output  |                 | 5            | —    | 420  | 710   | ns   |
|  |                 | 10           | —    | 160  | 270   |      |
|  |                 | 15           | —    | 110  | 190   |      |
| Clock inhibit to "Q" outputs                                       |                 | 5            | —    | 270  | 540   | ns   |
|  |                 | 10           | —    | 100  | 200   |      |
|  |                 | 15           | —    | 70   | 140   |      |
| Master reset to "Q" outputs  |                 | 5            | —    | 270  | 540   | ns   |
|  |                 | 10           | —    | 100  | 200   |      |
|  |                 | 15           | —    | 70   | 140   |      |
| Preset Enable Setup Time, $t_{su}$                                 |                 | 5            | —    | 0    | 0     | ns   |
|  |                 | 10           | —    | 0    | 0     |      |
|  |                 | 15           | —    | 0    | 0     |      |
| Preset Enable Hold Time, $t_h$                                     |                 | 5            | —    | 75   | 150   | ns   |
|  |                 | 10           | —    | 25   | 50    |      |
|  |                 | 15           | —    | 20   | 40    |      |
| Master Reset Removal Time, $t_{rem}$                               |                 | 5            | —    | 130  | 260   | ns   |
|  |                 | 10           | —    | 50   | 100   |      |
|  |                 | 15           | —    | 30   | 60    |      |
| Transition Time, $t_{THL}, t_{TLH}$                                |                 | 5            | —    | 100  | 200   | ns   |
|  |                 | 10           | —    | 50   | 100   |      |
|  |                 | 15           | —    | 40   | 80    |      |
| Minimum Pulse Width<br>Clock, $t_{W(CL)}$                          |                 | 5            | —    | 125  | 250   | ns   |
|  |                 | 10           | —    | 50   | 100   |      |
|  |                 | 15           | —    | 40   | 80    |      |
| Preset Enable, $t_{W(PE)}$   |                 | 5            | —    | 125  | 250   | ns   |
|  |                 | 10           | —    | 50   | 100   |      |
|  |                 | 15           | —    | 40   | 80    |      |
| Master Reset, $t_{W(MR)}$  |                 | 5            | —    | 175  | 350   | ns   |
|  |                 | 10           | —    | 125  | 250   |      |
|  |                 | 15           | —    | 100  | 200   |      |
| Max Clock Freq, $f_{CL}$   |                 | 5            | —    | 3    | 1.5   | MHz  |
|  |                 | 10           | —    | 6    | 3.0   |      |
|  |                 | 15           | —    | 8    | 4.0   |      |
| Max Clock or Clock Inhibit Rise & Fall Time, $t_{TLH}, t_{THL}$    |                 | 5            | —    | —    | 15    | us   |
|  |                 | 10           | —    | —    | 15    |      |
|  |                 | 15           | —    | —    | 15    |      |
| Input Capacitance, $C_{IN}$  | Any Input       | —            | —    | 5    | 7.5   | pF   |

**3**  
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**TERMINAL ASSIGNMENT**

**Fig. 6 — Typical dynamic power dissipation vs. frequency.**

## CD4522B Types

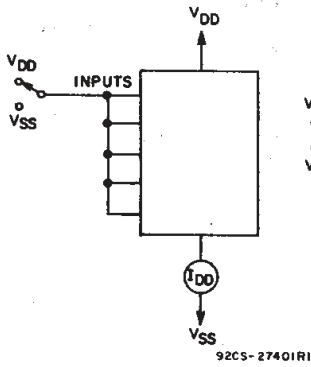


Fig. 7 — Quiescent device current test circuit.

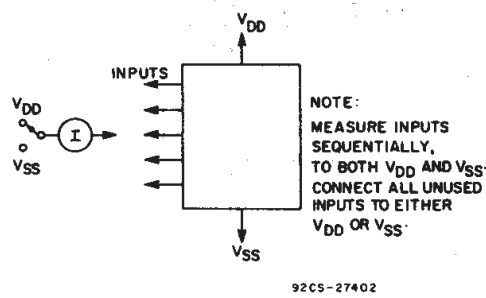


Fig. 8 — Input current test circuit.

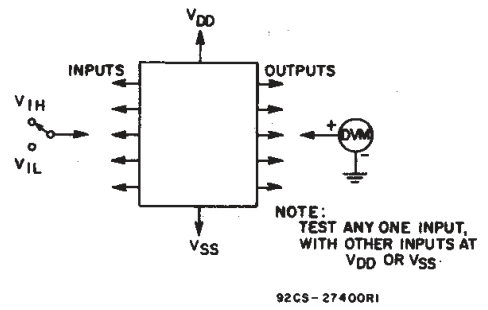


Fig. 9 — Input voltage test circuit.

## APPLICATION CIRCUITS

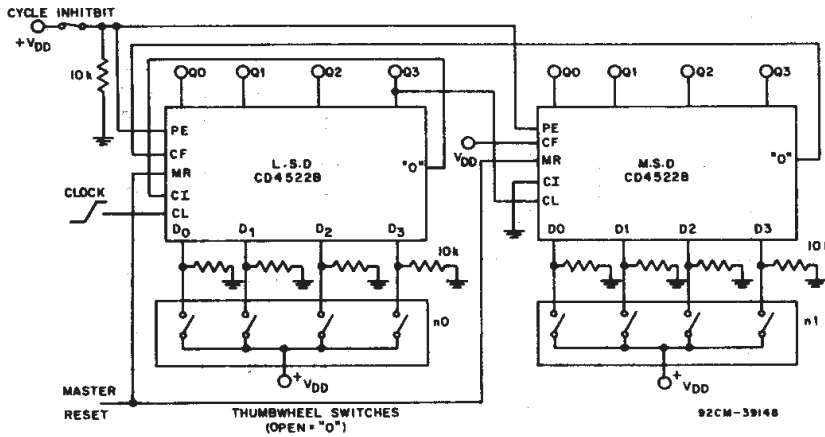


Fig. 10 — 2-Stage Programmable Down Counter (One Cycle)

| From  |                   | To    |     | Range of N        |
|-------|-------------------|-------|-----|-------------------|
| Stage | Pin               | Stage | Pin |                   |
| LSD   | "0"               | All   | PE  | LSD < N < MSD     |
| N     | "0"               | N-1   | CF  | LSD + 1 < N < MSD |
| N     | "0 <sub>3</sub> " | N+1   | CL  | LSD < N < MSD-1   |

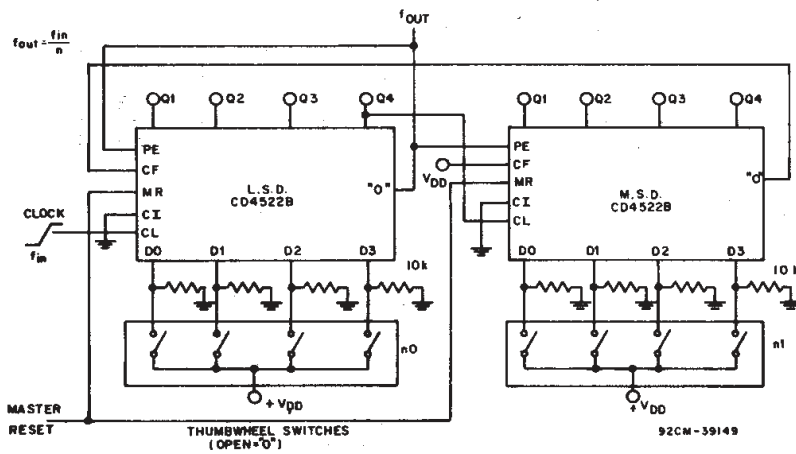
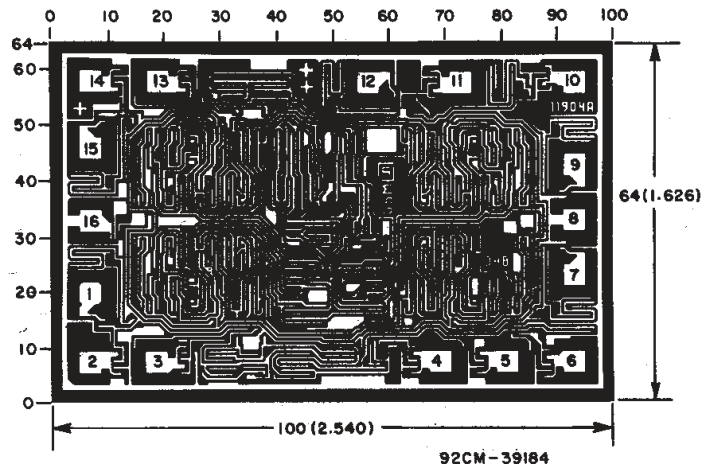


Fig. 11 — 2-Stage Programmable Frequency Divider

| From  |                   | To    |     | Range of N        |
|-------|-------------------|-------|-----|-------------------|
| Stage | Pin               | Stage | Pin |                   |
| LSD   | "0"               | All   | PE  | LSD < N < MSD     |
| N     | "0"               | N-1   | CF  | LSD + 1 < N < MSD |
| N     | "0 <sub>3</sub> " | N+1   | CL  | LSD < N < MSD-1   |

## CD4522B Types



*Dimensions and pad layout for CD4522BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

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**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4522BE         | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD4522BE                | <a href="#">Samples</a> |
| CD4522BM         | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4522BM                | <a href="#">Samples</a> |
| CD4522BMT        | ACTIVE        | SOIC         | D               | 16   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4522BM                | <a href="#">Samples</a> |
| CD4522BPW        | ACTIVE        | TSSOP        | PW              | 16   | 90          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM522B                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

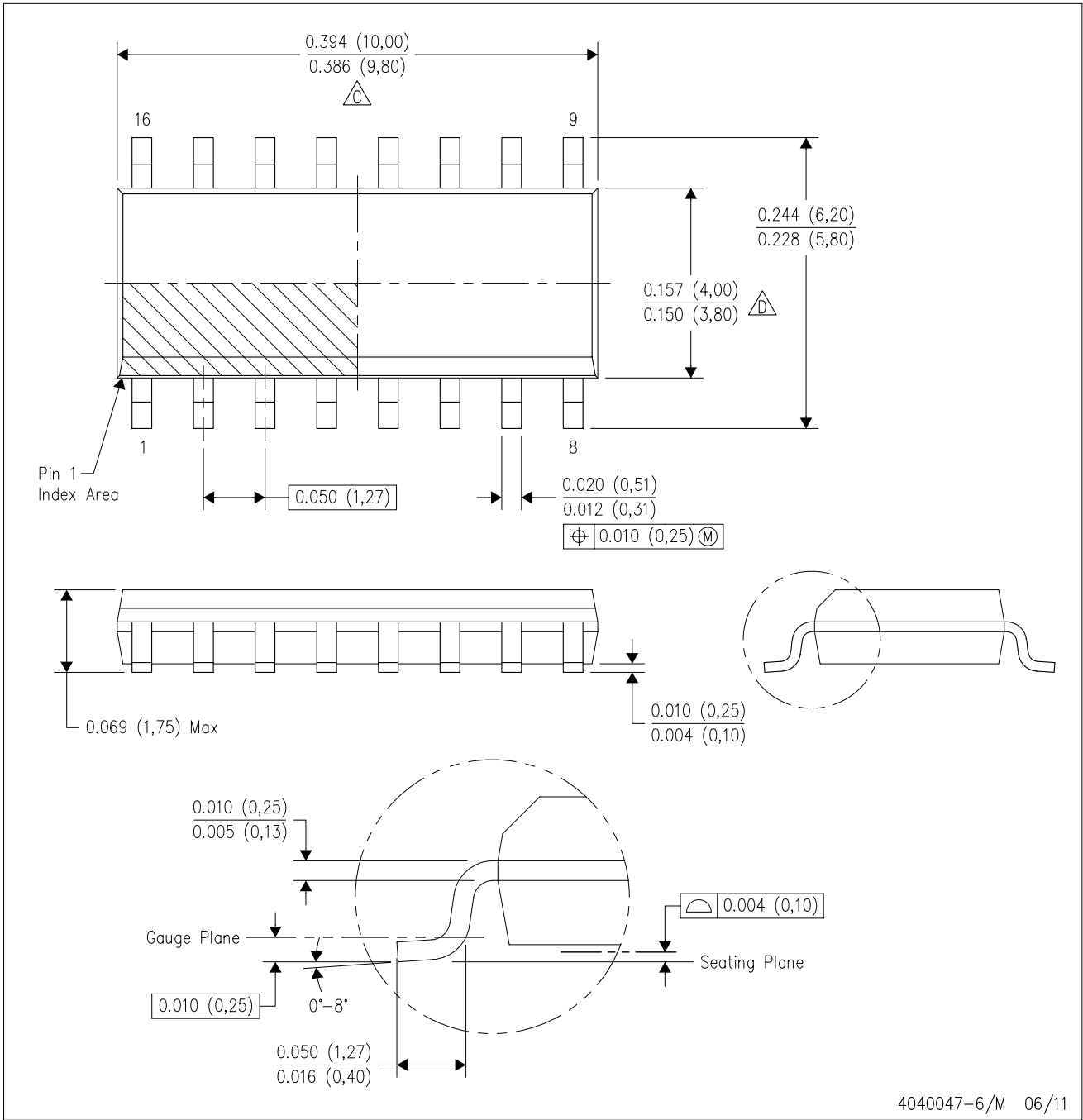
**TUBE**




\*All dimensions are nominal

| Device    | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4522BE  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4522BE  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD4522BM  | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| CD4522BPW | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |

D (R-PDSO-G16)

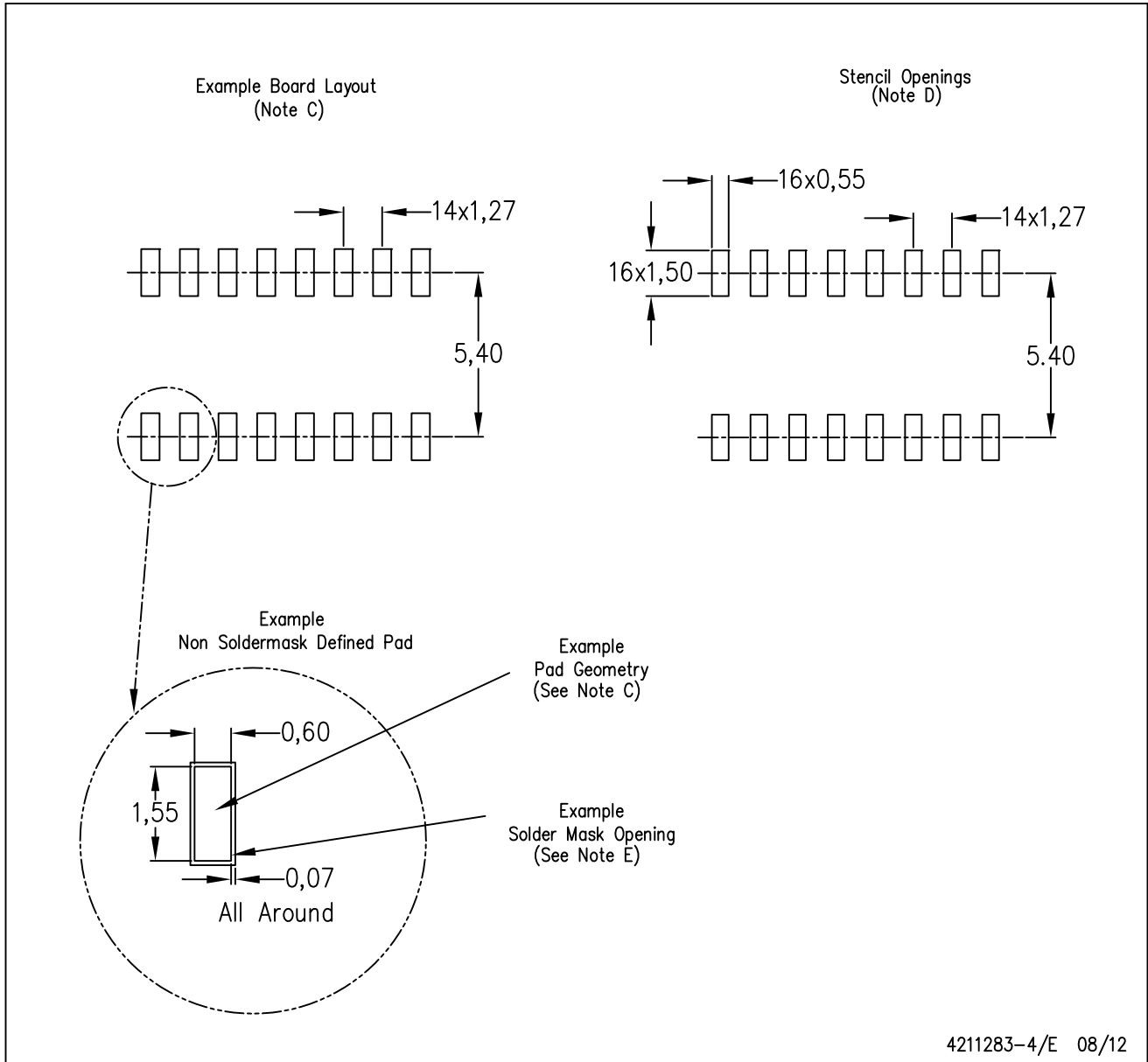
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

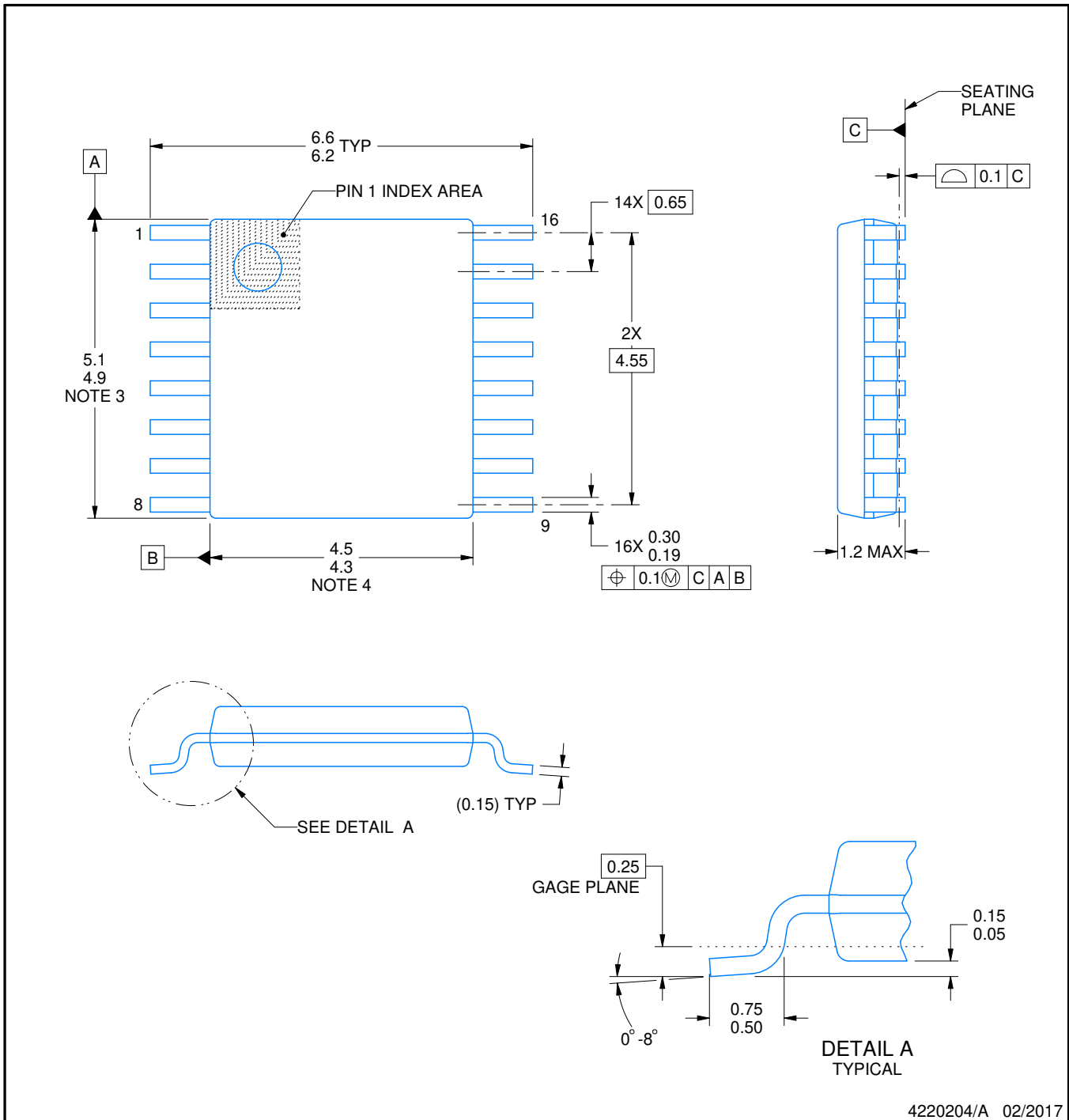
# PW0016A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

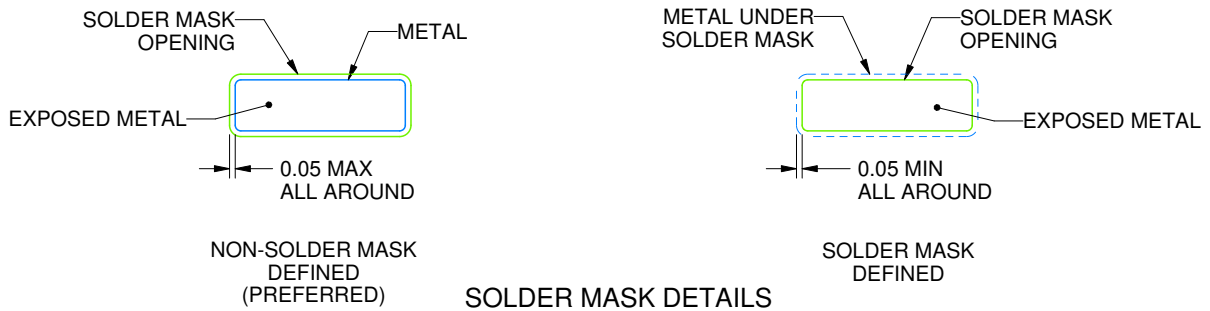
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



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