MC33762

Voltage Regulator - Dual, Ultra Low-Noise, Low Dropout, ON/OFF Control

1.0 V

The MC33762 is a dual Low DropOut (LDO) regulator featuring excellent noise performances. Thanks to its innovative design, the circuit reaches an impressive 40 μVRMS noise level ***without*** an external bypass capacitor. Housed in a small μ8 package, it represents the ideal designer's choice when space and noise are at premium.

The absence of external bandgap capacitor accelerates the response time to a wake−up signal and keeps it within 40 μs, making the MC33762 as a natural candidate for portable applications.

The MC33762 also hosts a novel architecture which prevents excessive undershoots in the presence of fast transient bursts, as in any bursting systems.

Finally, with a static line regulation better than −75 dB, it naturally shields the downstream electronics from choppy lines.

Features

- Nominal Output Current of 80 mA with a 100 mA Peak Capability
- Ultra−Low Noise: 150 nV/√Hz @ 100 Hz, 40 μVRMS 100 Hz−100 kHz Typical, I_{out} = 60 mA, Co = 1.0 μF
- Fast Response Time from OFF to ON: 40 μs Typical
- Ready for 1.0 V Platforms: ON with a 900 mV High Level
- Typical Dropout of 90 mV @ 30 mA, 160 mV @ 80 mA
- Ripple Rejection: 70 dB @ 1.0 kHz
- 1.5% Output Precision @ 25°C
- Thermal Shutdown
- V_{out} Available at 2.5 V, 2.8 V, and 3.0 V
- Separate Dice for Each Regulator Provides Maximum Isolation Between Regulators
- Operating Range from −40 to +85°C
- Pb−Free Packages are Available

Applications

- Noise Sensitive Circuits: VCOs RF Stages, etc.
- Bursting Systems (TDMA Phones)
- All Battery Operated Devices

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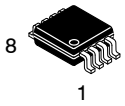
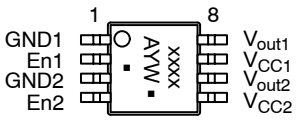


Micro8™
DM SUFFIX
CASE 846A

PIN CONFIGURATION AND MARKING DIAGRAM



(Top View)

xxxx = Device Code
See Table − Page 4
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

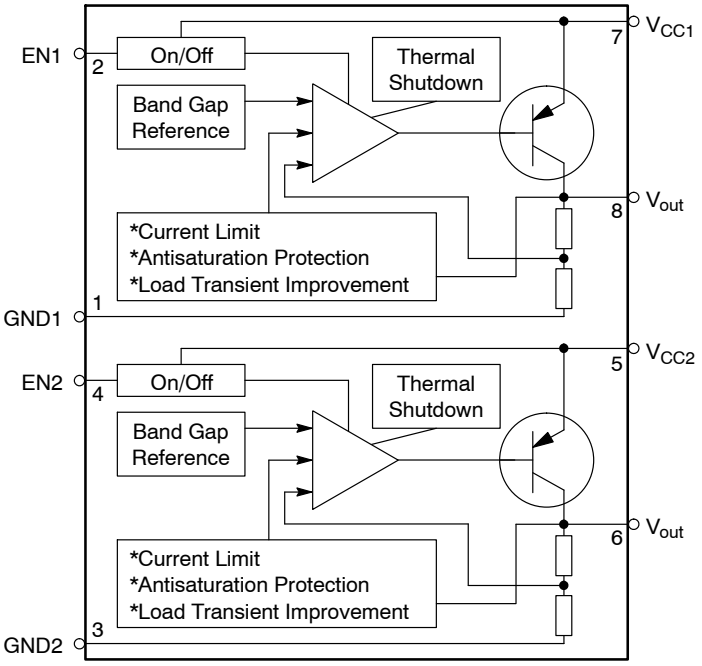


Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Function	Description
1	GND1	Ground of the 1st LDO	
2	En1	Enables the 1st LDO	A 900 mV level on this pin is sufficient to start this LDO. A 150 mV shuts it down.
3	GND2	Ground of the 2nd LDO	
4	En2	Enables the 2nd LDO	A 900 mV level on this pin is sufficient to start this LDO. A 150 mV shuts it down.
5	V_{cc2}	2nd LDO V_{cc} pin	This pin brings the power to the 1st LDO and requires adequate decoupling.
6	V_{out2}	Shuts or wakes−up the IC	This pin requires a 1.0 μF output capacitor to be stable.
7	V_{cc1}	1st LDO V_{cc} pin	This pin brings the power to the 1st LDO and requires adequate decoupling.
8	V_{out1}	Delivers the output voltage	This pin requires a 1.0 μF output capacitor to be stable.

MAXIMUM RATINGS

Rating	Pin #	Symbol	Value		Unit
			Min	Max	
Power Supply Voltage	1	V_{in}	−	12	V
ESD Capability, HBM Model	All Pins	−	−	1.0	kV
ESD Capability, Machine Model	All Pins	−	−	200	V
Maximum Power Dissipation NW Suffix, Plastic Package Thermal Resistance Junction−to−Air	− −	P_D $R_{\theta J-A}$	− −	Internally Limited 240	W °C/W
Operating Ambient Temperature Maximum Junction Temperature (Note 1) Maximum Operating Junction Temperature (Note 2)	− − −	T_A T_{Jmax} T_J	− − −	−40 to +85 150 125	°C °C °C
Storage Temperature Range	−	T_{stg}	−	−60 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Internally limited by shutdown.
2. Specifications are guaranteed below this value.

ELECTRICAL CHARACTERISTICS

(For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C, max T_J = 125°C unless otherwise noted)

Characteristics		Pin #	Symbol	Min	Typ	Max	Unit
LOGIC CONTROL SPECIFICATIONS							
Input Voltage Range		2–4	$V_{ON/\overline{OFF}}$	0	–	V_{in}	V
ON/$\overline{OFF}$ Input Resistance (all versions)		2–4	$R_{ON/\overline{OFF}}$	–	250	–	kΩ
ON/OFF Control Voltages (Note 3)	Logic Zero, OFF State, I_O = 50 mA Logic One, ON State, I_O = 50 mA	2–4	$V_{ON/\overline{OFF}}$	– 900	– –	150 –	mV
CURRENTS PARAMETERS							
Current Consumption in OFF State (all versions) OFF Mode Current: $V_{in} = V_{out}$ + 1.0 V, I_O = 0, V_{OFF} = 150 mV		–	IQ_{OFF}	–	0.1	2.0	μA
Current Consumption in ON State (all versions) ON Mode Current: $V_{in} = V_{out}$ + 1.0 V, I_O = 0, V_{ON} = 3.5 V		–	IQ_{ON}	–	180	–	μA
Current Consumption in ON State (all versions), ON Mode Saturation Current: $V_{in} = V_{out}$ − 0.5 V, No Output Load		–	IQ_{SAT}	–	800	–	μA
Current Limit $V_{in} = Vout_{nom}$ + 1.0 V, Output is brought to $Vout_{nom}$ − 0.3 V (all versions)		–	I_{MAX}	100	180	–	mA
OUTPUT VOLTAGES							
V_{out} + 1.0 V < V_{in} < 6.0 V, T_A = 25°C, 1.0 mA < I_{out} < 80 mA	2.5 V	5–7	V_{out}	2.462	2.5	2.537	V
	2.8 V	5–7	V_{out}	2.758	2.8	2.842	V
	3.0 V	5–7	V_{out}	2.955	3.0	3.045	V
	3.3 V	5–7	V_{out}	3.250	3.3	3.349	V
	3.6 V	5–7	V_{out}	3.546	3.6	3.654	V
Other Voltages up to 5.0 V Available in 50 mV Increment Steps		5–7	V_{out}	−1.5	X	+1.5	%
V_{out} + 1.0 V < V_{in} < 6.0 V, T_A = −40°C to +85°C, 1.0 mA < I_{out} < 80 mA	2.5 V	5–7	V_{out}	2.425	2.5	2.575	V
	2.8 V	5–7	V_{out}	2.716	2.8	2.884	V
	3.0 V	5–7	V_{out}	2.91	3.0	3.090	V
	3.3 V	5–7	V_{out}	3.201	3.3	3.399	V
	3.6 V	5–7	V_{out}	3.492	3.6	3.708	V
Other Voltages up to 5.0 V Available in 50 mV Increment Steps		5–7	V_{out}	−3.0	X	+3.0	%
LINE AND LOAD REGULATION, DROPOUT VOLTAGES							
Line Regulation (all versions)	V_{out} + 1.0 V < V_{in} < 12 V, I_{out} = 80 mA	5–7	Reg_{line}	–	–	20	mV
Load Regulation (all versions)	$V_{in} = V_{out}$ + 1.0 V, C_{out} = 1.0 μF, I_{out} = 1.0 to 80 mA	5–7	Reg_{load}	–	–	40	mV
Dropout Voltage (all versions) (Note 3)	I_{out} = 30 mA I_{out} = 60 mA I_{out} = 80 mA	5–7 5–7 5–7	$V_{in}-V_{out}$ $V_{in}-V_{out}$ $V_{in}-V_{out}$	– – –	90 140 160	150 200 250	mV
DYNAMIC PARAMETERS							
Ripple Rejection (all versions) $V_{in} = V_{out}$ + 1.0 V + 1.0 kHz 100 mVpp Sinusoidal Signal		5–7	Ripple	–	−70	–	dB
Output Noise Density @ 1.0 kHz		5–7	–	–	150	–	nV/√Hz
RMS Output Noise Voltage (all versions) C_{out} = 1.0 μF, I_{out} = 50 mA, F = 100 Hz to 1.0 MHz		5–7	Noise	–	35	–	μV
Output Rise Time (all versions) C_{out} = 1.0 μF, I_{out} = 50 mA, 10% of Rising ON Signal to 90% of Nominal V_{out}		5–7	t_{rise}	–	40	–	μs
THERMAL SHUTDOWN							
Thermal Shutdown (all versions)		–	–	–	–	125	°C

3. Voltage slope should be greater than 2.0 mV/μs

ORDERING INFORMATION

Device	Marking	Voltage Output	Package	Shipping†
MC33762DM−2525R2	2525	2.5 V	Micro8	4000 Units / Tape & Reel
MC33762DM−2525R2G			Micro8 (Pb−Free)	
MC33762DM−2828R2	2528	2.8 V	Micro8	
MC33762DM−2828R2G			Micro8 (Pb−Free)	
MC33762DM−3030R2	3030	3.0 V	Micro8	
MC33762DM−3030R2G			Micro8 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant chip temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential value). The dropout level is affected by the chip temperature, load current and minimum input supply requirements.

Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output current are kept constant during the measurement. Results are expressed in μVRMS.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specs.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected. One usually distinguishes *static line regulation* or *DC line regulation* (a DC step in the input voltage generates a corresponding step in the output voltage) from *ripple rejection* or *audio susceptibility* where the input is combined with a frequency generator to sweep from a few hertz up to a defined boundary while the output amplitude is monitored.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 125°C, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package power dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient temperature, it is possible to calculate the maximum power dissipation and thus the maximum available output current.

Characterization Curves

Curves are Common to Both Regulators

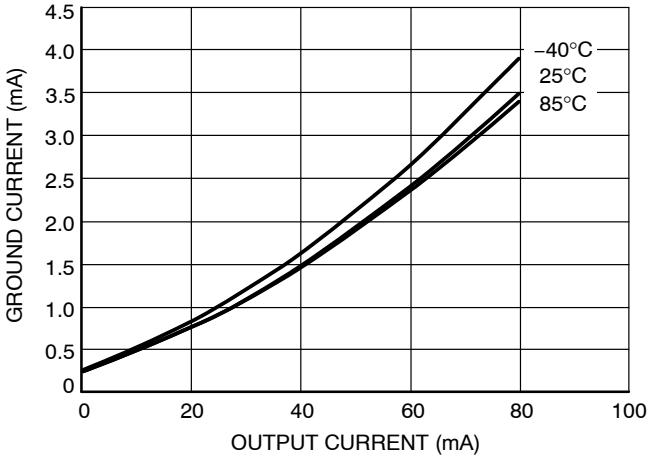


Figure 2. Ground Current versus Output Current

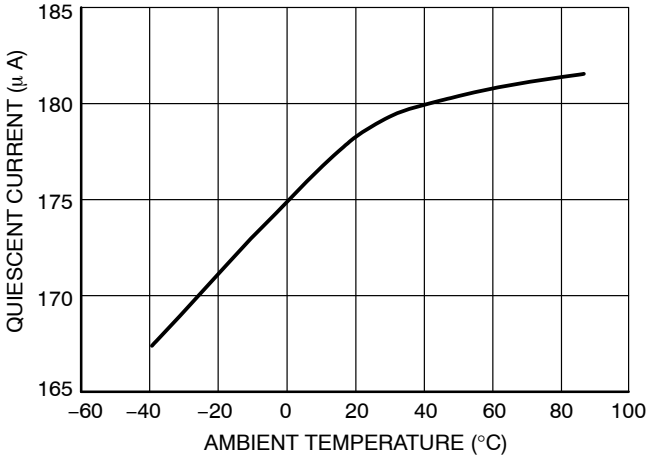


Figure 3. Quiescent Current versus Temperature

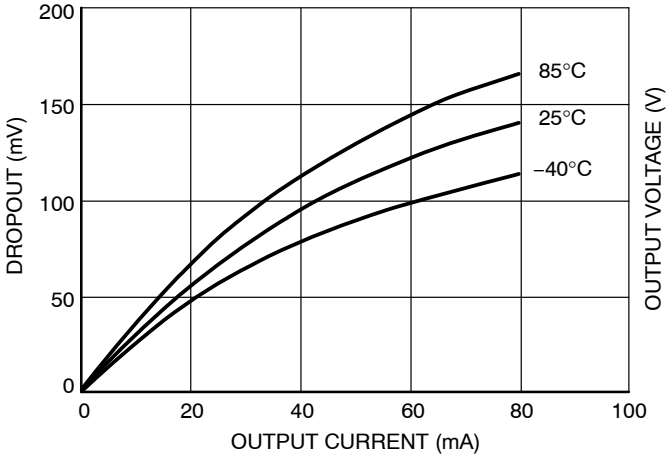


Figure 4. Dropout versus Output Current

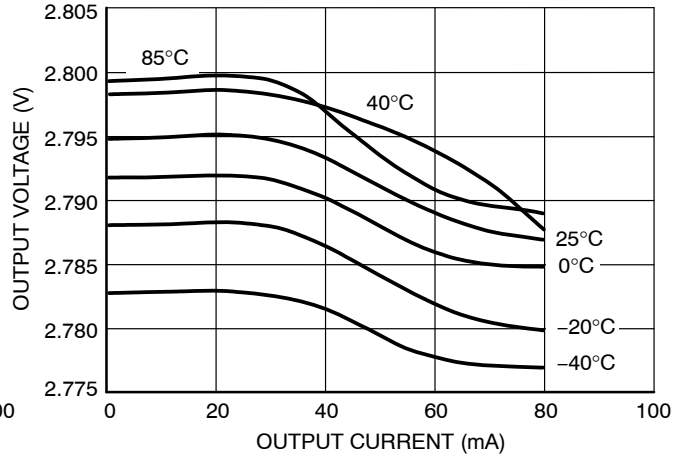


Figure 5. Output Voltage versus Output Current

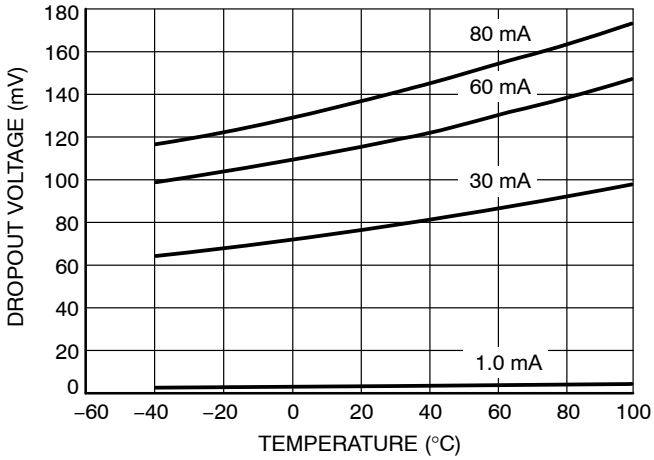


Figure 6. Dropout versus Temperature

APPLICATION HINTS

Input Decoupling

As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the MC33762 package. Higher values will correspondingly improve the overall line transient response.

Output Decoupling

Thanks to a novel concept, the MC33762 is a stable component and does not require any specific Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

Noise Performances

Unlike other LDOs, the MC33762 is a true low−noise regulator. Without the need of an external bypass capacitor, it typically reaches the incredible level of 40 μVRMS overall noise between 100 Hz and 100 kHz. To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics. The classical bypass capacitor impacts the startup phase of standard LDOs. However, thanks to its low−noise architecture, the MC33762 operates without a bypass element and thus offers a typical 40 μs startup phase.

Protections

The MC33762 hosts several protections, giving natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a maximum value of 180 mA *typical* while temperature shutdown occurs if the die heats up beyond 125°C. These values let you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$P_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

If T_{Jmax} is limited to 125°C, then the MC33762 can dissipate up to 395 mW @ 25°C. The power dissipated by the MC33762 can be calculated from the following formula:

$$Ptot = \left(V_{in} \times I_{gnd}(I_{out})\right) + \left(V_{in} - V_{out}\right) \times I_{out}$$

or

$$Vin_{max} = \frac{Ptot + V_{out} \times I_{out}}{I_{gnd} + I_{out}}$$

If a 80 mA output current is needed, the ground current is extracted from the data−sheet curves: 4.0 mA @ 80 mA. For a half 2.8 V MC33762 (2.8 V) operating at 25°C, the maximum input voltage will then be 7.3 V.

Typical Applications

The following picture portrays the typical application of the MC33762.

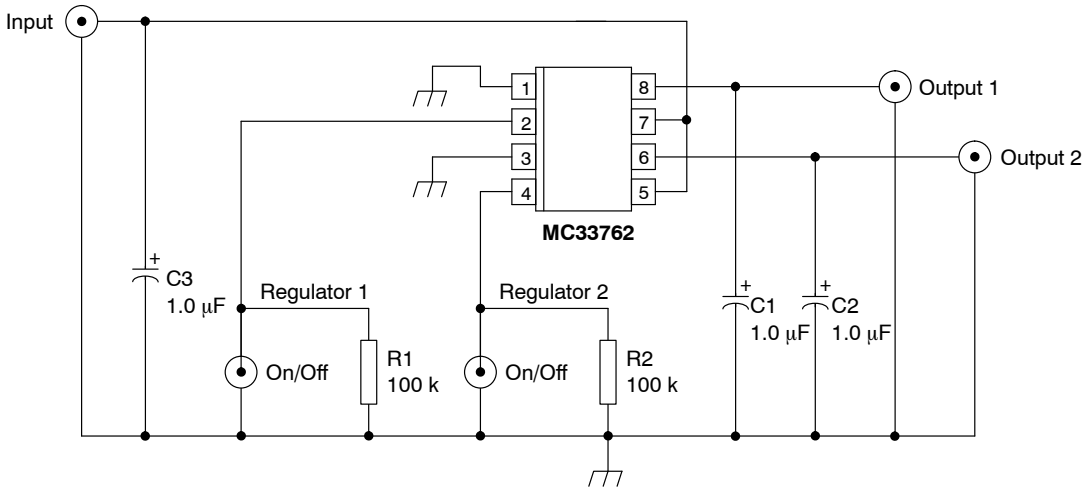


Figure 7. A Typical Application Schematic

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. Connections shall be kept short and wide. Layout example as given in the MC33761 application hints can be used as a starting basis.

Understanding the Load Transient Improvement

The MC33762 features a novel architecture which allows the user to easily implement the regulator in burst systems where the time between two current shots is kept very small.

The quality of the transient response time is related to many parameters, among which the closed−loop bandwidth with the corresponding phase margin plays an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open−loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place with a positive overshoot. The problem appears when this overshoot decays down to the LDO steady−state value. During this decreasing phase, the LDO stops the PNP bias and one can consider the LDO asleep (Figure 8). If by misfortune a current shot appears, the reaction time is incredibly lengthened and a strong undershoot takes place. This reaction is clearly not acceptable for line sensitive devices, such as VCOs or other Radio−Frequency parts. This problem is dramatically exacerbated when the output current drops to zero rather than a few mA. In this later case, the internal feedback network is the only discharge path, accordingly lengthening the output voltage decay period (Figure 9).

The MC33762 cures this problem by implementing a clever design where the LDO detects the presence of the overshoot and forces the system to go back to steady−state as soon as possible, ready for the next shot. Figure 10 and 11 show how it positively improves the response time and decreases the negative peak voltage.

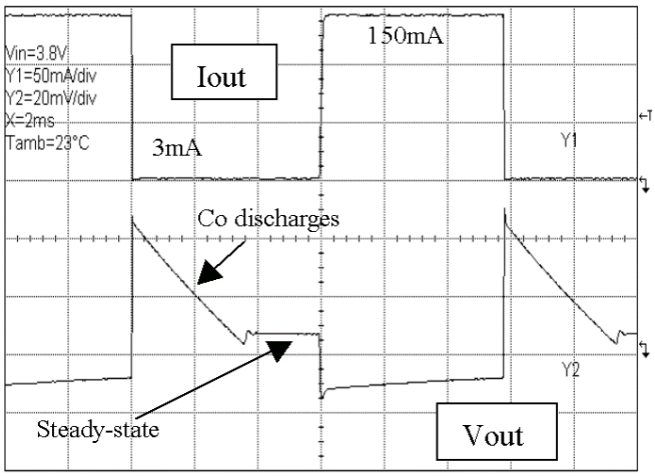


Figure 8. A Standard LDO Behavior when the Load Current Disappears

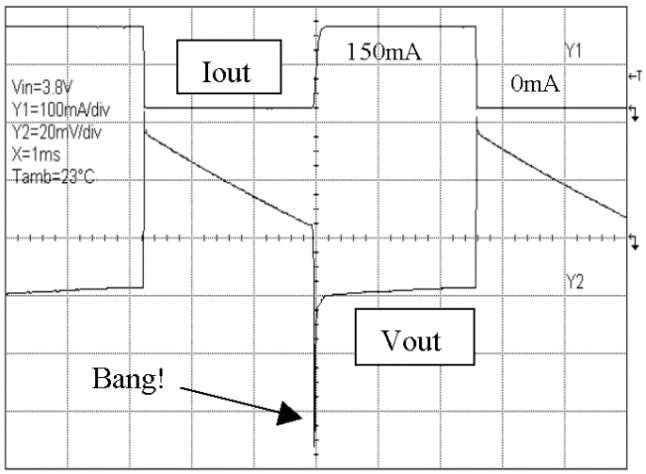


Figure 9. A Standard LDO Behavior when the Load Current Appears in the Decay Zone

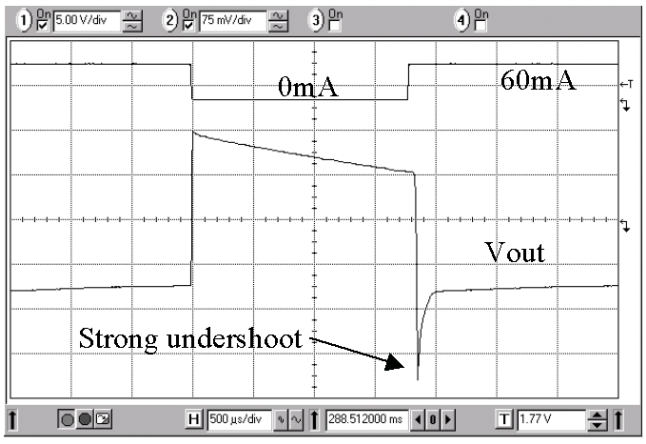


Figure 10. Without Load Transient Improvement

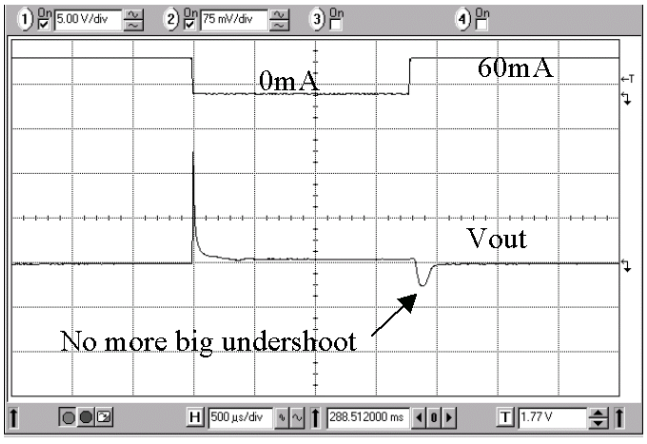


Figure 11. MC33762 with Load Transient Improvement

MC33762 Has a Fast Startup Phase

Thanks to the lack of bypass capacitor the MC33762 is able to supply its downstream circuitry as soon as the OFF to ON signal appears. In a standard LDO, the charging time of the external bypass capacitor hampers the response time. A simple solution consists in suppressing this bypass element but, unfortunately, the noise rises to an unacceptable level. MC33762 offers the best of both worlds since it no longer includes a bypass capacitor and starts in less than 40 μs typically (Repetitive at 200 Hz). It also ensures an incredible low−noise level of 40 μVRMS 100 Hz−100 kHz. The following picture details the typical 33762 startup phase.

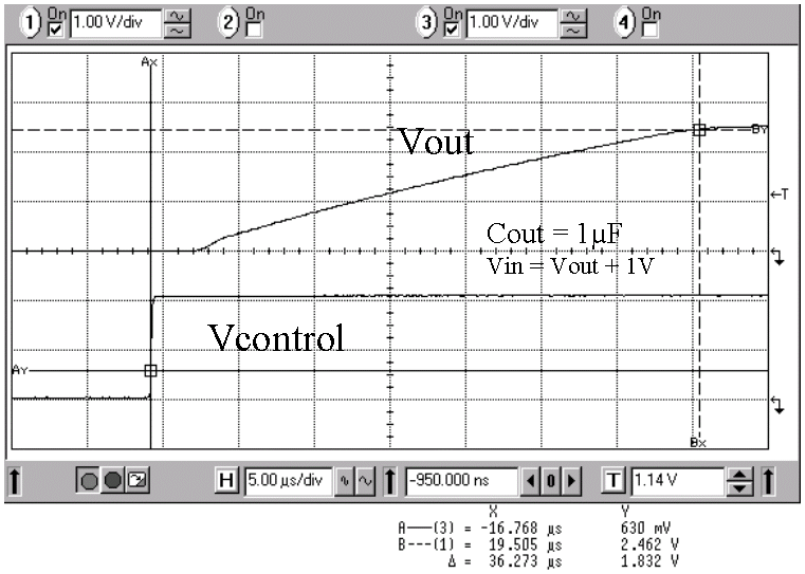


Figure 12. Repetitive Startup Waveforms

TYPICAL TRANSIENT RESPONSES

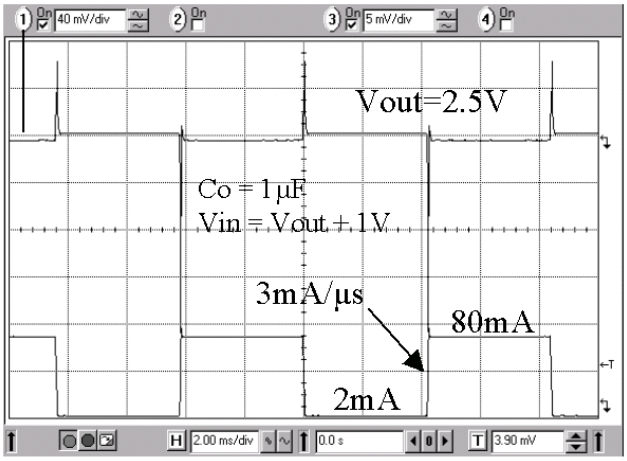


Figure 13. Output is Pulsed from 2.0 mA to 80 mA

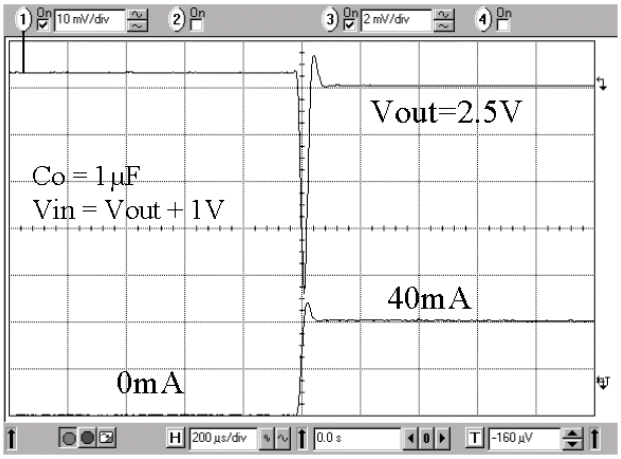


Figure 14. Discharge Effects from 0 to 40 mA

TYPICAL TRANSIENT RESPONSES

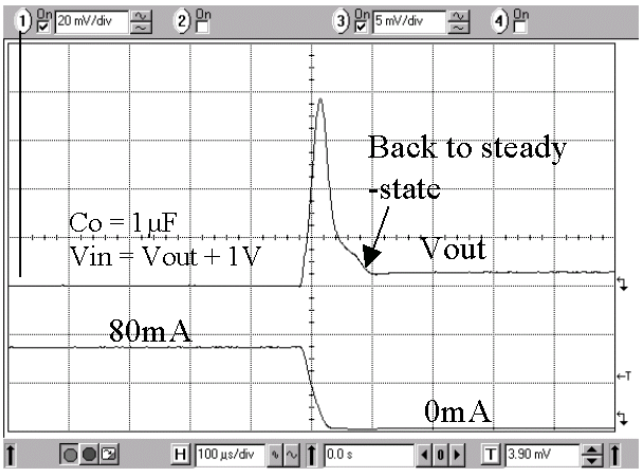


Figure 15. Load Transient Improvement Effect

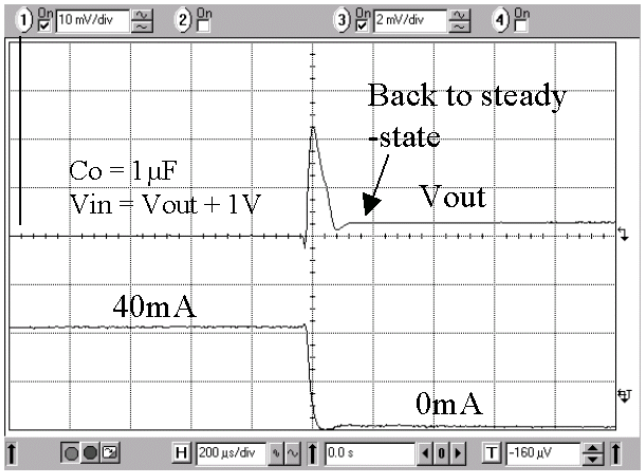


Figure 16. Load Transient Improvement Effect

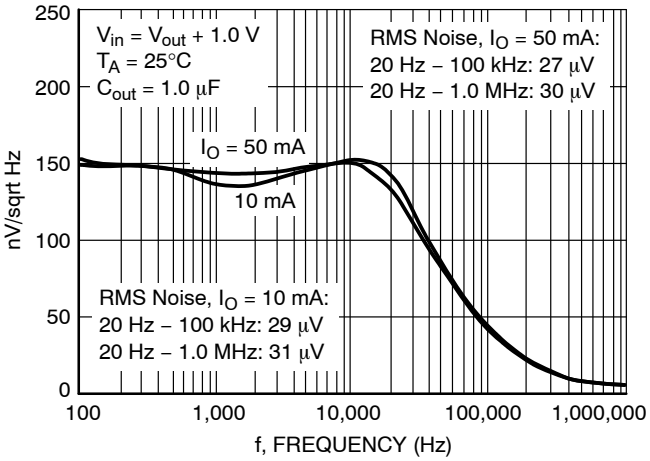


Figure 17. MC33762 Typical Noise Density Performance

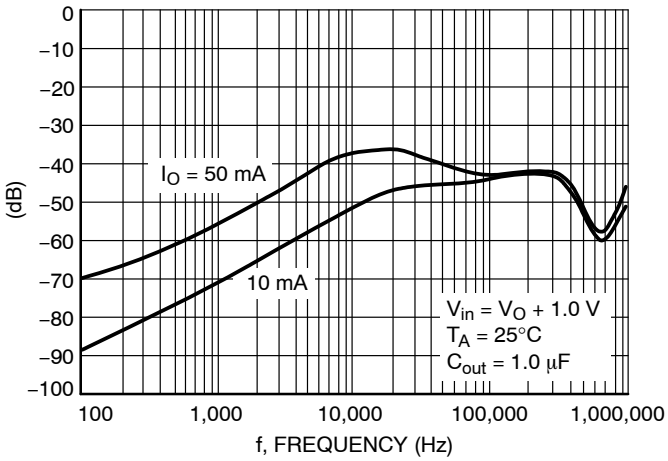


Figure 18. MC33762 Typical Ripple Rejection Performance

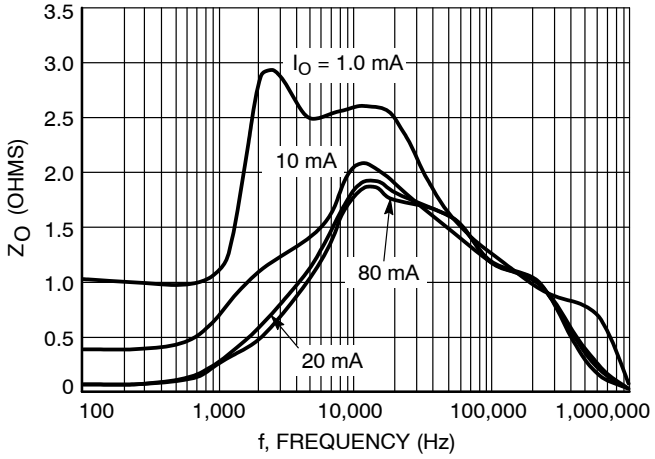


Figure 19. Output Impedance Plot
C_{out} = 1.0 μF, V_{in} = V_{out} + 1.0 V

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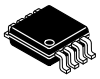
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

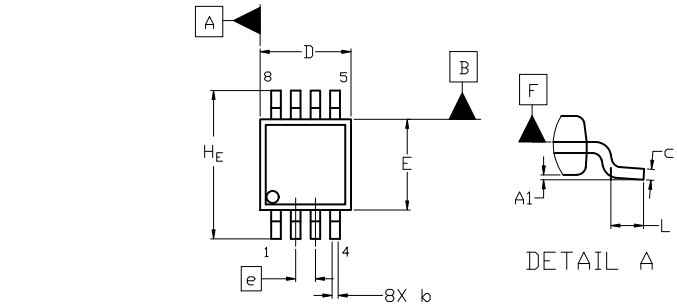
ON Semiconductor®

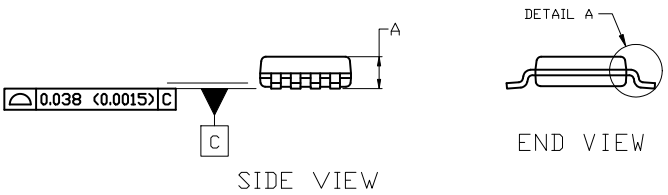


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

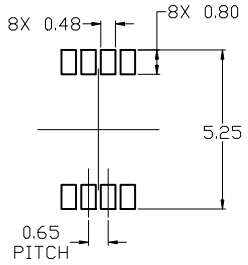
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

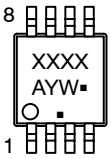


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

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