V386

8-BIT LVDS RECEIVER FOR VIDEO

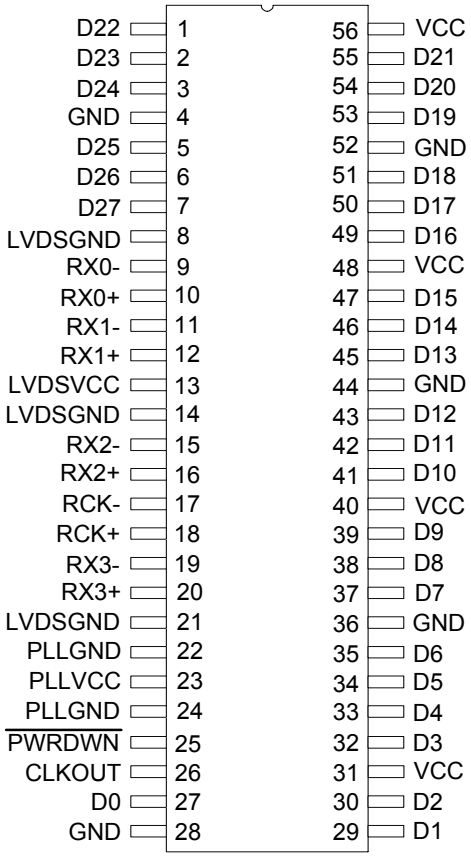
General Description

The V386 is an ideal LVDS receiver that converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data with bandwidth up to 2.38 Gbps throughput or 297.5 Mbytes per second.

This chip is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces through very low-swing LVDS signals.

ICS manufactures a large variety of video application devices. Consult ICS for all of your video application requirements.

Pin Assignments

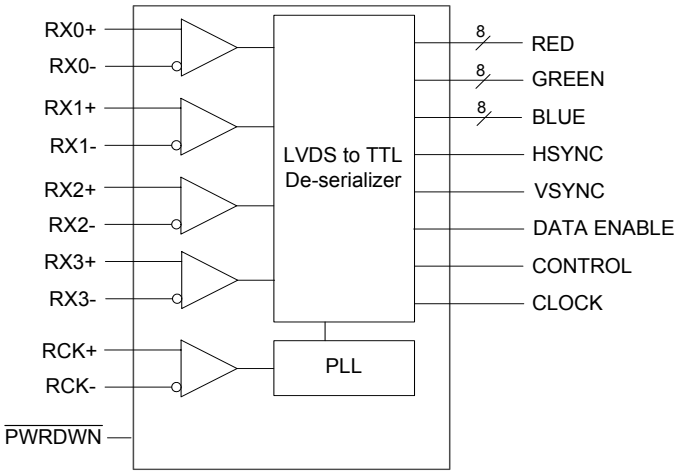


56-pin TSSOP
V386

Features

- Packaged in a 56-pin TSSOP (Pb free available)
- Converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data
- Up to 2.38 Gbps throughput or 297.5 Megabytes/sec bandwidth
- Wide clock frequency range from 25 MHz to 85 MHz (for lower frequency requirements, please use V386-2)
- Supports VGA, SVGA, XGA, and SXGA
- LVDS voltage swing of 350 mV for low EMI
- On-chip PLL requires no external components
- Single 3.3 V low-power CMOS design
- Falling edge clock triggered outputs
- Power-down control function
- Compatible with TIA/EIA-644 LVDS standards
- Pin and function compatible with the National DS90CF386, THine THC63LVDF84, TI SN65LVDS94

Block Diagram



V386

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Pin Descriptions

Pin Type	Pin Count	Pins	Pin Description/Name
LVDS Differential Input	10	9, 10, 11, 12, 15, 16, 17, 18, 19, 20	8 pins (4 pairs) for Data inputs (RX0+, RX0- ; RX1+, RX1- ; RX2+, RX2- ;RX3+, RX3-) 2 pins (1 pair) for Clock Inputs (RCK+, RCK-)
Data Output	28	1, 2, 3, 5, 6, 7, 27, 29, 30, 32, 33, 34, 35, 37, 38, 39, 41, 42, 43, 45, 46, 47, 49, 50, 51, 53, 54, 55	Data outputs on pins D0 through D27
Clock Output	1	26	CLKOUT
VCC	6	13, 23, 31, 40, 48, 56	1 pin for LVDS input pairs (LVDSVCC) 1 pin for PLL (PLLVCC) 4 pins for Logic and Data outputs (VCC)
Power Down	1	25	Power-down control input ($\overline{\text{PWRDWN}}$) Active low
Ground	10	4, 8, 14, 21, 22, 24, 28, 36, 44, 5	3 pins for LVDS input pairs (LVDSGND) 2 pins for PLL (PLLGND) 5 pins for Logic and Data outputs (GND)

External Components

The V386 require no external components.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V386. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VCC	-0.3 V to +4 V
CMOS/TTL Output Voltage	-0.3 V to (VCC+0.3 V)
LVDS Receiver Input Voltage	-0.3 V to (VCC+0.3 V)
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature (20 seconds max.)	260°C
Maximum Package Power	1.61 W (V386)
Package Derating	12.4 mW/°C above +25°C
	15 mW/°C above +25°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Ta)	0	25	+70	°C
3.3 V Supply Voltage (VCC)	3	3.3	3.6	V
CMOS/TTL Output Load (C_L)			8	pF
Receiver Input Range (V_{IN})	0		2.4	V
Supply Noise Voltage (V_N)			100	mVpp

Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS/TTL DC Specifications						
Input High Voltage	V_{IH}		2.0		VCC	V
Input Low Voltage	V_{IL}		GND		0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4		VCC	V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
Input Current	I_{IN}	0<V_{IN}<VCC			±10	µA
Output Short Circuit Current	I_{OS}	V_{OUT} = 0V			-60	mA
LVDS Receiver DC Specifications						
Differential Input High Threshold	V_{TH}	V_{CM} = +1.2 V			+100	mV
Differential Input Low Threshold	V_{TL}		-100			mV
Input Current	I_{IN}	V_{IN} = +2.4 V, VCC = 3.6 V			±10	µA
		V_{IN} = 0V, VCC = 3.6 V			±10	µA
Receiver Supply Current						
Receiver Supply Current (worst case)	I_{CCRW}	C_L = 8 pF, worst case pattern (V386), f = 65 MHz			121	mA
		C_L = 8 pF, worst case pattern (V386), f = 85 MHz			140	mA
Receiver Supply Current (16 Grayscale)	I_{CCRG}	C_L= 8 pF, 16 Grayscale pattern, f = 65 MHz			72	mA
		C_L= 8 pF, 16 Grayscale pattern, f = 85 MHz			82	mA
Receiver Supply Current (Power Down)	I_{CCRZ}	Power_Down = Low, Receiver outputs stay low during Power-down mode			400	µA
Receiver Switching Characteristics						
CMOS Low-to-High Transition Time for Data	DLHT	20% to 80% VCC		2	6	ns
CMOS Low-to-High Transition Time for Data	DHLT	80% to 20% VCC		1.8	6	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS Low-to-High Transition Time for Clock	CLHT	20% to 80% VCC		2	6	ns
CMOS Low-to-High Transition Time for Clock	CHLT	80% to 20% VCC		1.8	6	ns
CLKOUT period	RCOP		11.76		40	ns
CLKOUT High Time	RCOH	At 2.0 V	4.5	5	25	ns
CLKOUT Low Time	RCOL	At 0.8 V	4	5	25	ns
Data Setup to CLKOUT	RSRC	At 2.0 V	3.5			ns
Data Hold to CLKOUT	RHRC	At 0.8 V	3.5			ns
RCK+/- to CLKOUT Delay	RCCD	At 85 MHz	5.5	7	9.5	ns
Receiver PLL Setup Time	RPLLS				10	ms
Receiver Power Down Delay	RPDD				10	µs
Receiver Input Strobe Position for Bit0	RSPos0	At 85 MHz, T = 11.76 ns	0.49	0.84	1.19	ns
Receiver Input Strobe Position for Bit1	RSPos1	At 85 MHz, T = 11.76 ns	2.17	2.52	2.87	ns
Receiver Input Strobe Position for Bit2	RSPos2	At 85 MHz, T = 11.76 ns	3.85	4.2	4.55	ns
Receiver Input Strobe Position for Bit3	RSPos3	At 85 MHz, T = 11.76 ns	5.53	5.88	6.23	ns
Receiver Input Strobe Position for Bit4	RSPos4	At 85 MHz, T = 11.76 ns	7.21	7.56	7.91	ns
Receiver Input Strobe Position for Bit5	RSPos5	At 85 MHz, T = 11.76 ns	8.89	9.24	9.59	ns
Receiver Input Strobe Position for Bit6	RSPos6	At 85 MHz, T = 11.76 ns	10.57	10.92	11.27	ns
RxIn Skew Margin (see note and Figure 8)	Rskm	At 85 MHz, T = 11.76 ns	300			ps
		At 65 MHz, T = 15.38 ns	500			ps

Note: The skew margins mean the maximum timing tolerance between the clock and data channel when the receiver still works well. This margin takes into acount the receiver input setup and hold time, and internal clock jitter (i.e., internal data sampling window - RSPos). Thyis margin allows for LVDS transmitter pulse position, interconnect skew, inter-symbol interference and intrinsic channel mismatch which will cause the skew between clock (RC+ and RCK-) and data (RX[n]+ and RX[n]- ; n =0, 1, 2, 3) channels.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		84		°C/W
	θ_{JA}	1 m/s air flow		76		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			50		°C/W

Timing Diagrams

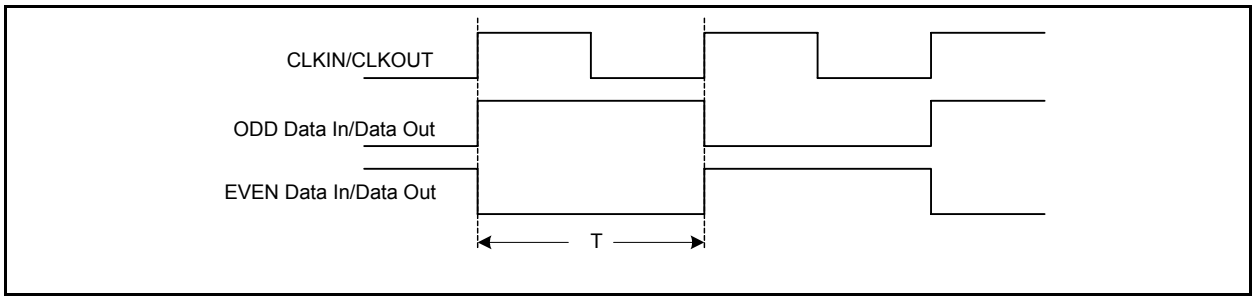


Figure 1a. “Worst Case” Test Pattern

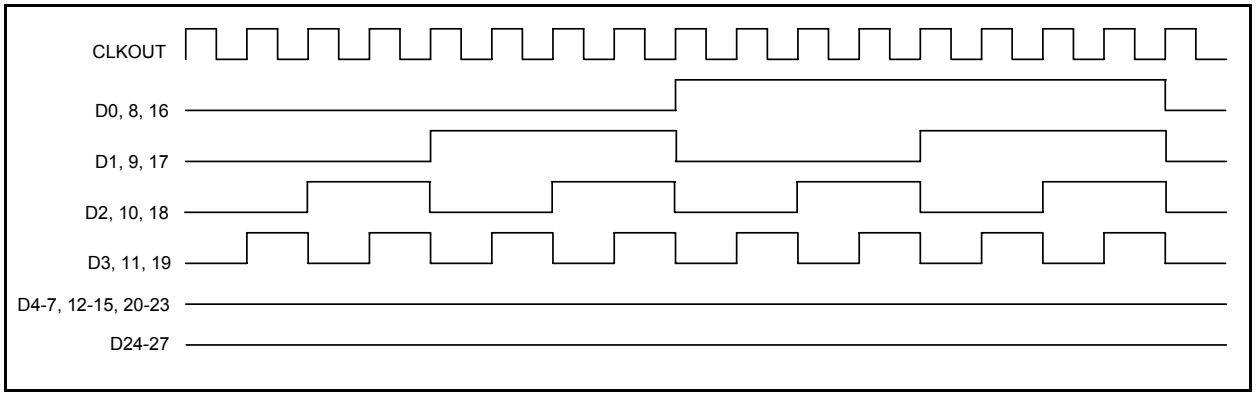


Figure 1b. 16-Grayscale Test-Pattern Waveforms

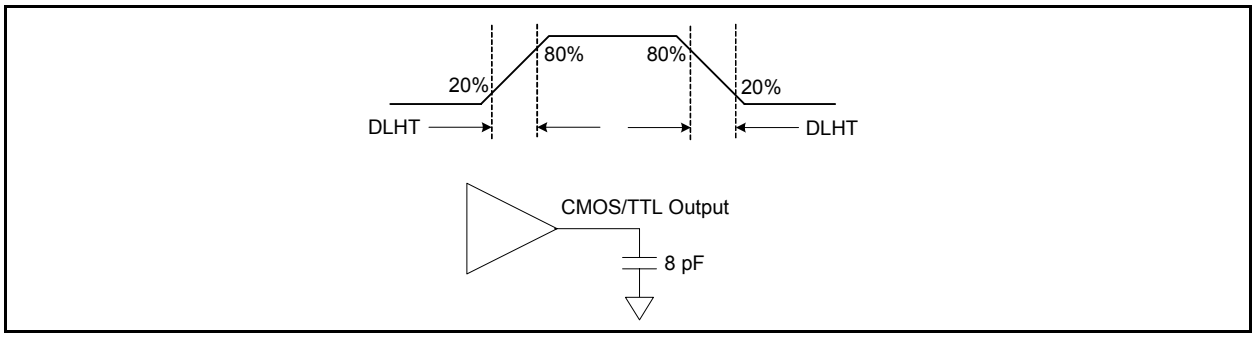


Figure 2. V386 CMOS/TTL Output Load and Transition Time

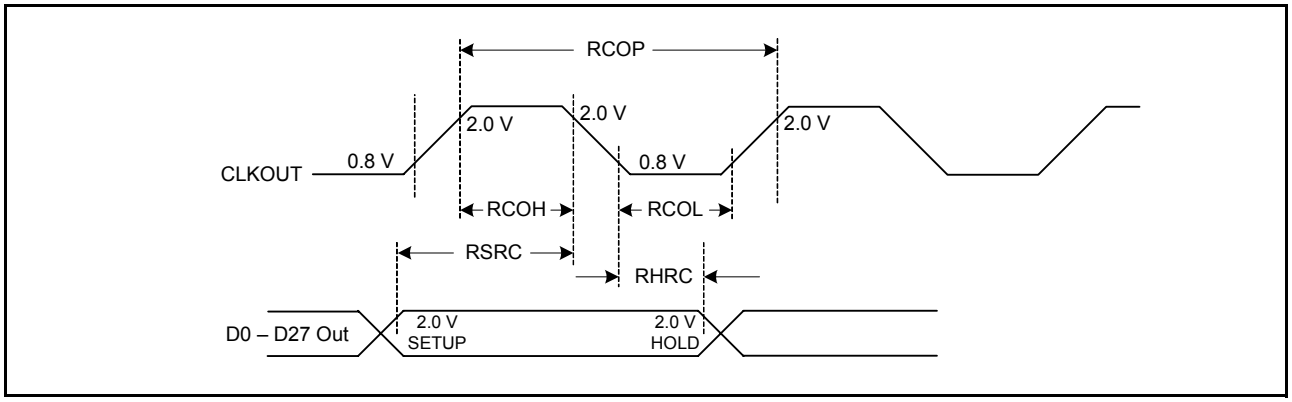


Figure 3. V386 SETUP/HOLD and High/Low Times

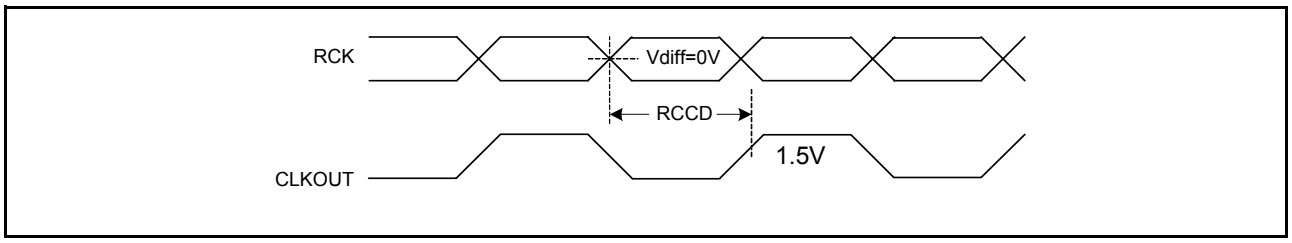


Figure 4. V386 Clock In to Clock Out Delay

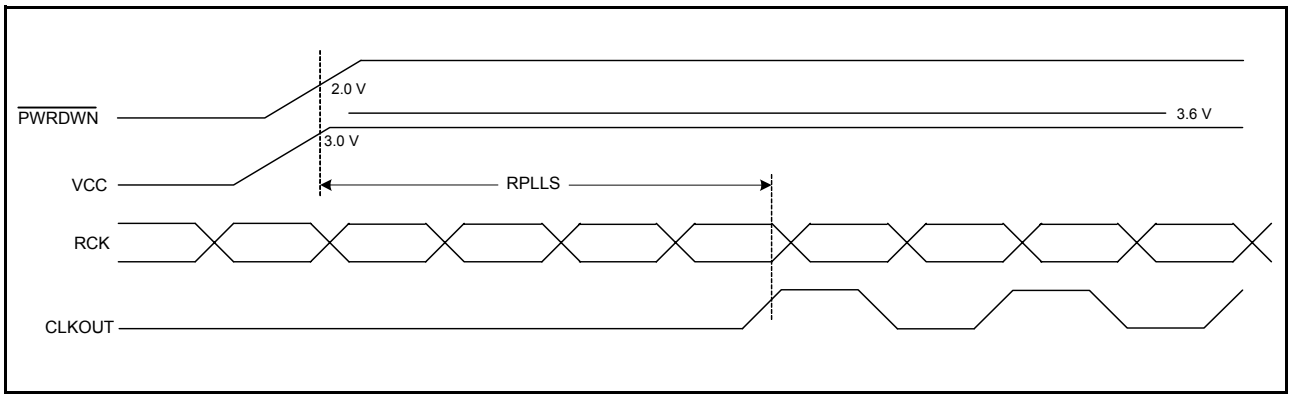


Figure 5. V386 Phase Lock Loop Set Time

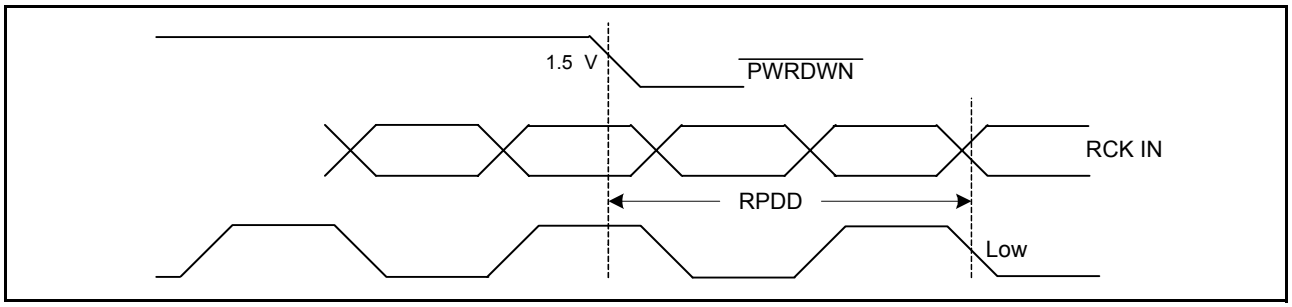


Figure 6. V386 Power Down Delay

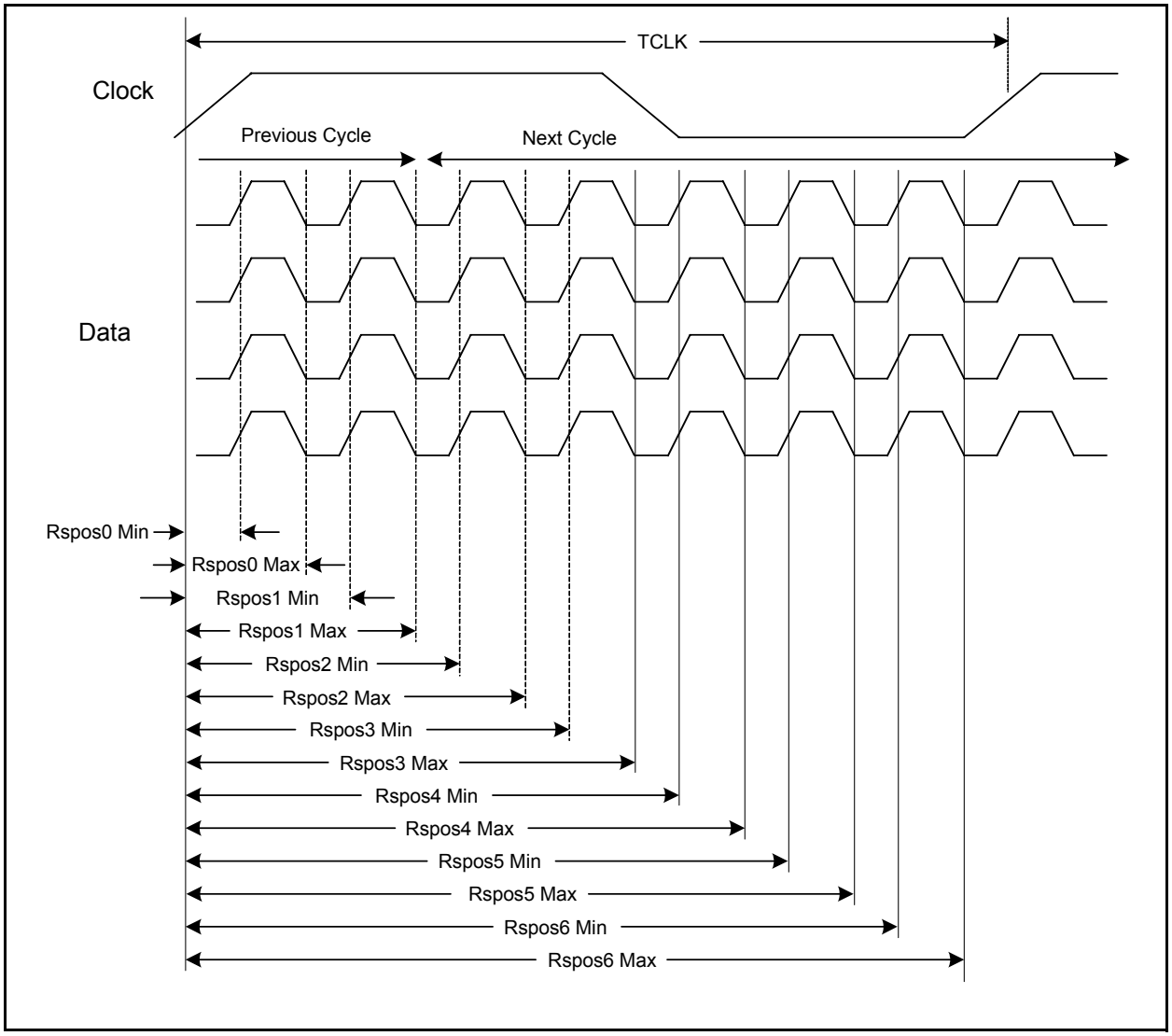


Figure 7. V386 LVDS Input Strobe Position

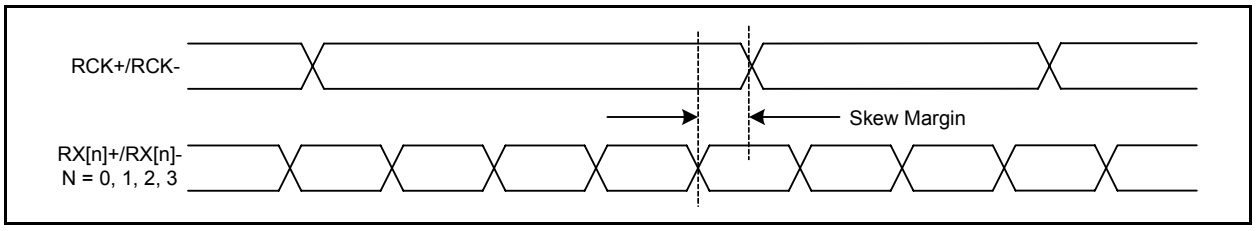
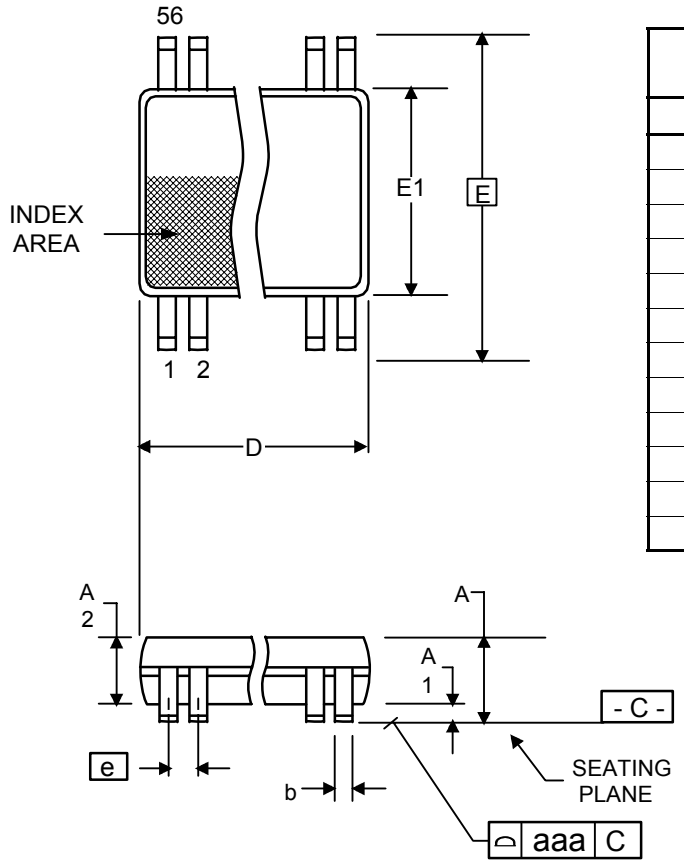


Figure 8. Receiver Input Skew Margin

Package Outline and Package Dimensions (56-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.17	0.27	0.007	0.011
C	0.09	0.20	0.0035	0.008
D	13.90	14.10	0.547	0.555
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	0.236	0.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	0.018	0.030
a	0°	8°	0°	8°
aaa	—	0.10	—	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
V386G	V386G	Tubes	56-pin TSSOP	0 to +70°C
V386GT	V386G	Tape and Reel	56-pin TSSOP	0 to +70°C
V386GLF	V386GLF	Tubes	56-pin TSSOP	0 to +70°C
V386GLFT	V386GLF	Tape and Reel	56-pin TSSOP	0 to +70°C

"LF" denotes Pb (lead) free annealed packaging.