USB Dedicated Charging Port Controller and Current Limiting Power Switch

Check for Samples: TPS2511-Q1

FEATURES

- **Qualified for Automotive Application**
- **AEC-Q100 Qualified with the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HMB ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Supports a DCP Shorting D+ to D–**
- **Supports a DCP Applying 2.0 V on D+ and 2.7 V on D– (or 2.7 V on D+ and 2.0 V on D–)**
- **Supports a DCP Applying 1.2 V on Data Lines**
- **Automatically Switch D+ and D– Lines Connections for an Attached Device**
- **Hiccup Mode for Short-Circuit Protection**
- **Provides $\overline{CS}$ Pin for USB Cable Compensation**
- **Programmable Current Limit (ILIM_SET Pin)**
- **80-mΩ typical High-Side MOSFET**
- **Accurate ±10% Current-Limit at 2.3 A typical**
- **Meets USB Power Switch Requirements**
- **Drop-In and List of materials Compatible with TPS2511**
- **Operating Range: 4.5 V to 5.5 V**
- **Available in MSOP, 8-Pin Package**
- **UL Listed and CB File Number E169910**

APPLICATIONS

- **Vehicle USB Power Charger**
- **AC-DC Wall Adapter with USB Port**
- **Other USB Charger**
- **Automotive Infotainment Systems**

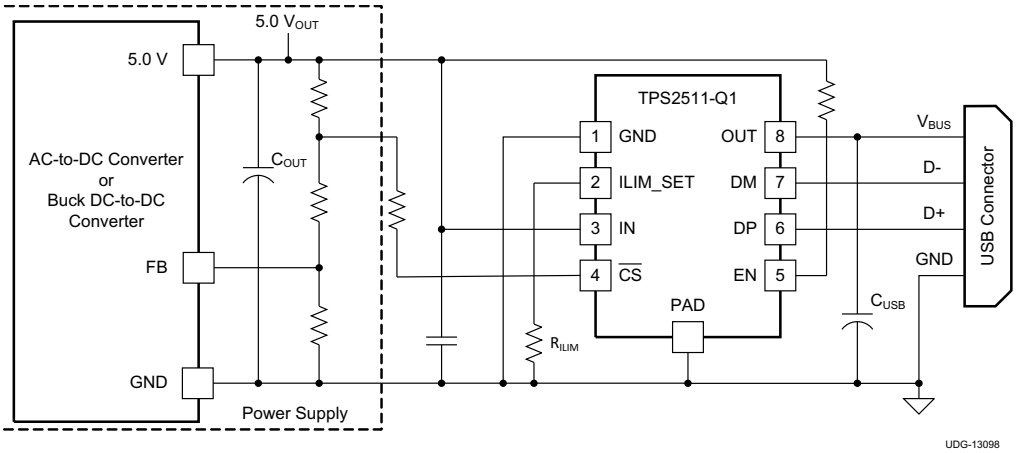
DESCRIPTION

The TPS2511-Q1 is a USB dedicated charging port (DCP) controller and current limiting power switch. An auto-detect feature monitors USB data line voltage, and automatically provides the correct electrical signatures on the data lines to charge compliant devices among the following charging schemes:

- Divider DCP, required to apply 2.7 V on D+ and 2.0 V on D– or 2.0 V on D+ and 2.7 V on D–;
- BC1.2 DCP, required to short D+ to D–;
- 1.2 V on both D+ and D–.

The TPS2511-Q1 is a 80-mΩ power-distribution switch intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device also provides hiccup mode when the output (OUT) voltage is less than 3.80 V typical or when an over-temperature protection occurs during an overload condition. Accurate and programmable current limit provides flexibility and convenience for applications. The TPS2511-Q1 provides a $\overline{CS}$ pin for USB cable resistance compensation and a EN pin to turn on and turn off the device.

SIMPLIFIED APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

$T_A = T_J$	PACKAGE	PINS	TRANSPORT MEDIA	MINIMUM QUANTITY	ORDERABLE DEVICE NUMBER	TOP-SIDE MARKING
–40°C to 125°C	MSOP (DGN)	8	Tube	80	TPS2511QDGNQ1	2511Q
			Tape and Reel	2500	TPS2511QDGNRQ1	2511Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over recommended junction temperature range, voltages are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	IN	–0.3	7	V
Input voltage range	EN, ILIM_SET	–0.3	7	
Voltage range	OUT, $\overline{CS}$	–0.3	7	
	IN to OUT	–7	7	
	DP output voltage, DM output voltage	–0.3	IN+0.3 or 5.7	
	DP input voltage, DM input voltage	–0.3	IN+0.3 or 5.7	
Continuous output sink current	DP input current, DM input current		35	mA
Continuous output source current	DP output current, DM output current		35	
Continuous output sink current	$\overline{CS}$		10	
Continuous output source current	ILIM_SET		Internally limited	
ESD rating	Human Body Model (HBM) QSS 009-105 (JESD22-A114A) and AEC-Q100 Classification Level H2		2	kV
	Charging Device Model (CDM) QSS 009-147 (JESD22-C101B.01) and AEC-Q100 500V Classification Level C3B		750	V
Operating junction temperature, T_J			Internally limited	
Storage temperature range, T_{stg}		–65	150	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2511-Q1 DGN (8 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	65.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.3	
θ_{JB}	Junction-to-board thermal resistance	36.9	
ψ_{JT}	Junction-to-top characterization parameter	3.9	
ψ_{JB}	Junction-to-board characterization parameter	36.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	13.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

voltages are referenced to GND (unless otherwise noted), positive current are into pins.

		MIN	MAX	UNIT
V_{IN}	Input voltage of IN	4.5	5.5	V
$V_{\overline{CS}}$	Input voltage of $\overline{CS}$	0	5.5	
V_{EN}	Input voltage of EN	0	5.5	
V_{DP}	DP data line input voltage	0	5.5	
V_{DM}	DM data line input voltage	0	5.5	
I_{DP}	Continuous sink/source current		±10	mA
I_{DM}	Continuous sink/source current		±10	
$I_{\overline{CS}}$	Continuous sink current		2	
I_{OUT}	Continuous output current of OUT		2.2	A
R_{ILIM_SET}	A resistor of current-limit, ILIM_SET to GND	16.9	750	kΩ
T_J	Operating junction temperature	-40	125	° C

ELECTRICAL CHARACTERISTICS

Conditions are –40°C ≤ (T_J = T_A) ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN} and R_{ILIM_SET} = 22.1 kΩ. Positive current are into pins. Typical values are at 25°C. All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Static drain-source on-state resistance	I_{OUT} = 2 A		80	125	mΩ
		I_{OUT} = 2 A, –40ºC ≤ (T_J =T_A) ≤ 85ºC		80	110	
		I_{OUT} = 2 A, T_J =T_A = 25ºC		80	89	
t_r	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V see Figure 1, Figure 3		1.0	1.5	ms
t_f	OUT voltage fall time	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V see Figure 1, Figure 3	0.2	0.35	0.5	
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = V_{EN} = 0 V		0.01	2	µA
DISCHARGE						
R_{DCHG}	Discharge resistance	V_{OUT} = 4 V	400	500	630	Ω
CURRENT LIMIT						
I_{OS}	OUT short-circuit current limit	R_{ILIM_SET} = 44.2 kΩ	1060	1160	1270	mA
		R_{ILIM_SET} = 22.1 kΩ	2110	2300	2550	
		R_{ILIM_SET} = 16.9 kΩ	2760	3025	3330	
t_{IOS}	Short-circuit response time(1)	V_{IN} = 5.0 V, R_L = 50 mΩ, 2 inches lead length, See Figure 4		1.5		µs
HICCUP MODE						
V_{OUT_SHORT}	OUT voltage threshold of going into hiccup mode	V_{IN} = 5.0 V, R_{ILIIM_SET} = 210 kΩ	3.6	3.8	4.1	V
t_{OS_DEG}	On time of hiccup mode(1)	V_{IN} = 5.0 V, R_L = 0		16		ms
$t_{SC\_TURN\_OFF}$	Off time of hiccup mode(1)	V_{IN} = 5.0 V, R_L = 0		12		s
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	IN UVLO threshold voltage, rising		3.9	4.1	4.3	V
	Hysteresis(1)			100		mV
SUPPLY CURRENT						
I_{IN_OFF}	Disabled, IN supply current	V_{EN} = 0 V, V_{IN} = 5.5 V, –40ºC ≤ T_J ≤ 85ºC		0.1	5	µA
I_{IN_ON}	Enabled, IN supply current	V_{EN} = V_{IN}, R_{ILIM_SET} = 210 kΩ		180	230	

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Conditions are –40°C ≤ (T_J = T_A) ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN} and R_{ILIM_SET} = 22.1 kΩ. Positive current are into pins. Typical values are at 25°C. All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
	Temperature rising threshold(2)	Not in current limit	155			°C
		In current limit	135			
	Hysteresis (2)			10		
OUT CURRENT DETECTION						
I_{HCC_TH}	Load detection current threshold, rising (2)	R_{ILIM_SET} = 22.1 kΩ		1060		mA
		R_{ILIM_SET} = 44.2 kΩ		560		
$I_{HCC\_TH\_HYS}$	Load detection current Hysteresis(2)	R_{ILIM_SET} = 22.1 kΩ		230		mA
		R_{ILIM_SET} = 44.2 kΩ		120		
$V_{\overline{CS}}$	$\overline{CS}$ output active low voltage(2)	$I_{\overline{CS}}$ = 1 mA	0	80	140	mV
t_{CS_EN}	$\overline{CS}$ deglitch time during turning on (2)	$I_{\overline{CS}}$ = 1 mA		8		ms
ENABLE INPUT (EN)						
V_{EN_TRIP}	EN threshold voltage, falling		0.9	1.1	1.65	V
$V_{EN\_TRIP\_HYS}$	Hysteresis		100	200	300	mV
I_{EN}	Leakage current	V_{EN} = 0 V or V_{EN} = 5.5 V	–0.5		0.5	µA
t_{on}	OUT voltage turn-on time	C_L = 1 µF, R_L = 100 Ω, see Figure 1, Figure 2		2.6	5	ms
t_{off}	OUT voltage turn-off time			1.7	3	
BC 1.2 DCP MODE (SHORT MODE)						
R_{DPM_SHORT}	DP and DM shorting resistance	V_{DP} = 0.8 V, I_{DM} = 1 mA		125	200	Ω
R_{DCHG_SHORT}	Resistance between DP/DM and GND	V_{DP} = 0.8 V	400	700	1300	kΩ
$V_{DPL\_TH\_DETACH}$	Voltage threshold on DP under which the device goes back to divider mode		310	330	350	mV
$V_{DPL\_TH\_DETACH\_HYS}$	Hysteresis			50 (2)		mV
DIVIDER MODE						
$V_{DP\_2.7V}$	DP output voltage	V_{IN} = 5.0 V	2.57	2.7	2.84	V
$V_{DM\_2.0V}$	DM output voltage	V_{IN} = 5.0 V	1.9	2.0	2.1	
R_{DP_PAD1}	DP output impedance	I_{DP} = –5 µA	24	30	40	kΩ
R_{DM_PAD1}	DM output impedance	I_{DM} = –5 µA	24	30	40	
1.2 V / 1.2 V MODE						
$V_{DP\_1.2V}$	DP output voltage	V_{IN} = 5.0 V	1.12	1.2	1.28	V
$V_{DM\_1.2V}$	DM output voltage	V_{IN} = 5.0 V	1.12	1.2	1.28	V
R_{DP_PAD2}	DP output impedance	I_{DP} = –5 uA	80	105	130	kΩ
R_{DM_PAD2}	DM output impedance	I_{DM} = –5 uA	80	105	130	kΩ

(2) Specified by design. Not production tested.

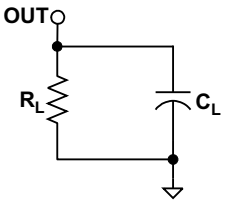


Figure 1. Output Rise and Fall Test Load

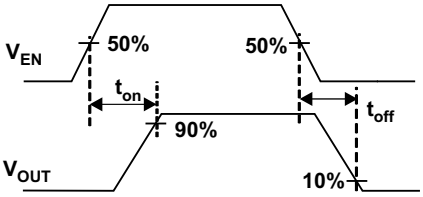


Figure 2. Enable Timing, Active High Enable

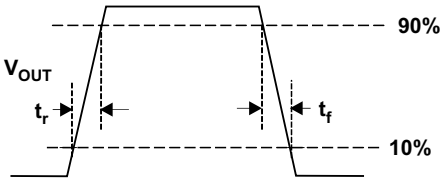


Figure 3. Power-On and Off

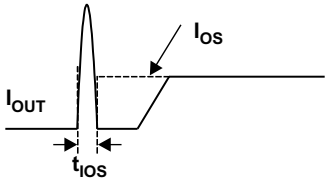
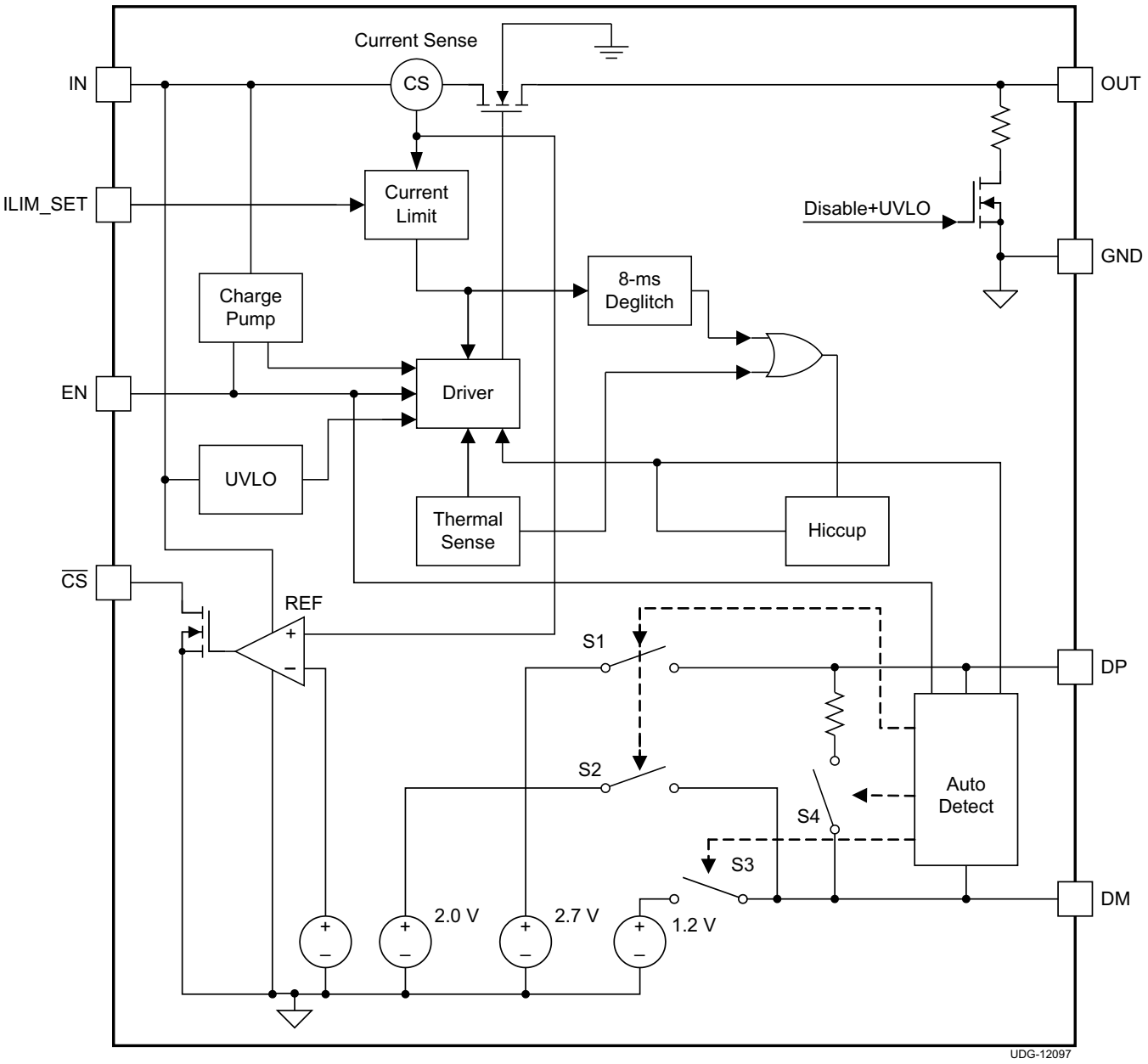


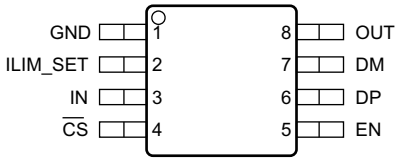
Figure 4. Output Short-Circuit Parameters

FUNCTIONAL BLOCK DIAGRAM



DEVICE INFORMATION

DGN PACKAGE (MSOP)
8 PINS
(Top View)



PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{CS}$	4	O	Active low open -drain output, when OUT current is more than approximately half of the current limit set by a resistor on ILIM_SET pin, the output is active low. Maximum sink current is 10 mA.
DM	7	I/O	Connected to the D– or D+ line of USB connector, provide the correct voltage with an attached portable equipment for DCP detection, high impedance while disabled.
DP	6	I/O	Connected to the D+ or D– line of USB connector, provide the correct voltage with an attached portable equipment for DCP detection, high impedance while disabled.
EN	5	I	Logic-level control input, when it is high, turns power switch on, when it is low, turns power switch off and turns DP and DM into the high impedance state.
GND	1	G	Ground connection.
ILIM_SET	2	I	External resistor used to set current-limiting threshold, recommended 16.9 kΩ ≤ R_{ILIM_SET} ≤ 750 kΩ.
IN	3	P	Power supply. Input voltage connected to power switch, connect a ceramic capacitor with a value of 0.1-µF or greater from the IN pin to GND as close to the device as possible.
OUT	8	O	Power-switch output. Connect to VBUS of USB
PowerPAD		G	Ground connection.

(1) G = Ground, I = Input, O = Output, P = Power

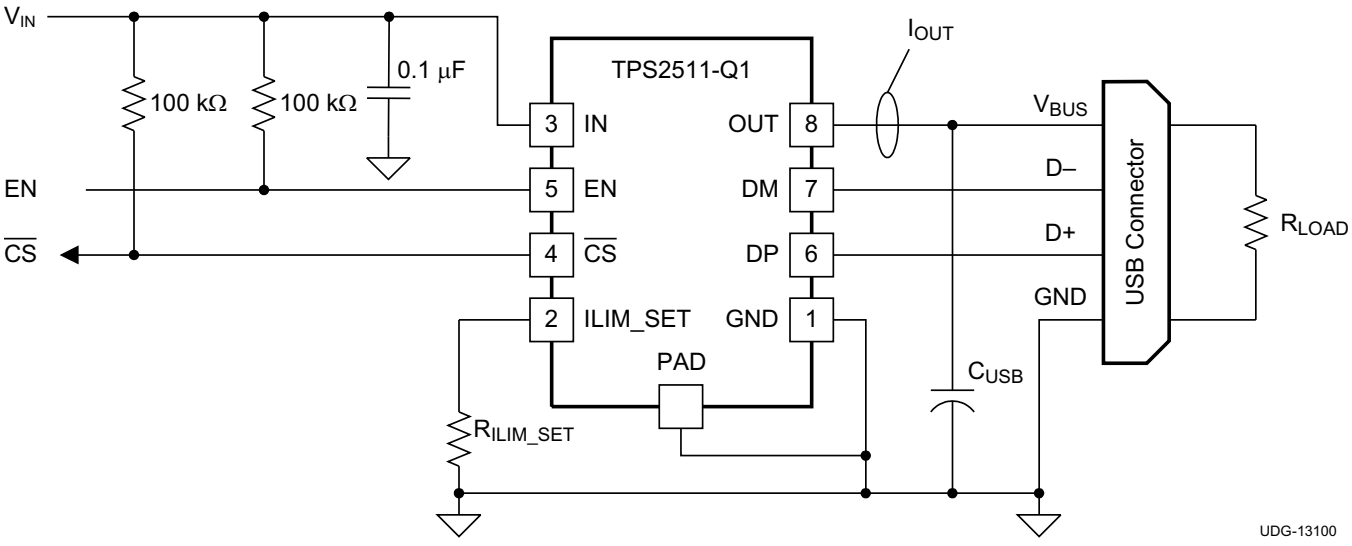


Figure 5. Test Circuit for System Operation in Typical Characteristics Section

TYPICAL CHARACTERISTICS

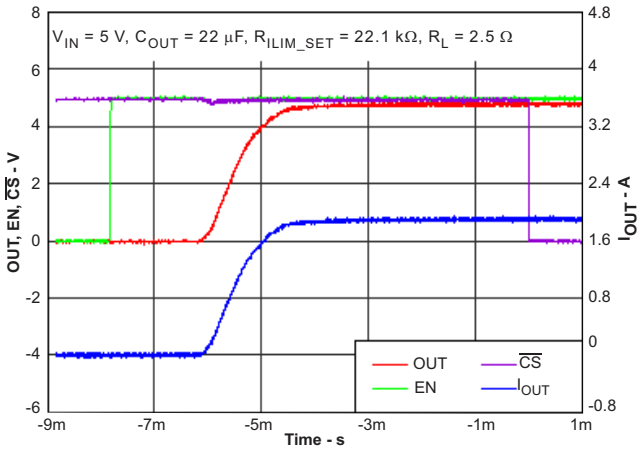


Figure 6. Turn on Delay and Rise Time With 22-µF Load

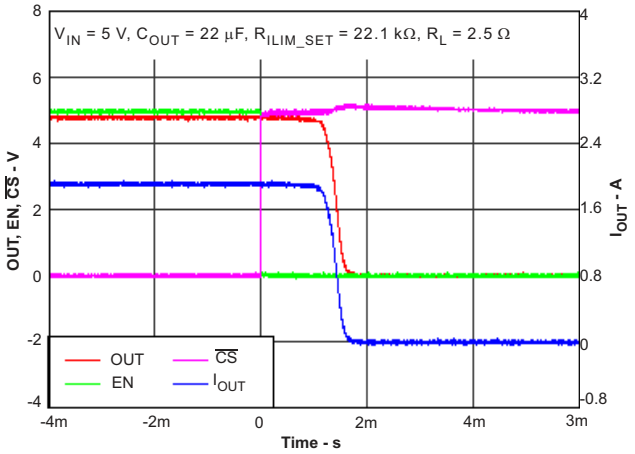


Figure 7. Turn off Delay and Fall Time With 22-µF Load

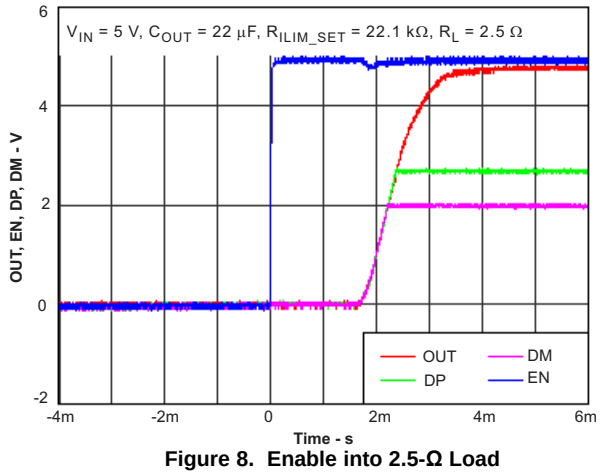


Figure 8. Enable into 2.5-Ω Load

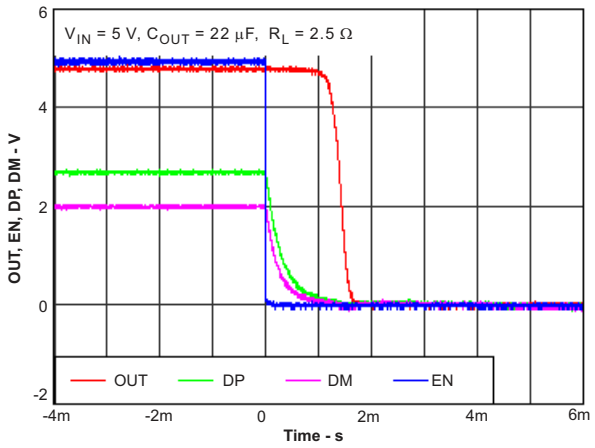


Figure 9. Disable with 2.5-Ω Load

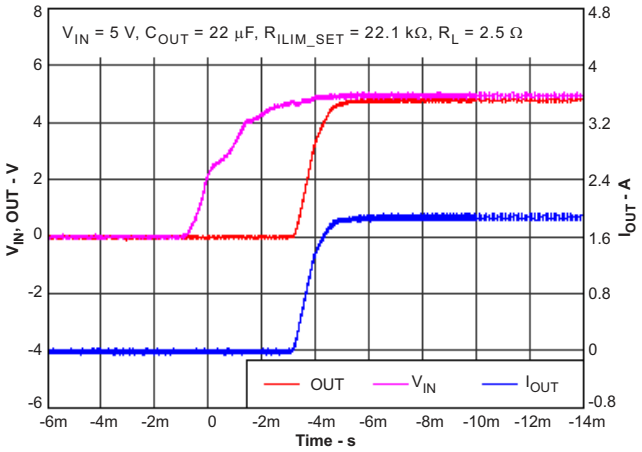


Figure 10. Power Up – Enabled

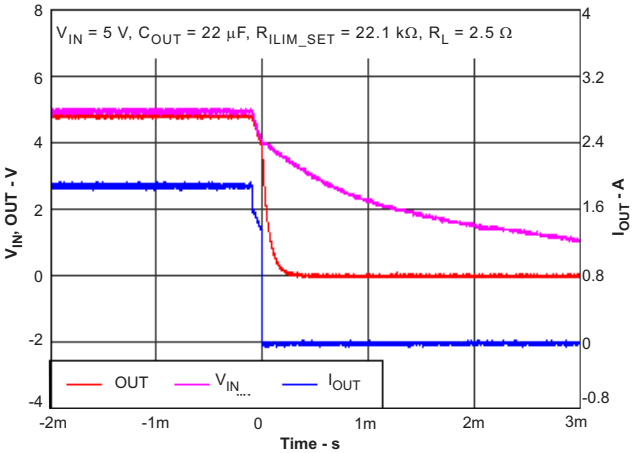


Figure 11. Power Down – Enabled

TYPICAL CHARACTERISTICS (continued)

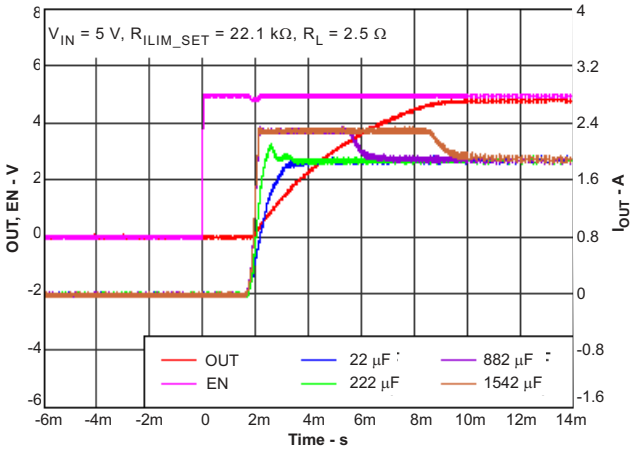


Figure 12. Inrush Current with Different Capacitance Load

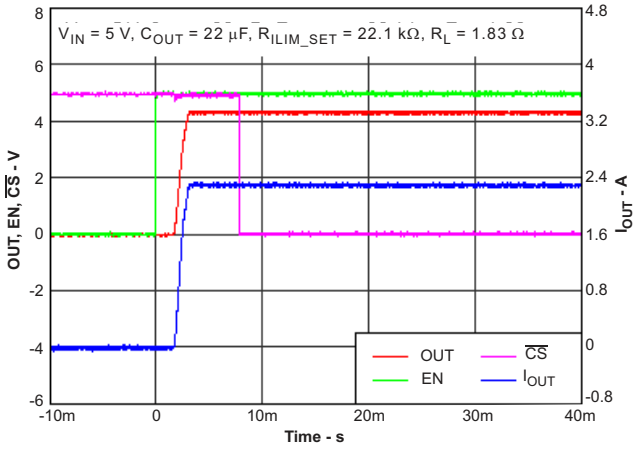


Figure 13. Enable into 1.83-ΩLoad

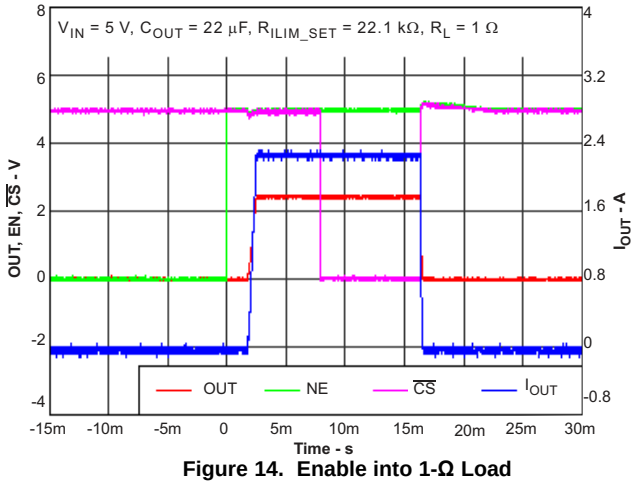


Figure 14. Enable into 1-Ω Load

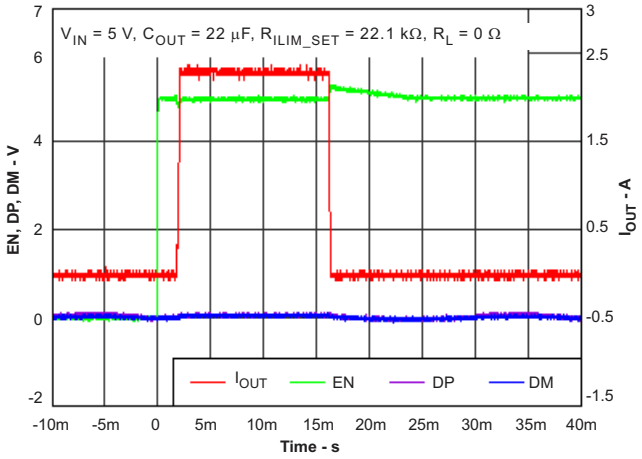


Figure 15. Enable into Short

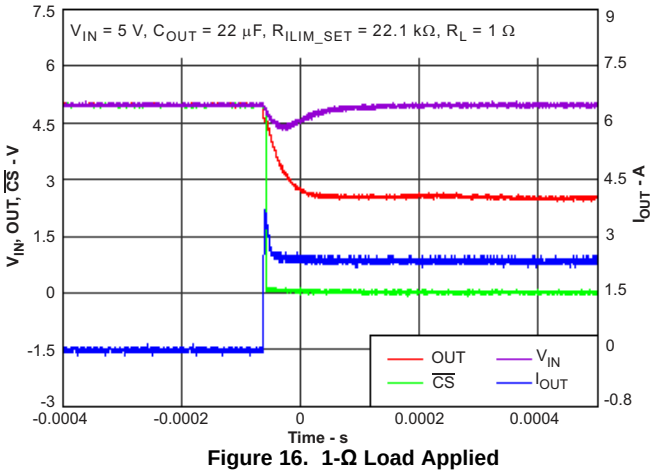


Figure 16. 1-Ω Load Applied

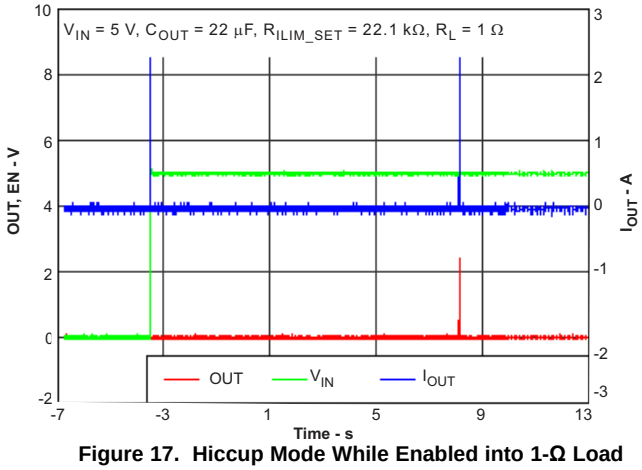


Figure 17. Hiccup Mode While Enabled into 1-Ω Load

TYPICAL CHARACTERISTICS (continued)

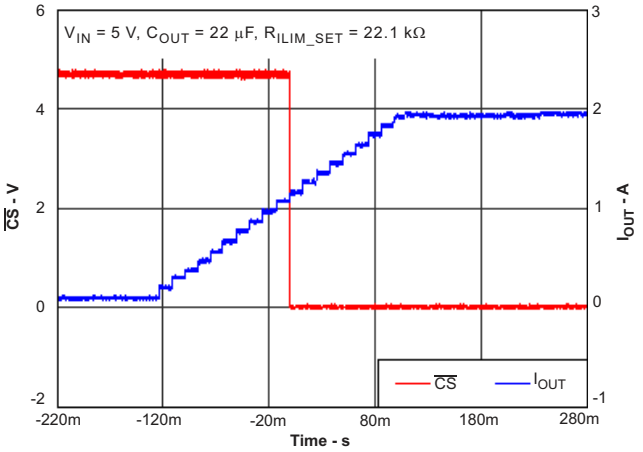


Figure 18. Output Current Sensing Report

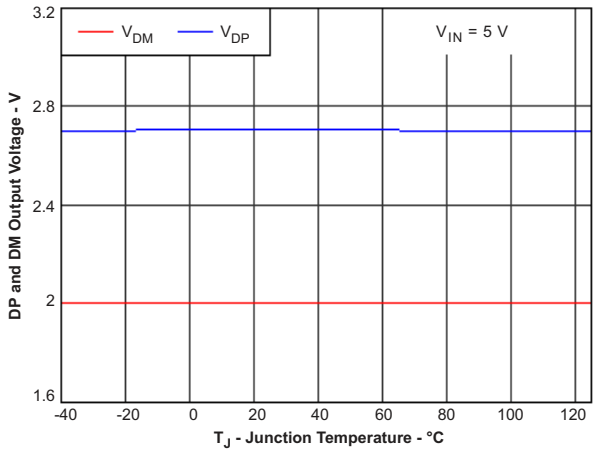


Figure 19. DP and DM Output Voltage vs Temperature

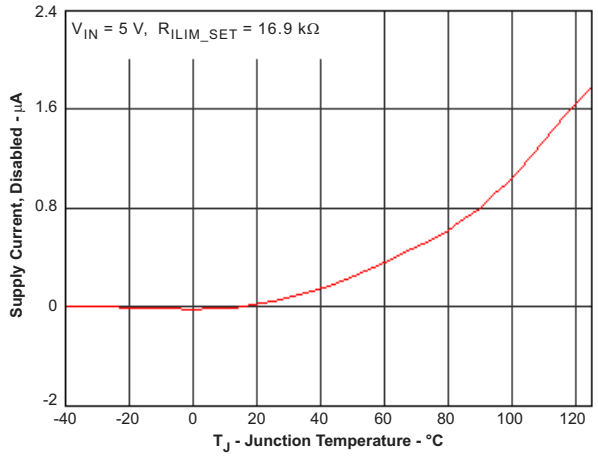


Figure 20. Supply Current Disabled vs Temperature

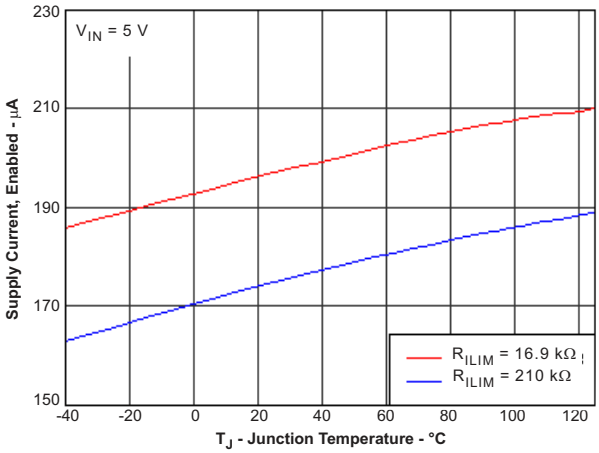


Figure 21. Supply Current Enabled vs Temperature

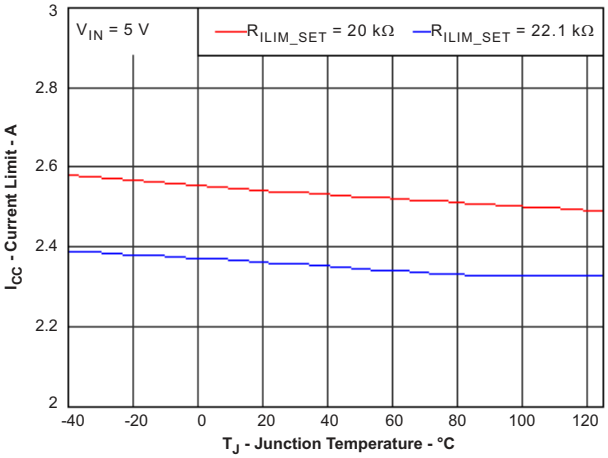


Figure 22. Current Limit vs Temperature

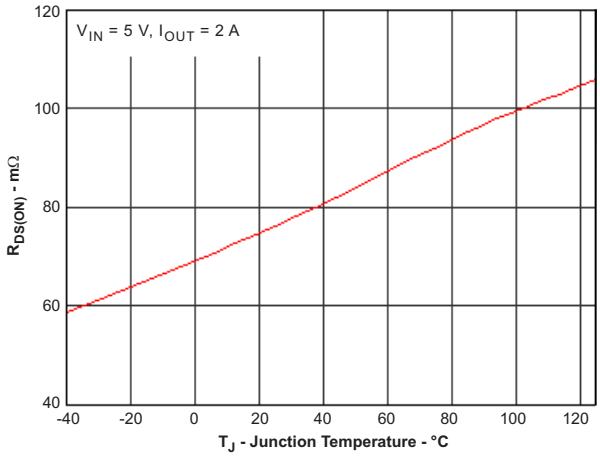


Figure 23. Power Switch On-Resistance ($R_{DS(ON)}$) vs Temperature

DETAILED DESCRIPTION

Overview

The following overview references various industry standards. It is always recommended to consult the latest standard to ensure the most recent and accurate information.

Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are convenient locations for charging because of an available 5-V power source. Universally accepted standards are required to ensure host and client-side devices meet the power management requirements. Traditionally, USB host ports following the USB 2.0 Specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate the power allotment from the host to guarantee the total current draw does not exceed 500 mA. The TPS2511-Q1 provides 100 mA of current to each USB device. Each USB device can subsequently request more current, which is granted in steps of 100 mA up 500 mA total.. The host may grant or deny the request based on the available current.

Additionally, the success of the USB technology makes the micro-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector.

One common difficulty has resulted from this. As USB charging has gained popularity, the 500-mA minimum defined by the USB 2.0 Specification or 900 mA defined in the USB 3.0 Specification, has become insufficient for many handsets, tablets and personal media players (PMP) which have a higher rated charging current. Wall adapters and car chargers can provide much more current than 500 mA or 900 mA to fast charge portable devices. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500 mA (defined in the USB 2.0 Specification) or 900 mA (defined in the USB 3.0 Specification) minimum while using a single micro-USB input connector.

The TPS2511-Q1 supports three of the most common protocols:

- USB Battery Charging Specification, Revision 1.2 (BC1.2)
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode

In these protocols there are three types of charging ports defined to provide different charging current to client-side devices. These charging ports are defined as:

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

The BC1.2 Specification defines a charging port as a downstream facing USB port that provides power for charging portable equipment.

Table 1 shows different port operating modes according to the BC1.2 Specification.

Table 1. Operating Modes Table

PORT TYPE	SUPPORTS USB 2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

The BC1.2 Specification defines the protocol necessary to allow portable equipment to determine what type of port it is connected to so that it can allot its maximum allowable current drawn. The hand-shaking process is two steps. During step one, the primary detection, the portable equipment outputs a nominal 0.6 V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to a SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

The second step, the secondary detection, is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being remains is less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

Dedicated Charging Port (DCP)

A dedicated charging port (DCP) is a downstream port on a device that outputs power through a USB connector, but is not capable of enumerating a downstream device, which generally allows portable devices to fast charge at their maximum rated current. A USB charger is a device with a DCP, such as a wall adapter or car power adapter. A DCP is identified by the electrical characteristics of its data lines. The following DCP identification circuits are usually used to meet the handshaking detections of different portable devices.

Short the D+ Line to the D– Line

The USB BC1.2 Specification and the Chinese Telecommunications Industry Standard YD/T 1591-2009 define that the D+ and D– data lines should be shorted together with a maximum series impedance of 200 Ω. This is shown in Figure 24.

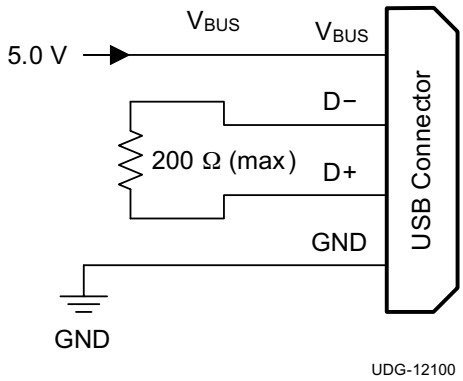


Figure 24. DCP Short Mode

Divider1 (DCP Applying 2.0 V on D+ Line and 2.7 V on D– Line) or Divider2 (DCP Applying 2.7 V on D+ Line and 2.0 V on D– Line)

There are two charging schemes for divider DCP. They are named after Divider1 and Divider2 DCPs that are shown in Figure 25 and Figure 26. The Divider1 charging scheme is used for 5-W adapters, Divider1 applies 2.0 V to the D+ line and 2.7 V to the D– data line. The Divider2 charging scheme is used for 10-W adapters and applies 2.7 V on the D+ line and 2.0 V is applied on the D– line.

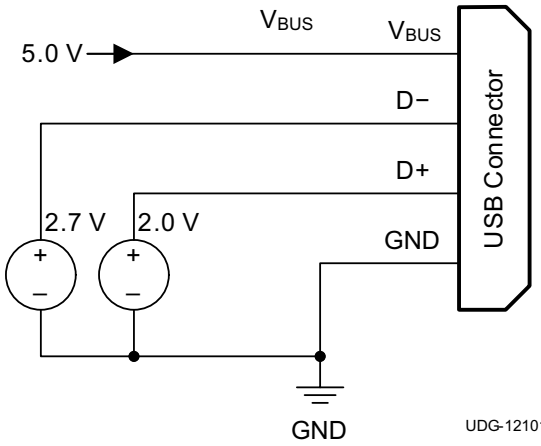


Figure 25. Divider1 DCP

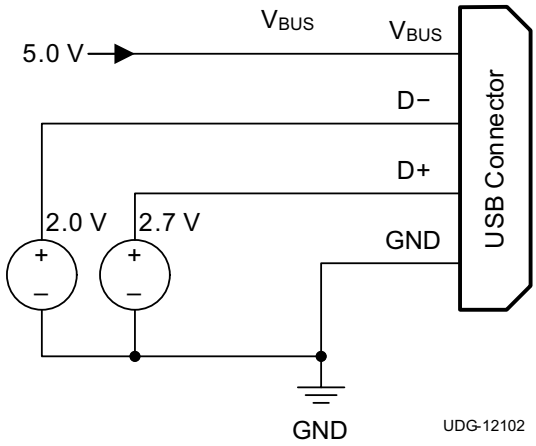


Figure 26. Divider2 DCP

Applying 1.2 V to the D+ Line and 1.2 V to the D– Line

As shown in Figure 27, some tablet USB chargers require 1.2 V on the shorted data lines of the USB connector. The maximum resistance between the D+ line and the D- line is 200 Ω.

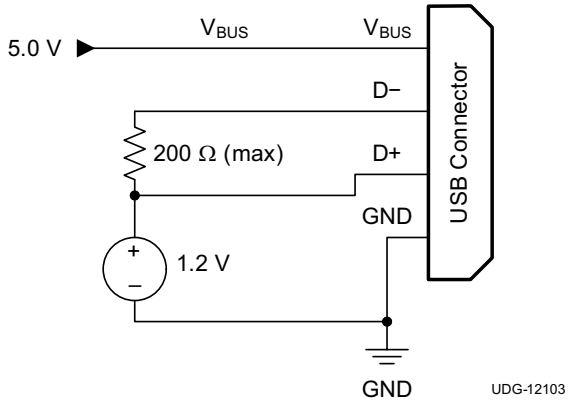


Figure 27. DCP Applying 1.2 V to the D+ Line and 1.2 V to the D– Line

The TPS2511-Q1 is a combination of a current-limiting USB power switch and an USB DCP identification controller. Applications include vehicle power charger, wall adapters with USB DCP and other USB chargers. The TPS2511-Q1 DCP controller has the auto-detect feature that monitors the D+ and D– line voltages of the USB connector, providing the correct electrical characteristics on the DP and DM pins for the correct detections of compliant portable devices to fast charge. These portable devices include smart phones, 5-V tablets and personal media players.

The TPS2511-Q1 power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered, incorporating a 70-mΩ, N-channel MOSFET in a single package. This device provides hiccup mode when in current limit and OUT voltage is less than 3.8 V (typ) or an over temperature protection occurs under an overload condition. Hiccup mode operation can reduce the output short-circuit current down to several milliamperes. The TPS2511-Q1 provides a logic-level enable EN pin to control the device turn-on and tuen-off and an open drain output $\overline{CS}$ for compensating V_{BUS} to account for cable I × R voltage loss.

DCP *Auto-Detect*

The TPS2511-Q1 integrates an *auto-detect* feature to support divider mode, short mode and 1.2 V / 1.2 V mode. If a divider device is attached, 2.7 V is applied to the DP pin and 2.0 V is applied to the DM pin. If a BC1.2-compliant device is attached, the TPS2511-Q1 automatically switches into short mode. If a device compliant with the 1.2 V / 1.2 V charging scheme is attached, 1.2 V is applied on both the DP pin and the DM pin. The functional diagram of DCP auto-detect feature is shown in Figure 28.

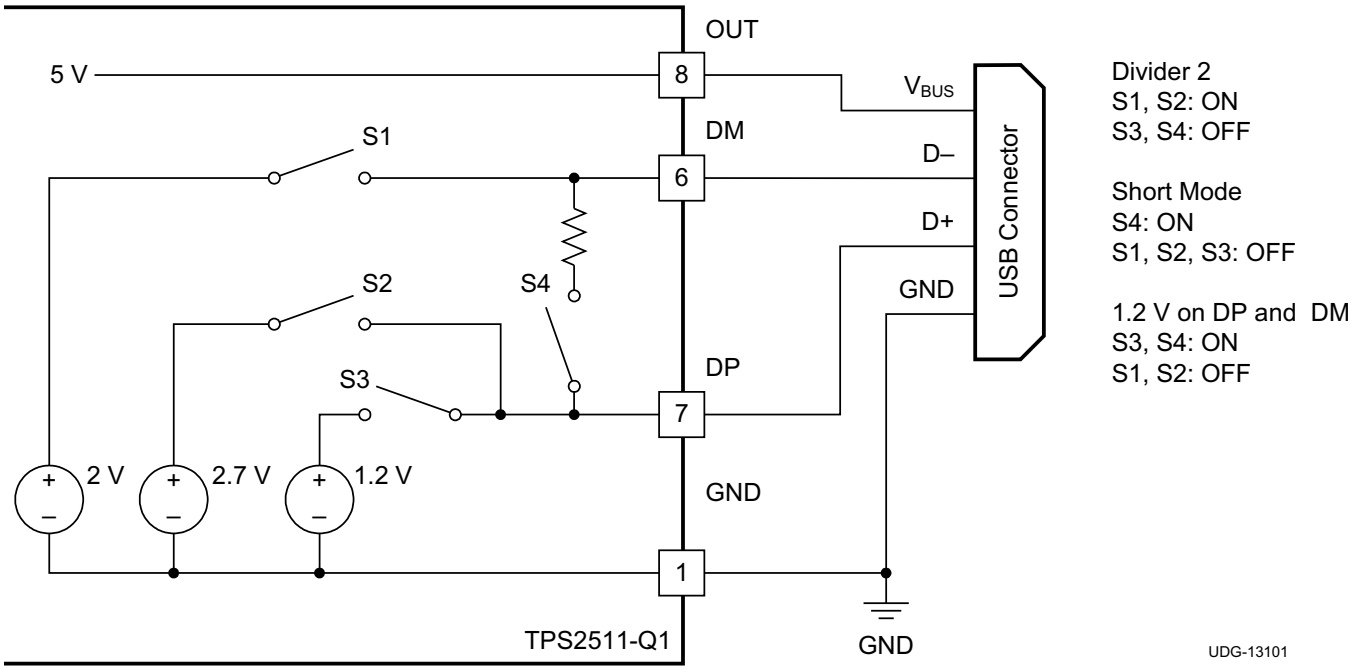


Figure 28. TPS2511-Q1 DCP Auto-Detect Functional Diagram

Overcurrent Protection

During an overload condition, the TPS2511-Q1 maintains a constant output current and reduces the output voltage accordingly. If the output voltage falls below 3.8 V for 16 ms, the TPS2511-Q1 turns off the output for a period of 12 seconds as shown in Figure 29. This operation is referred to as hiccup mode. The device stays in hiccup mode (power cycling) until the overload condition is removed. Therefore the average output current is significantly reduced to greatly improve the thermal stress of the device while the OUT pin is shorted.

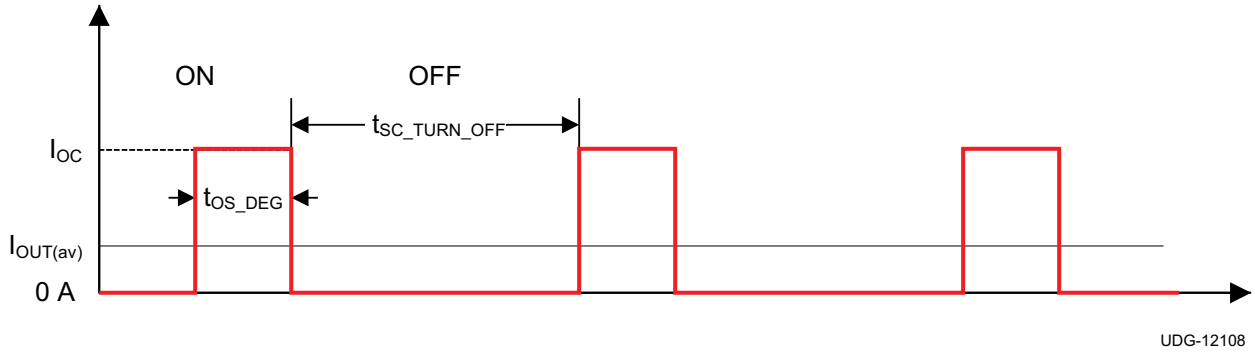


Figure 29. OUT Pin Short-Circuit Current in Hiccup Mode

Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before the voltage of IN has been applied. The TPS2511-Q1 senses the short and immediately switches into hiccup mode of constant-current limiting. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for several microseconds before the current-limit circuit can react. The device operates in constant-current mode for a period of 16 ms after the current-limit circuit has responded, then switches into hiccup mode (power cycling).

Current-Limit Threshold

The TPS2511-Q1 has a current-limiting threshold that is externally programmed with a resistor. Equation 1 and Figure 30 help determine the typical current-limit threshold:

$$I_{OS\_TYP} = \frac{51228}{R_{ILIM}} \quad (1)$$

where

- I_{OS_TYP} is in mA and R_{ILIM} is in kΩ
- I_{OS_TYP} has a better accuracy if R_{ILIM} is less than 210 kΩ

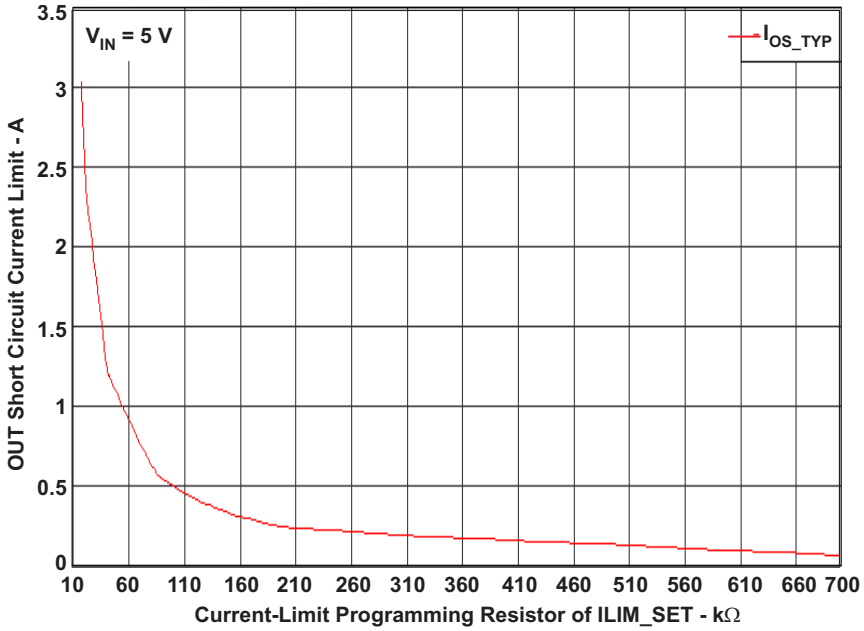


Figure 30. Typical Current Limit vs Programming Resistor

Current Sensing Report ($\overline{CS}$)

The $\overline{CS}$ open-drain output is asserted immediately when the OUT pin current is more than about half of the current limit set by a resistor on ILIM_SET pin. Built-in hysteresis improves the ability to resist current noise on the OUT pin. The $\overline{CS}$ output is active low. The recommended operating sink current is less than 2 mA and maximum sink current is 10 mA.

Undervoltage Lockout (UVLO) and Enable (EN)

The undervoltage lockout (UVLO) circuit disables the power switch and other functional circuits until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

The logic input of the EN pin disables all of the internal circuitry while maintaining the power switch off. A logic-high input on the EN pin enables the driver, control circuits, and power switch. The EN input voltage is compatible with both TTL and CMOS logic levels.

Soft-Start, Reverse Blocking and Discharge Output

The power MOSFET driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The TPS2511-Q1 power switch blocks current from the OUT pin to the IN pin when turned off by the UVLO or disabled. The TPS2511-Q1 includes an output discharge function. A 500-Ω (typ.) discharge resistor dissipates stored charge and leakage current on the OUT pin when the device is in UVLO or disabled. However as this circuit is biased from the IN pin, the output discharge is not active when the input approaches 0 V.

Thermal Sense

The TPS2511-Q1 provides thermal protection from two independent thermal sensing circuits that monitor the operating temperature of the power distribution switch and turn off for 12 seconds (typ) if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition and OUT pin voltage is above 3.8 V (typ), which has a relatively large voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during the over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the device is within the current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled approximately 10°C. The switch continues to cycle off and on until the fault is removed.

APPLICATION INFORMATION

Programming the Current Limit Threshold

The user-programmable R_{ILIM} resistor on the ILIMIT_SET pin sets the current limit. The TPS2511-Q1 uses an internal regulation loop to provide a regulated voltage on the ILIM_SET pin. The current-limiting threshold is proportional to the current sourced out of the ILIM_SET pin. The recommended 1% resistor range for R_{ILIM} is between 16.9 kΩ and 750 kΩ to ensure stability of the internal regulation loop, although not exceeding 210 kΩ results in a better accuracy. Many applications require that the minimum current limit remain above a certain current level or that the maximum current limit remain below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The Equation 2 and Equation 3 calculate the resulting overcurrent thresholds for a given external resistor value (R_{ILIM}). The traces routing the R_{ILIM} resistor to the TPS2511-Q1 should be as short as possible to reduce parasitic effects on the current limit accuracy. The equations and the graph below can be used to estimate the minimum and maximum variation of the current limit threshold for a predefined resistor value. This variation disregards the inaccuracy of the resistor itself.

$$I_{OS\_MIN} = \frac{51228}{R_{ILIM}^{1.030}} \quad (2)$$

where

- I_{OS_MIN} is in mA
- R_{ILIM} is in kΩ

$$I_{OS\_MAX} = \frac{51228}{R_{ILIM}^{0.967}} \quad (3)$$

where

- I_{OS_MAX} is in mA
- R_{ILIM} is in kΩ

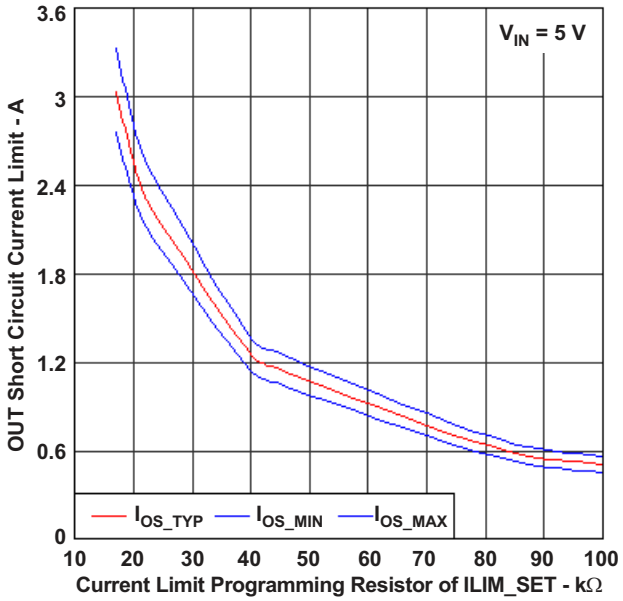


Figure 31. Current Limit Threshold vs Current Limit Resistance

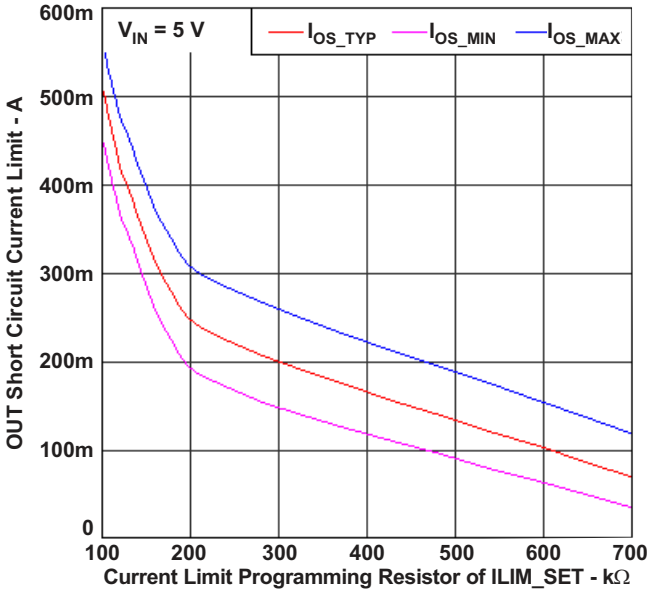


Figure 32. Current Limit Threshold vs Current Limit Resistance

Current Limit Setpoint Example

In the following example, choose the ILIM_SET resistor to ensure that TPS2511-Q1 does not trip off under worst case conditions of current limit and resistor tolerance (assume 1% resistor tolerance). For this example, I_{OS_MIN} = 2100 mA.

$$I_{OS\_MIN} = \frac{51228}{R_{ILIM}^{1.03}} = 2100 \text{ mA} \tag{4}$$

$$R_{ILIM} = \left(\frac{51228}{I_{OS\_MIN}}\right)^{\frac{1}{1.03}} = \left(\frac{51228}{2100}\right)^{\frac{1}{1.03}} = 22.227 \text{ k}\Omega \tag{5}$$

Including resistor tolerance, target nominal resistance value:

$$R_{ILIM} = \frac{22.227 \text{ k}\Omega}{1.01 \text{ k}\Omega} = 22.007 \text{ k}\Omega \tag{6}$$

Choose:

$$R_{ILIM} = 22.0 \text{ k}\Omega \tag{7}$$

V_{BUS} Voltage Drop Compensation

Figure 33 shows a USB charging design using the TPS2511-Q1. In general V_{BUS} has some voltage loss due to USB cable resistance and TPS2511-Q1 power switch on-state resistance. The sum of voltage loss is likely several hundred millivolts from $5V_{OUT}$ to V_{PD_IN} that is the input voltage of PD while the high charging current charges the PD. For example, in Figure 34, assuming that the loss resistance is 170 mΩ (includes 100 mΩ of USB cable resistance and 70 mΩ of power switch resistance) and $5V_{OUT}$ is 5.0 V, the input voltage of PD (V_{PD_IN}) is about 4.66 V at 2.0 A. (see Figure 34)

The charging current of most portable devices is less than their maximum charging current while V_{PD_IN} is less than the certain voltage value. Furthermore actual charging current of PD decreases with input voltage falling. Therefore, a portable devices cannot accomplish a fast charge with its maximum charging rated current if V_{BUS} voltage drop across the power path is not compensated at the high charging current. The TPS2511-Q1 provides $\overline{CS}$ pin to report the high charging current for USB chargers to increase the $5V_{OUT}$ voltage. This is shown by the solid lines of Figure 34.

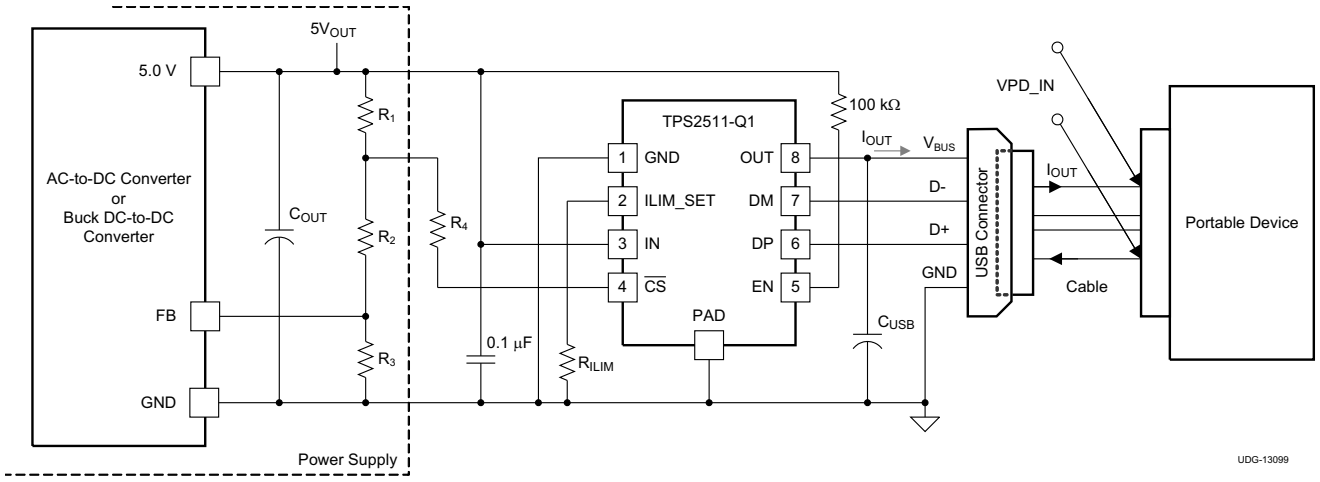


Figure 33. TPS2511-Q1 Charging System Schematic Diagram

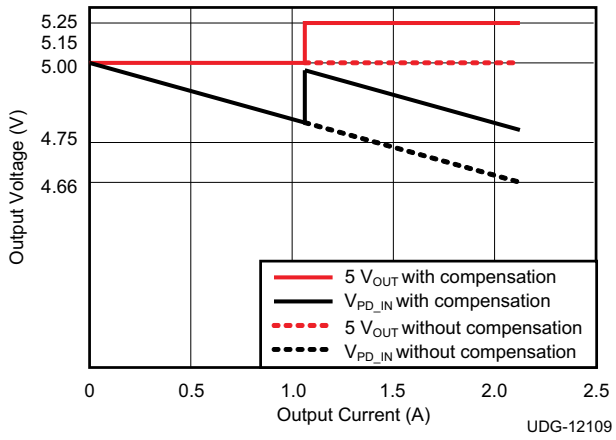


Figure 34. TPS2511-Q1 $\overline{CS}$ Function

Equation 8 through Equation 11 refer to Figure 33.

The power supply output voltage is calculated in Equation 8.

$$5V_{OUT} = \frac{(R_1 + R_2 + R_3) \times V_{FB}}{R_3} \tag{8}$$

$5V_{OUT}$ and V_{FB} are known. If R_3 is given and R_1 is fixed, R_2 can be calculated. The $5V_{OUT}$ voltage change with compensation is shown in Equation 9 and Equation 10.

$$\Delta V = \frac{(R_2 + R_3) \times R_1 \times V_{FB}}{R_3 \times R_4} \tag{9}$$

$$\Delta V = \left(\frac{5V_{OUT}}{V_{FB}} - \frac{R_1}{R_3} \right) \frac{R_1 \times V_{FB}}{R_4} \tag{10}$$

If R_1 is less than R_3, then Equation 10 can be simplified as Equation 11.

$$\Delta V \approx \frac{5V_{OUT} \times R_1}{R_4} \tag{11}$$

Divide Mode Selection of 5-W and 10-W USB Chargers

The TPS2511-Q1 provides two types of connections between the DP pin and the DM pin and between the D+ data line and the D– data line of the USB connector for a 5-W USB charger and a 10-W USB charger with a single USB port. For a 5-W USB charger, the DP pin is connectd to the D– line and the DM pin is connected to the D+ line. This is shown in Figure 37 and Figure 38. It is necessary to apply DP and DM to D+ and D– of USB connector for 10-W USB chargers. See Figure 35 and Figure 36. Table 2. shows different charging schemes for both 5-W and 10-W USB charger solutions

Table 2. Charging Schemes for 5-W and 10-W USB Chargers

USB CHARGER TYPE	CONTAINING CHARGING SCHEMES		
5-W	Divider1	1.2 V on both D+ and D– Lines	BC1.2 DCP
10-W	Divider2	1.2 V on both D+ and D– Lines	BC1.2 DCP

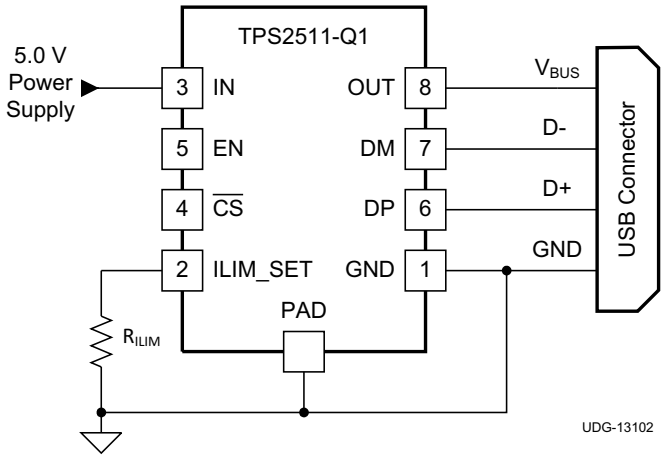


Figure 35. 10-W USB Charger Application with Power Switch

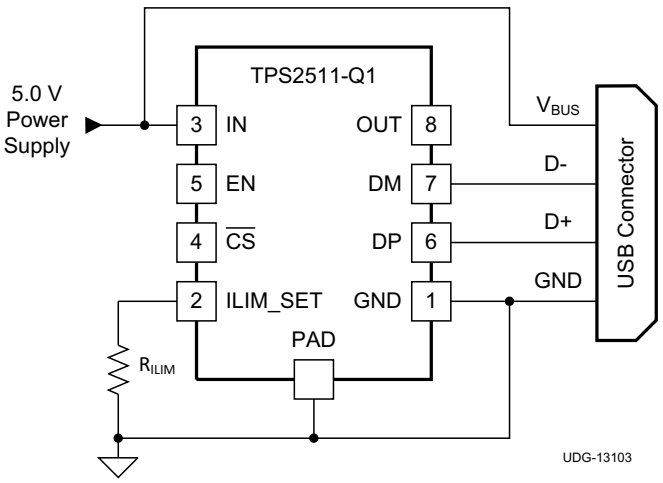


Figure 36. 10-W USB Charger Application without Power Switch

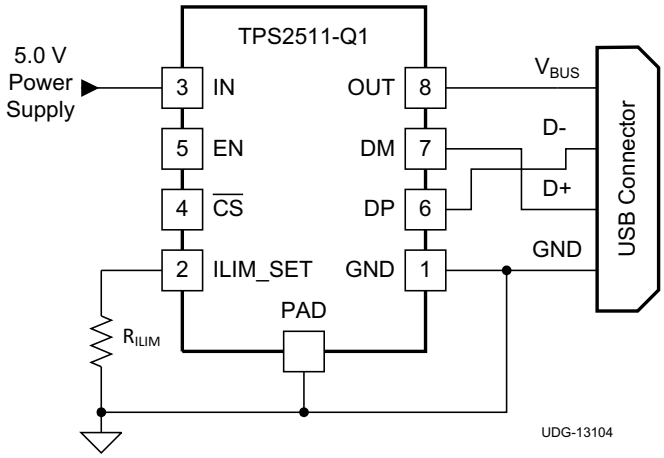


Figure 37. 5-W USB Charger Application with Power Switch

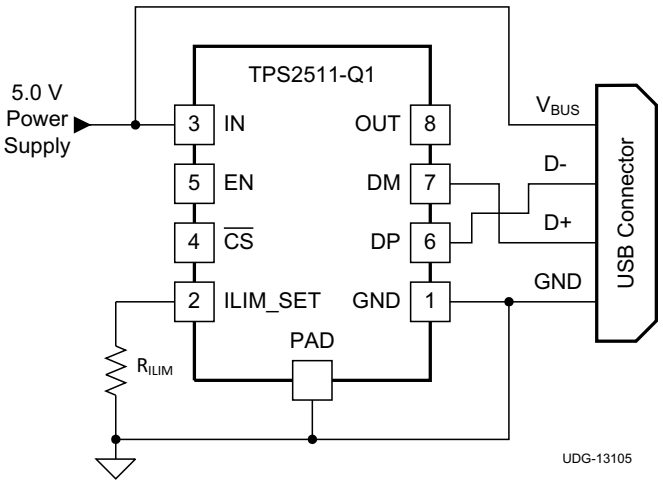


Figure 38. 5-W USB Charger Application without Power Switch

Layout Guidelines

- **TPS2511-Q1 placement.** Place the TPS2511-Q1 near the USB output connector and at lest 22-µF OUT pin filter capacitor. Connect the exposed Power PAD to the GND pin and to the system ground plane using a via array.
- **IN pin bypass capacitance.** Place the 0.1-µF bypass capacitor near the IN pin and make the connection using a low-inductance trace.
- **ILIM_SET pin connection.** Current limit set point accuracy can be compromised by stray leakage from a higher voltage source to the ILIM_SET pin. Ensure that there is adequate spacing between IN pin copper/trace and ILIM_SET pin trace to prevent contaminant buildup during the PCB assembly process. The traces routing the R_{ILIM} resistor to the device should be as short as possible to reduce parasitic effects on the current-limit accuracy.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2511QDGNQ1	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2511Q	Samples
TPS2511QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2511Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

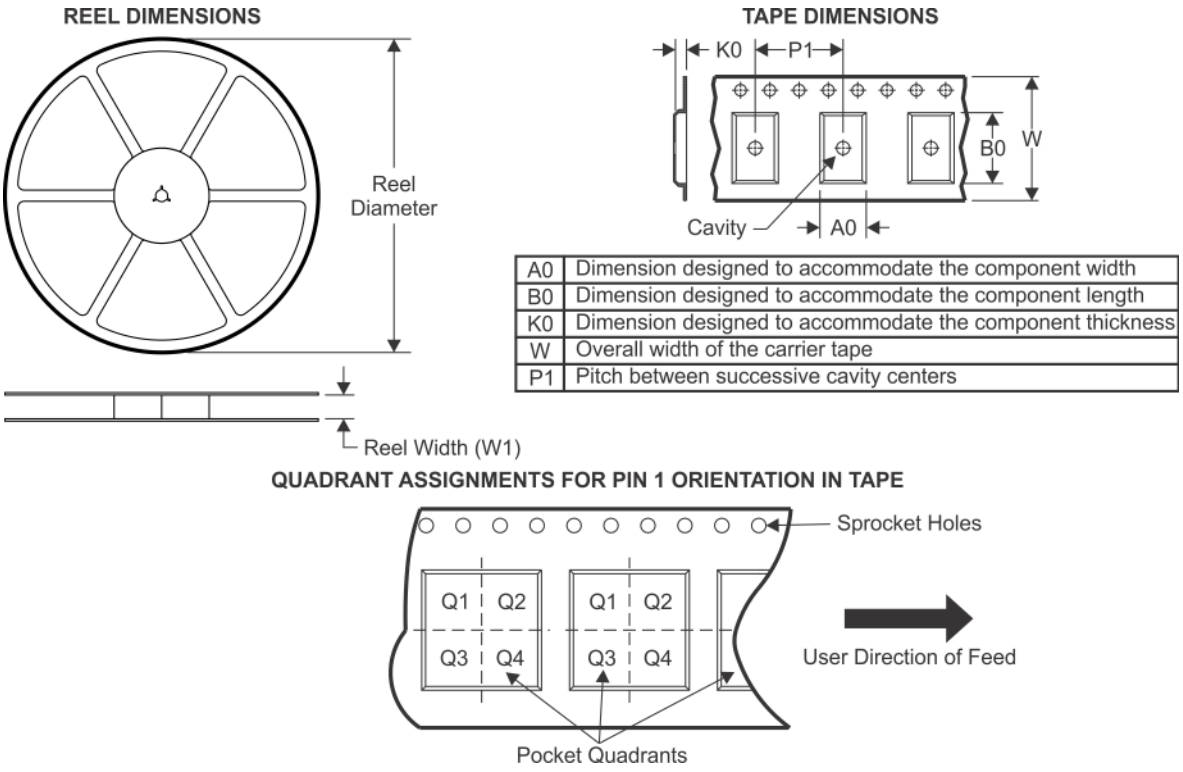
OTHER QUALIFIED VERSIONS OF TPS2511-Q1 :

- Catalog: TPS2511

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

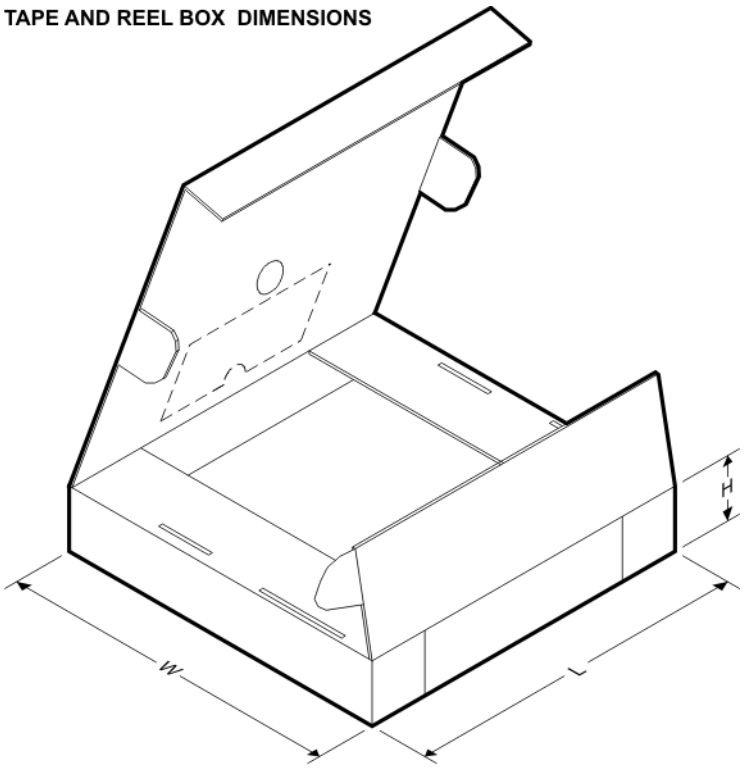


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2511QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

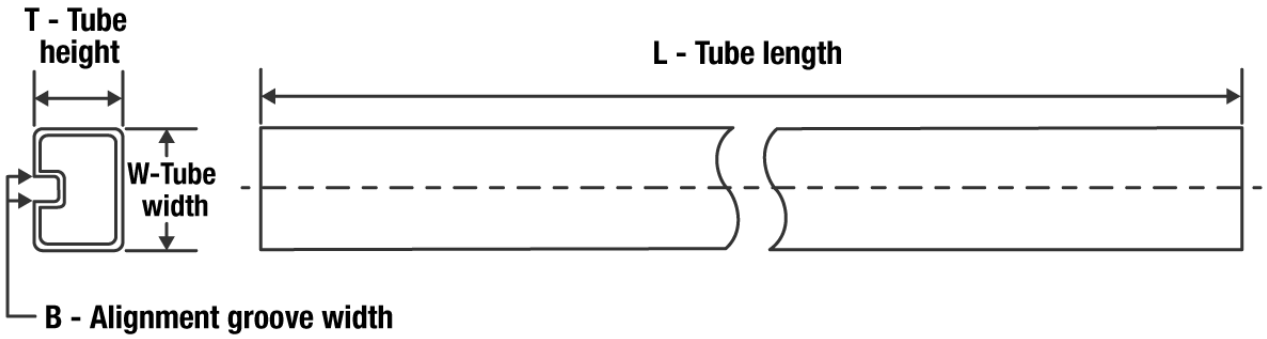
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2511QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2511QDGNQ1	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

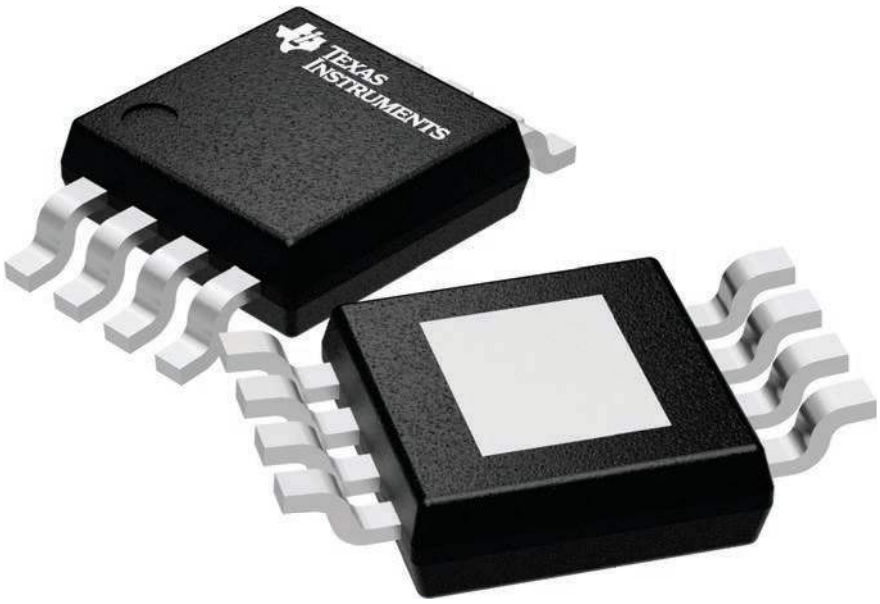
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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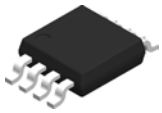
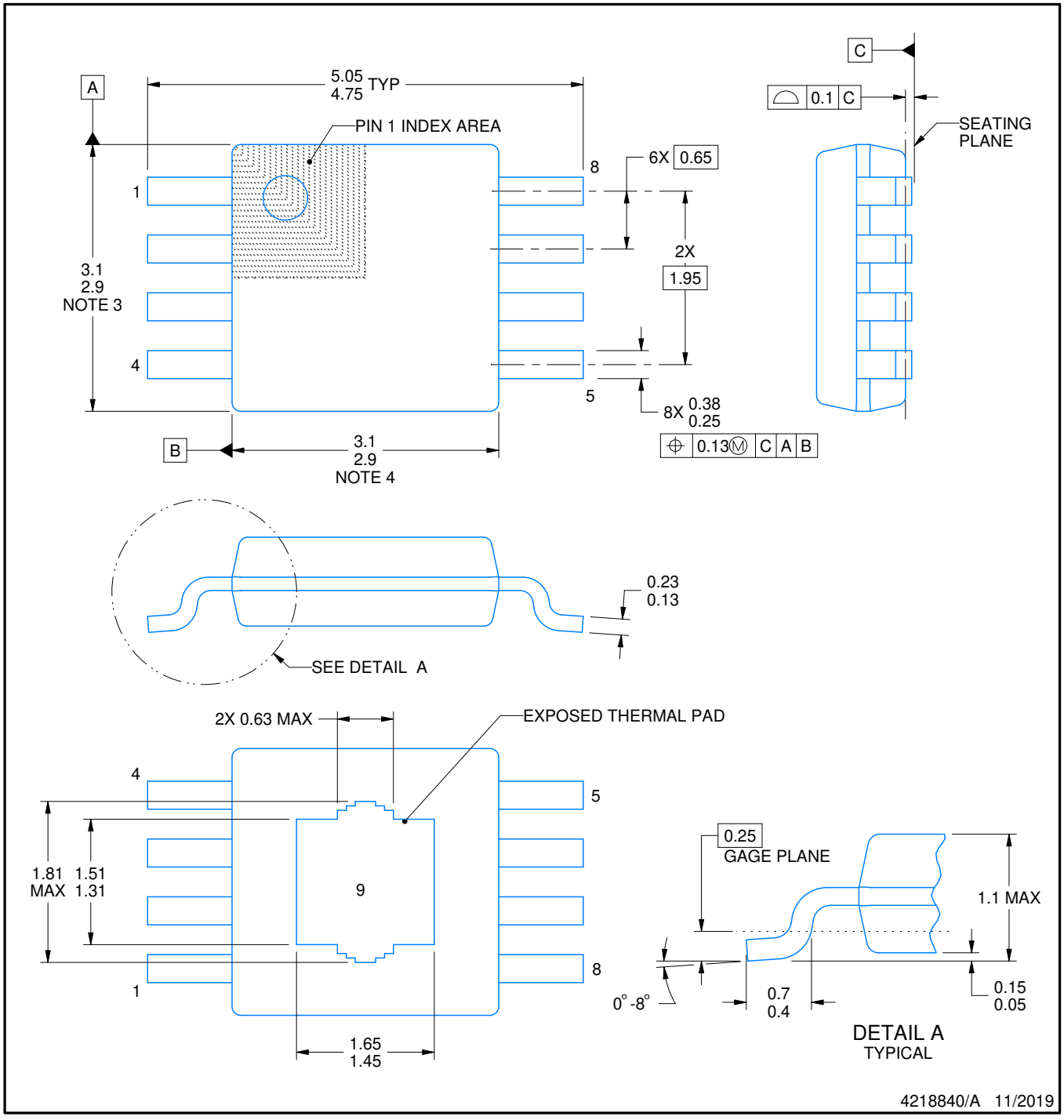
PACKAGE OUTLINE

DGN0008E



PowerPAD™ VSSOP - 1.1 mm max height

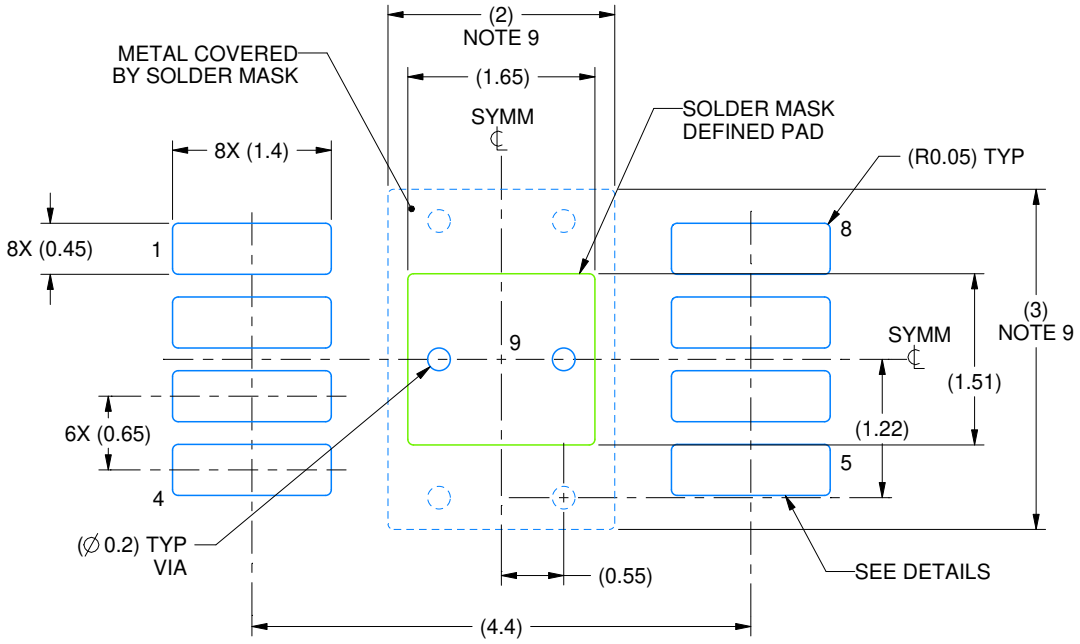
SMALL OUTLINE PACKAGE



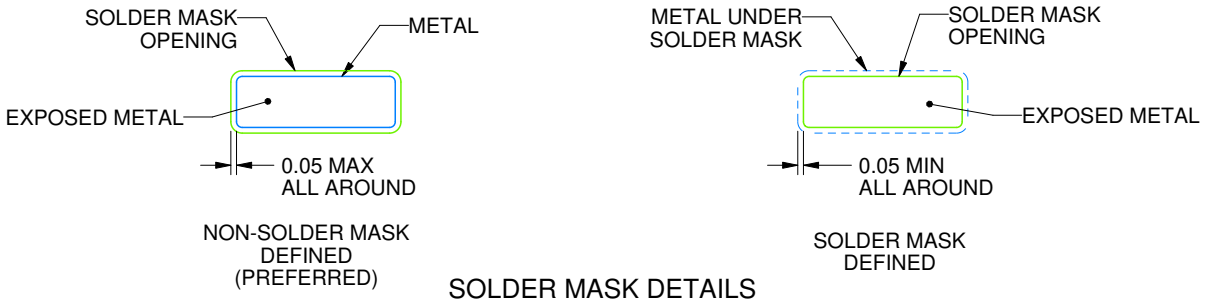
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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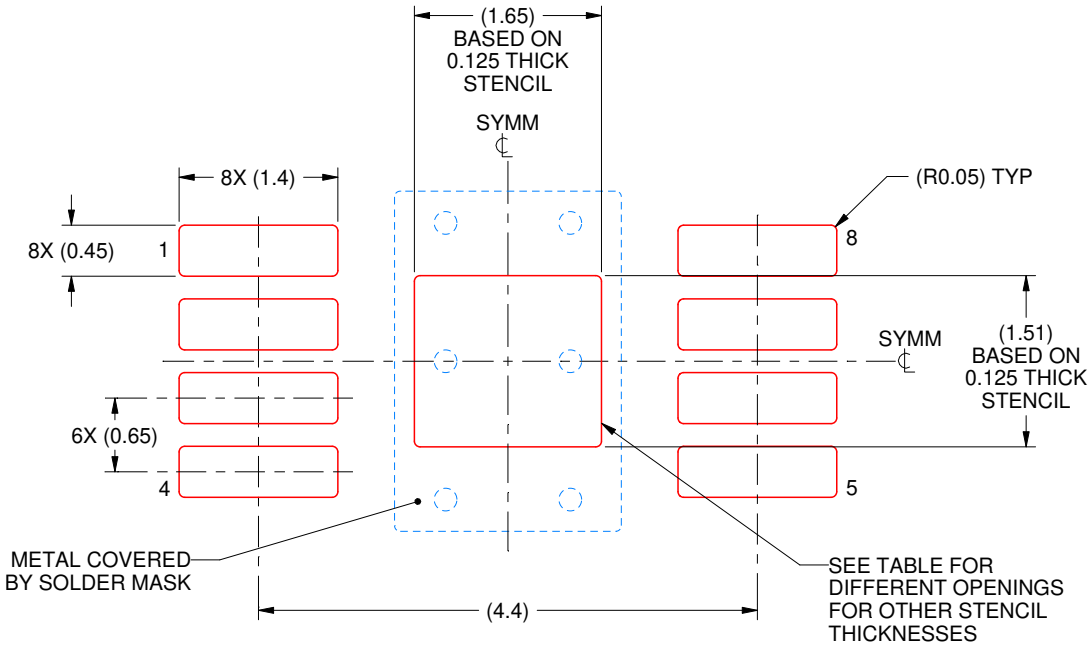
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 1.69
0.125	1.65 X 1.51 (SHOWN)
0.15	1.51 X 1.38
0.175	1.39 X 1.28

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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