19-3330; Rev 0; 4/00

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

General Description

The MAX3170 is a three-driver/three-receiver multiprotocol transceiver that operates from a +3.3V single supply. The MAX3170, along with the MAX3171/MAX3173 and MAX3172/MAX3174, form a complete software-selectable data terminal equipment (DTE) or data communications equipment (DCE) interface port that supports the V.28 (RS-232), V.11 (RS-449/V.36, EIA530, EIA530-A, X.21), and V.35 protocols. The MAX3170 transceiver carries the high-speed clock and data signals, while the MAX3171 or MAX3173 carries the control signals. The MAX3170 can be terminated by the MAX3172 or MAX3174 software-selectable resistor termination network or by a discrete termination network.

An internal charge pump and proprietary low-dropout transmitter output stage allow V.11-, V.28-, and V.35-compliant operation from a +3.3V single supply. A no-cable mode is entered when all mode pins (M0, M1, and M2) are pulled high or left unconnected. In no-cable mode, supply current decreases to 1mA and all transmitter and receiver outputs are disabled (high impedance). Short-circuit limiting and thermal shutdown circuitry protect the drivers against excessive power dissipation.

Applications

Data Networking
CSU and DSU
Data Routers
PCI Cards
Telecommunications

Features

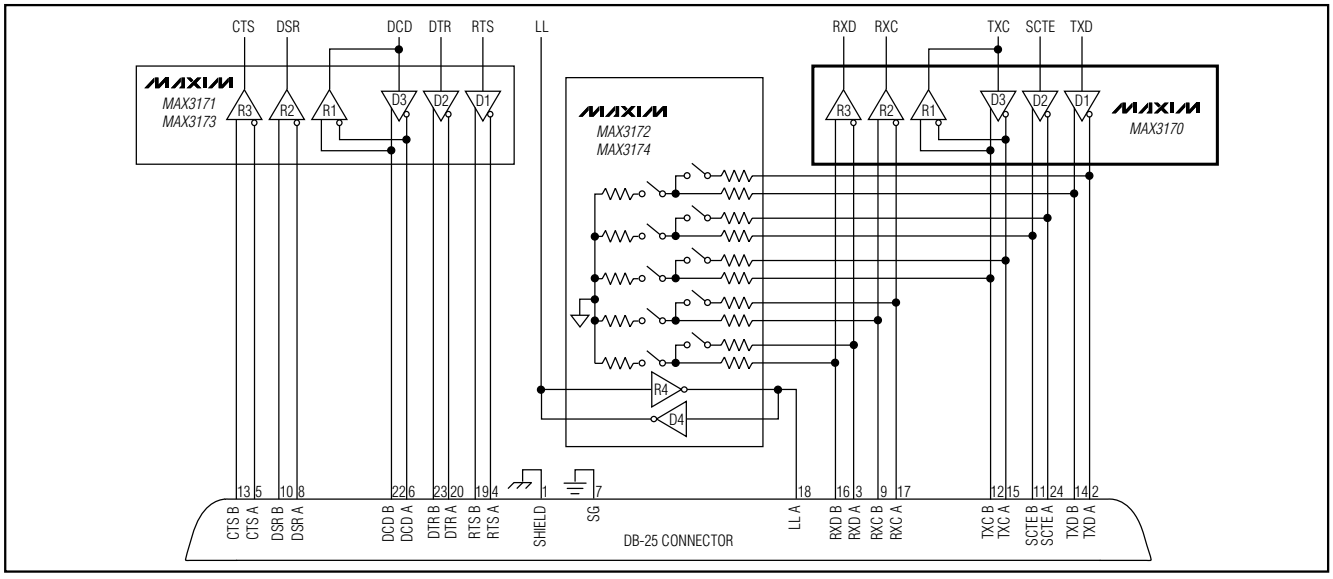
- ♦ **Industry's First +3.3V Single-Supply Transceiver**
- ♦ **3V/5V Logic-Compatible I/O**
- ♦ **Certified TBR-1 and TBR-2 Compliant (NET1 and NET2)—Pending Completion**
- ♦ **Supports V.28 (RS-232), V.11 (RS-449/V.36, EIA530, EIA530-A, X.21), and V.35 Protocols**
- ♦ **Software-Selectable DTE/DCE**
- ♦ **Complete DTE/DCE Port with MAX3171/MAX3173 and MAX3172/MAX3174**
- ♦ **True Fail-Safe Receiver Operation**
- ♦ **Available in Small 28-Pin SSOP Package**
- ♦ **10Mbps Operation (V.11/V.35)**
- ♦ **Requires Only Four Tiny Surface-Mount Capacitors**
- ♦ **All Transmitter Outputs Are Fault Protected to ±15V to Survive Cable Miswiring**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3170CAI	0°C to +70°C	28 SSOP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND unless otherwise noted.)
Supply Voltages
- V_{CC} ..... -0.3V to +4V
- V+ (Note 1) ..... -0.3V to +7V
- V- (Note 1) ..... +0.3V to -7V
- V+ to V- (Note 1) 13V

Logic Input Voltages
- M0, M1, M2, DCE/$\overline{DTE}$, T_IN ..... -0.3V to +6V

Logic Output Voltages
- R_OUT ..... -0.3V to (V_{CC} + 0.3V)
- Short-Circuit Duration ..... Continuous

Transmitter Outputs
- T_OUT_ ..... -15V to +15V
- Short-Circuit Duration 60s

Receiver Inputs
- R_IN_ ..... -15V to +15V

Continuous Power Dissipation (T_A = +70°C)
- 28-Pin SSOP (derate 11.1mW/°C above +70°C) 889mW

Operating Temperature Range
- MAX3170CAI ..... 0°C to +70°C

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±5%, C1 = C2 = 1µF, C3 = C4 = 3.3µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Current (DCE Mode) (Digital Inputs = GND or V_{CC}) (All Outputs Static)	I_{CC}	V.11 mode		190	250	mA
		V.11 mode with no load		3	7	
		V.35 mode		160	210	
		V.35 mode with no load		20	40	
		V.28 mode		10	20	
		V.28 mode with no load		4	7	
		No-cable mode		0.8	2	
Internal Power Dissipation (DCE Mode)	P_D	V.11 mode, full load		410		mW
		V.35 mode, full load		510		
		V.28 mode, full load		15		
V+ Output Voltage (DCE Mode) (Full Load)	V+	V.11 mode	4			V
		V.35 mode	4.25			
		V.28 mode	5.55			
		No-cable mode		5		
V- Output Voltage (DCE Mode) (Full Load)	V-	V.11 mode			-4.1	V
		V.35 mode			-3.7	
		V.28 mode			-5.45	
		No-cable mode		-4.25		
Charge-Pump Enable Time		Delay until V+ and V- specifications met		1		ms
LOGIC INPUTS (M0, M1, M2, DCE/$\overline{DTE}$, T_IN)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Logic Input Current	I_{IN}	T_IN			±1	µA
	I_{IH}	M0, M1, M2, DCE/$\overline{DTE}$ = V_{CC}			±1	
	I_{IL}	M0, M1, M2, DCE/$\overline{DTE}$ = GND	30	50	100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V ±5%, C1 = C2 = 1µF, C3 = C4 = 3.3µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS (R_OUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 1.0mA	V_{CC} - 1.0			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
Rise or Fall Time	t_r, t_f	10% to 90%		15		ns
Output Leakage Current (Receiver Output Tristated)		R_OUT = GND	30	50	100	µA
		R_OUT = V_{CC}			±1	
TRANSMITTER OUTPUTS						
Output Leakage Current	I_Z	-0.25V < V_{OUT} < +0.25V power-off or no-cable mode			±100	µA
Data Rate		V.11/ V.35 mode		10		Mbps
		V.28 mode		240		kbps
RECEIVER INPUTS						
Receiver Input Resistance	R_{IN}	-10V < $V_{A,B}$ < +10V, V_A or V_B grounded (V.11/V.35/no-cable mode)	20	40		kΩ
		-15V < V_A < +15V (V.28 mode)	3	5	7	
Data Rate		V.11/ V.35 mode		10		Mbps
		V.28 mode		240		kbps
V.11 TRANSMITTER						
Unloaded Differential Output Voltage	V_{ODO}	R = 1.95kΩ, Figure 1	4.0		6.0	V
Loaded Differential Output Voltage	V_{ODL}	R = 50Ω, Figure 1	2.0 0.5 x V_{ODO}			V
Change in Magnitude of Output	ΔV_{OD}	R = 50Ω, Figure 1			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω, Figure 1			3.0	V
Change in Magnitude of Output Common-Mode Voltage	ΔV_{OC}	R = 50Ω, Figure 1			0.2	V
Short-Circuit Current	I_{SC}	V_{OUT} = GND		60	150	mA
Rise or Fall Time	t_r, t_f	10% to 90%, Figure 2		10	25	ns
Transmitter Input to Output	t_{PHL}, t_{PLH}	Figure 2		50	80	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figure 2		2	10	ns
Output-to-Output Skew	t_{SKEW}	Figure 2		2		ns
Channel-to-Channel Output				2		ns
V.11 RECEIVER						
Differential Threshold Voltage	V_{TH}	-7V < V_{CM} < +7V	-200	-100	-25	mV
Input Hysteresis	ΔV_{TH}	-7V < V_{CM} < +7V		15		mV
Receiver Input to Output	t_{PHL}, t_{PLH}	V_{CM} = 0, Figure 2		60	120	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	V_{CM} = 0, Figure 2		5	16	ns

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V ±5%, C1 = C2 = 1µF, C3 = C4 = 3.3µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3.3V.)

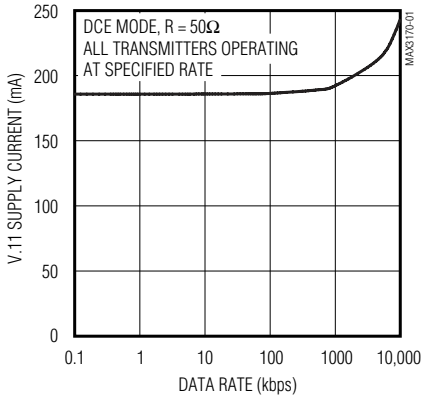
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V.35 TRANSMITTER						
Differential Output Voltage		-4V < V_{CM} < +4V, Figure 3	0.44	0.55	0.66	V
Output High Current	I_{OH}	$V_{A, B}$ = 0	9	11	13	mA
Output Low Current	I_{OL}	$V_{A, B}$ = 0	-13	-11	-9	mA
Rise or Fall Time	t_r, t_f	10% to 90%, Figure 3		10		ns
Transmitter Input to Output	t_{PHL}, t_{PLH}	Figure 3		50	80	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figure 3		5	10	ns
Output-to-Output Skew		Figure 3		2		ns
Channel-to-Channel Output Skew				2		ns
V.35 RECEIVER						
Differential Input Voltage	V_{TH}	-4V < V_{CM} < +4V, Figure 3	-200	-100	-25	mV
Input Hysteresis	ΔV_{TH}	-4V < V_{CM} < +4V, Figure 3		15		mV
Receiver Input to Output	t_{PHL}, t_{PLH}	V_{CM} = 0		70	120	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	V_{CM} = 0		5	16	ns
V.28 TRANSMITTER						
Output Voltage Swing	V_O	All transmitters loaded with R_L = 3kΩ	±5.0	±5.4		V
		No load			±6.5	
Short-Circuit Current	I_{SC}			±25	±60	mA
Output Slew Rate	SR	R_L = 3kΩ, C_L = 2500pF, measured from +3V to -3V or -3V to +3V, Figure 4	4		30	V/µs
		R_L = 7kΩ, C_L = 150pF, measured from +3V to -3V or -3V to +3V, Figure 4	6		30	
Transmitter Input to Output	t_{PHL}, t_{PLH}	Figure 4		1		µs
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figure 4		100		ns
V.28 RECEIVER						
Input Threshold Low	V_{IL}	Figure 5	0.8	1.1		V
Input Threshold High	V_{IH}	Figure 5		1.6	2.0	V
Input Hysteresis	V_{HYS}			0.5		V
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figure 5		100		ns

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

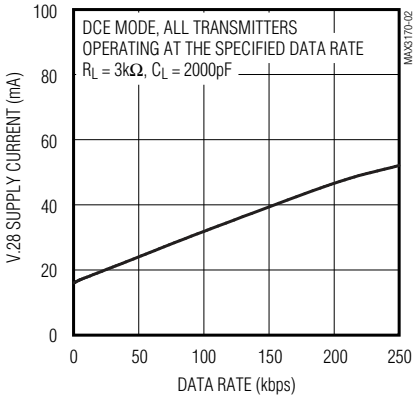
Typical Operating Characteristics

(V_{CC} = +3.3V, C1 = C2 = 1.0µF, C3 = C4 = 3.3µF, T_A = +25°C, unless otherwise noted.)

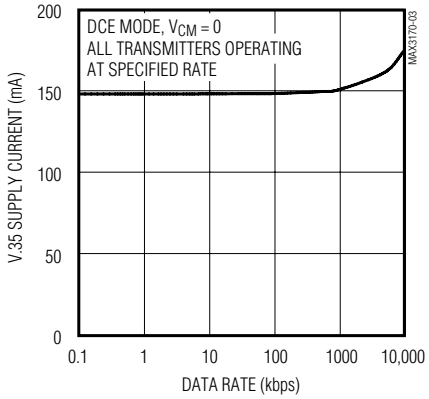
V.11 SUPPLY CURRENT vs. DATA RATE



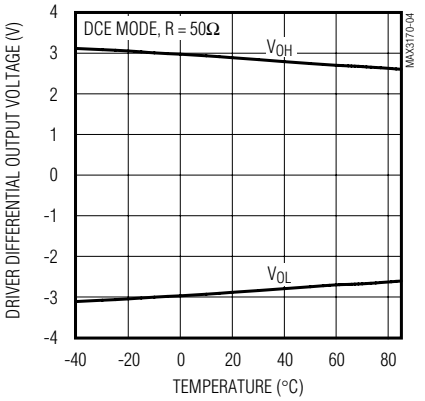
V.28 SUPPLY CURRENT vs. DATA RATE



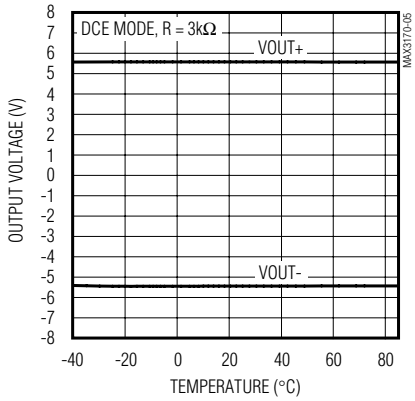
V.35 SUPPLY CURRENT vs. DATA RATE



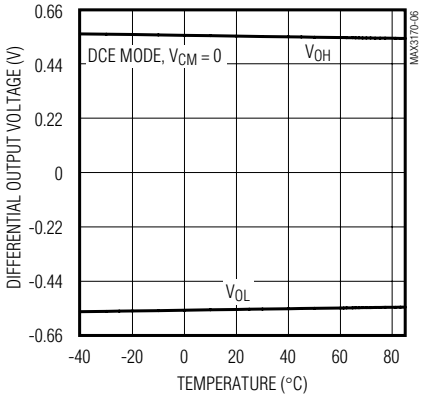
V.11 DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



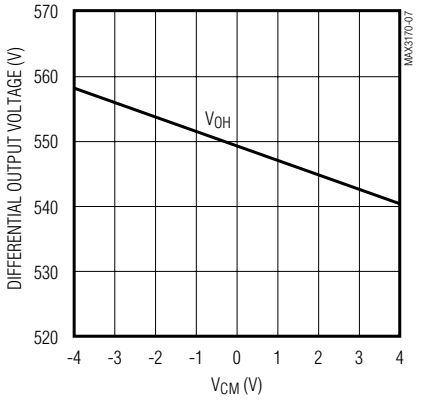
V.28 OUTPUT VOLTAGE vs. TEMPERATURE



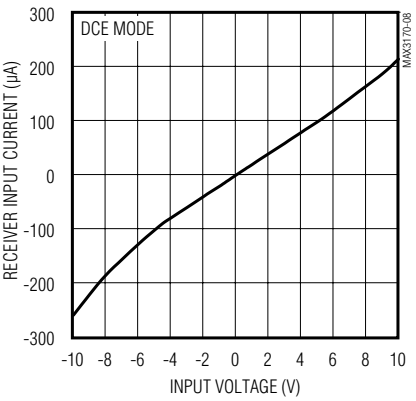
V.35 DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



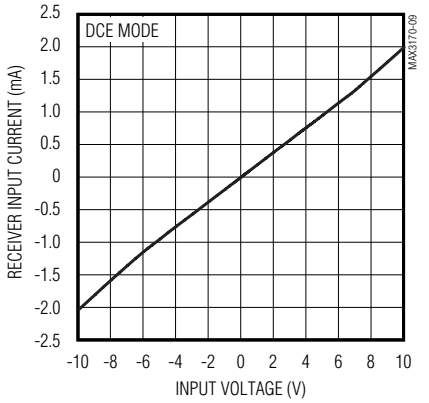
V.35 DIFFERENTIAL OUTPUT VOLTAGE vs. COMMON-MODE VOLTAGE



V.11/V.35 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



V.28 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE

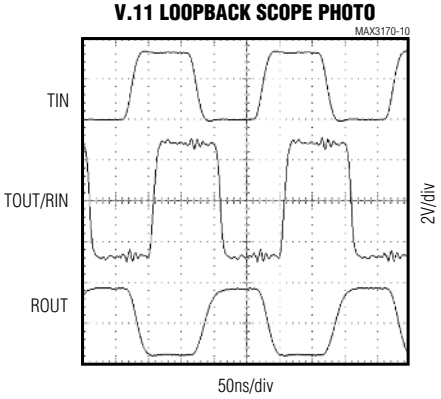


+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

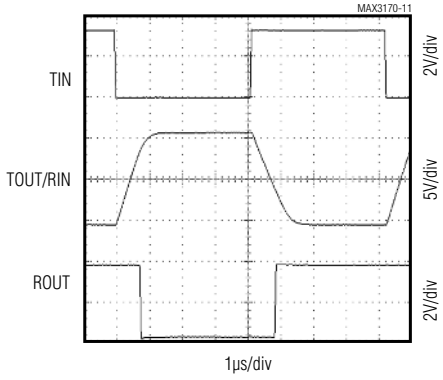
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C1 = C2 = 1.0µF, C3 = C4 = 3.3µF, T_A = +25°C, unless otherwise noted.)

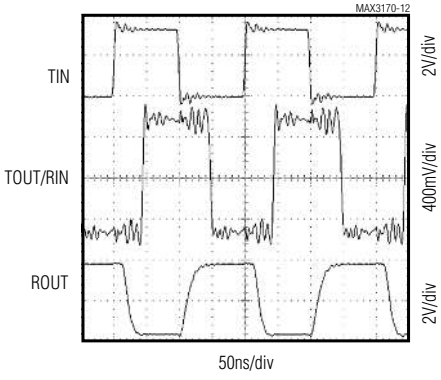
V.11 LOOPBACK SCOPE PHOTO



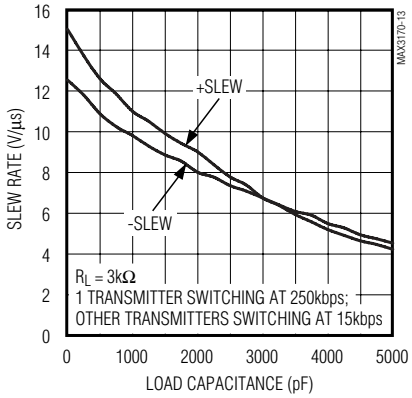
V.28 LOOPBACK SCOPE PHOTO



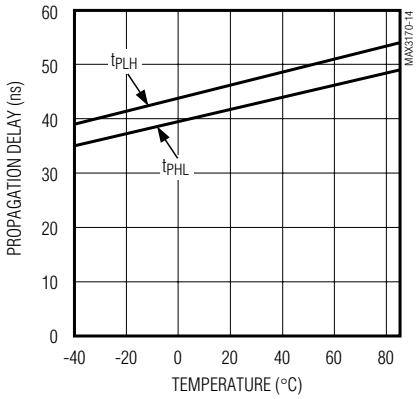
V.35 LOOPBACK SCOPE PHOTO



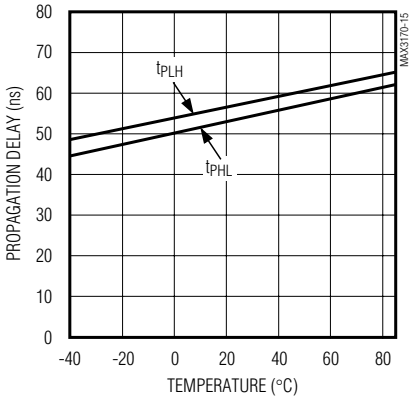
V.28 SLEW RATE vs. LOAD CAPACITANCE



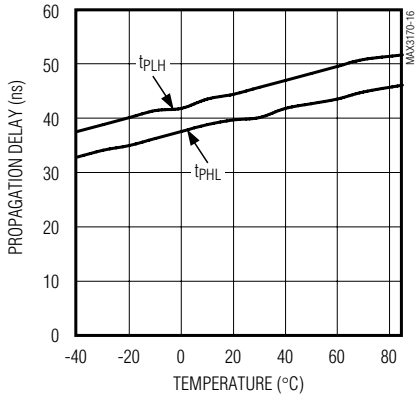
V.11 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



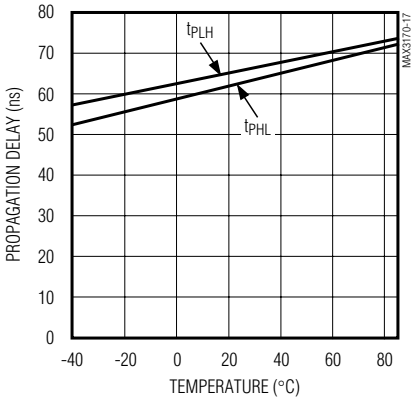
V.11 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



V.35 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



V.35 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



Test Circuits

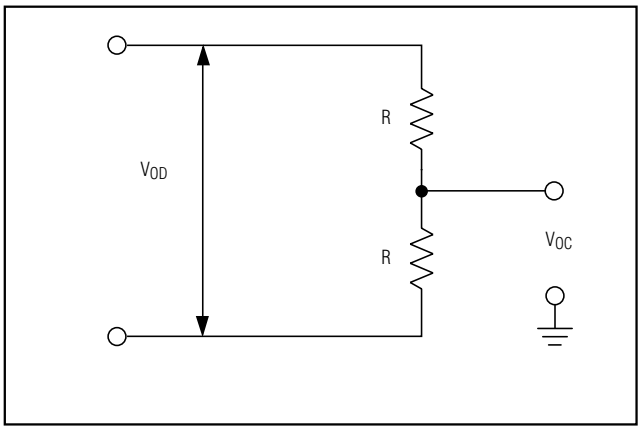


Figure 1. V.11 DC Test Circuit

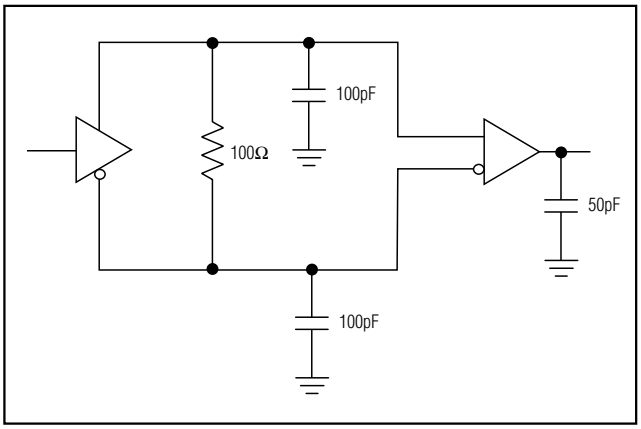


Figure 2. V.11 AC Test Circuit

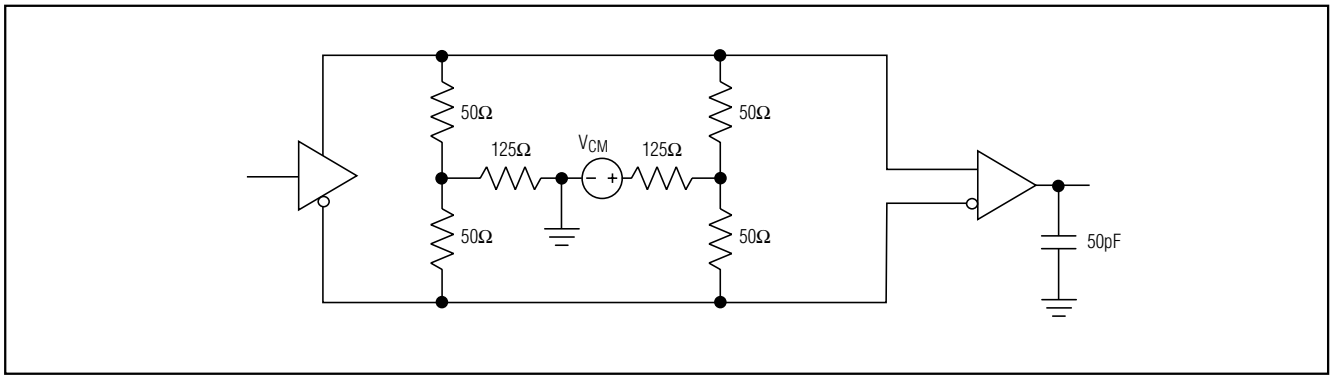


Figure 3. V.35 Transmitter/Receiver Test Circuit

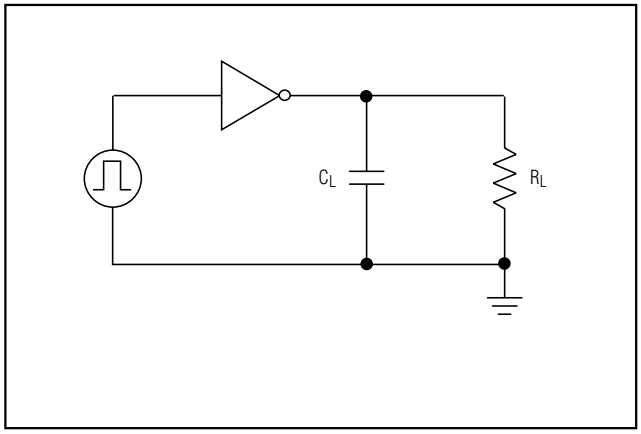


Figure 4. V.28 Driver Test Circuit

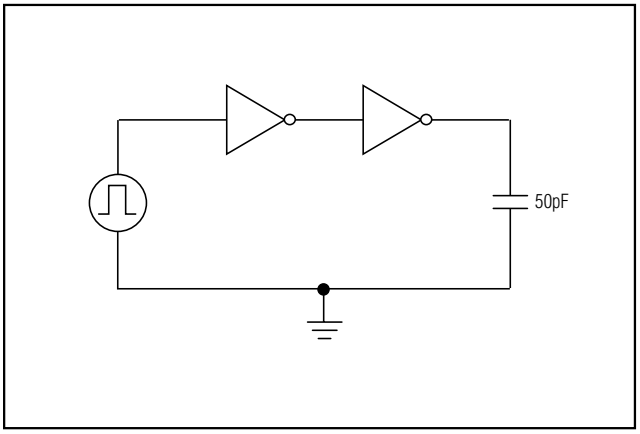


Figure 5. V.28 Receiver Test Circuit

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

Pin Description

PIN	NAME	FUNCTION
1	V+	Positive Supply Generated by the Charge Pump. Bypass V+ to ground with a 3.3µF ceramic capacitor.
2	C2+	Positive Terminal of the Inverting Charge-Pump Capacitor. Connect C2+ to C2- with a 1µF ceramic capacitor.
3	C2-	Negative Terminal of the Inverting Charge-Pump Capacitor. Connect C2+ to C2- with a 1µF ceramic capacitor.
4	V-	Negative Supply Generated by the Charge Pump. Bypass V- to ground with a 3.3µF ceramic capacitor.
5, 6, 7	T_IN	Transmitter CMOS Inputs (T1IN, T2IN, T3IN)
8, 9, 10	R_OUT	Receiver CMOS Outputs (R1OUT, R2OUT, R3OUT)
11, 12, 13	M_	Mode Select Pins (M0, M1, M2). Internally pulled up to V_{CC}. See Table 1 for detailed information.
14	DCE/$\overline{DTE}$	DCE/$\overline{DTE}$ Mode Select Pin. Logic level high selects DCE interface; logic level low selects DTE interface. Internally pulled up to V_{CC}.
15, 18	R_INB	Noninverting Receiver Inputs (R3INB, R2INB)
16, 17	R_INA	Inverting Receiver Inputs (R3INA, R2INA)
19	T3OUTB/R1INB	Noninverting Transmitter Output/Noninverting Receiver Input
20	T3OUTA/R1INA	Inverting Transmitter Output/Inverting Receiver Input
21, 23	T_OUTB	Noninverting Transmitter Outputs (T2OUTB, T1OUTB)
22, 24	T_OUTA	Inverting Transmitter Outputs (T2OUTA, T1OUTA)
25	C1-	Negative Terminal of the Voltage-Doubler Charge-Pump Capacitor. Connect C1+ to C1- with a 1µF ceramic capacitor.
26	GND	Ground
27	V_{CC}	+3.3V Supply Voltage (±5%). Bypass V_{CC} to ground with a 3.3µF capacitor.
28	C1+	Positive Terminal of the Voltage-Doubler Charge-Pump Capacitor. Connect C1+ to C1- with a 1µF ceramic capacitor.

Detailed Description

The MAX3170 is a three-driver/three-receiver multiprotocol transceiver that operates from a +3.3V single supply. The MAX3170, along with the MAX3171/MAX3173 and MAX3172/MAX3174, form a complete software-selectable DTE or DCE interface port that supports the V.28 (RS-232), V.11 (RS-449/V.36, EIA530, EIA530-A, and X.21), and V.35 protocols. The MAX3170 transceiver carries the high-speed clock and data signals, while the MAX3171 or MAX3173 carries the control signals. The MAX3170 can be terminated by the MAX3172 or MAX3174 software-selectable resistor termination network or by a discrete termination network.

The MAX3170 features a 1mA no-cable mode, true fail-safe operation, and thermal shutdown circuitry. Thermal shutdown protects the drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high-impedance state.

Table 1. Mode Selection

PROTOCOL	LOGIC INPUTS				TRANSMITTERS			RECEIVERS		
	M2	M1	M0	DCE/$\overline{\text{DTE}}$	T1	T2	T3	R1	R2	R3
V.11	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530A	0	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS-449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS-232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No cable	1	1	1	0	Z	Z	Z	Z	Z	Z
V.11	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530A	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.35	V.35	V.35	Z	V.35	V.35
RS-449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS-232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No cable	1	1	1	1	Z	Z	Z	Z	Z	Z

Z = High impedance

Mode Selection

The state of the mode select pins M0, M1, and M2 determines which serial interface protocol is selected (Table 1). The state of the DCE/$\overline{\text{DTE}}$ input determines whether the transceiver will be configured as a DTE or a DCE serial port. When the DCE/$\overline{\text{DTE}}$ input is logic HIGH, driver T3 is activated and receiver R1 is disabled. When the DCE/$\overline{\text{DTE}}$ input is logic LOW, driver T3 is disabled and receiver R1 is activated. M0, M1, M2, and DCE/$\overline{\text{DTE}}$ are internally pulled up to V_{CC} to ensure a logic HIGH if left unconnected.

The MAX3170's mode can be selected through software control of the M0, M1, M2, and DCE/$\overline{\text{DTE}}$ inputs. Alternatively, the mode can be selected by shorting the appropriate combination of mode control inputs to GND. The inputs left floating will be internally pulled up to V_{CC} (logic HIGH). If the M0, M1, and M2 mode inputs are all unconnected, the MAX3170 will enter no-cable mode and the supply current will drop to 1mA.

No-Cable Mode

The MAX3170 will enter no-cable mode when the mode select pins are left unconnected or tied high (M0 = M1 = M2 = 1). In this mode, the multiprotocol drivers and receivers are disabled and the supply current drops to 1mA. The receiver outputs enter a high-impedance state in no-cable mode, which allows these output lines to be shared with other receivers (the receiver outputs have an internal pull-up resistor to pull the outputs HIGH if not driven). Also, in no-cable mode, the transmitter outputs enter a high-impedance state so that these output lines can be shared with other devices.

Dual Charge-Pump Voltage Converter

The MAX3170's internal power supply consists of a regulated dual charge pump that provides positive and negative output voltages from a +3.3V supply. The charge pump operates in discontinuous mode: if the output voltage is less than the regulated voltage, the charge pump is enabled; if the output voltage exceeds the regulated voltage, the charge pump is disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies. See Figure 6 for charge-pump connections.

Fail-Safe Receivers

The MAX3170 guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

receiver threshold between -25mV and -200mV in the V.11 and V.35 modes. If the differential receiver input voltage (B - A) is ≥-25mV, R_OUT is logic HIGH. If (B - A) is ≤ -200mV, R_OUT is logic LOW. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination. With the receiver thresholds of the MAX3170, this results in a logic HIGH with a 25mV minimum noise margin.

Applications Information

Capacitor Selection

The capacitors used for the charge pumps, as well as the supply bypassing, should have a low equivalent series resistance (ESR) and low temperature coefficient. Multilayer ceramic capacitors with an X7R dielectric offer the best combination of performance, size, and cost. The flying capacitors (C1, C2) should have a value of 1µF, while the reservoir capacitors (C3, C4) and bypass capacitor (C5) should have a minimum value of 3.3µF (Figure 6). To reduce the ripple present on the transmitter outputs, capacitors C3, C4, and C5 can be increased. The values of C1 and C2 should not be increased.

Cable Termination

The MAX3172/MAX3174 software-selectable resistor network is designed to be used with the MAX3170. The MAX3172/MAX3174 multiprotocol termination network provides V.11- and V.35-compliant termination, while V.28 receiver termination is internal to the MAX3170. These cable termination networks provide compatibility with V.11, V.28, and V.35 protocols. Using the MAX3172/MAX3174 termination network provides the advantage of not having to build expensive termination networks out of resistors and relays, manually changing termination modules, or building termination networks into custom cables.

Cable-Selectable Mode

A cable-selectable multiprotocol interface is shown in Figure 7. The mode control lines M0, M1, and DCE/$\overline{\text{DTE}}$ are wired to the DB-25 connector. To select the serial interface mode, the appropriate combination of M0, M1, M2, and DCE/$\overline{\text{DTE}}$ are grounded within the cable wiring. The control lines that are not grounded are pulled high by the internal pull-ups on the MAX3170. The serial interface protocol of the MAX3170 (and MAX3171/MAX3173 and MAX3172/MAX3174) is selected based on the cable that is connected to the DB-25 interface.

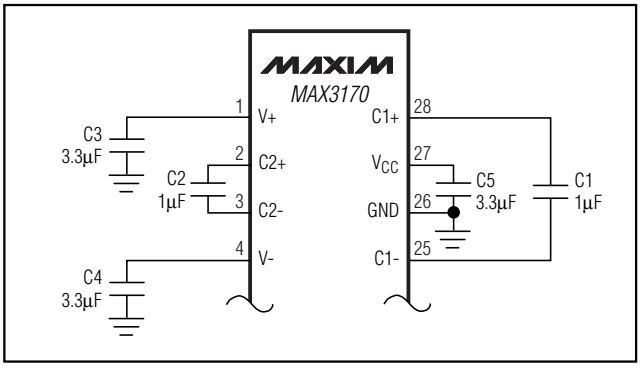


Figure 6. Charge-Pump Connections

V.11 (RS-422) Interface

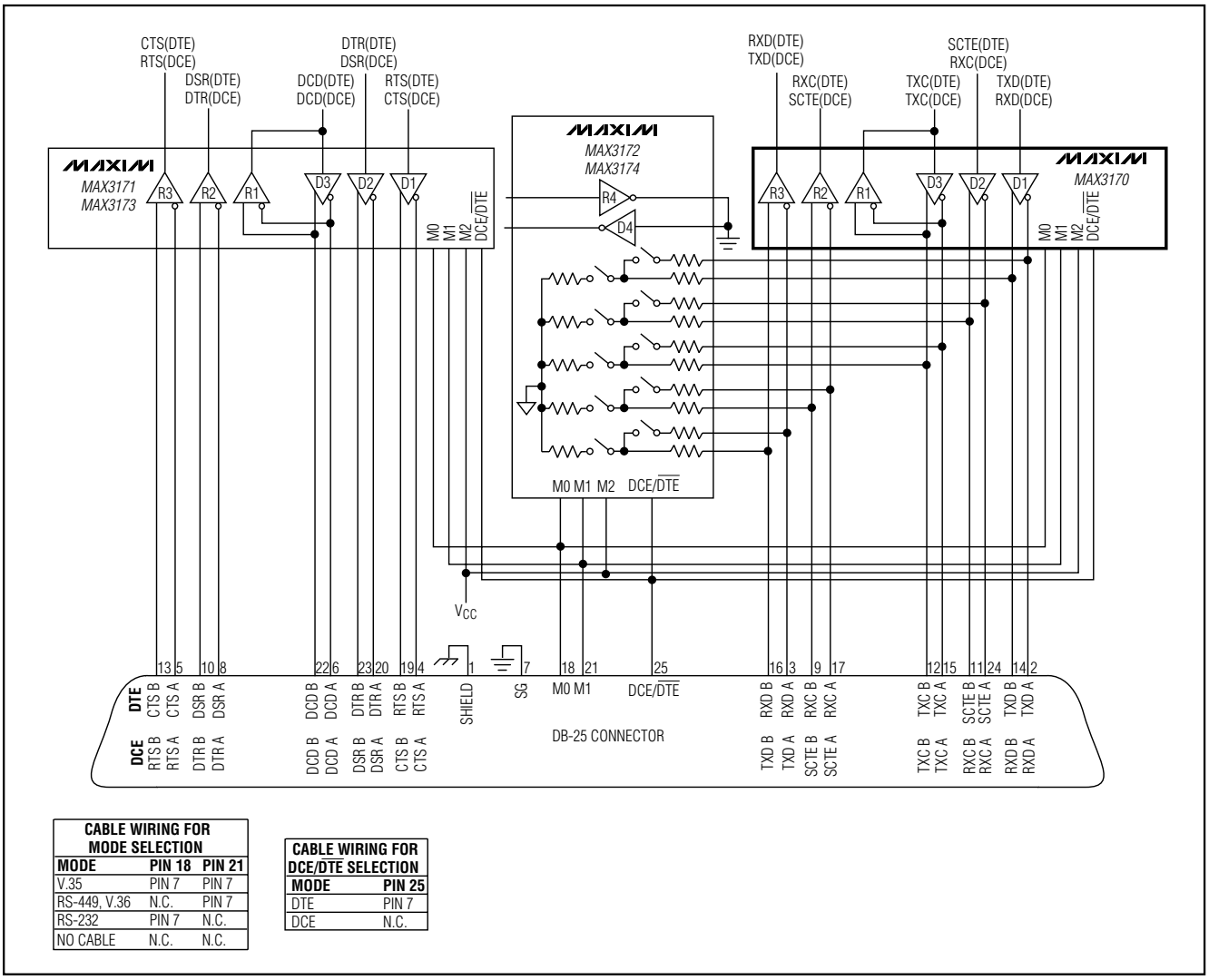
As shown in Figure 8, the V.11 protocol is a fully balanced differential interface. The V.11 driver generates a minimum of ±2V between nodes A and B when a 100Ω (min) resistance is presented at the load. The V.11 receiver is sensitive to ±200mV differential signals at the receiver inputs, A′ and B′. The V.11 receiver rejects common-mode signals developed across the cable (referenced from C to C′) of up to ±7V, allowing for error-free reception in noisy environments. The receiver inputs must comply with the impedance curve shown in Figure 9.

For high-speed data transmission, the V.11 specification recommends terminating the cable at the receiver with a 100Ω minimum resistor. This resistor, although not required, prevents reflections from corrupting transmitted data. In Figure 10, the MAX3172 or MAX3174 is used to terminate the V.11 receiver. Internal to the MAX3172/MAX3174, S1 is closed and S2 is open to present a 100Ω minimum differential resistance. The MAX3170's internal V.28 termination is disabled by opening S3.

V.35 Interface

Figure 11 shows a fully balanced differential standard V.35 interface. The generator and the load must both present a 100Ω ±10Ω differential impedance and a 150Ω ±15Ω common-mode impedance as shown by the resistive T-networks in Figure 11. The V.35 driver generates a current output (±11mA typ) that develops an output voltage of ±550mV across the generator and load termination networks. The V.35 receiver is sensitive to ±200mV differential signals at the receiver inputs A′ and B′. The V.35 receiver rejects common-mode signals developed across the cable (referenced from C to C′) of up to ±4V, allowing for error-free reception in noisy environments.

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver



CABLE WIRING FOR MODE SELECTION		
MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
RS-449, V.36	N.C.	PIN 7
RS-232	PIN 7	N.C.
NO CABLE	N.C.	N.C.

CABLE WIRING FOR DCE/DTE SELECTION	
MODE	PIN 25
DTE	PIN 7
DCE	N.C.

Figure 7. Cable-Selectable Multiprotocol DCE/DTE Port

In Figure 12, the MAX3172 or MAX3174 is used to implement the resistive T-network that is needed to properly terminate the V.35 driver and receiver. Internal to the MAX3172/MAX3174, S1 and S2 are closed to connect the T-network resistors to the circuit. The V.28 termination resistor (internal to the MAX3170) is disabled by opening S3 to avoid interference with the T-network impedances.

V.28 Interface

The V.28 interface is an unbalanced single-ended interface (Figure 13). The V.28 driver generates a minimum of ±5V across the load impedance between A′ and C′. The V.28 receiver has a single-ended input and does not reject any common-mode differences between C and C′. The V.28 receiver has input trip points at ±3V. To aid in rejecting system noise, the MAX3170 V.28 receiver has a typical hysteresis of 0.5V.

Figure 14 shows that the MAX3172/MAX3174 termination network is disabled by opening S1 and S2. The MAX3170's internal 5kΩ V.28 termination is enabled by closing S3.

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

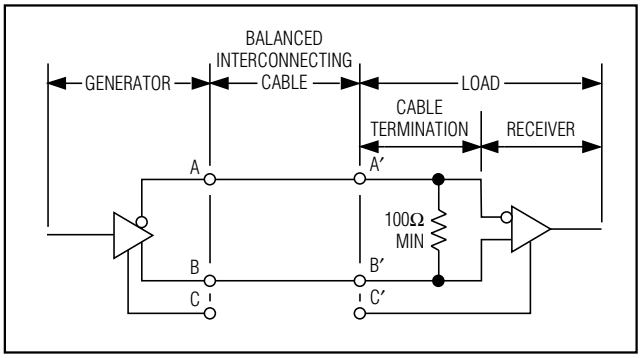


Figure 8. Typical V.11 Interface

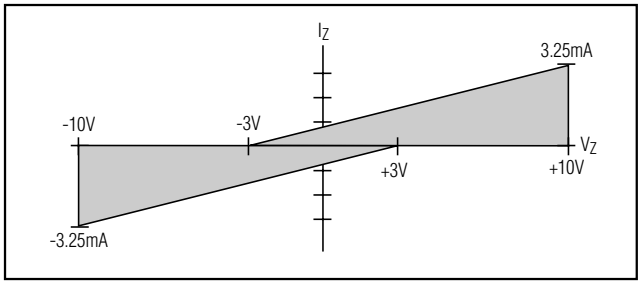


Figure 9. Receiver Input Impedance Curve

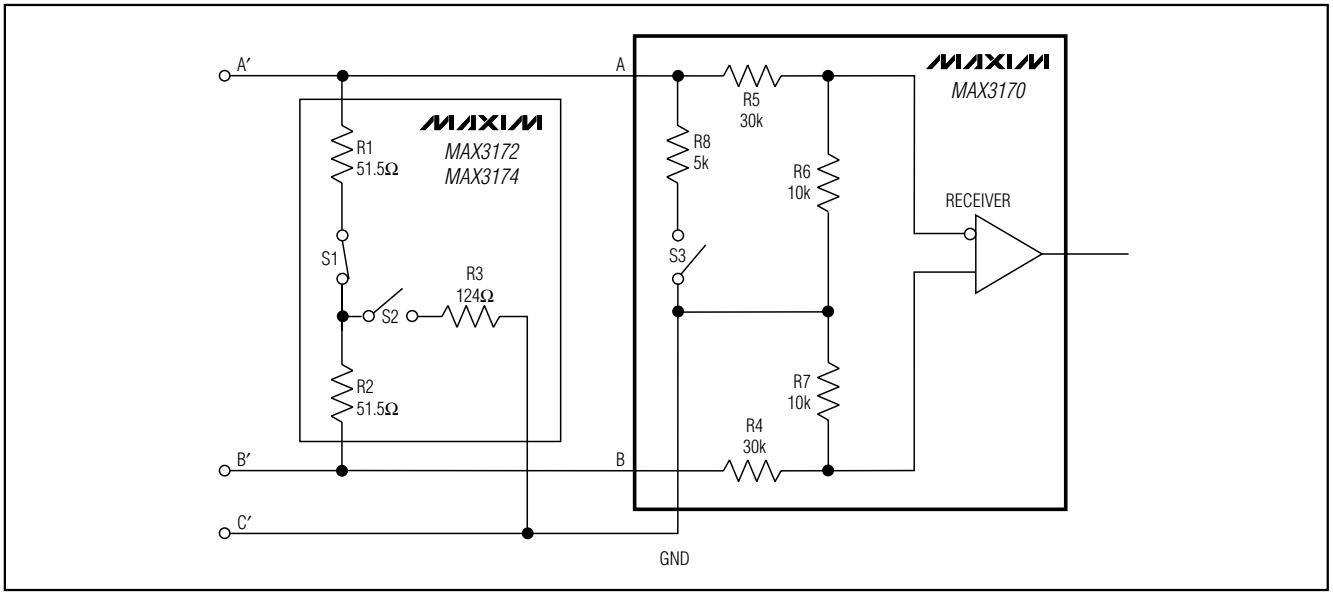


Figure 10. V.11 Termination and Internal Resistance Networks

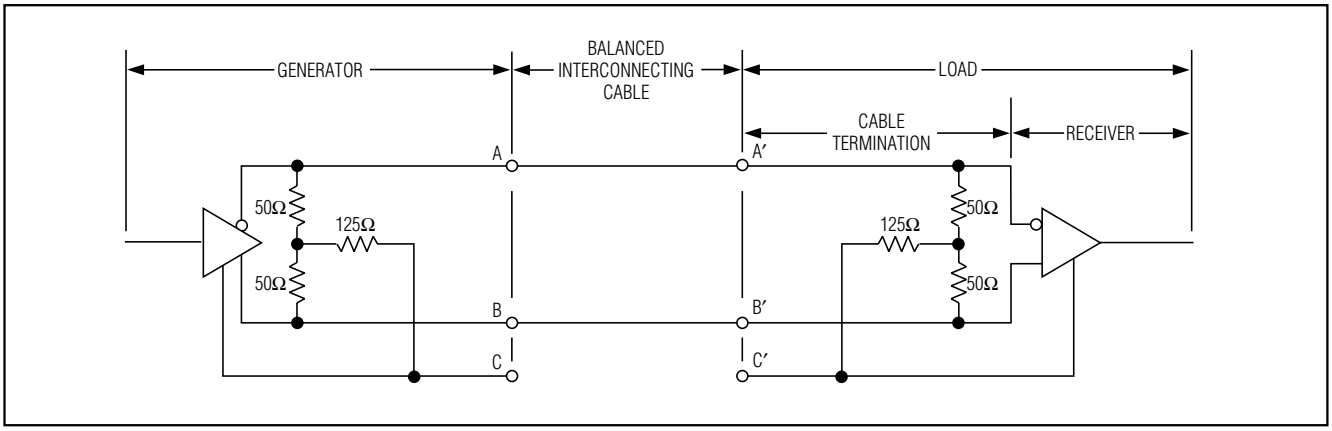


Figure 11. Typical V.35 Interface

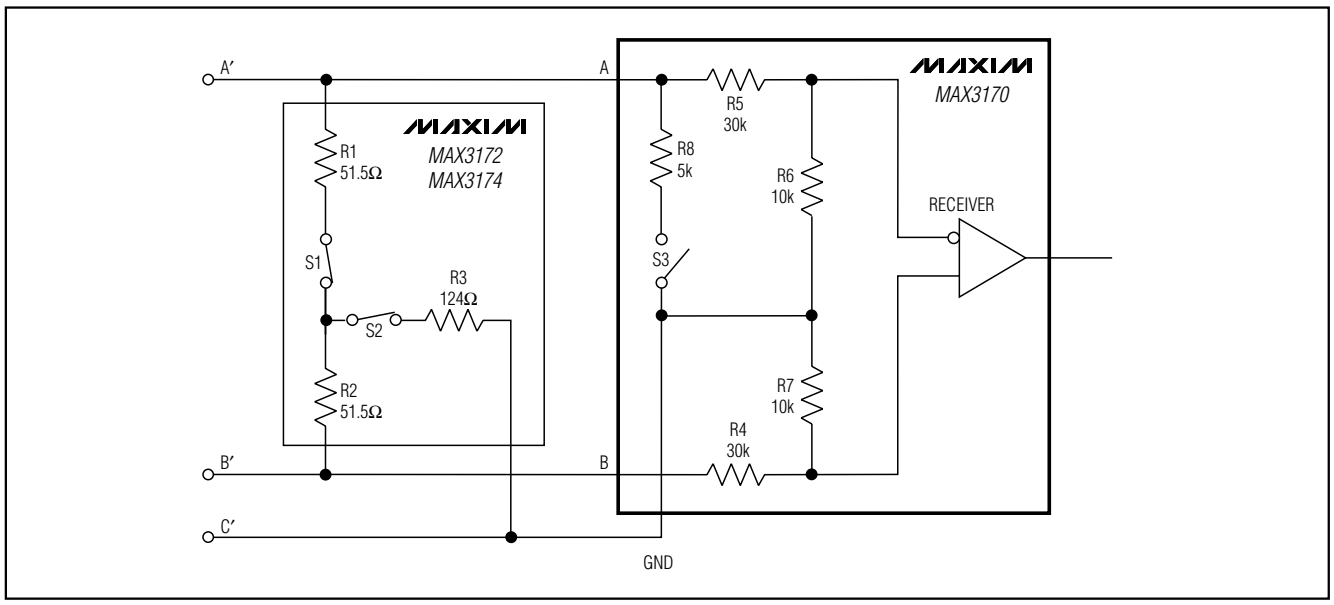


Figure 12. V.35 Termination and Internal Resistance Networks

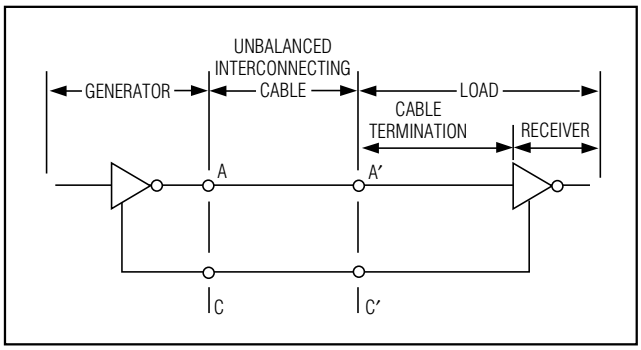


Figure 13. Typical V.28 Interface

DTE vs. DCE Operation

Figure 15 shows a DCE or DTE controller-selectable interface. The DCE/$\overline{\text{DTE}}$ pin (pin 14) switches the port's mode of operation. A logic HIGH selects DCE, which enables D3 on the MAX3170, D3 on the MAX3171/MAX3173, and D4 on the MAX3172/MAX3174. A logic LOW selects DTE, which enables R1 on the MAX3170, R1 on the MAX3171/MAX3173, and R4 on the MAX3172/MAX3174.

This application requires only one DB-25 connector, but separate cables for DCE or DTE signal routing. See Figure 15 for complete signal routing in DCE and DTE modes. For example, the MAX3170's D3 routes the TXC (DCE) signal to pins 12 and 15 in DCE mode, while in DTE mode, the MAX3170's R1 routes pins 12 and 15 to TXC (DTE).

Complete Multiprotocol X.21 Interface

A complete DTE-to-DCE interface operating in X.21 mode is shown in Figure 16. The MAX3170 is used to generate the clock and data signals, and the MAX3171/MAX3173 generate the control signals. The MAX3172/MAX3174 generate local loopback (LL), and are used to terminate the clock and data signals to support the V.11 protocol for cable termination. The control signals do not need external termination.

Compliance Testing

A European Standard EN 45001 test report is available for the MAX3170/MAX3171/MAX3173/MAX3172/MAX3174 chipset. A copy of the test report will be available from Maxim upon completion.

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

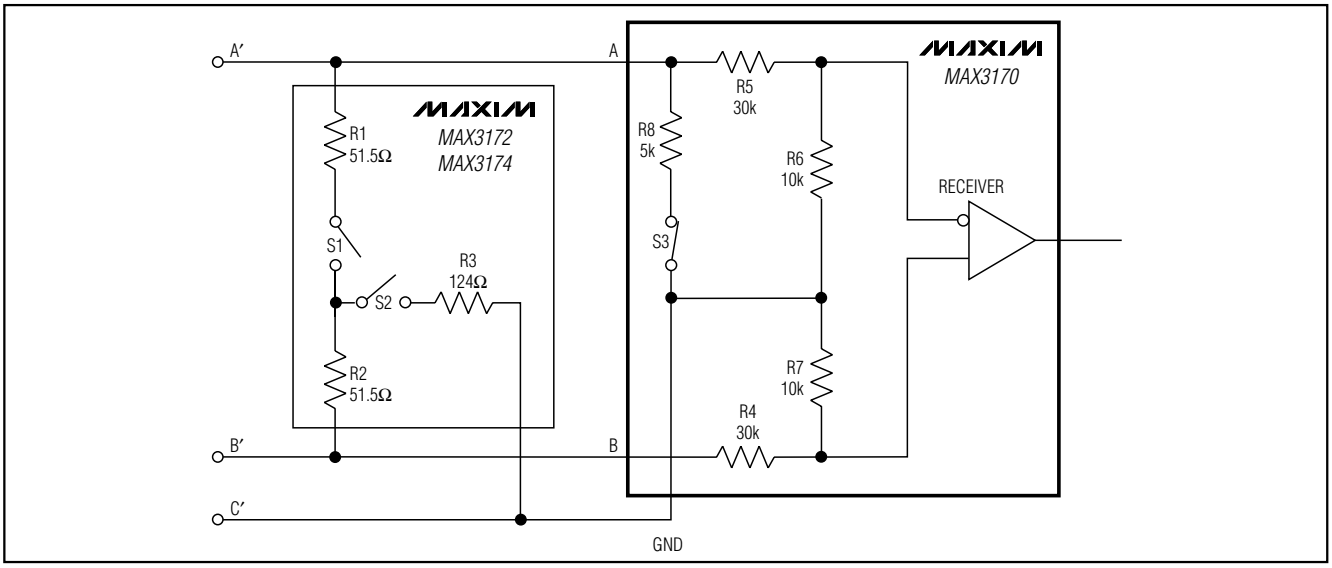


Figure 14. V.28 Termination and Internal Resistance Networks

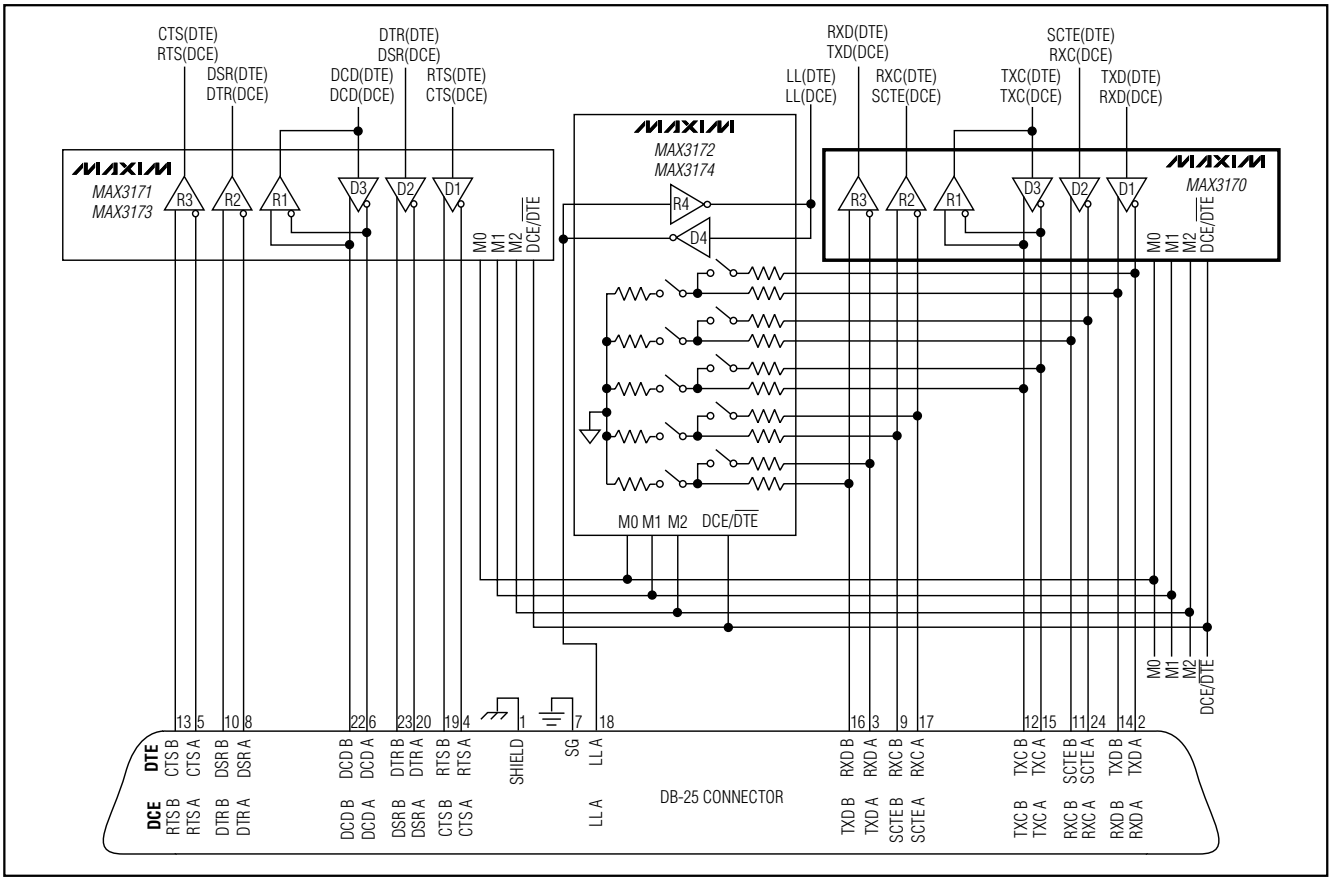


Figure 15. Multiprotocol DCE/DTE Port

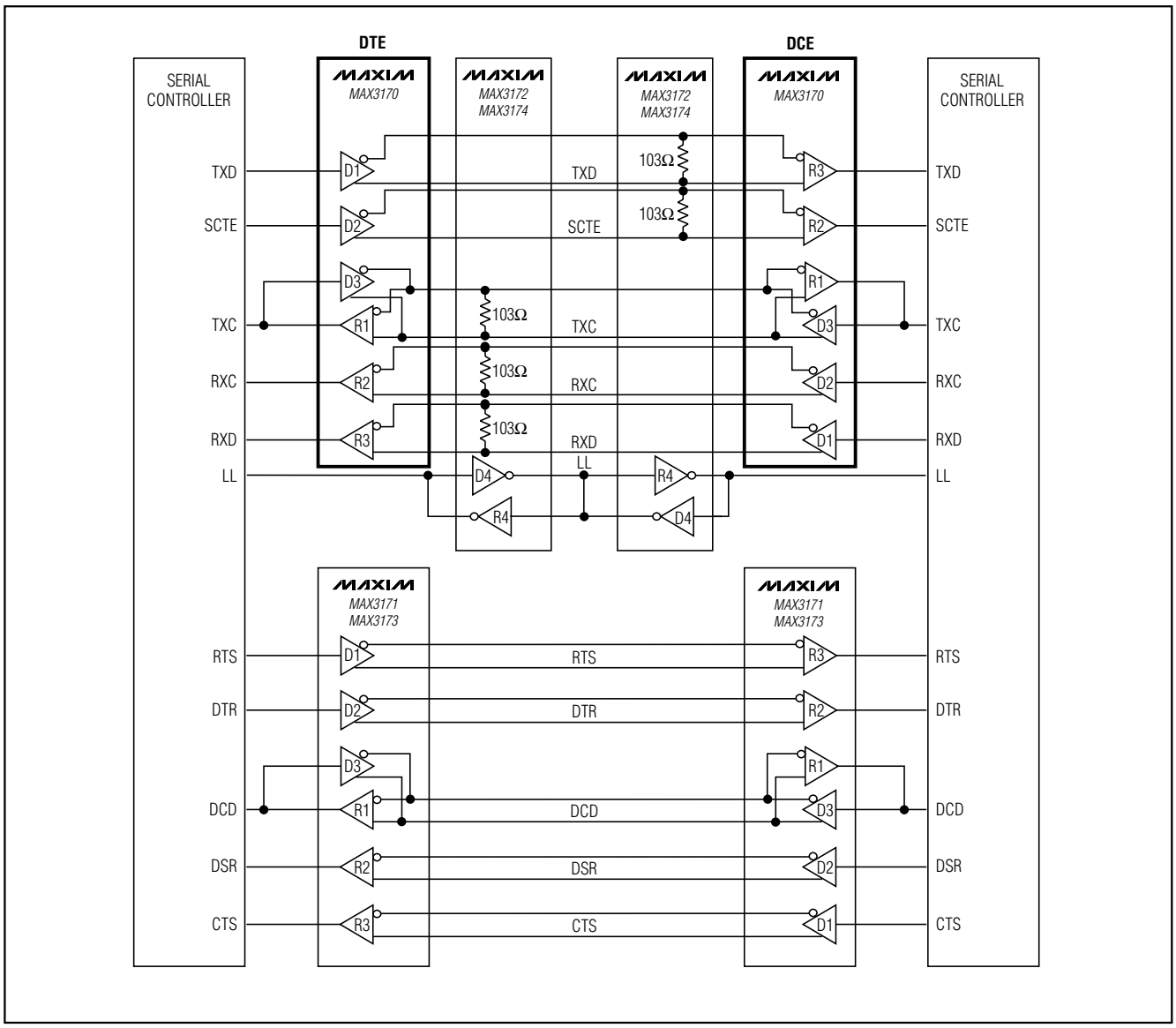
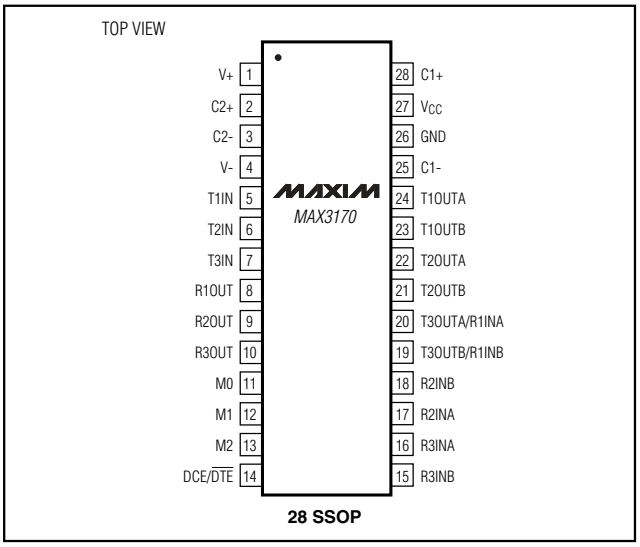


Figure 16. DCE-to-DTE X.21 Interface

+3.3V, Multiprotocol, 3 Tx/3 Rx, Software-Selectable Clock/Data Transceiver

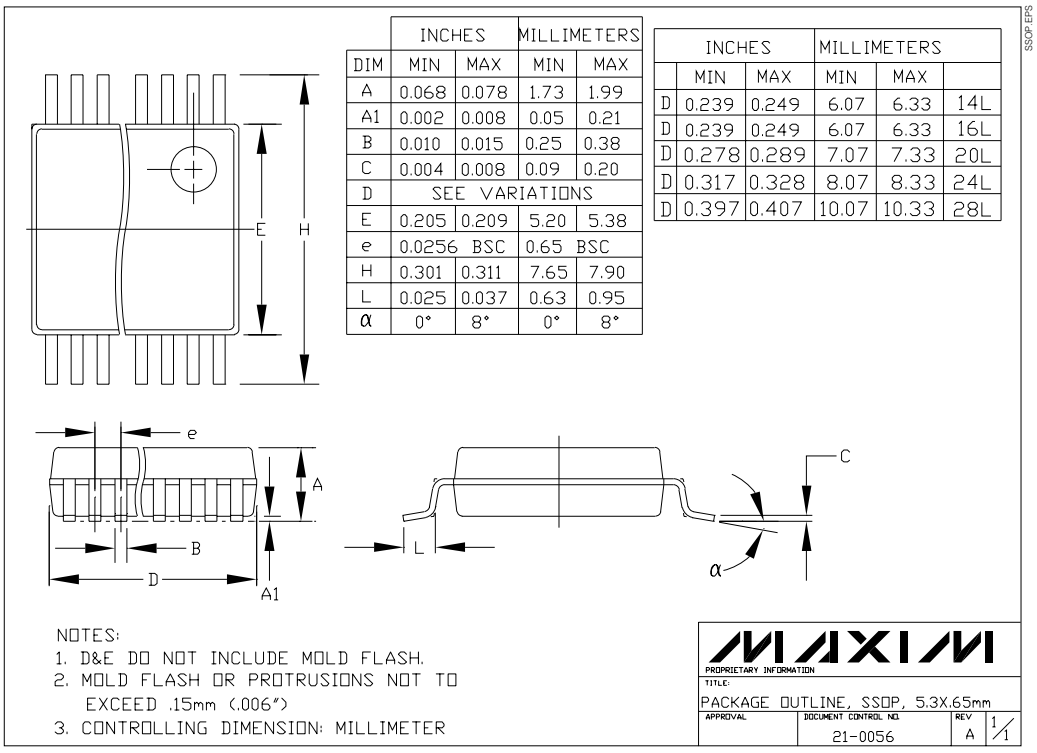
Pin Configuration



Chip Information

TRANSISTOR COUNT: 4058

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SSOP, 5.3X.65mm
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV A | 1/1