AN200810

S25FL-P (32 Mb / 64 Mb) Package Routing Guide

AN200810 provides a general routing guide for packages (substrate/leadframe) designed with Cypress S25FL-P (32 Mb or 64 Mb) die.

1 Introduction

This document provides a general routing guide for packages (substrate/leadframe) designed with Cypress S25FL-P (32 Mb or 64 Mb) die.

This document does not eliminate the need for customer signal integrity/power delivery simulations. Customers should use Cypress provided IBIS models for timing/crosstalk analysis.

2 Signal Descriptions

The following table describes various pads used in the S25FL-P die.

Signal/Supply Pad Name	Description
SCK	Serial Clock input.
CS#	Chip Select input.
SI/IO0	Serial Data Input. Functions as an output pin in Dual and Quad IO mode.
W#/ACC/IO2	Write Protect. Functions as an output in Quad IO mode.
SO/IO1	Serial Data Output.
HOLD#/IO3	Hold input pin. Functions as an output in Quad IO mode.
V_{CC}	Power supply (2.7-3.6V).
V_{SS}	Device ground.

3 Signal Groupings

The following table describes various signal/supply groupings to assist in package routing and signal integrity simulations.

Signal/Supply Group	Description
SI/IO0, SO/IO1,W#/ACC/IO2, HOLD#/IO3	Data I/O
SCK, CS#	Control signals
V_{CC}, V_{SS}	Supply

4 Supply Routing Guidelines

Cypress recommends meeting or beating the supply routing recommendations below.

1. Provide a dedicated V_{CC} ball/pin to which the V_{CC} pad is routed to.
2. Provide a dedicated V_{SS} ball/pin to which the V_{CC} pad is routed to.
3. Maintain a low inductance/resistance path from supply pad (V_{CC}, V_{SS}) to solder ball/pin.
4. Keep path inductance for each of the supply nets (from each supply pad to its solder ball/pin) $\leq$ 3.0 nH.

5. Keep path resistance from each supply pad to its solder ball ≤ 100 mΩ.
6. Except for necking/bondfinger breakout region, maintain supply (V_{CC}/V_{SS}) trace width ≥ 100 µm (wider the better).
7. Route V_{CC} close to V_{SS} trace (regardless of the bondwire location) to maintain V_{CC}-V_{SS} inductance loop constant. In general a 50 µm separation between V_{CC}/V_{SS} supply traces is ideal, whenever possible.
8. Select V_{CC} and V_{SS} solder ball location next to each other on the ball map.
9. While doing layer transitions in a BGA substrate, use dual vias as much as possible to reduce via current crowding.

5 Signal Routing Guidelines

Cypress recommends meeting or beating the signal routing recommendations below.

1. Maintain data IO signal routing to within ± 1 nH of each other. Limit DQ routing to ≤ 5 nH.
2. Maintain all DQ routing within +/- 1 nH of SCK.
3. Route control traces (SCK and CS#) ≤ 4 nH.
4. As much as possible, maintain similar via count on all signals within data I/O group.
5. Route flash traces away from other interface high speed signals to avoid crosstalk.
6. Avoid long plating traces for SCK (will cause reflections and impact timing).

6 Multi-Chip Package Routing

If S25FL-P die is used along with other (non-flash) dies in a single MCP, the following routing recommendations should be followed in addition to those in Section 4 and Section 5

1. Keep flash V_{CC}/V_{SS} separate from other die/interface V_{CC}/V_{SS} (routing as well as solderball/pin allocations).
2. It may be possible to share V_{SS} between Cypress flash and PSRAM die (if present) provided PSRAM speed doesn't exceed flash speed. Controller V_{SS} can only be shared if it pertains to flash interface only. Do not share V_{SS} between different interfaces (e.g. DDR and flash).
3. Provide V_{SS} shielding between flash traces/supplies and other interface supply/signal traces (150 µm min. trace width).
4. If signals are shared with another die (e.g. PSRAM) the following general rules should be used:

   All control signals should be routed in Y configuration. Maintain the overall inductance from pad to ball within guidelines specified in Section 4 and Section 5 However, the fork lengths going to both dies should be electrically matched (provided both dies have similar input capacitance. If they have different input capacitances, IBIS simulations need to be performed to determine fork lengths).

   All Data I/O topologies need to be simulated to provide adequate topology (daisy chain or Y). However, it is recommended that flash path inductance from signal pad to ball/pin follows guidelines specified in Section 4 and Section 5

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	11/10/2011	Initial version
*A	4994102	MSWI	10/29/2015	Updated in Cypress template
*B	5846477	AESATMP8	08/08/2017	Updated logo and Copyright.

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