

#### **Operational Amplifier**

# **Automotive Excellent EMI Immunity Ground Sense Operational Amplifier**

#### LM2904EYxxx-C

#### **General Description**

LM2904EYxxx-C is high-gain and ground sense input operational amplifier. This IC is monolithic IC integrated dual independent operational amplifier on a single chip. An operating voltage range is wide with 3 V to 36 V. This operational amplifier is the most suitable for automotive requirements such as engine control unit, electric power steering, anti-lock braking system and so on because it has features of low supply current.

Furthermore, they have the advantage of EMI tolerance. It makes easier replacing with conventional products or simpler designing EMI.

#### **Features**

- EMARMOUR<sup>TM</sup> Series
- AEC-Q100 Qualified<sup>(Note 1)</sup>
- Operable from Almost GND Level for Both Input and Output
- Single or Dual Power Supply Operation
- Standard Op-Amp Pin-assignments
- Low Supply Current
- Wide Operating Supply Voltage Range
- High Open Loop Voltage Gain
- Wide Operating Temperature Range (Note 1) Grade 1

#### **Applications**

- Engine Control Unit
- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Automotive Electronics

#### **Key Specifications**

Operating Supply Voltage Range

Single Supply: 3.0 V to 36.0 V
Dual Supply: ±1.5 V to ±18.0 V
■ Operating Temperature Range: -40 °C to +150 °C

■ Low Supply Current: 0.6 mA (Typ)
■ Input Offset Current: 2 nA (Typ)
■ Input Bias Current: 20 nA (Typ)

**Package** 

SOP8 SOP-J8 MSOP8 W (Typ) x D (Typ) x H (Max) 5.0 mm x 6.2 mm x 1.71 mm 4.9 mm x 6.0 mm x 1.65 mm 2.9 mm x 4.0 mm x 0.9 mm



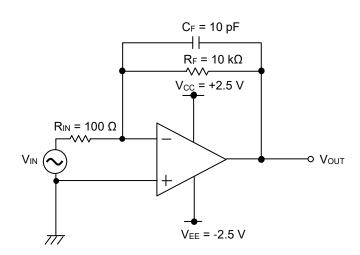


SOP8

SOP-J8



**Typical Application Circuit** 

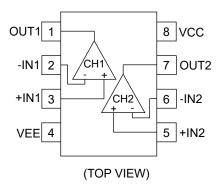


$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

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#### **Pin Configuration**

LM2904EYF-C: SOP8 LM2904EYFJ-C: SOP-J8 LM2904EYFVM-C: MSOP8



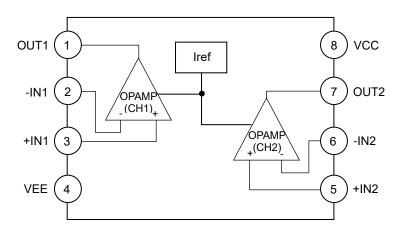
#### **Pin Description**

LM2904EYF-C: SOP8 LM2904EYFJ-C: SOP-J8 LM2904EYFVM-C: MSOP8

VIVI-C. IVISOPO	/W-G. M3OF6							
Pin No. Pin Name		Function						
1 OUT1		Output (1 ch)						
2 -IN1		Inverting input (1 ch)						
3	+IN1	Non-inverting input (1 ch)						
4 VEE		Negative power supply / Ground						
5	+IN2	Non-inverting input (2 ch)						
6	-IN2	Inverting input (2 ch)						
7 OUT2		Output (2 ch)						
8	VCC	Positive power supply						

#### **Block Diagram**

LM2904EYF-C: SOP8 LM2904EYFJ-C: SOP-J8 LM2904EYFVM-C: MSOP8



#### **Description of Blocks**

- 1. OPAMP:
  - This block is a ground sense operational amplifier with differential input stage.
- 2. Iref:

This block supplies reference current which is needed to operate OPAMP block.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc-Vee	36	V
Differential Input Voltage <sup>(Note 1)</sup>	V <sub>ID</sub>	Vcc-Vee	V
Common-mode Input Voltage Range	VICMR	(V <sub>EE</sub> - 0.3) to (V <sub>EE</sub> + 36)	V
Output Current <sup>(Note 2)</sup>	Іоит	±40	mA
Input Current	II	±10	mA
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

- Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.
- Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.
- (Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input. The input pin voltage is set to VEE or more.
- (Note 2) The excessive heat generation may occur due to the short-circuit from the output pin to the power supply pin. Do not use the output pin short to power supply. Use the output current less than 40mA regardless of the power supply voltage.

#### Thermal Resistance(Note 3)

Davamatan	Currele el	Thermal Re	Linit	
Parameter	Symbol	1s <sup>(Note 5)</sup>	2s2p <sup>(Note 6)</sup>	- Unit
SOP8				
Junction to Ambient	θја	197.4	109.8	°C/W
Junction to Top Characterization Parameter <sup>(Note 4)</sup>	$\Psi_{JT}$	21	19	°C/W
SOP-J8	·			
Junction to Ambient	θја	149.3	76.9	°C/W
Junction to Top Characterization Parameter <sup>(Note 4)</sup>	Ψ <sub>JT</sub>	18	11	°C/W
MSOP8				
Junction to Ambient	θја	284.1	135.4	°C/W
Junction to Top Characterization Parameter <sup>(Note 4)</sup>	Ψ <sub>JT</sub>	21	11	°C/W

(Note 3) Based on JESD51-2A(Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-3.

(Note 6) Using a PCB board based on JESD51-7.

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Layer Number of Measurement Board	Material	Board Size			
Single	FR-4	114.3 mm x 76.2 mm x	114.3 mm x 76.2 mm x 1.57 mmt		
Тор					
Copper Pattern	Thickness				
Footprints and Traces	70 µm				
Layer Number of Measurement Board	Material	Board Size			
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt			
Тор		2 Internal Laye	ers	Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	
Footprints and Traces	70 um	74.2 mm x 74.2 mm	35 um	74.2 mm x 74.2 mm	

**Thickness** 70 µm

**Recommended Operating Conditions** 

Parameter	Symbol	Min	Тур	Max	Unit	
Operating Supply Voltage	Single Supply	V	3.0	-	36.0	V
	Dual Supply	Vcc	±1.5	-	±18.0	
Operating Temperature	Topr	-40	+25	+150	°C	

#### **Function Explanation**

#### 1. EMARMOUR™

EMARMOUR<sup>TM</sup> is the brand name given to ROHM products developed by leveraging proprietary technologies covering layout, process, and circuit design to achieve ultra-high noise immunity that limits output voltage fluctuation to ±300 mV or less across the entire noise frequency band during noise evaluation testing under the international ISO11452-2 standard. This unprecedented noise immunity reduces design load while improving reliability by solving issues related to noise in the development of vehicle electrical systems.

#### Electrical Characteristics (Unless otherwise specified V<sub>CC</sub> = 5 V, V<sub>EE</sub> = 0 V)

Dt	0	Temperature		Limit		11	0 1:4:	
Parameter	Symbol	Range	Min	Тур	Max	Unit	Conditions	
		25 °C	-	2	6		V <sub>OUT</sub> = 1.4 V Absolute value	
Input Offset Voltage	Vio	-40 °C to +150 °C	-	-	9	mV	V <sub>CC</sub> = 5 V to 30 V V <sub>OUT</sub> = 1.4 V Absolute value	
Input Offset Current	IIO	25 °C	-	2	40	nA	V <sub>OUT</sub> = 1.4 V	
input Onset Current	IIO	-40 °C to +150 °C	-	-	50	IIA	Absolute value	
Input Pice Current	I_	25 °C	-	20	60	nΛ	V <sub>OUT</sub> = 1.4 V	
Input Bias Current	lΒ	-40 °C to +150 °C	-	-	100	- nA	Absolute value	
Supply Current	1	25 °C	-	0.6	1.2	mΛ	D. = as All On Amna	
Supply Current	Icc	-40 °C to +150 °C	-	-	1.2	- mA	R <sub>L</sub> = ∞, All Op-Amps	
		25 °C	3.5	-	-		D = 210	
Output Voltage High	V <sub>OH</sub>	-40 °C to +150 °C	3.2	-	-	V	$R_L = 2 k\Omega$	
		-40 °C to +150 °C	27	28			$V_{CC}$ = 30 V, $R_L$ = 10 k $\Omega$	
Output Voltage Low	Vol	-40 °C to +150 °C	-	5	20	mV	R <sub>L</sub> = ∞	
Lawre Ciarall Veltaria Cair	Av	25 °C	88	100	-	dB	$R_L \ge 2 \text{ k}\Omega, V_{CC} = 15 \text{ V}$ $V_{OUT} = 1.4 \text{ V to } 11.4 \text{ V}$	
Large Signal Voltage Gain		-40 °C to +150 °C	88	-	-			
	VICMR	25 °C	0	-	3.5	V	(Vcc-Vee) = 5 V Vout = Vee + 1.4 V	
Common-mode Input Voltage Range		-40 °C to +125 °C	0	-	3.0			
3		-40 °C to +150 °C	0.2	-	3.0			
Common-mode Rejection Ratio	CMRR	-40 °C to +150 °C	60	80	-	dB	V <sub>OUT</sub> = 1.4 V	
Power Supply Rejection Ratio	PSRR	-40 °C to +150 °C	70	100	-	dB	V <sub>CC</sub> = 5 V to 30 V	
0 1 10 0 (Mate 1)		25 °C	20	30	40		V <sub>+IN</sub> = 1 V, V <sub>-IN</sub> = 0 V V <sub>OUT</sub> = 0 V	
Output Source Current <sup>(Note 1)</sup>	Іон	-40 °C to +150 °C	10	-	-	- mA	1 ch is short circuit Absolute value	
		25 °C	20	27	40		V <sub>+IN</sub> = 0 V, V <sub>-IN</sub> = 1 V V <sub>OUT</sub> = 5 V	
Output Sink Current <sup>(Note 1)</sup>	loL	-40 °C to +150 °C	2	-	-	mA	1 ch is short circuit Absolute value	
		25 °C	20	50	-	μA	V <sub>+IN</sub> = 0 V, V <sub>-IN</sub> = 1 V V <sub>OUT</sub> = 200 mV	
Slew Rate	SR	25 °C	-	0.2	-	V/µs	$V_{CC} = 15 \text{ V}, A_V = 0 \text{ dB}$ $R_L = 2 \text{ k}\Omega, C_L = 100 \text{ pF}$	
Gain Bandwidth Product	GBW	25 °C	-	0.5	-	MHz	$V_{CC} = +15 \text{ V}, V_{EE} = -15 \text{ V}$ $R_L = 2 \text{ k}\Omega, C_L = 100 \text{ pF}$	
Channel Separation	cs	25 °C	-	120	-	dB	f = 1 kHz, Input Referred	

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

#### **Typical Performance Curves**

 $V_{EE} = 0 V$ 

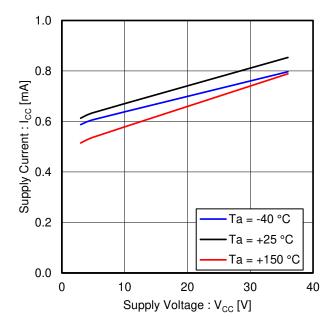


Figure 1. Supply Current vs Supply Voltage

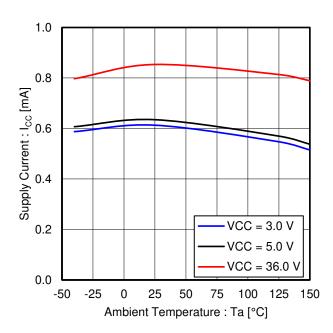


Figure 2. Supply Current vs Ambient Temperature

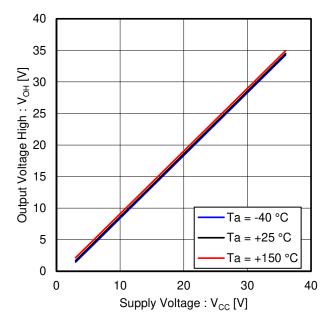


Figure 3. Output Voltage High vs Supply Voltage  $(R_L = 10 \text{ k}\Omega)$ 

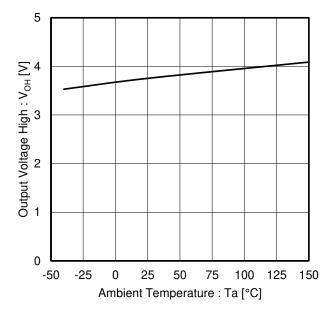


Figure 4. Output Voltage High vs Ambient Temperature  $(V_{CC} = 5 \text{ V}, \text{ R}_L = 2 \text{ k}\Omega)$ 

## Typical Performance Curves - continued $V_{\text{EE}}$ = 0 V

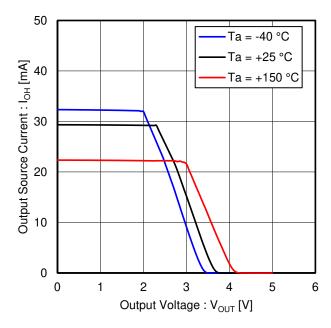


Figure 5. Output Source Current vs Output Voltage  $(V_{CC} = 5 V)$ 

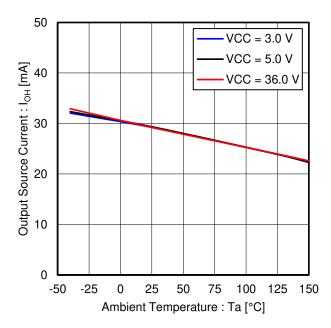


Figure 6. Output Source Current vs Ambient Temperature (Vout = 0 V)

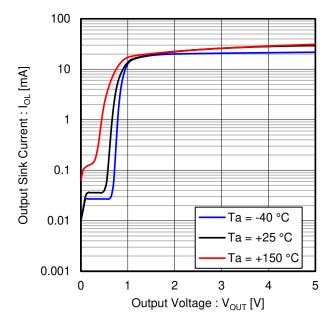


Figure 7. Output Sink Current vs Output Voltage (Vcc = 5 V)

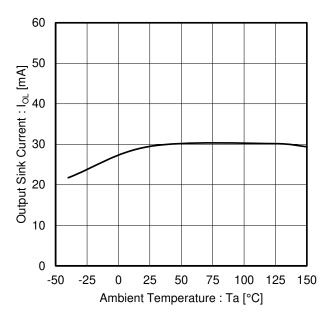


Figure 8. Output Sink Current vs Ambient Temperature  $(V_{CC} = 5 \text{ V}, V_{OUT} = 5 \text{ V})$ 

## Typical Performance Curves - continued $V_{\text{FF}} = 0 \text{ V}$

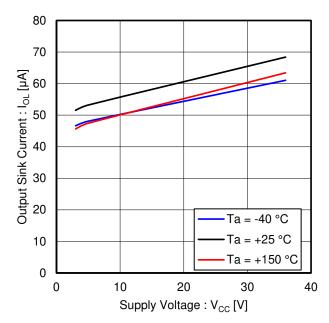


Figure 9. Output Sink Current vs Supply Voltage (Vout = 0.2 V)

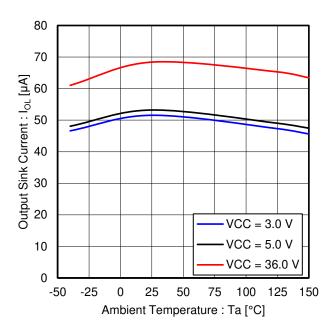


Figure 10. Output Sink Current vs Ambient Temperature (Vout = 0.2 V)

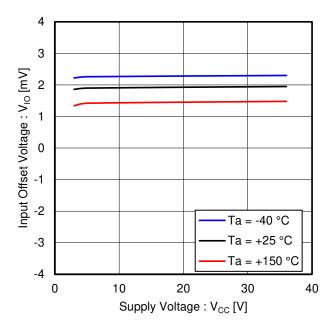


Figure 11. Input Offset Voltage vs Supply Voltage  $(V_{ICM} = V_{CC}/2)$ 

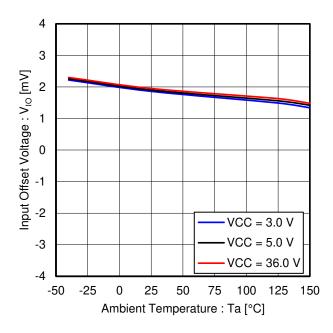


Figure 12. Input Offset Voltage vs Ambient Temperature  $(V_{ICM} = V_{CC}/2)$ 

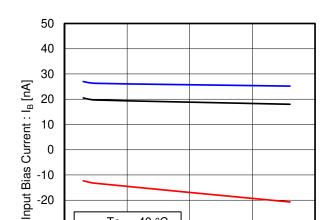
-30

-40

-50

0

#### **Typical Performance Curves - continued** $V_{EE} = 0 V$



Ta = -40 °C

Ta = +25 °C

10

Ta = +150 °C

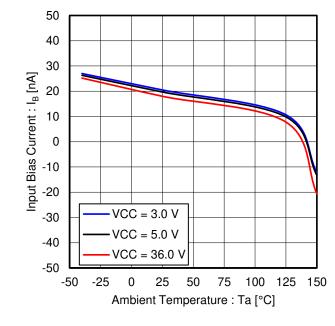


Figure 13. Input Bias Current vs Supply Voltage  $(V_{ICM} = V_{CC}/2)$ 

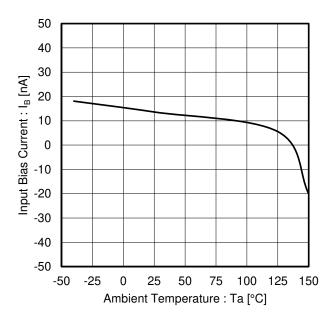
20

Supply Voltage: V<sub>CC</sub> [V]

40

30

Figure 14. Input Bias Current vs Ambient Temperature  $(V_{ICM} = V_{CC}/2)$ 



10 Ta = -40 °C 8 Ta = +25 °C6 Input Offset Voltage: V<sub>IO</sub> [mV] Ta = +125 °C 4 Ta = +150 °C 2 0 -2 -4 -6 -8 -10 2 -1 0 1 3 5 Common-mode Input Voltage : V<sub>ICM</sub> [V]

Figure 15. Input Bias Current vs Ambient Temperature  $(V_{CC} = 30 \text{ V}, V_{ICM} = 28 \text{ V}, V_{OUT} = 1.4 \text{ V})$ 

Figure 16. Input Offset Voltage vs Common-mode Input Voltage  $(V_{CC} = 5 V)$ 

## Typical Performance Curves - continued $V_{FF} = 0 \text{ V}$

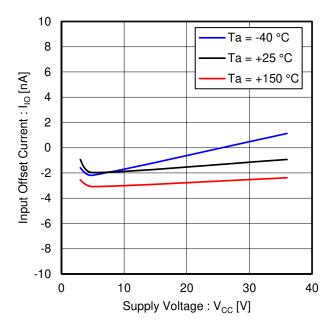


Figure 17. Input Offset Current vs Supply Voltage (V<sub>ICM</sub> = V<sub>CC</sub>/2)

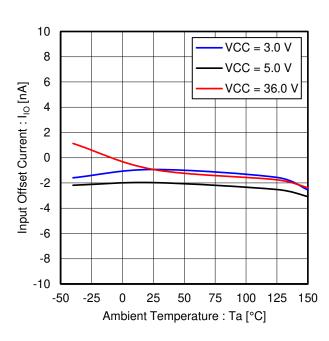


Figure 18. Input Offset Current vs Ambient Temperature (V<sub>ICM</sub> = V<sub>CC</sub>/2)

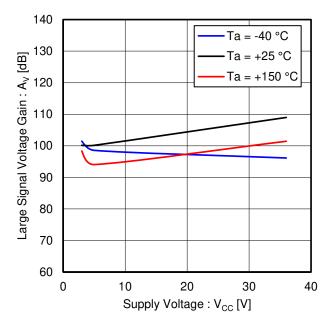


Figure 19. Large Signal Voltage Gain vs Supply Voltage  $(R_L = 2 \text{ k}\Omega)$ 

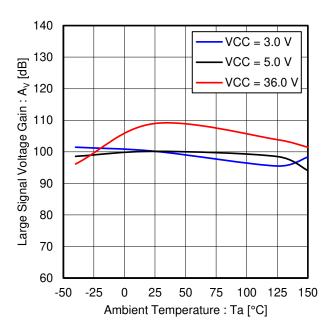


Figure 20. Large Signal Voltage Gain vs Ambient Temperature  $(R_L = 2 \text{ k}\Omega)$ 

#### **Typical Performance Curves - continued**

 $V_{EE} = 0 V$ 

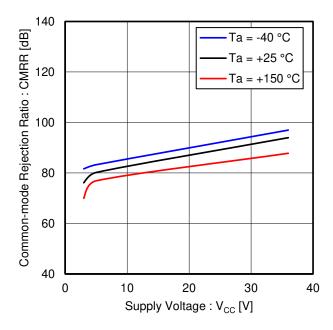


Figure 21. Common-mode Rejection Ratio vs Supply Voltage (Vout = 1.4 V)

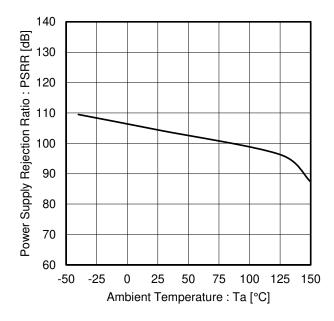


Figure 23. Power Supply Rejection Ratio vs Ambient Temperature  $(V_{CC} = 5 V)$ 

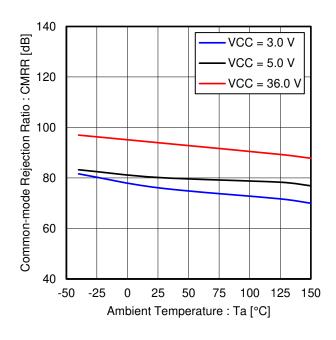


Figure 22. Common-mode Rejection Ratio vs Ambient Temperature
(Vout = 1.4 V)

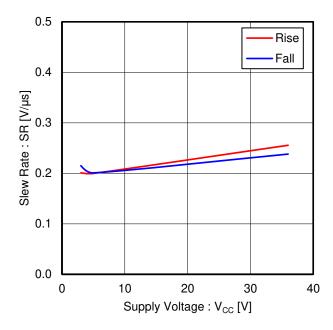


Figure 24. Slew Rate vs Supply Voltage (Ta = 25 °C,  $R_L$  = 2 k $\Omega$ )

#### **Typical Performance Curves - continued**

 $V_{EE} = 0 V$ 

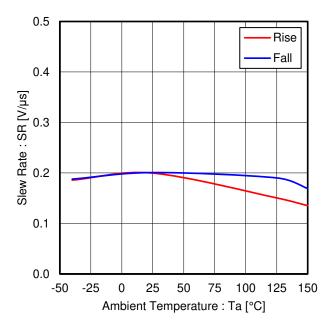


Figure 25. Slew Rate vs Ambient Temperature  $(V_{CC} = 5 \text{ V}, R_L = 2 \text{ k}\Omega)$ 

 $\textit{(Note)} \ \ \text{The above data are measurement value of typical sample; it is not guaranteed}.$ 

#### **Application Information**

#### **EMI** Immunity

LM2904EYxxx-C has high tolerance for electromagnetic interference from the outside because they have EMI filter, and the EMI design is simple. They are most suitable to replace from conventional products. The data of the IC simple substance on ROHM board are as follows. The test condition is based on ISO11452-2.

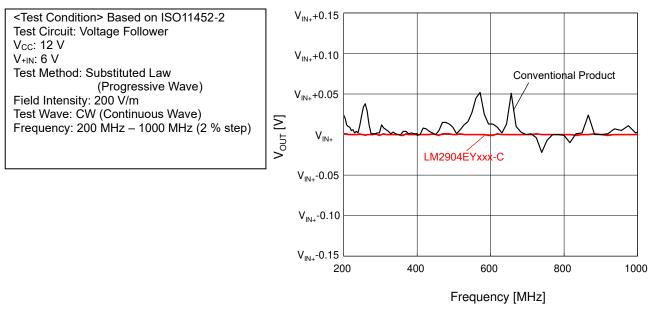


Figure 26. EMI Characteristics

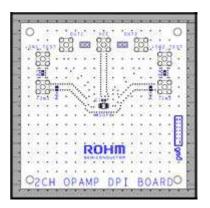


Figure 27. EMI Evaluation Board

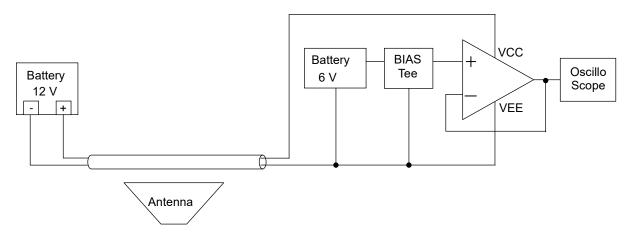


Figure 28. Measurement Circuit of EMI Evaluation

(Note) The above data is obtained using typical IC simple substance on ROHM board. These values are not guaranteed. Design and Evaluate in actual application before use.

·VCC

#### **Application Information - continued**

#### 1. Unused Circuits

When there are unused circuits, it is recommended that they are connected as in right figure, and set the non-inverting input pin to electric potential within the input common-mode voltage range (VICMR).

#### 2. Input Voltage

Applying  $V_{\text{EE}}$  + 36 V to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure circuit operation. Note that the circuit operates normally only when the input voltage is within the common-mode input voltage range of the electric characteristics.

The Op-Amp operates when the voltage is supplied between the VCC and VEE pin. Therefore, the single supply Op-Amp can be used as dual supply

## input voltage range of the electric characteristics. Figure 29. Example of application unused circuit processing 3. Power Supply (single/dual)

Connect to V<sub>ICM</sub>

#### 4. Output Capacitor

Op-Amp as well.

When the VCC pin is shorted to V<sub>EE</sub> (GND) electric potential in a state where electric charge is accumulated in the external capacitor that is connected to the output pin, the accumulated electric charge flow through parasitic elements or pin protection elements inside the circuit and discharges to the VCC pin. It may cause damage to the elements inside the circuit (thermal destruction). When using this IC as an application circuit which does not constitute a negative feedback circuit and does not occur the oscillation by an output capacitive load such as a voltage comparator, connect a capacitor of 0.1 µF or less to the output pin to prevent IC damage caused by the accumulation of electric charge as mentioned above.

#### 5. Oscillation by Output Capacitor

Pay attention to the oscillation by capacitive load in designing an application which constitutes a negative feedback loop circuit with this IC.

#### 6. Handling the IC

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations of the electrical characteristics due to the piezo resistance effects. Pay attention to defecting or bending the board.

#### **Application Examples**

#### Voltage Follower

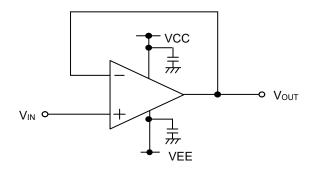


Figure 30. Voltage Follower Circuit

Using this circuit, the output voltage  $(V_{OUT})$  is configured to be equal to the input voltage  $(V_{IN})$ . This circuit also stabilizes the output voltage  $(V_{OUT})$  due to high input impedance and low output impedance. Computation for output voltage  $(V_{OUT})$  is shown below.

$$V_{OUT} = V_{IN}$$

#### olnverting Amplifier

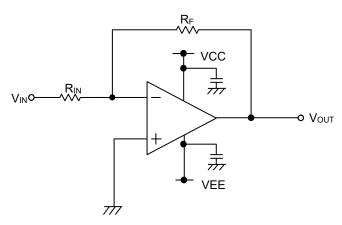


Figure 31. Inverting Amplifier Circuit

For inverting amplifier, input voltage  $(V_{IN})$  is amplified by a voltage gain which depends on the ratio of  $R_{IN}$  and  $R_{F}$ , and then it outputs phase-inverted voltage. The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R<sub>IN</sub>.

#### oNon-inverting Amplifier

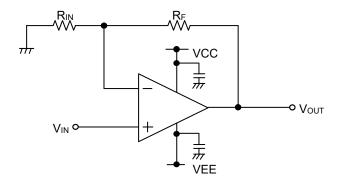


Figure 32. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage  $(V_{IN})$  is amplified by a voltage gain, which depends on the ratio of  $R_{IN}$  and  $R_{F}$ . The output voltage  $(V_{OUT})$  is in-phase with the input voltage  $(V_{IN})$  and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

J	Equivalence	Circuits		
	Pin No.	Pin Name	Pin Description	Equivalence Circuit
	1 7	OUT1 OUT2	Output	1, 7
	2 3 5 6	-IN1 +IN1 +IN2 -IN2	Input	2, 3, 5, 6 VEE

#### **Operational Notes**

#### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

#### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

#### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

#### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

#### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

#### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

#### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

#### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

#### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

#### **Operational Notes - continued**

#### 10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

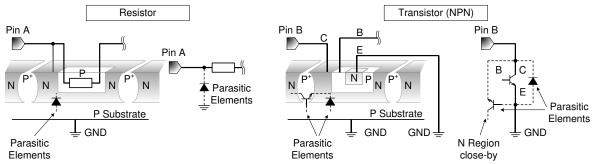
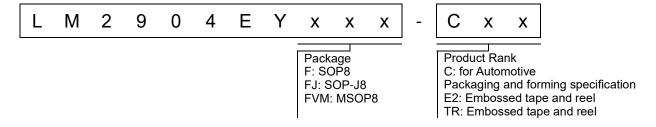


Figure 33. Example of Monolithic IC Structure

#### 11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

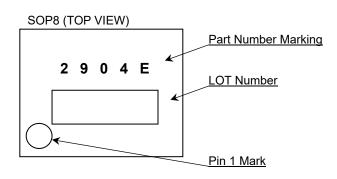
#### **Ordering Information**

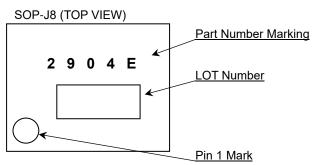


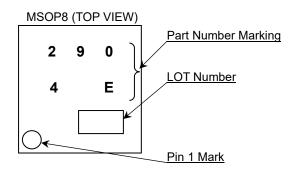
#### Lineup

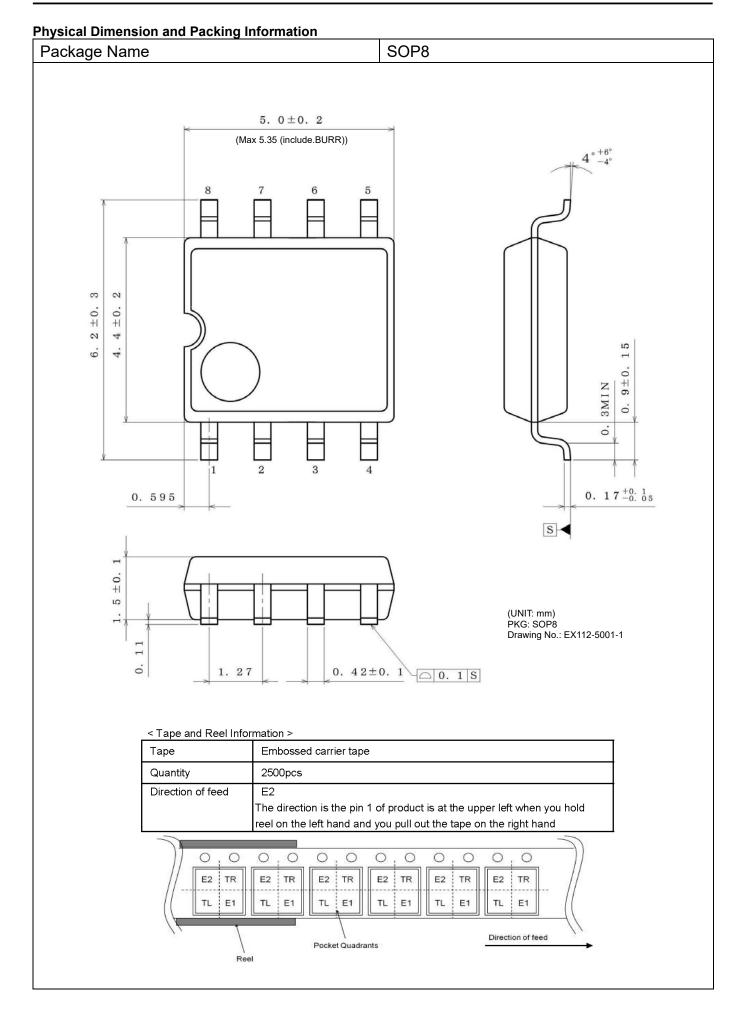
Temperature Range	Operating Supply Voltage Range	Number of Channels	Package		Orderable Part Number
			SOP8	Reel of 2500	LM2904EYF-CE2
-40 °C to +150 °C	3 V to 36 V	Dual	SOP-J8	Reel of 2500	LM2904EYFJ-CE2
			MSOP8	Reel of 3000	LM2904EYFVM-CTR

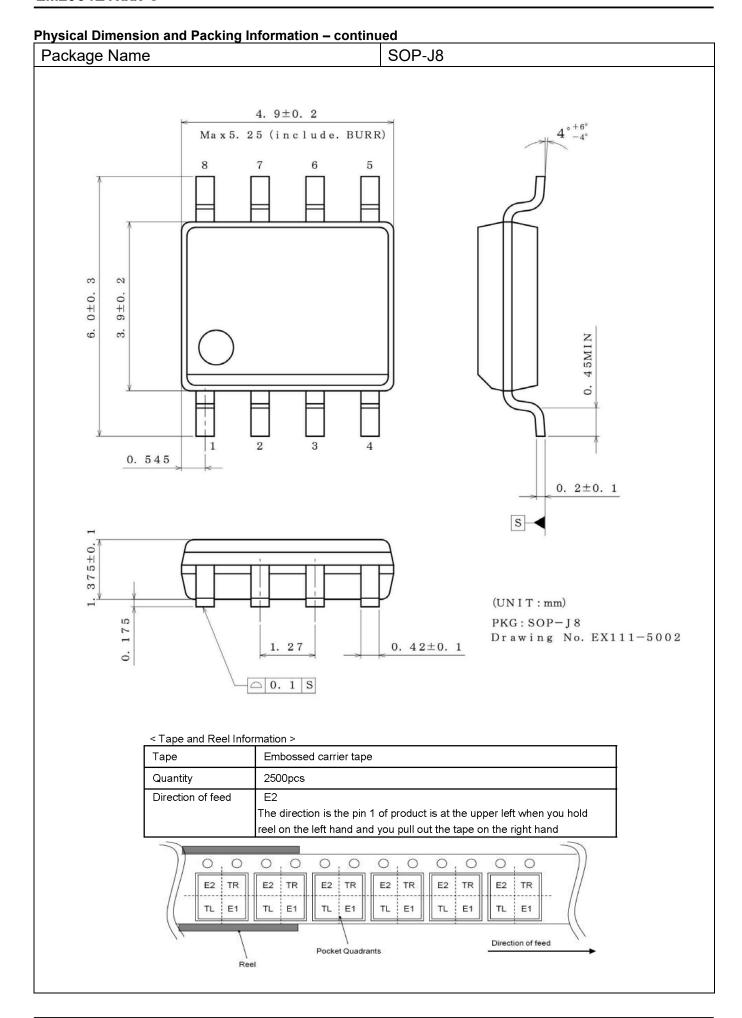
#### **Marking Diagram**











Physical Dimension and Packing Information - continued MSOP8 Package Name 2.  $9\pm0.1$ Max3. 25 (include. BURR)  $8 \pm 0.1$ 4.  $0\pm 0$ . 2.  $29\pm0.15$ 0 0 0.475 1PIN MARK  $0. \ 1\ 4\ 5\ ^{+\ 0\ .}_{-\ 0\ .}\ 0\ 5$ S 9MAX 05 05  $0.75\pm0.$  $08\pm 0$ .  $0.\ \ 2\ 2 \, {}^{+\, 0\, .}_{-\, 0\, .}\,\, {}^{0\, 5}_{0\, 4}$ (UNIT:mm) 0.65 PKG:MSOP8 0 ○ 0. 08 S Drawing No. EX181-5002 < Tape and Reel Information > Tape Embossed carrier tape 3000pcs Quantity Direction of feed The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand 0 0 0 0 0 0 0 0 0 0 0 0 E2 TR E2 TR E2 TR E2 TR TR E2 TR E2 TL E1 TL E1 TL E1 TL E1 TL E1 TL E1 Direction of feed Pocket Quadrants Reel

#### **Revision History**

Date	Revision	Changes
13.Feb.2020	001	New Release
17.Jan.2022	002	Changed the "Absolute Maximum Ratings" and "Recommended Operating Conditions" of the supply voltage.
29.Jun.2022	003	Added Lineup
01.Oct.2022	004	Modified title

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(Note1) Medical Equipment Classification of the Specific Applications

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSIIb	CLASSⅢ
CLASSIV	CLASSIII	CLASSⅢ	CLASSIII

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  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
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  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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For details, please refer to ROHM Mounting specification

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#### **Precaution for Storage / Transportation**

- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
  may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is
  exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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