

# Self Protected Very Low $I_q$ High Side Driver with Analog Current Sense

## NCV84160

The NCV84160 is a fully protected single channel high side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids, and other actuators. The device incorporates advanced protection features such as active inrush current management, over-temperature shutdown with automatic restart and an overvoltage active clamp. A dedicated Current Sense pin provides precision analog current monitoring of the output as well as fault indication of short to  $V_D$ , short circuit to ground and ON and OFF state open load detection. An active high Current Sense Disable pin allows all diagnostic and current sense features to be disabled.

### Features

- Short Circuit Protection with Inrush Current Management
- CMOS (3 V / 5 V) Compatible Control Input
- Very Low Standby Current
- Very Low Current Sense Leakage
- Proportional Load Current Sense
- Current Sense Disable
- Off State Open Load Detection
- Output Short to  $V_D$  Detection
- Overload and Short to Ground Indication
- Thermal Shutdown with Automatic Restart
- Undervoltage Shutdown
- Integrated Clamp for Inductive Switching
- Loss of Ground and Loss of  $V_D$  Protection
- ESD Protection
- Reverse Battery Protection
- AEC-Q100 Qualified
- This is a Pb-Free Device

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

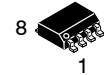
### FEATURE SUMMARY

Max Supply Voltage	$V_D$	41	V
Operating Voltage Range	$V_D$	4.5 to 28	V
$R_{DSon}$ (max) $T_J = 25^\circ\text{C}$	$R_{ON}$	160	m $\Omega$
Output Current Limit (typical)	$I_{LIM}$	12	A
OFF-state Supply Current (typical)	$I_{D(off)}$	0.01	$\mu\text{A}$



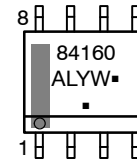
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SOIC-8  
CASE 751  
STYLE 11

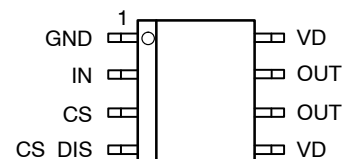
### MARKING DIAGRAM



84160 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NCV84160DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Block Diagram & Pin Configuration

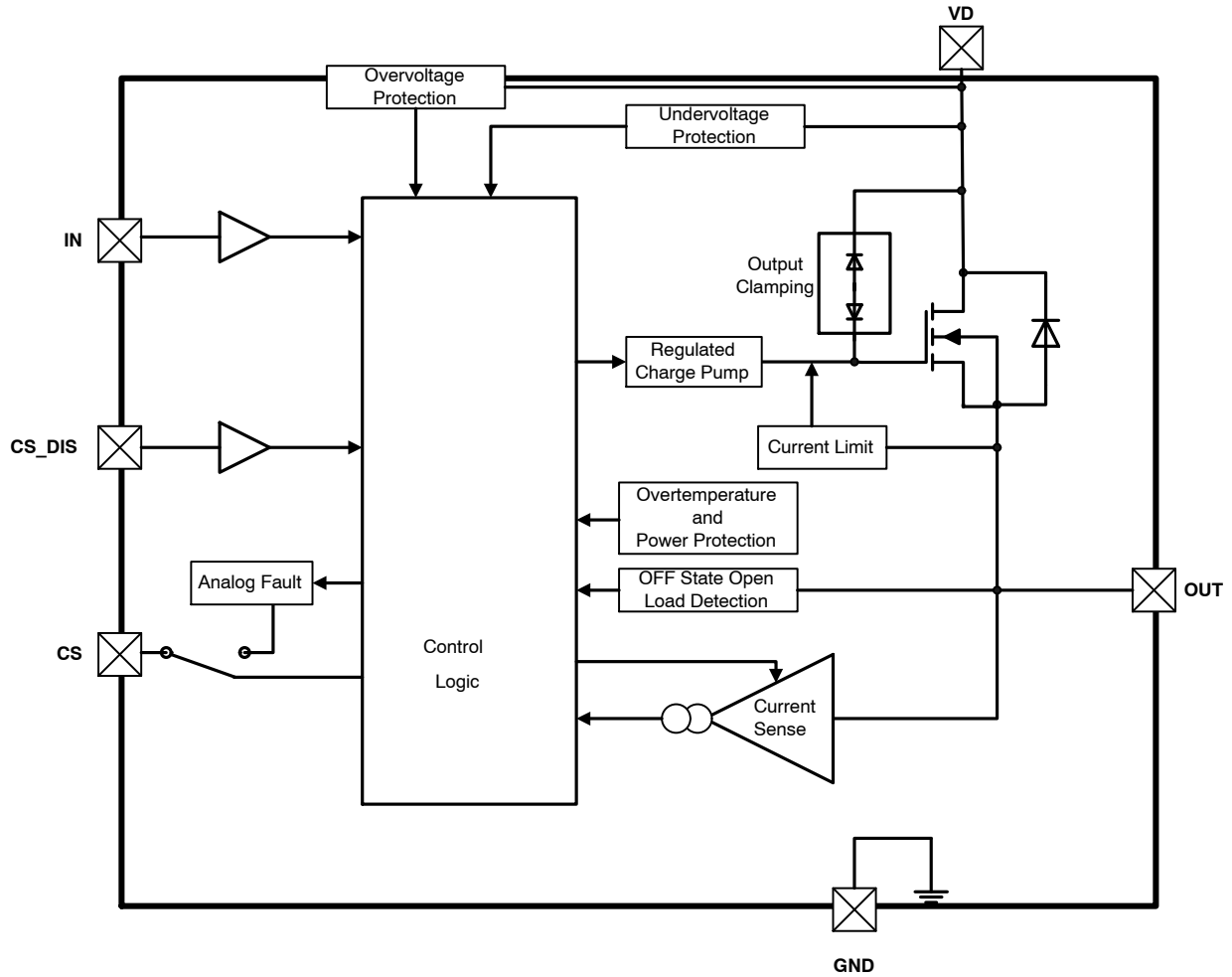


Figure 1. Block Diagram

Table 1. SO8 PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	GND	Ground
2	IN	Logic Level Input
3	CS	Analog Current Sense Output
4	CS_DIS	Active High Current Sense Disable
5	V <sub>D</sub>	Supply Voltage
6	OUT	Output
7	OUT	Output
8	V <sub>D</sub>	Supply Voltage

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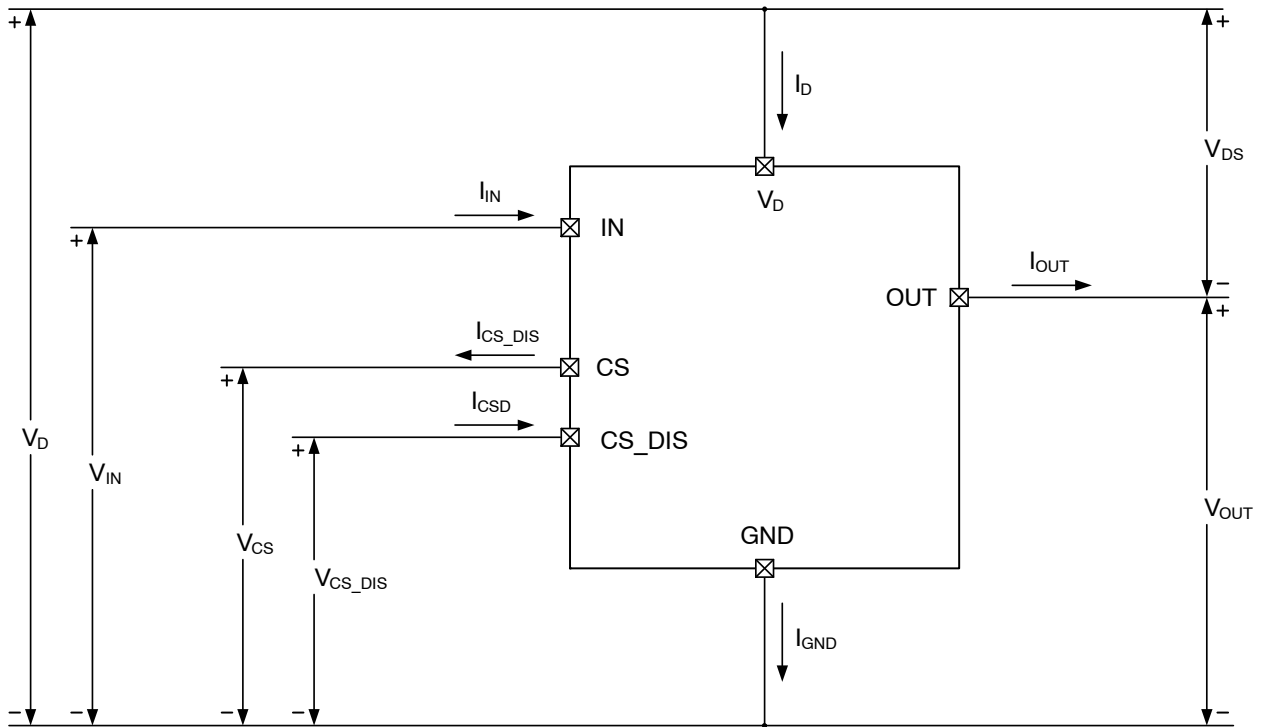


Figure 2. Voltage and Current Conventions

Table 2. Connection suggestions for unused and or unconnected pins

Connection	Input	Output	Current Sense	Current Sense Enable
Floating	X	X	Not Allowed	X
To Ground	Through 10 k $\Omega$ resistor	Not Allowed	Through 1 k $\Omega$ Resistor	Through 10 k $\Omega$ resistor

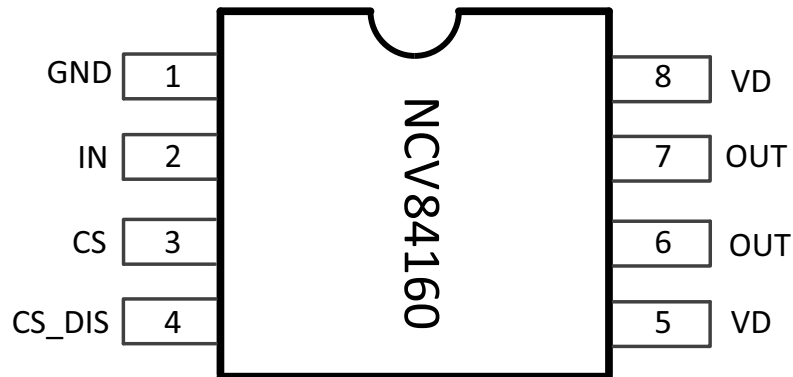


Figure 3. Pin Configuration (top view)

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## ELECTRICAL SPECIFICATIONS

**Table 3. MAXIMUM RATINGS**

Rating	Symbol	Value		Unit
		Min	Max	
DC Supply Voltage	$V_D$	-0.3	41	V
Peak Transient Input Voltage (Load Dump 46 V, $V_D = 14$ V, ISO16750-2: 2012 Test B)	$V_{peak}$		48	V
Input Voltage	$V_{IN}$	-10	10	V
Input Current	$I_{IN}$	-5	5	mA
Reverse Ground Pin Current	$I_{GND}$		-200	mA
Output Current (Note 2)	$I_{OUT}$	-6	Internally Limited	A
CS Current	$I_{CS}$		200	mA
CS Voltage	$V_{CS}$	$V_D - 41$	$V_D$	V
CS_DIS Voltage	$V_{CS\_DIS}$	-10	10	V
CS_DIS Current	$I_{CS\_DIS}$	-5	5	mA
Power Dissipation $T_c = 25^\circ\text{C}$ (Note 4)	$P_{tot}$	1.49		W
Electrostatic Discharge (HBM Model 100 pF / 1500 $\Omega$ )	$V_{ESD}$			DC
Input		4		kV
Current Sense		3		kV
Current Sense Enable		4		kV
Output		3		kV
$V_D$		3		kV
Charge Device Model CDM-AEC-Q100-011		750		V
Single Pulse Inductive Load Switching Energy (Note 1) ( $L = 8$ mH, $V_{bat} = 13.5$ V; $I_L = 3.08$ A, $T_{J\_Start} = 150^\circ\text{C}$ )	$E_{AS}$		53.71	mJ
Operating Junction Temperature	$T_J$	-40	+150	$^\circ\text{C}$
Storage Temperature	$T_{storage}$	-55	+150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Not subjected to production testing
2. Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance.

**Table 4. THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Max. Value	Units
Thermal Resistance			$^\circ\text{C}/\text{W}$
Junction-to-Lead	$R_{\theta JL}$	32	
Junction-to-Ambient (Note 3)	$R_{\theta JA}$	98	
Junction-to-Ambient (Note 4)	$R_{\theta JA}$	84	

3. Min. pad size, 1 oz. Cu with backside plane covered with 1 oz. Cu (backside plane not electrically connected).
4. 2 cm<sup>2</sup> pad size, 1 oz. Cu with backside plane covered with 1 oz. Cu (backside plane not electrically connected).

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## ELECTRICAL CHARACTERISTICS ( $8 \leq V_D \leq 28$ V; $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ unless otherwise specified)

**Table 5. POWER**

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Operating Supply Voltage	$V_D$		4.5	–	28	V
Undervoltage Shutdown	$V_{UV}$			3.5	4.5	V
Undervoltage Shutdown Hysteresis	$V_{UV\_HYST}$			0.5		V
On Resistance	$R_{ON}$	$I_{OUT} = 1$ A, $T_J = 25^\circ\text{C}$			160	m $\Omega$
		$I_{OUT} = 1$ A, $T_J = 150^\circ\text{C}$			320	
		$I_{OUT} = 1$ A, $V_D = 5$ V, $T_J = 25^\circ\text{C}$			210	
Supply Current (Note 5)	$I_D$	OFF-state: $V_D = 13$ V, $V_{IN} = V_{OUT} = 0$ V, $T_J = 25^\circ\text{C}$		0.01	0.5	$\mu$ A
		ON-state: $V_D = 13$ V, $V_{IN} = 5$ V, $I_{OUT} = 0$ A		1.9	3.5	mA
Output Leakage Current	$I_{L(OFF)}$	$V_{IN} = V_{OUT} = 0$ V, $V_D = 13$ V, $T_J = 25^\circ\text{C}$			0.5	$\mu$ A
		$V_{IN} = V_{OUT} = 0$ V, $V_D = 13$ V, $T_J = 125^\circ\text{C}$			0.5	

5. Includes PowerMOS leakage current.

**Table 6. LOGIC INPUTS** ( $V_D = 13.5$  V;  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ )

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Voltage – Low	$V_{IN\_LOW}$				0.9	V
Input Current – Low	$I_{IN\_LOW}$	$V_{IN} = 0.9$ V	1			$\mu$ A
Input Voltage – High	$V_{IN\_HIGH}$		2.1			V
Input Current – High	$I_{IN\_HIGH}$	$V_{IN} = 2.2$ V			10	$\mu$ A
Input Hysteresis Voltage	$V_{IN\_HYST}$		0.2			V
Input Clamp Voltage	$V_{IN\_CL}$	$I_{IN} = 1$ mA	12	13	14	V
		$I_{IN} = -1$ mA	-14	-13	-12	
CS_DIS Voltage – Low	$V_{CS\_DIS\_LOW}$				0.9	V
CS_DIS Current – Low	$I_{CS\_DIS\_LOW}$	$V_{CS\_DIS} = 0.9$ V	1			$\mu$ A
CS_DIS Voltage – High	$V_{CS\_DIS\_HIGH}$		2.1			V
CS_DIS Current – High	$I_{CS\_DIS\_HIGH}$	$V_{CS\_DIS} = 2.2$ V			10	$\mu$ A
CS_DIS Hysteresis Voltage	$V_{CS\_DIS\_HYST}$		0.2			V
CS_DIS Clamp Voltage	$V_{CS\_DIS\_CL}$	$I_{CS\_DIS} = 1$ mA	12	13	14	V
		$I_{CS\_DIS} = -1$ mA	-14	-13	-12	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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**Table 7. SWITCHING CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$ )

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Turn-On Delay Time	$t_{d\_on}$	to 10% $V_{OUT}$ , $V_D = 13\text{ V}$ , $R_L = 13\ \Omega$		10		$\mu\text{s}$
Turn-Off Delay Time	$t_{d\_off}$	to 90% $V_{OUT}$ , $V_D = 13\text{ V}$ , $R_L = 13\ \Omega$		10		$\mu\text{s}$
Slew Rate On	$dV_{OUT}/dt_{on}$	10% to 80% $V_{OUT}$ , $V_D = 13\text{ V}$ , $R_L = 13\ \Omega$		0.7		$\text{V} / \mu\text{s}$
Slew Rate Off	$dV_{OUT}/dt_{off}$	90% to 10% $V_{OUT}$ , $V_D = 13\text{ V}$ , $R_L = 13\ \Omega$		0.7		$\text{V} / \mu\text{s}$
Turn-On Switching Loss (Note 6)	$E_{on}$	$V_D = 13\text{ V}$ , $R_L = 13\ \Omega$		0.04		mJ
Turn-Off Switching Loss (Note 6)	$E_{off}$	$V_D = 13\text{ V}$ , $R_L = 13\ \Omega$		0.04		mJ

6. Not subjected to production testing

**Table 8. OUTPUT DIODE CHARACTERISTICS**

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Forward Voltage	$V_F$	$I_{OUT} = -1\text{ A}$ , $T_J = 150^\circ\text{C}$ , $V_F = V_{OUT} - V_D$			0.7	V

**Table 9. PROTECTION FUNCTIONS** (Note 8)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Temperature Shutdown (Note 7)	$T_{SD}$		150	175	200	$^\circ\text{C}$
Temperature Shutdown Hysteresis ( $T_{SD} - T_R$ ) (Note 7)	$T_{SD\_HYST}$			7		$^\circ\text{C}$
Reset Temperature (Note 7)	$T_R$		$T_{R\_CS}+1$	$T_{R\_CS}+5$		$^\circ\text{C}$
Thermal Reset of CS_FAULT (Note 7)	$T_{R\_CS}$		135			$^\circ\text{C}$
DC Output Current Limit	$I_{LIM\_H}$	$V_D = 13\text{ V}$	6	12	18	A
		$5\text{ V} < V_D < 28\text{ V}$			18	A
Short Circuit Current Limit during Thermal Cycling (Note 7)	$I_{LIM\_L}$	$V_D = 13\text{ V}$ $T_R < T_J < T_{SD}$		6.5		A
Switch Off Output Clamp Voltage	$V_{OUT\_CLAMP}$	$I_{OUT} = 1\text{ A}$ , $V_{IN} = 0\text{ V}$ , $L = 20\text{ mH}$	$V_D - 41$	$V_D - 45$	$V_D - 52$	V
Overvoltage Protection	$V_{OV}$	$V_{IN} = 0\text{ V}$ , $I_D = 20\text{ mA}$	41	45	52	V
Output Voltage Drop Limitation	$V_{DS\_ON}$	$I_{OUT} = 0.025\text{ A}$ , $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$		25		mV

7. Not subjected to production testing.

8. To ensure long term reliability during overload or short circuit conditions, protection and related diagnostic signals must be used together with a fitting hardware & software strategy. If the device operates under abnormal conditions, this hardware & software solution must limit the duration and number of activation cycles.

**Table 10. OPEN-LOAD DETECTION** ( $8 \leq V_D \leq 18\text{ V}$ )

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Open-load Off-State Detection Threshold	$V_{OL}$	$V_{IN} = 0\text{ V}$	2	-	4	V
Open-load On-State Detection Threshold	$I_{OL}$	$V_{IN} = 5\text{ V}$ , $I_{CS} = 5\ \mu\text{A}$	0.5		5	mA
Open-load Detection Delay at Turn-Off	$t_{d\_OL\_off}$		100		800	$\mu\text{s}$
Off-State Output Current	$I_{OLOFF1}$	$V_{IN} = 0\text{ V}$ , $V_{OUT} = V_{OL}$	-3		3	$\mu\text{A}$
Output rising edge to CS rising edge during open-load	$t_{D\_OL}$	$V_{OUT} = 4\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{CS} = 90\%$ of $V_{CS\_HIGH}$			20	$\mu\text{s}$

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**Table 11. CURRENT SENSE CHARACTERISTICS** ( $8 \leq V_D \leq 18 \text{ V}$ )

Rating	Symbol	Conditions	Value			Unit
			min	typ	max	
Current Sense Ratio	$K_0$	$I_{OUT} = 0.025 \text{ A}$ , $V_{CS} = 0.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	260	490	760	$I_{OUT} / I_{CS}$
Current Sense Ratio	$K_1$	$I_{OUT} = 0.35 \text{ A}$ , $V_{CS} = 0.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	310	465	620	
		$I_{OUT} = 0.35 \text{ A}$ , $V_{CS} = 0.5 \text{ V}$ , $T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	360	465	545	
Current Sense Ratio Drift (Note 9)	$\Delta K_1 / K_1$	$I_{OUT} = 0.35 \text{ A}$ , $V_{CS} = 0.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	-11		11	%
Current Sense Ratio	$K_2$	$I_{OUT} = 0.5 \text{ A}$ , $V_{CS} = 4 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	350	455	570	
		$I_{OUT} = 0.5 \text{ A}$ , $V_{CS} = 4 \text{ V}$ , $T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	380	455	530	
Current Sense Ratio Drift (Note 9)	$\Delta K_2 / K_2$	$I_{OUT} = 0.5 \text{ A}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	-8		8	%
Current Sense Ratio	$K_3$	$I_{OUT} = 1.5 \text{ A}$ , $V_{CS} = 4 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	405	455	505	
		$I_{OUT} = 1.5 \text{ A}$ , $V_{CS} = 4 \text{ V}$ , $T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	415	455	495	
Current Sense Ratio Drift (Note 9)	$\Delta K_3 / K_3$	$I_{OUT} = 1.5 \text{ A}$ , $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	-4		4	%
Current Sense Leakage Current	$CS_{I_{lk}}$	$I_{OUT} = 0 \text{ A}$ , $V_{CS} = 0 \text{ V}$ $V_{CS\_DIS} = 5 \text{ V}$ , $V_{IN} = 0 \text{ V}$ $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$			1	$\mu\text{A}$
		$I_{OUT} = 0 \text{ A}$ , $V_{CS} = 0 \text{ V}$ $V_{CS\_DIS} = 0 \text{ V}$ , $V_{IN} = 5 \text{ V}$ $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$			2	
		$I_{OUT} = 1 \text{ A}$ , $V_{CS} = 0 \text{ V}$ $V_{CS\_DIS} = 5 \text{ V}$ , $V_{IN} = 5 \text{ V}$ $T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$			1	
CS Max Voltage	$CS_{Max}$	$R_{CS} = 10 \text{ k}\Omega$ , $I_{OUT} = 1 \text{ A}$	5			V
Current Sense Voltage in Fault Condition (Note 10)	$V_{CS\_FAULT}$	$V_D = 13 \text{ V}$ , $R_{CS} = 3.9 \text{ k}\Omega$		8		V
Current Sense Current in Fault Condition (Note 10)	$I_{CS\_FAULT}$	$V_D = 13 \text{ V}$ , $V_{CS} = 5 \text{ V}$		10		mA
CS_DIS Low to CS High Delay Time	$t_{CS\_HIGH1}$	$V_{CS} < 4 \text{ V}$ , $0.025 \text{ A} < I_{OUT} < 1.5 \text{ A}$ $I_{CS} = 90\%$ of $I_{CS} \text{ Max}$		40	100	$\mu\text{s}$
CS_DIS High to CS Low Delay Time	$t_{CS\_LOW1}$	$V_{CS} < 4 \text{ V}$ , $0.025 \text{ A} < I_{OUT} < 1.5 \text{ A}$ $I_{CS} = 10\%$ of $I_{CS} \text{ Max}$		5	20	$\mu\text{s}$
$V_{IN}$ High to CS High Delay Time	$t_{CS\_HIGH2}$	$V_{CS} < 4 \text{ V}$ , $0.025 \text{ A} < I_{OUT} < 1.5 \text{ A}$ $I_{CS} = 90\%$ of $I_{CS} \text{ Max}$		30	160	$\mu\text{s}$
$V_{IN}$ Low to CS Low Delay Time	$t_{CS\_LOW2}$	$V_{CS} < 4 \text{ V}$ , $0.025 \text{ A} < I_{OUT} < 1.5 \text{ A}$ $I_{CS} = 10\%$ of $I_{CS} \text{ Max}$		80	250	$\mu\text{s}$
Delay Time $I_D$ Rising Edge to Rising Edge of CS	$\Delta t_{CS\_HIGH2}$	$V_{CS} < 4 \text{ V}$ , $I_{CS} = 90\%$ of $I_{CS} \text{ Max}$ , $I_{OUT} = 90\%$ of $I_{OUTmax}$ , $I_{OUTmax} = 1.5 \text{ A}$			110	$\mu\text{s}$

9. Not subjected to production testing.

10. The following fault conditions are: Overtemperature, Power Limitation, and OFF State Open-Load Detection.

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**Table 12. TRUTH TABLE**

Conditions	Input	Output	CS ( $V_{CS\_DIS} = 0\text{ V}$ ) (Note 11)
Normal Operation	L H	L H	0 $I_{CS} = I_{OUT}/K_{NOMINAL}$
Over-temperature	L H	L L	0 $V_{CS\_FAULT}$
Under-voltage	L H	L L	0 0
Overload	H H	H (no active current mgmt) Cycling (active current mgmt)	$I_{CS} = I_{OUT}/K_{NOMINAL}$ $V_{CS\_FAULT}$
Short circuit to Ground	L H	L L	0 $V_{CS\_FAULT}$
OFF State Open-Load	L	H	$V_{CS\_FAULT}$

11. If the  $V_{CS\_DIS}$  is high, the Current Sense output is at a high impedance, its potential depends on leakage currents and external circuitry.



ELECTRICAL CHARACTERISTICS WAVEFORMS AND GRAPHS

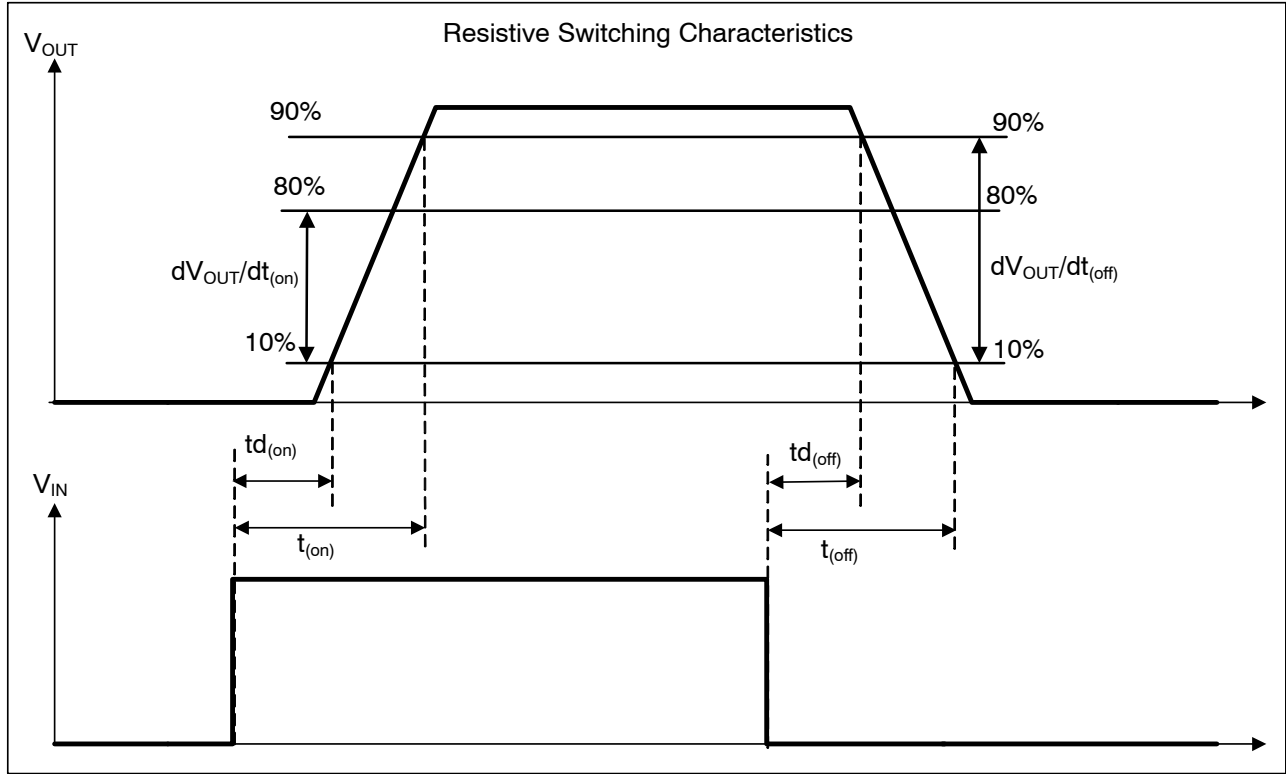


Figure 4. Switching Characteristics

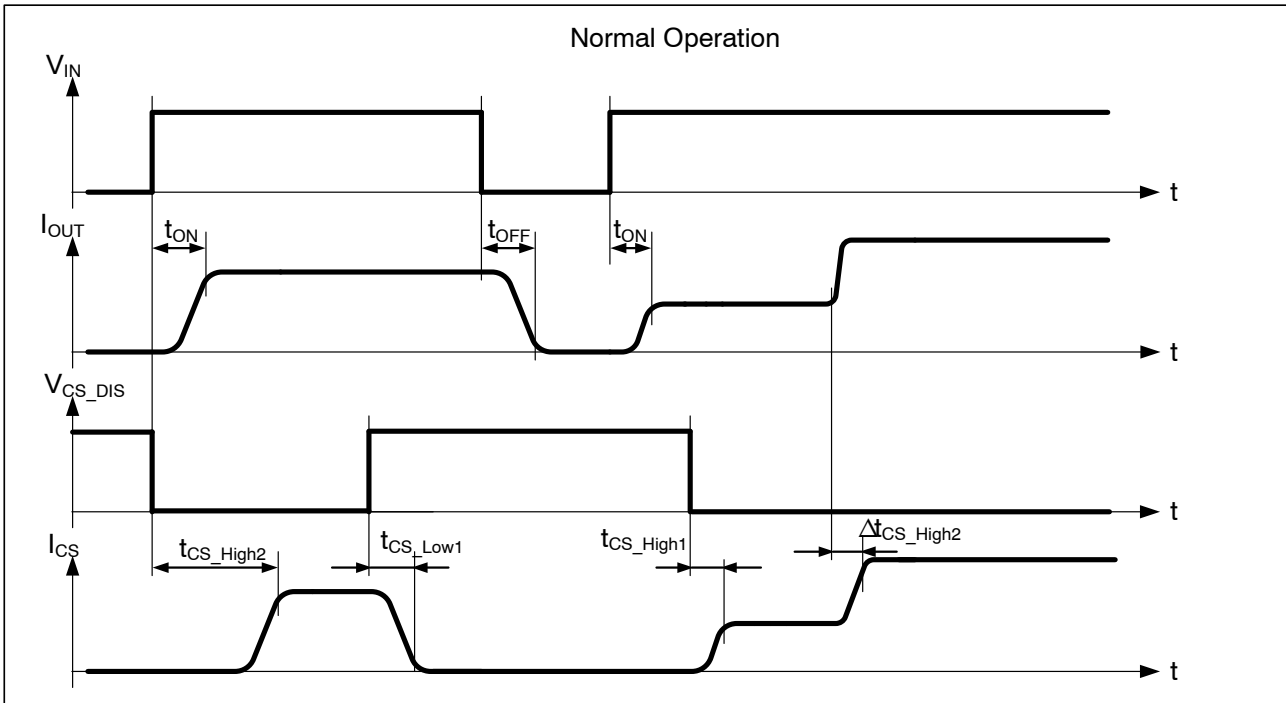


Figure 5. Normal Operation with Current Sense Timing Characteristics

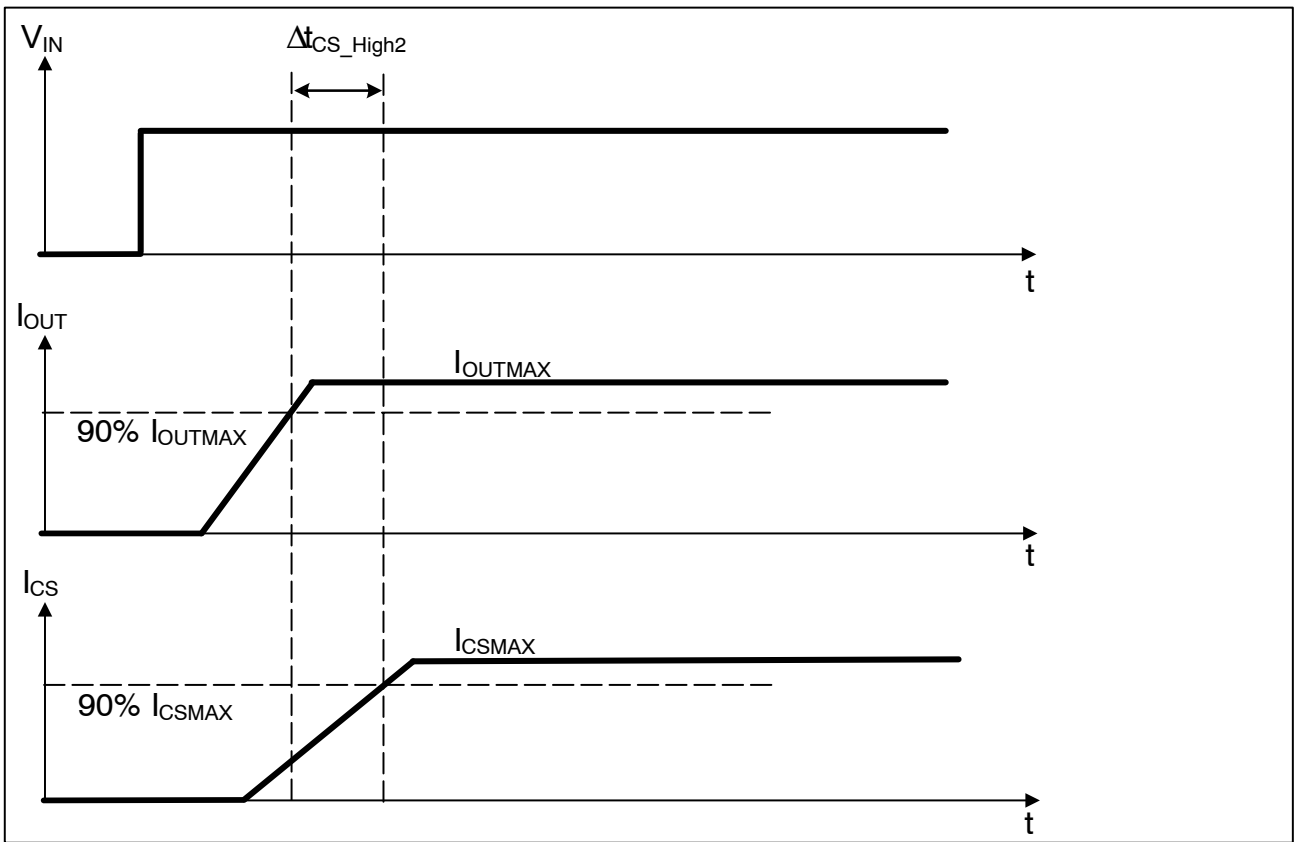


Figure 6. Delay Response from Rising Edge of  $I_{OUT}$  and Rising Edge of CS (for  $CS\_EN = 5V$ )

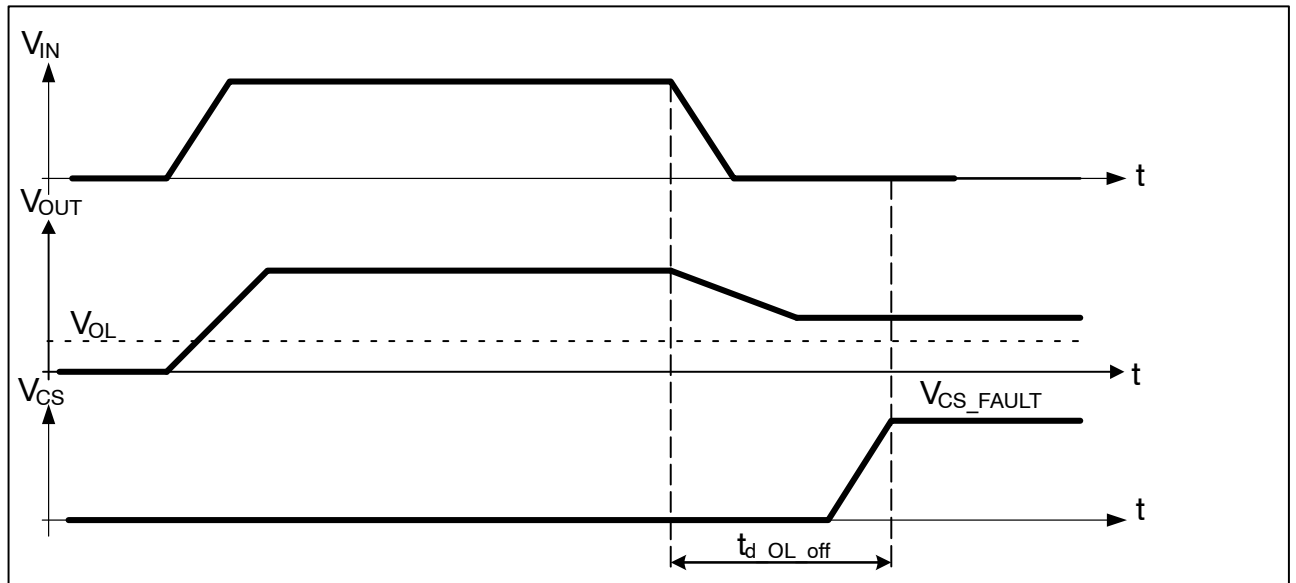


Figure 7. OFF-State Open-Load Flag Delay Timing

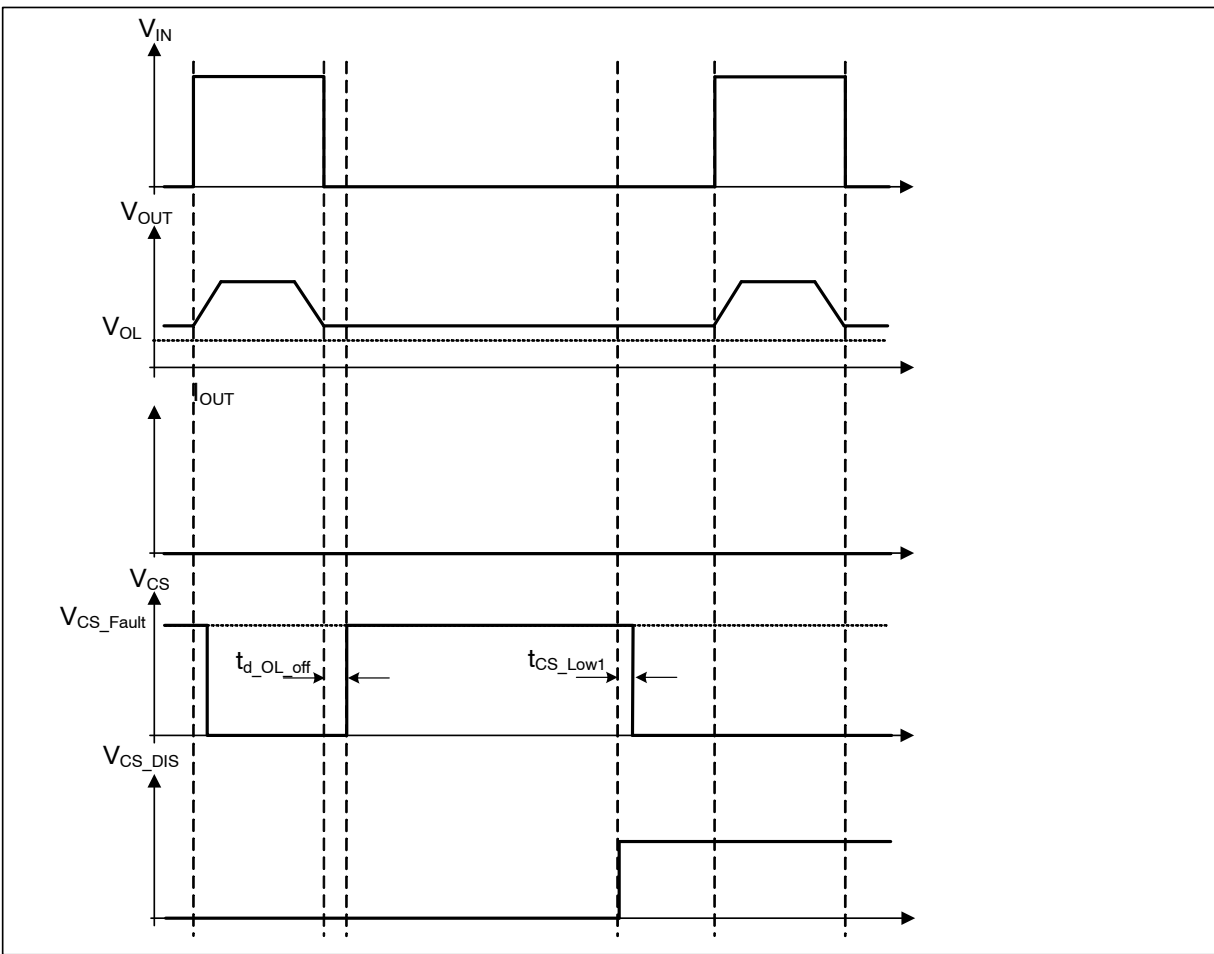


Figure 8. Off-State Open-Load with added external components

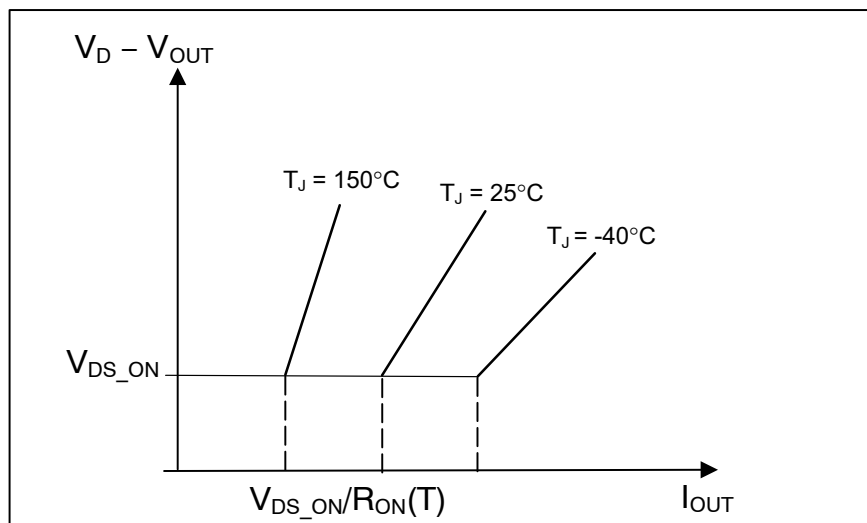


Figure 9. Voltage Drop Limitation for  $V_{DS\_ON}$

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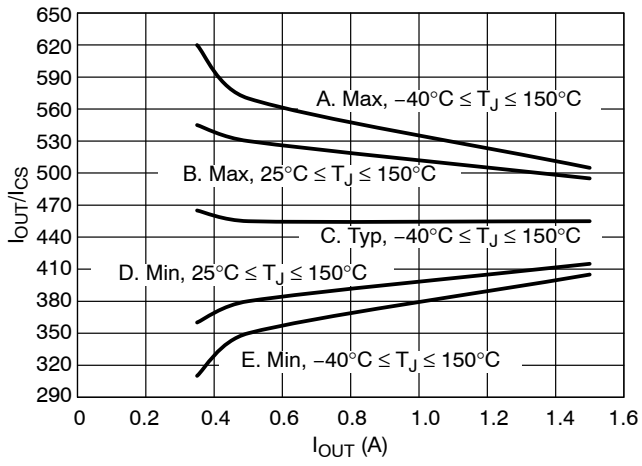


Figure 10.  $I_{OUT}/I_{Sense}$  vs  $I_{OUT}$

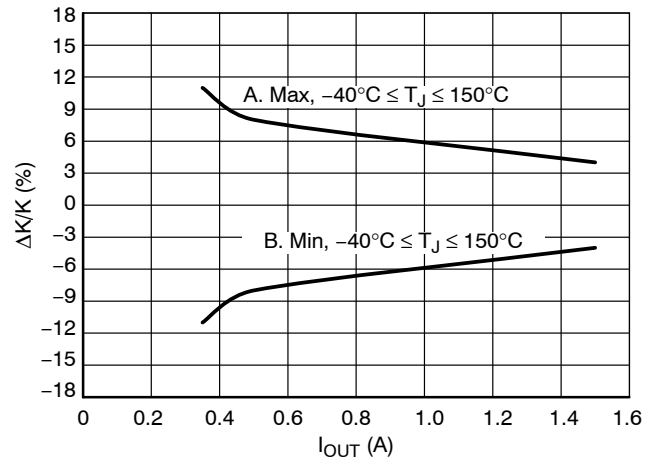


Figure 11. Maximum Current Sense Ratio Drift vs Load Current

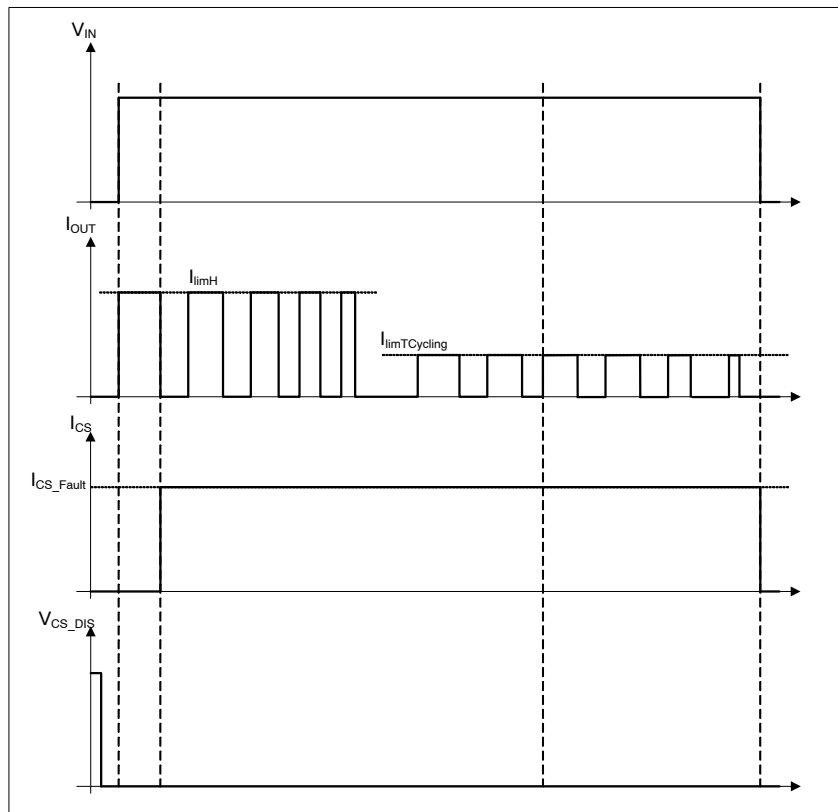


Figure 12. Short to GND or Overload

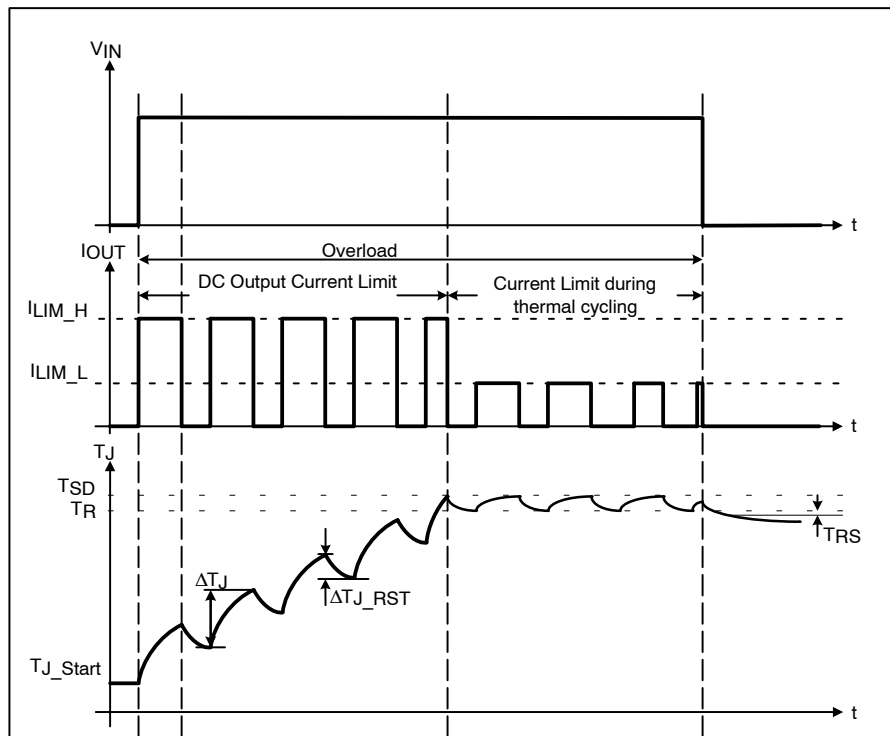


Figure 13. How  $T_J$  Progresses During Short to GND or Overload

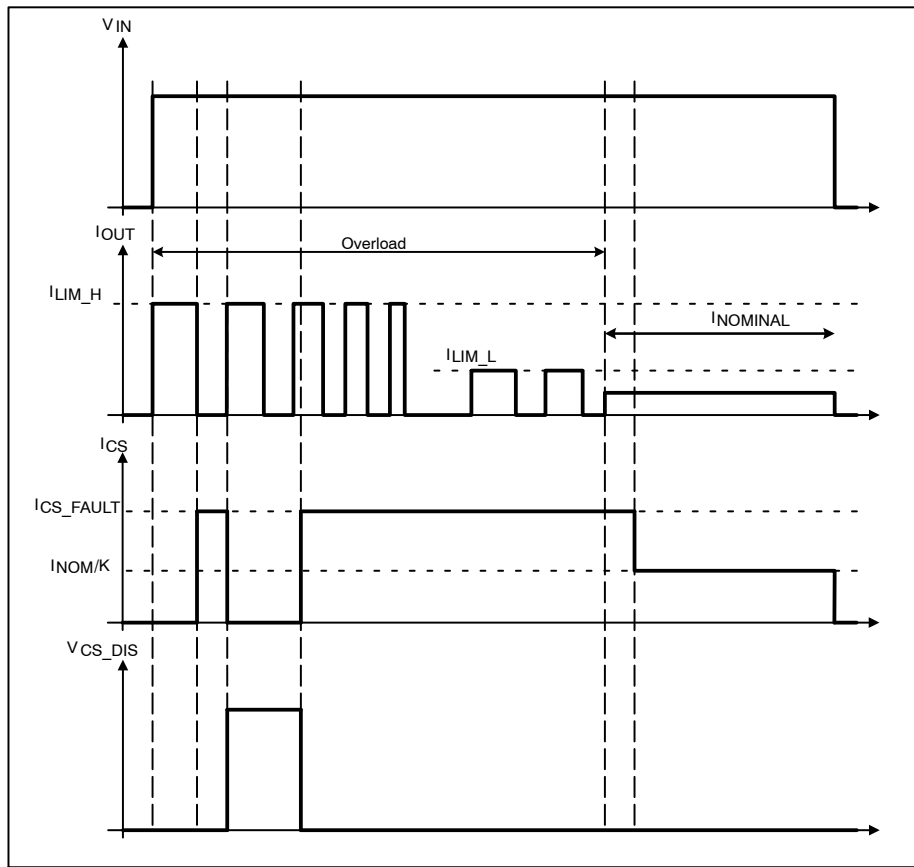


Figure 14. Discontinuous Overload or Short to GND

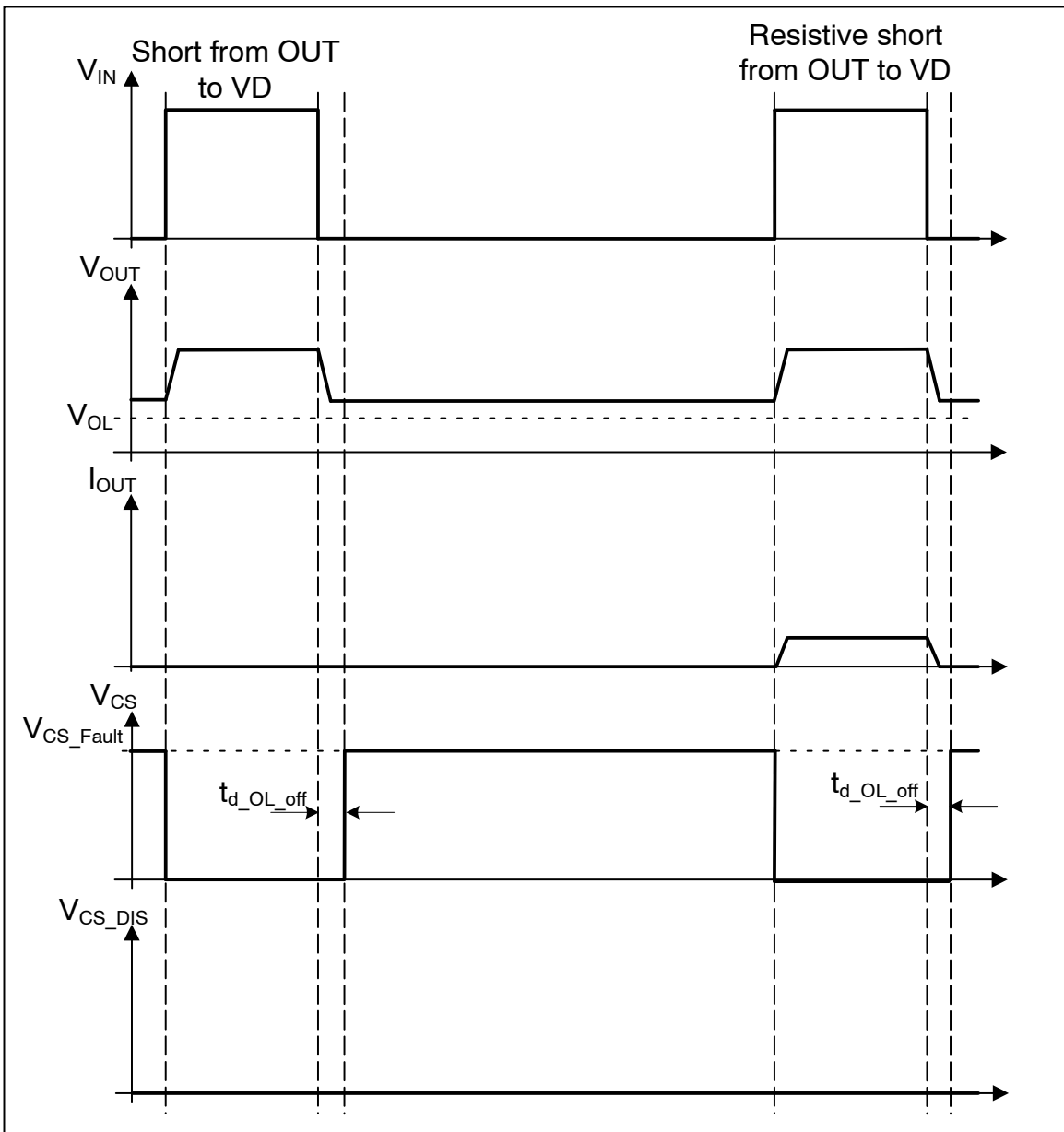


Figure 15. Short Circuit from OUT to VD

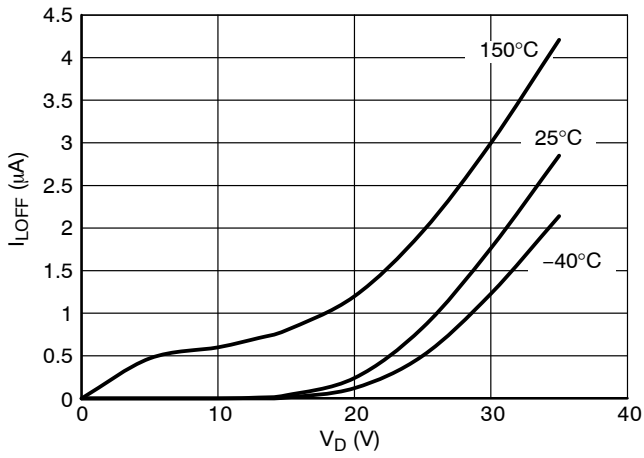


Figure 16. Output Leakage Current vs. VD Voltage & Temperature, VOUT = 0 V

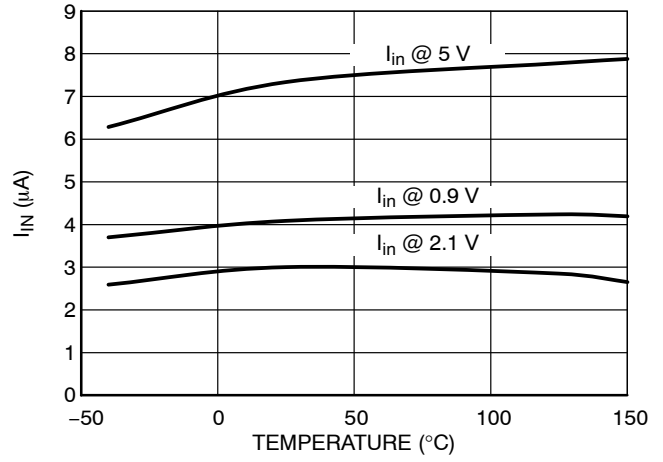


Figure 17. Input Current vs. Temperature

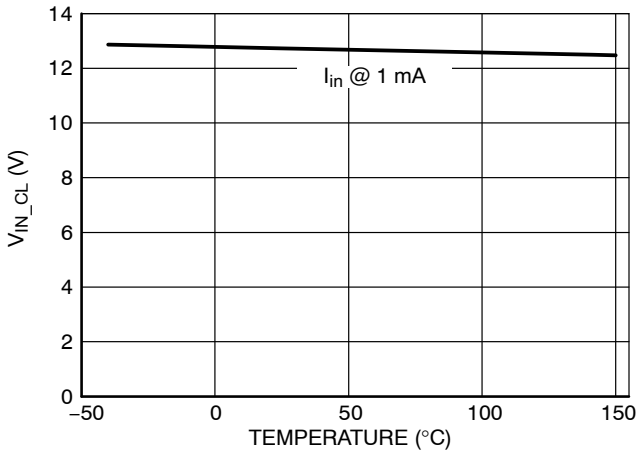


Figure 18. Input Clamp Voltage (Positive) vs. Temperature

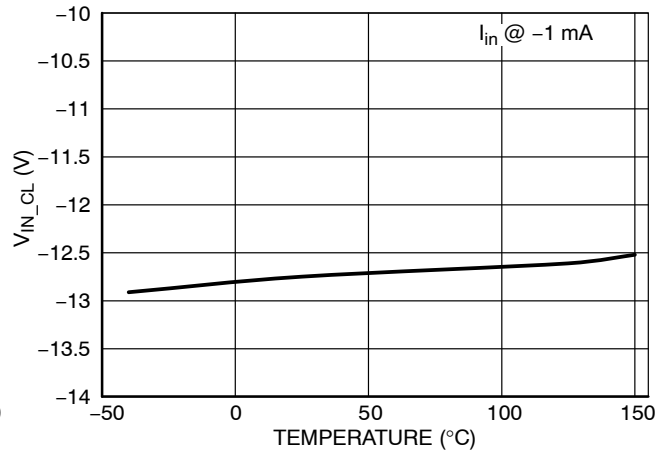


Figure 19. Input Clamp Voltage (Negative) vs. Temperature

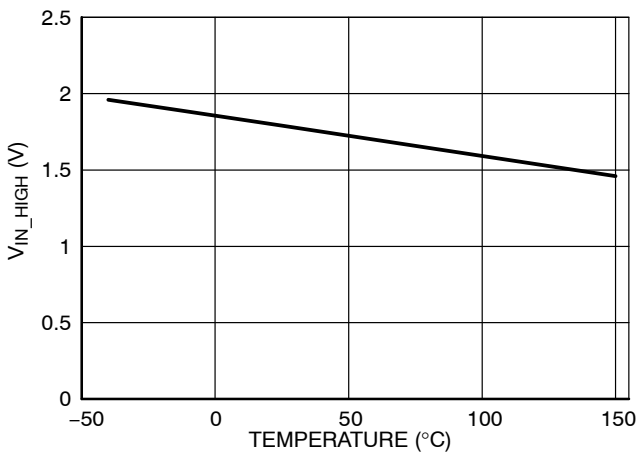


Figure 20. V<sub>IN</sub> Threshold High vs. Temperature

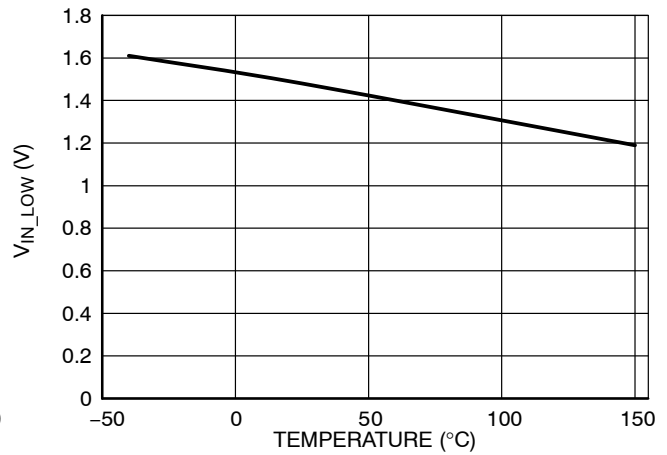


Figure 21. V<sub>IN</sub> Threshold Low vs. Temperature



# NCV84160

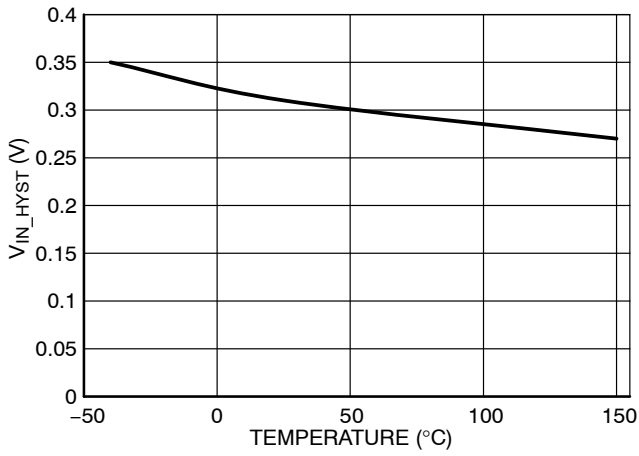


Figure 22. Hysteresis Input Voltage vs. Temperature

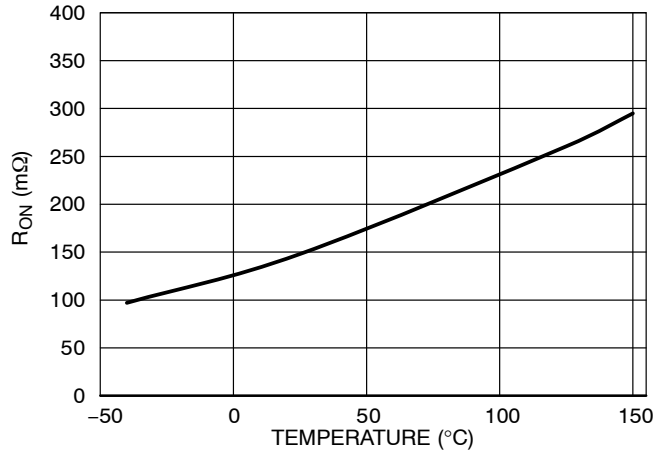


Figure 23. R<sub>ON</sub> vs. Temperature

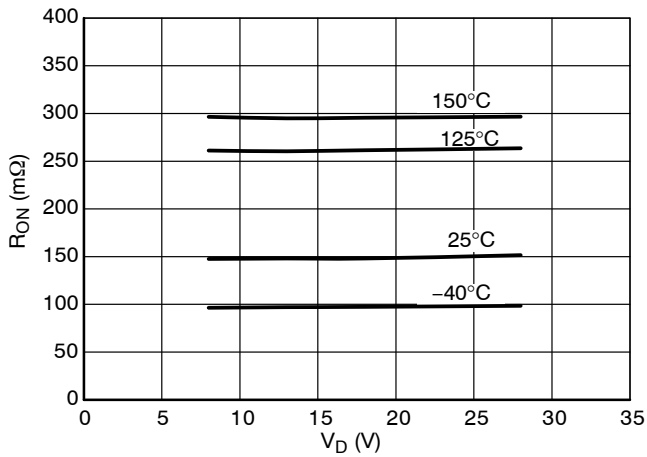


Figure 24. R<sub>ON</sub> vs. Temperature & V<sub>D</sub> Voltage

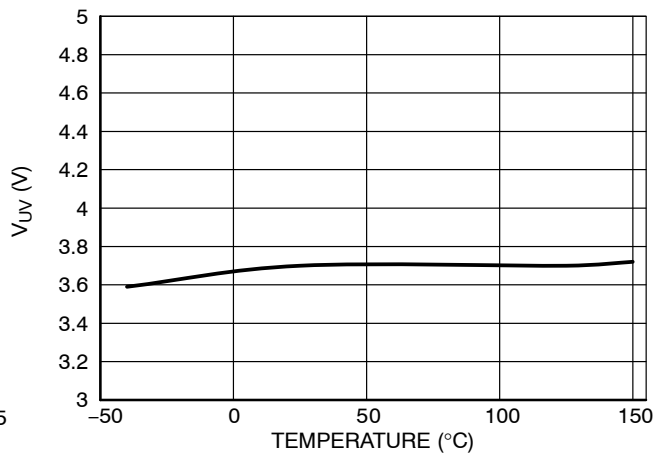


Figure 25. Undervoltage Shutdown vs. Temperature

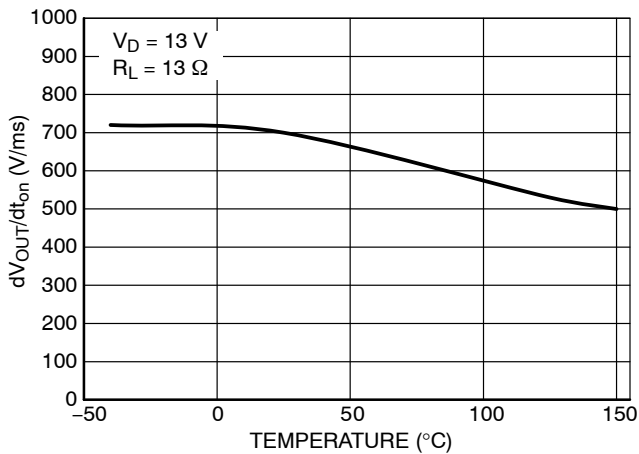


Figure 26. Slew Rate On vs. Temperature

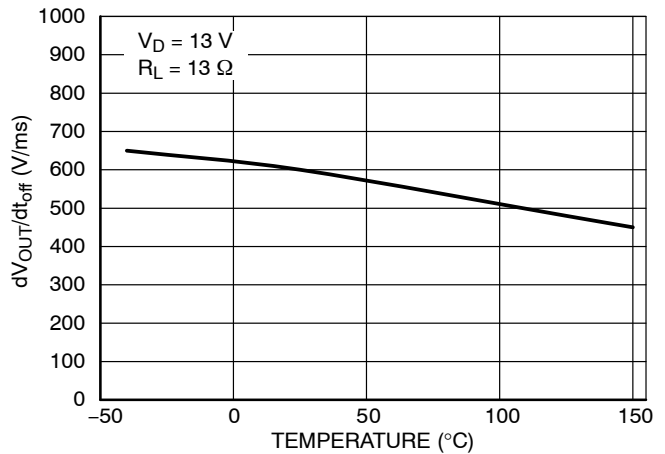


Figure 27. Slew Rate Off vs. Temperature

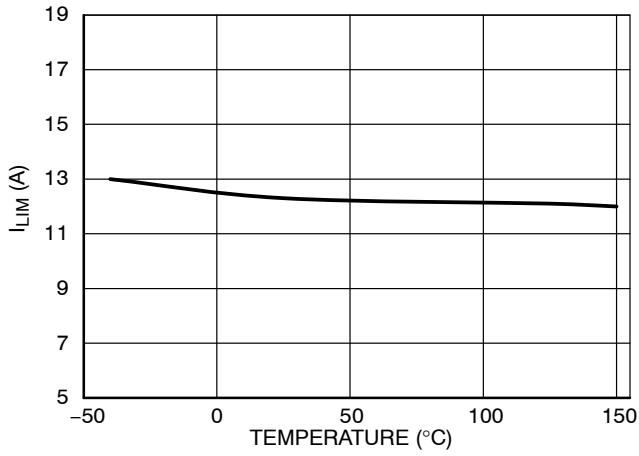


Figure 28. Current Limit vs. Temperature,  $V_D = 13.5\text{ V}$

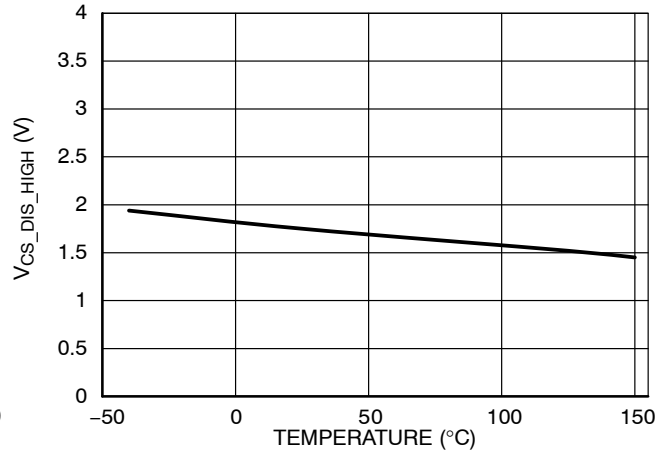


Figure 29. CS\_DIS Threshold High vs. Temperature

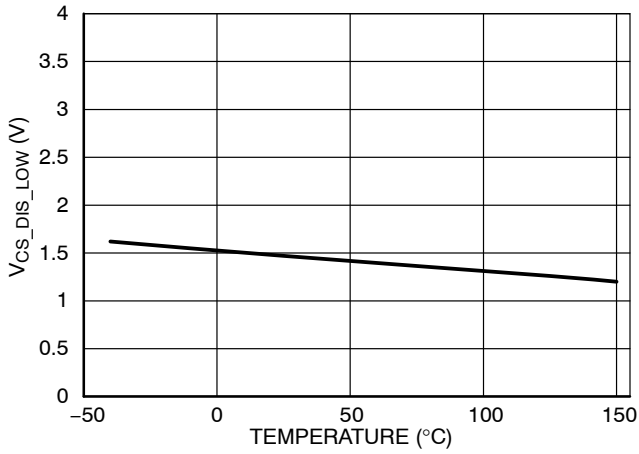


Figure 30. CS\_DIS Threshold Low vs. Temperature

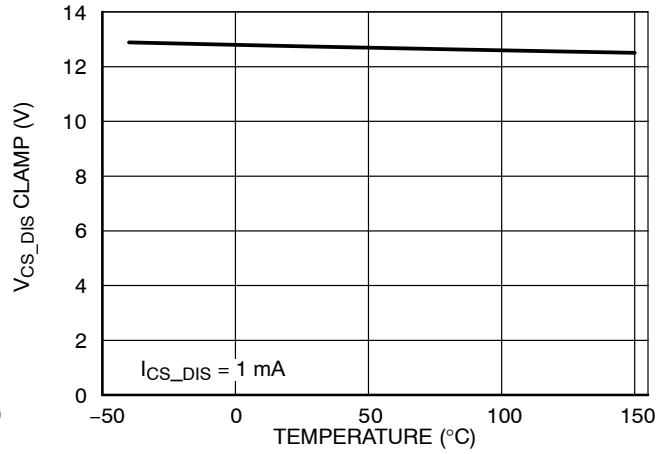


Figure 31. CS\_DIS Clamp Voltage (Positive) vs. Temperature

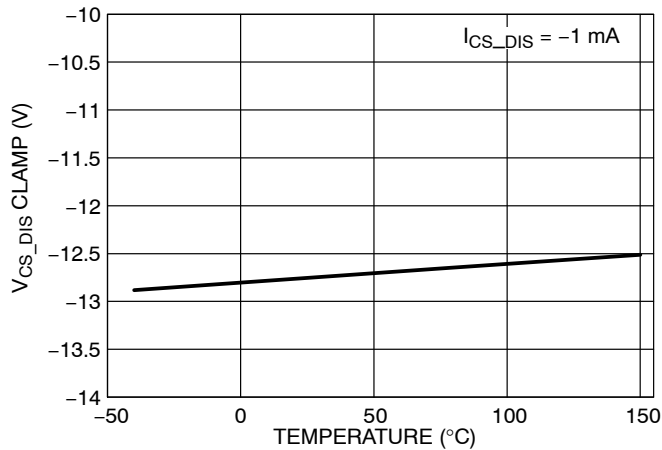


Figure 32. CS\_DIS Clamp Voltage (Negative) vs. Temperature

# NCV84160

## ISO 7637-2: 2011(E) PULSE TEST RESULTS

ISO 7637-2:2011 Test Pulse	Test Severity Levels		Delays and Impedance	# of Pulses or Test Time	Pulse / Burst rep. time
	III	IV			
1	-112	-150	2 ms, 10 $\Omega$	500 pulses	0.5 s
2a	55	112	0.05 ms, 2 $\Omega$	500 pulses	0.5 s
3a	-165	-220	0.1 $\mu$ s, 50 $\Omega$	1 h	100 ms
3b	112	150	0.1 $\mu$ s, 50 $\Omega$	1 h	100 ms
ISO 7637-2:2011 Test Pulse	Test Results				
	III	IV			
1		A			
2a	A	E			
3a		A			
3b		A			
Class	Functional Status				
A	All functions of a device perform as designed during and after exposure to disturbance.				
B	All functions of a device perform as designed during exposure. However, one or more of them can go beyond specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A.				
C	One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed.				
D	One or more functions of a device do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device is reset by simple "operator/use" action.				
E	One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.				

Application Information

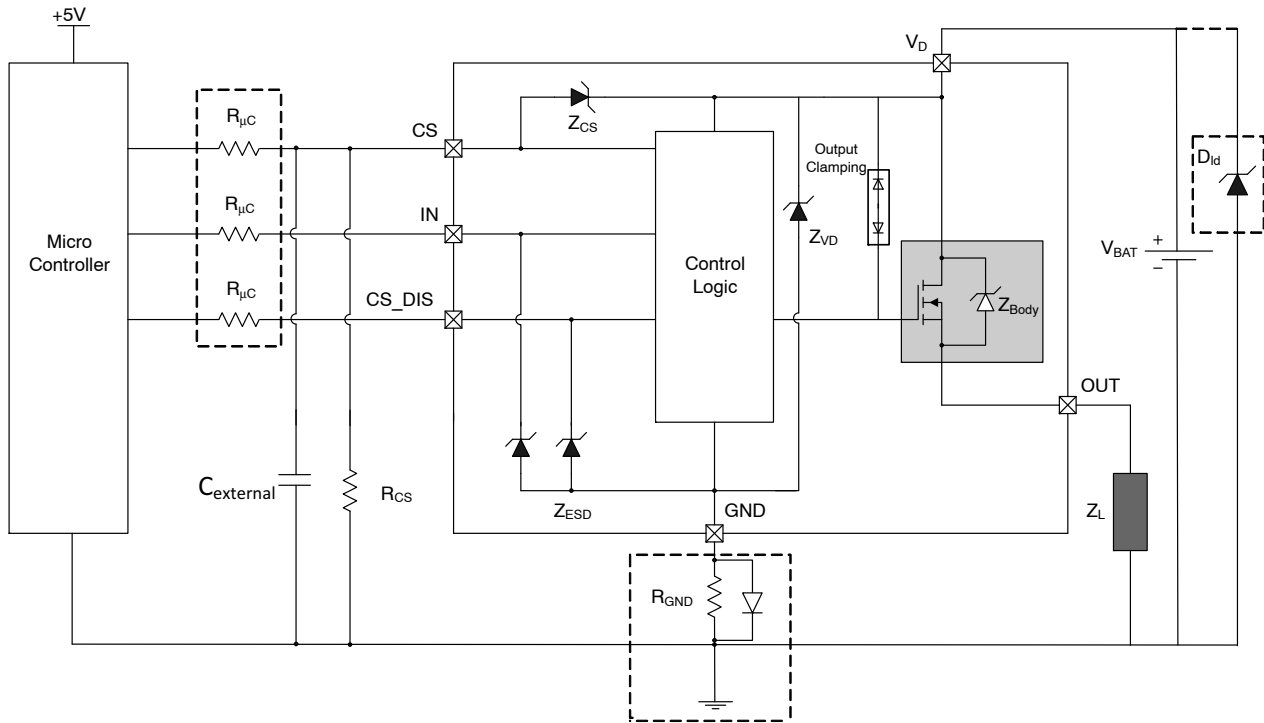


Figure 33. Application Schematic

**Loss of Ground Protection**

When device or ECU ground connection is lost and load is still connected to ground, the device will turn the output OFF. In loss of ground state, the output stage is held OFF independent of the state of the input. Input resistors are recommended between the device and microcontroller.

**Reverse Battery Protection**

Solution 1: Resistor in the GND line only (no parallel Diode)

The following calculations are true for any type of load.

In the case for no diode in parallel with R<sub>GND</sub>, the calculations below explain how to size the resistor.

Consider the following parameters: -I<sub>GND</sub> Maximum = 200 mA for up to -V<sub>D</sub> = 32 V.

Where -I<sub>GND</sub> is the DC reverse current through the GND pin and -V<sub>D</sub> is the DC reverse battery voltage.

$$-I_{GND} = \frac{-V_D}{R_{GND}} \quad (\text{eq. 1})$$

Since this resistor can be used amongst multiple High-Side devices, please take note the sum of the maximum active GND currents (I<sub>GND(On)max</sub>) for each device when sizing the resistor. Please note that if the microprocessor GND is not shared by the device GND, then R<sub>GND</sub> produces a shift of (I<sub>GND(On)max</sub> \* R<sub>GND</sub>) in the input thresholds and CS output values. If the calculated power dissipation leads to too large of a resistor size or several devices have to share the same resistor, please look at the second solution for Reverse Battery Protection. Refer to the figure below for selecting the proper R<sub>GND</sub>.

NCV84160 Reverse Battery Considerations  
 Normal Operation VIN = 5 V, Reverse Battery = 32 V

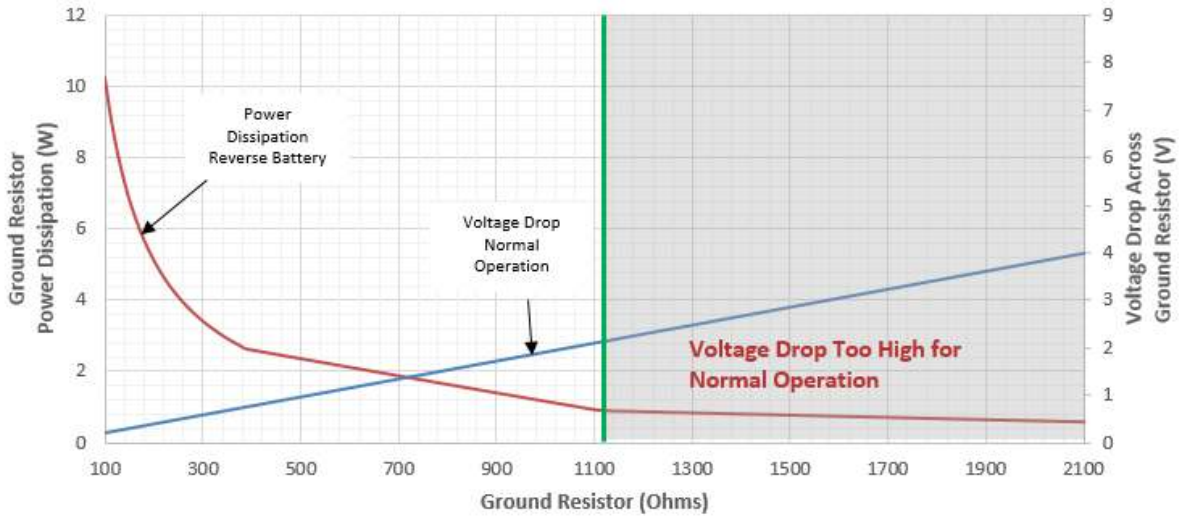


Figure 34. Reverse Battery R<sub>GND</sub> Considerations

Solution 2: Diode (D<sub>GND</sub>) in parallel with R<sub>GND</sub> in the ground line.

A resistor value of R<sub>GND</sub> = 1 kOhm should be selected and placed in parallel to D<sub>GND</sub> if the device drives an inductive load. The diode (D<sub>GND</sub>) provides a ~600–700 mV shift in the input threshold and current sense values if the micro controller ground is not common to the device ground. This shift will not vary even in the case of multiple high-side devices using the same resistor/diode network.

**Undervoltage Protection**

The device has two under-voltage threshold levels, V<sub>D\_MIN</sub> and V<sub>UV</sub>. Switching function (ON/OFF) requires supply voltage to be at least V<sub>D\_MIN</sub>. The device features a lower supply threshold V<sub>UV</sub>, above which the output can remain in ON state. While all protection functions are guaranteed when the switch is ON, diagnostic functions are operational only within nominal supply voltage range V<sub>D</sub>.

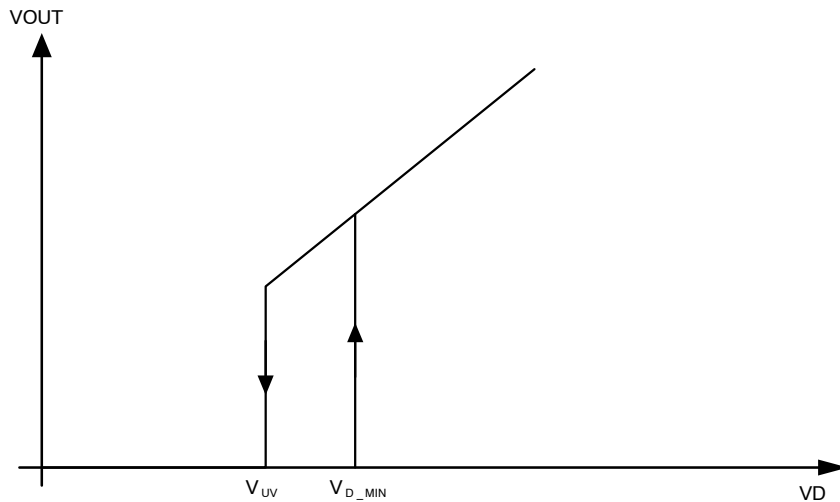


Figure 35. Undervoltage Behavior

**Overvoltage Protection**

The NCV84160 has two Zener diodes  $ZV_D$  and  $ZCS$ , which provide integrated overvoltage protection.  $ZV_D$  protects the logic block by clamping the voltage between supply pin  $V_D$  and ground pin  $GND$  to  $VZV_D$ .  $ZCS$  limits voltage at current sense pin  $CS$  to  $V_D - VZCS$ . The output power MOSFET's output clamping diodes provide protection by clamping the voltage across the MOSFET (between  $V_D$  pin and  $OUT$  pin) to  $V_{CLAMP}$ . During overvoltage protection, current flowing through  $ZV_D$ ,  $ZCS$  and the output clamp must be limited. Load impedance  $Z_L$  limits the current in the body diode  $Z_{Body}$ . In order to limit the current in  $ZV_D$  a resistor,  $R_{GND}$  ( $150\ \Omega$ ), is required in the  $GND$  path. External resistors  $R_{CS}$  and  $R_{SENSE}$  limit the current flowing through  $ZCS$  and out of the  $CS$  pin into the micro-controller I/O pin. With  $R_{GND}$ , the  $GND$  pin voltage is elevated to  $V_D - VZV_D$  when the supply voltage  $V_D$  rises above  $VZV_D$ . ESD diodes  $ZESD$  pull up the voltage at logic pins  $IN$ ,  $CS\_Dis$  close to the  $GND$  pin voltage  $V_D - VZV_D$ . External resistors  $R_{IN}$ , and  $R_{CS\_DIS}$  are required to limit the current flowing out of the logic pins into the micro-controller I/O pins. During overvoltage exposure, the device transitions into a self-protection state, with automatic recovery after the supply voltage comes back to the normal operating range. The specified parameters as well as short circuit robustness and energy capability cannot be guaranteed during overvoltage exposure.

**Overload Protection**

Current limitation as well as over-temperature shutdown mechanisms are integrated into the NCV84160 to provide protection from overload conditions such as bulb inrush or short to ground.

**Current Limitation**

In case of overload, the NCV84160 limits the current in the output power MOSFET to a safe value. Due to high power dissipation during current limitation, the device's junction temperature increases rapidly. In order to protect the device, the output driver is shut down by one of the two over-temperature protection mechanisms. The output current limitation level is dependent on the drain-to-source voltage of the power MOSFET. If the input remains active during the shutdown, the output power MOSFET will automatically be re-activated after a minimum OFF time or when the junction temperature returns to a safe level.

**Output Clamping with Inductive Load Switch Off:**

The output voltage  $V_{OUT}$  drops below  $GND$  potential when switching off inductive loads. This is because the inductance develops a negative voltage across the load in response to a decaying current. The integrated clamp of the device clamps the negative output voltage to a certain level relative to the supply voltage  $V_{BAT}$ . During output clamping with inductive load switch off, the energy stored in the inductance is rapidly dissipated in the device resulting in high power dissipation. This is a stressful condition for the device and the maximum energy allowed for a given load inductance should not be exceeded in any application.

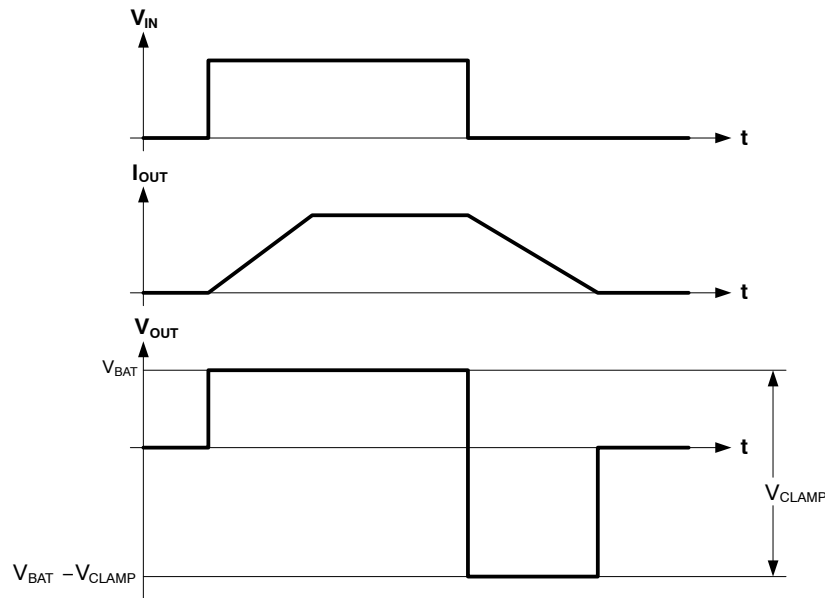


Figure 36. Inductive Load Switching

# NCV84160

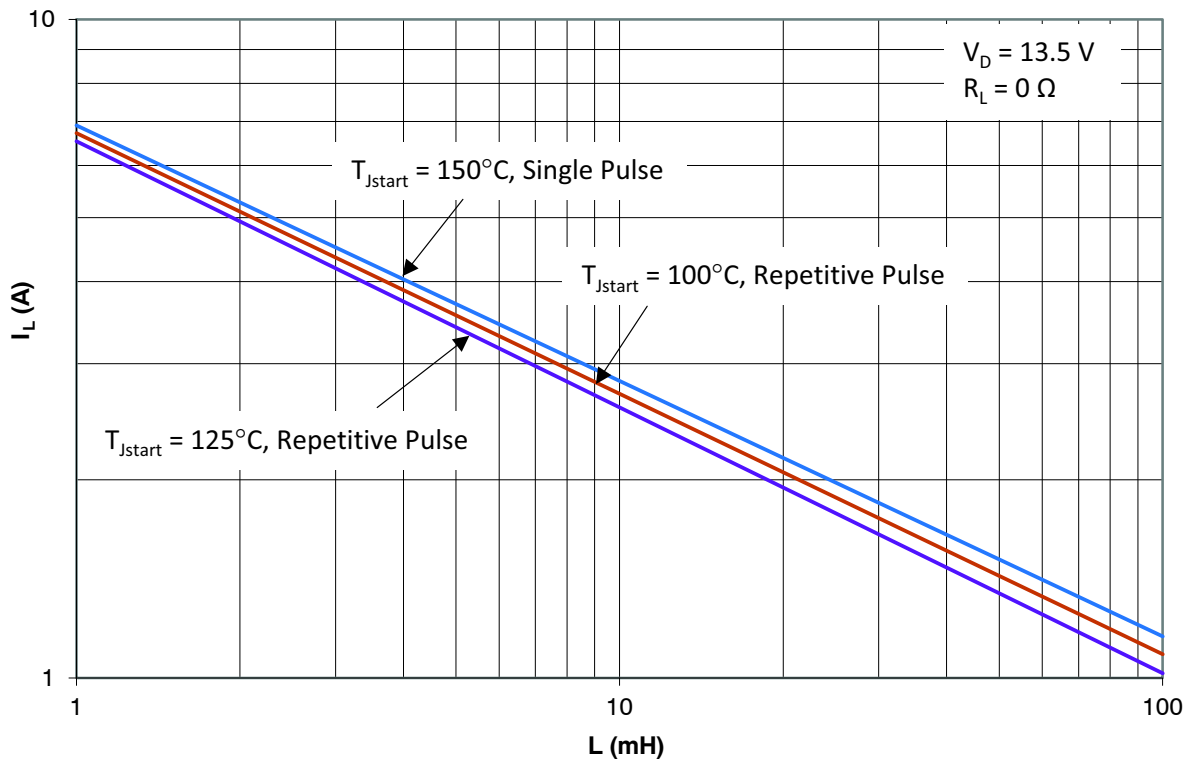
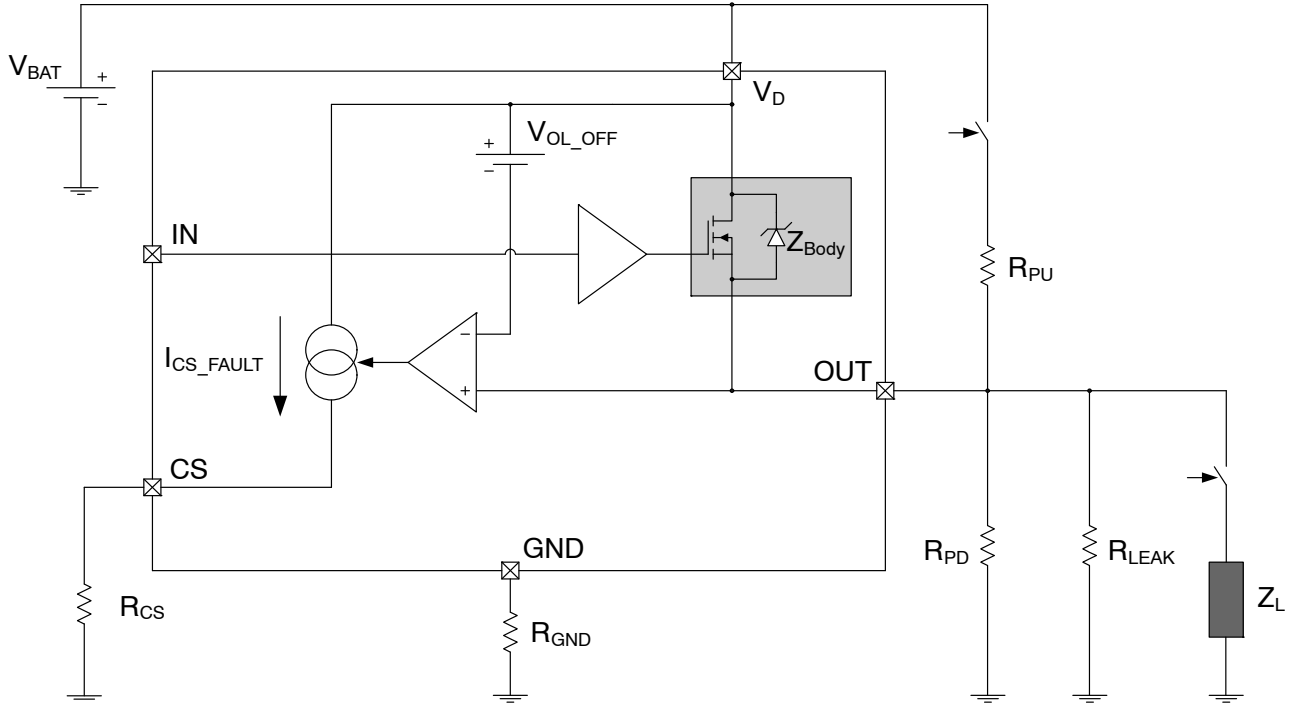


Figure 37. Maximum Switch-Off Current vs. Load Inductance,  $V_D = 13.5 \text{ V}$ ;  $R_L = 0 \Omega$

**Open Load Detection in OFF State**

Open load diagnosis in the OFF-state can be performed by activating an external resistive pull-up path (RPU) to VBAT. To calculate the pull-up resistance, external leakage

currents (designed pull-down resistance, humidity-induced leakage etc) as well as the open load threshold voltage VOL have to be taken into account.



**Figure 38. Off State Open Load Detection Circuit**

**Current Sense in PWM Mode**

While operating in PWM mode, the current sense functionality can be used, but the timing of the input signal and the response time of the current sense need to be considered. When operating in PWM mode, the following performance is to be expected. The CS\_DIS pin should be left low to eliminate any unnecessary delay time to the circuit. When VIN switches from low to high, there will be

a typical delay (tCS\_High2) before the current sense responds. Once this timing delay has passed, the rise time of the current sense output ( $\Delta t_{CS\_High2}$ ) also needs to be considered. When VIN switches from high to low a delay time (tCS\_Low1) needs to be considered. As long as these timing delays are allowed, the current sense pin can be operated in PWM mode.



# NCV84160

## PACKAGE AND PCB THERMAL DATA (Note 1)

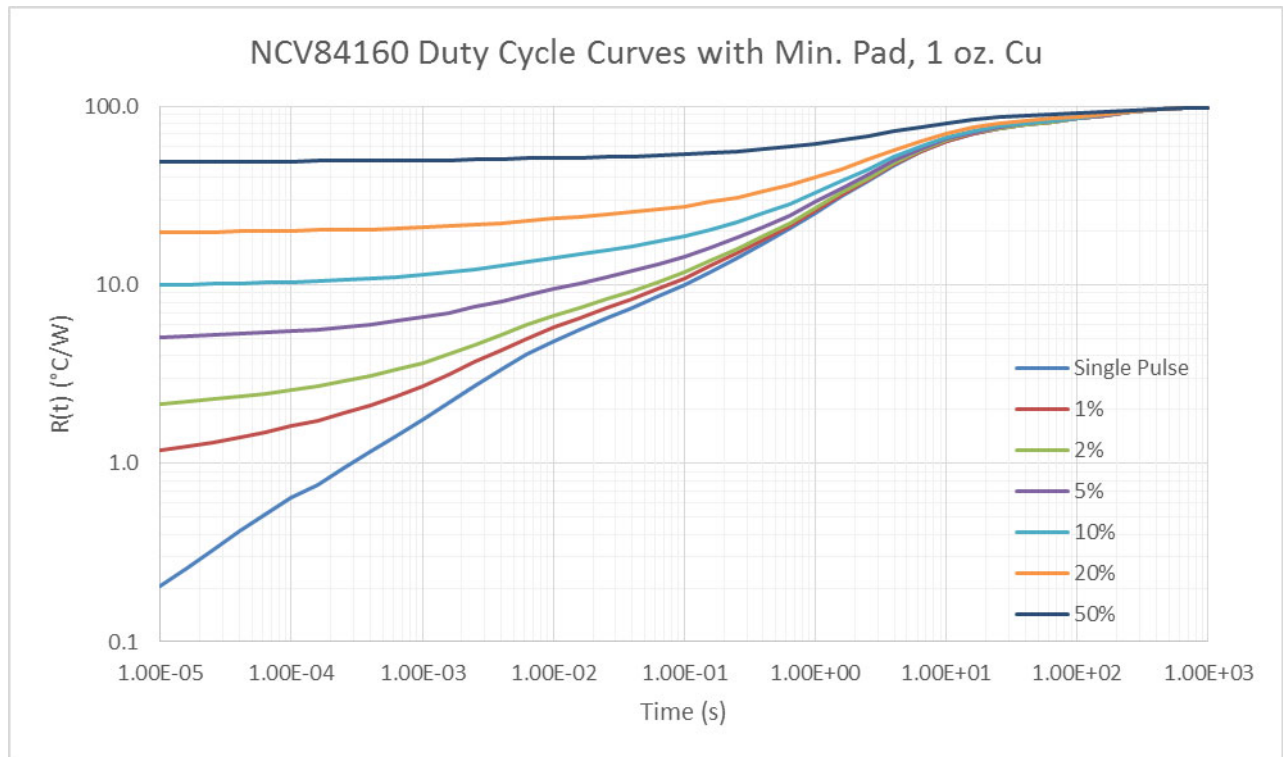


Figure 39. Junction to Ambient Transient Thermal Impedance (Min. Pad Cu Area)

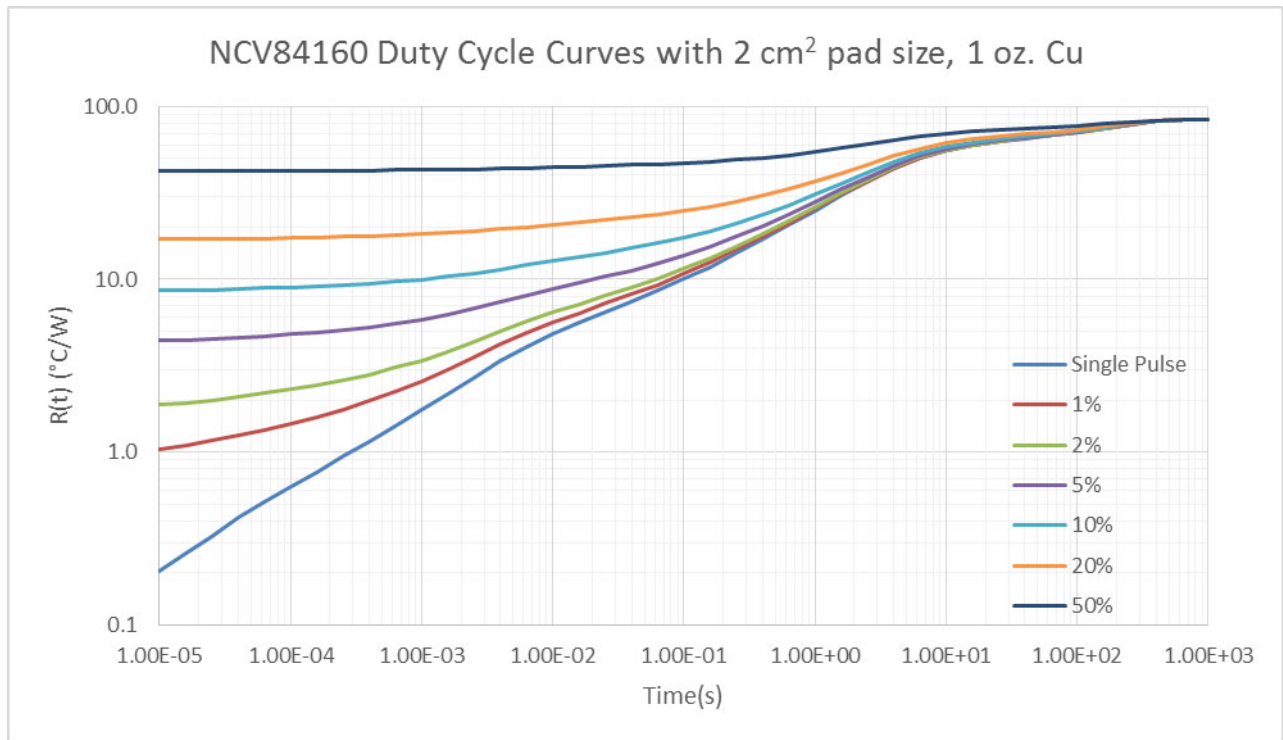
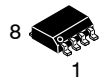


Figure 40. Junction to Ambient Transient Thermal Impedance (2 cm<sup>2</sup> Cu Area)

1. PCB FR4 Area = 4.8 cm x 4.8 cm, PCB Thickness = 1.6 mm, backside plane covered with 1 oz. Cu (backside plane not electrically connected)

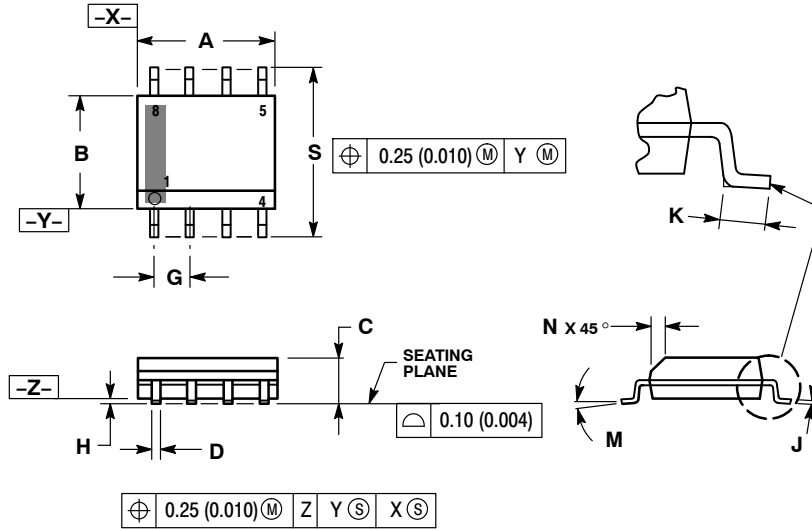
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

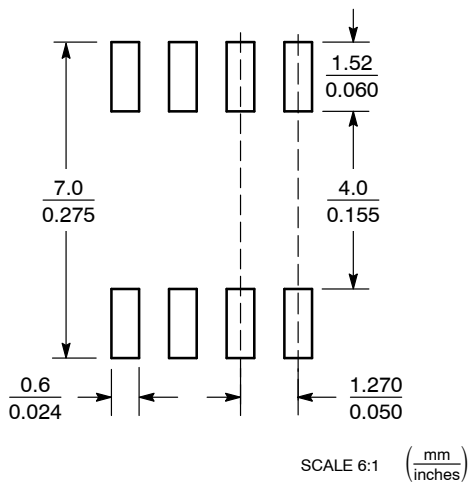
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

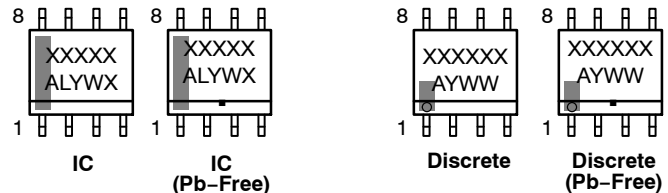
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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