

RFD4N06L RFD4N06LSM

N-Channel Logic Level
Power Field Effect Transistors

August 1991

Features

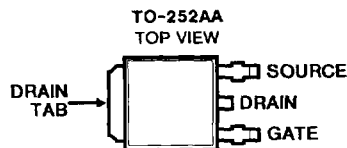
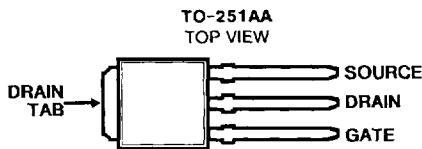
- 4A, 60V
- $R_{DS(on)} = 0.60\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power-Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

Description

The RFD4N06L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

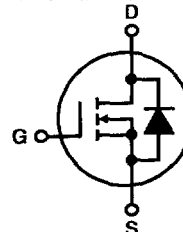
The RFD4N06L is supplied in the JEDEC TO-251 plastic package and the RFD4N06LSM is supplied in the JEDEC TO-252 plastic package.

Packages



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

Drain-Source Voltage, V_{DS}	60V
Drain-Gate Voltage, V_{DG}	60V
Gate-Source Voltage, V_{GS}	$\pm 10\text{V}$
Drain Current:	
RMS Continuous, I_D	4A
Pulsed, I_{DM}	10A
Power Dissipation, P_D :	
$T_C = +25^\circ\text{C}$	30W
Derate Above $T_C = +25^\circ\text{C}$	0.20W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175 $^\circ\text{C}$

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PREVIEW
PRODUCTS

Specifications RFD4N06L, RFD4N06LSM

Electrical Characteristics ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$	60	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50\text{V}$	-	1	μA
		$V_{DS} = 50\text{V} @ T_C = 125^\circ\text{C}$	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10\text{V}, V_{DS} = 0\text{V}$	-	100	nA
Drain-Source on Voltage	$V_{DS(on)}$	$I_D = 1\text{A}, V_{GS} = 5\text{V}$	-	0.8	V
		$I_D = 2\text{A}, V_{GS} = 5\text{V}$	-	2.0	V
		$I_D = 4\text{A}, V_{GS} = 7.5\text{V}$	-	4.0	V
On Resistance	$R_{DS(on)}$	$I_D = 1\text{A}, V_{GS} = 5\text{V}$	-	0.6	Ω
Total Gate Charge	$Q_g(\text{total})$	$V_{GS} = 0 \text{ to } 10\text{V}$	-	8	nC
Gate Charge at 5V	$Q_g(5)$	$V_{GS} = 0 \text{ to } 5\text{V}$			
Threshold Gate Charge	$Q_g(\text{th})$	$V_{GS} = 0 \text{ to } 1\text{V}$			
Plateau Voltage	V_{plateau}	$I_D = 4\text{A}, V_{DS} = 15\text{V}$	-	4.5	V
Turn-On Delay Time	$t_{D(on)}$	$V_{DD} = 30\text{V}, I_D = 1\text{A}$ $R_G = 6.25\text{V}, V_{GS} = 5\text{V}$	-	20	ns
Rise Time	t_R		-	130	ns
Turn-Off Delay Time	$t_{D(off)}$		-	40	ns
Fall Time	t_F		-	160	ns
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	5	$^\circ\text{C/W}$

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX.	
Forward Voltage	V_{SD}	$I_{SD} = 1\text{A}$	-	1.4	V
Reverse Recovery Time	t_{rr}	$I_f = 2\text{A}, di_f/dt = 100\text{A}/\mu\text{s}$	-	150(typ.)	ns