FAIRCHILD

SEMICONDUCTOR ™

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$QFET^{TM}$

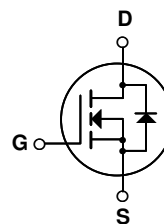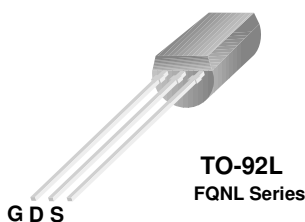# FQNL1N50B

500V N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- 0.27A, 500V, $R_{DS(on)}$ = 9.0Ω @V_{GS} = 10 V
- Low gate charge (typical 4.0 nC)
- Low Crss (typical 3.0 pF)
- Fast switching
- Improved dv/dt capability

TO-92L
FQNL Series

G D S

D

G

S

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FQNL1N50B	Units
V_{DSS}	Drain-Source Voltage			500	V
I_D	Drain Current	- Continuous (T_C = 25°C)		0.27	A
		- Continuous (T_C = 100°C)		0.17	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	1.08	A
V_{GSS}	Gate-Source Voltage			± 30	V
I_{AR}	Avalanche Current		(Note 1)	0.27	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	0.15	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 2)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)			1.5	W
	- Derate above 25°C			0.012	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	83	°C/W

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 400$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	2.3	3.0	3.7	V
		$V_{DS} = V_{GS}$, $I_D = 250$ mA	3.6	4.3	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 0.135$ A	--	6.8	9.0	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50$ V, $I_D = 0.135$ A (Note 3)	--	0.55	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	115	150	pF
C_{oss}	Output Capacitance		--	20	30	pF
C_{rss}	Reverse Transfer Capacitance		--	3.0	4.0	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250$ V, $I_D = 1.4$ A, $R_G = 25$ Ω	--	5	20	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	8	25	ns
t_f	Turn-Off Fall Time	(Note 3, 4)	--	20	50	ns
Q_g	Total Gate Charge	$V_{DS} = 400$ V, $I_D = 1.4$ A, $V_{GS} = 10$ V	--	4.0	5.5	nC
Q_{gs}	Gate-Source Charge		--	1.1	--	nC
Q_{gd}	Gate-Drain Charge	(Note 3, 4)	--	2.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.27	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	1.08	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 0.27$ A	--	--	1.4	V
trr	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 1.4$ A,	--	170	--	ns
Qrr	Reverse Recovery Charge	$dI_F / dt = 100$ A/us (Note 3)	--	0.4	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{SD} \leq 1.4$A, di/dt $\leq$ 200A/us, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
3. Pulse Test : Pulse width $\leq$ 300us, Duty cycle $\leq$ 2%
4. Essentially independent of operating temperature

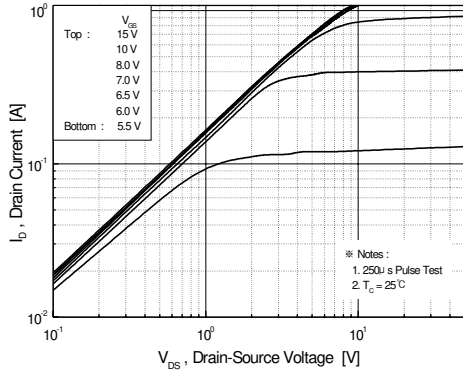# Typical Characteristics

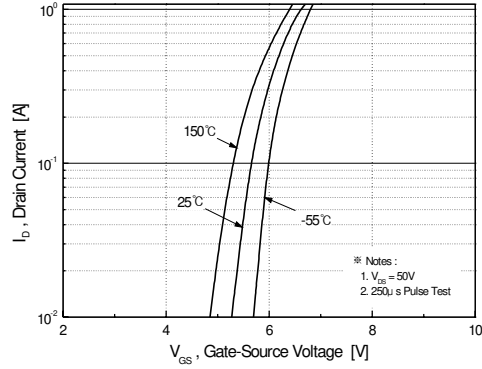Figure 1. On-Region Characteristics.
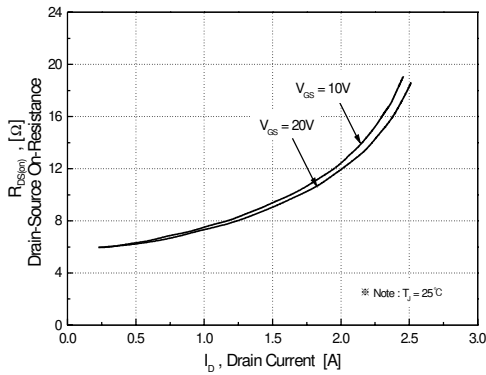

Figure 2. Transfer Characteristics.

Figure 3. On-Resistance Variation vs
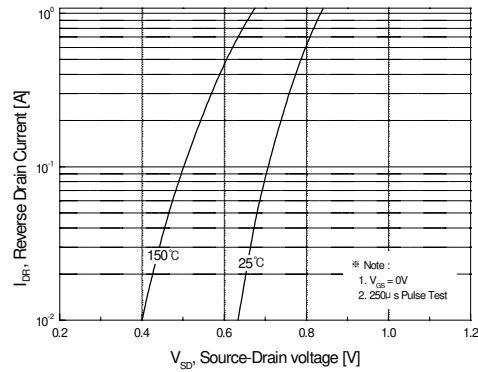Drain Current and Gate Voltage.

Figure 4. Body Diode Forward Voltage
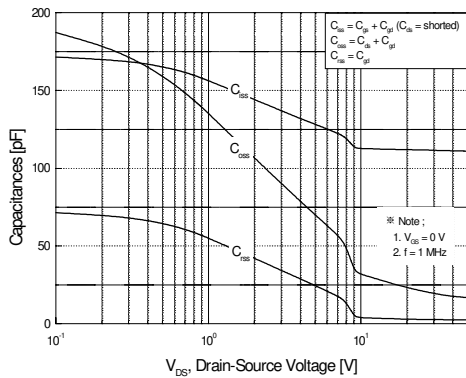Variation with Source Current
and Temperature.
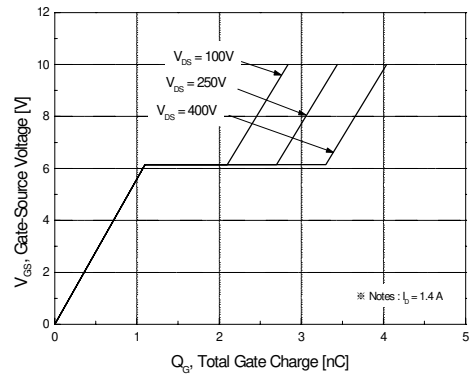

Figure 5. Capacitance Characteristics.

Figure 6. Gate -Charge Characteristics.

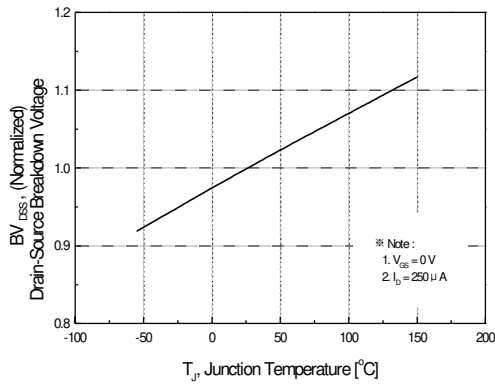# Typical Characteristics (Continued)

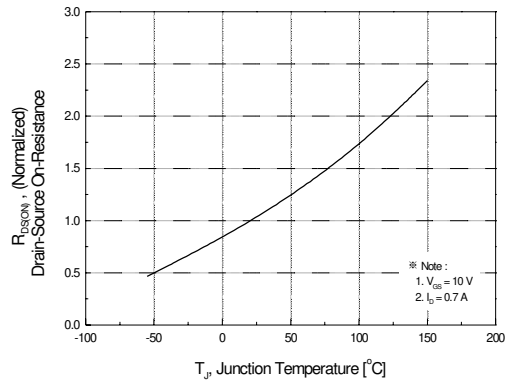Figure 7. Breakdown Voltage Variation
vs Temperature.

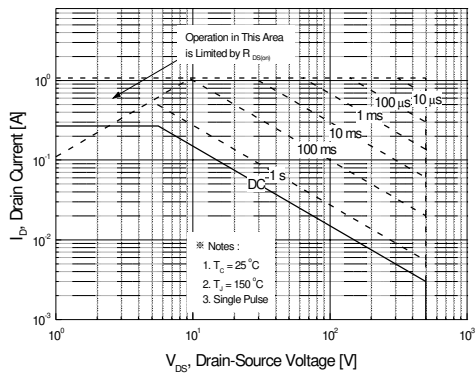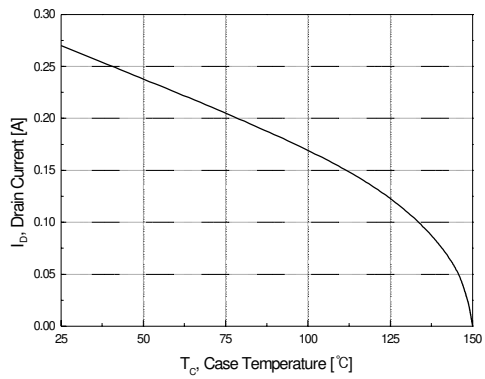Figure 8. On-Resistance Variation
vs Temperature.

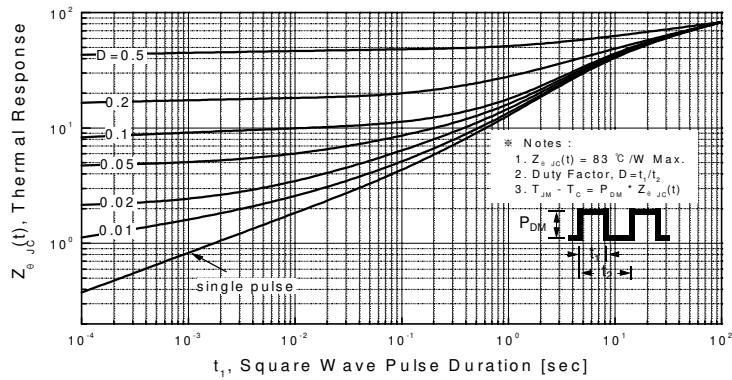Figure 9. Maximum Safe Operating Area.

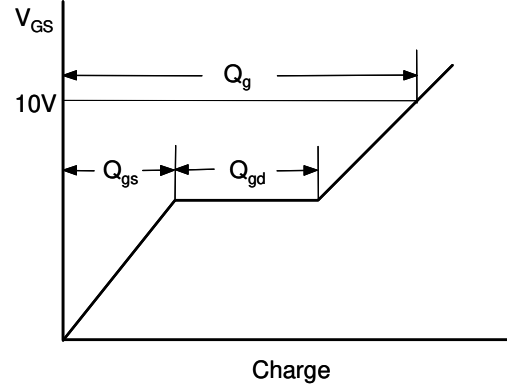Figure 10. Maximum Drain Current
vs Case Temperature.

Figure 11. Transient Thermal Response Curve.

Gate Charge Test Circuit & Waveform
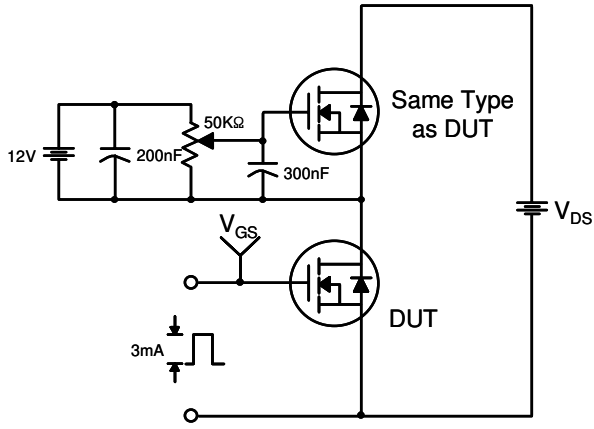
Resistive Switching Test Circuit & Waveforms
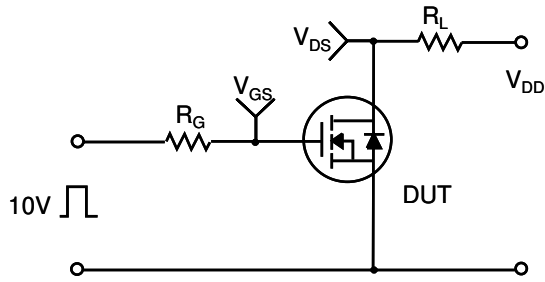
Peak Diode Recovery dv/dt Test Circuit & Waveform

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
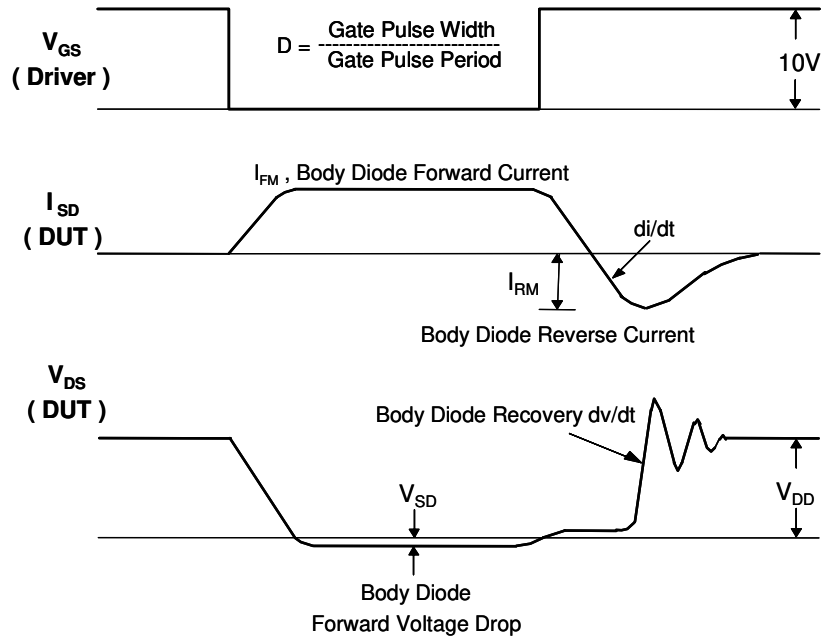
Package Dimensions

TO-92L

4.90 ±0.20

8.00 ±0.20

13.50 ±0.40

1.70 ±0.20

1.00 ±0.10

0.70MAX.

0.80 ±0.10

1.00MAX.

0.50 ±0.10

1.27TYP
[1.27 ±0.20]

2.54 TYP

0.45 ±0.10

1.45 ±0.20

3.90 ±0.20

3.90 ±0.20

0.45 ±0.10

Rev. A, March 2001
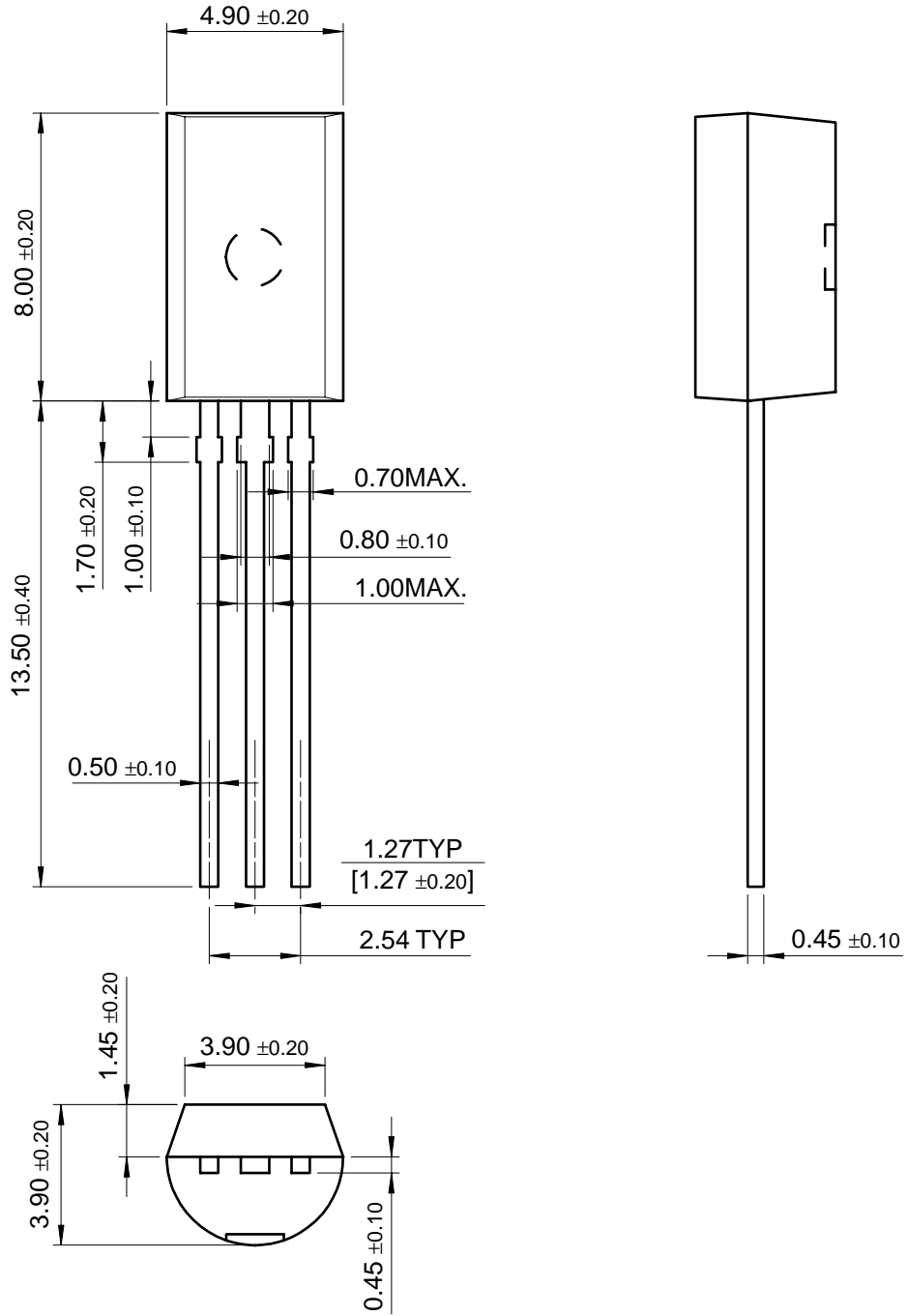
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