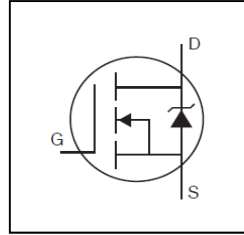


HEXFET® Power MOSFET

**Applications**

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



<b>V<sub>DSS</sub></b>	<b>100V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>3.7mΩ</b>
<b>R<sub>DS(on)</sub> max.</b>	<b>4.5mΩ</b>
<b>I<sub>D</sub></b>	<b>72A</b>

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free



TO-220 Full-Pak

<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFI4110GPbF	TO-220 Full-Pak	Tube	50	IRFI4110GPbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	72	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	51	
I <sub>DM</sub>	Pulsed Drain Current ①	290	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	61	W
	Linear Derating Factor	0.41	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt③	27	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Avalanche Characteristics**

E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	71	mJ
I <sub>AR</sub>	Avalanche Current ①	43	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	6.1	mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ③	—	2.46	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount)②	—	65	

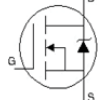
**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA ①
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	3.7	4.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 43A
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

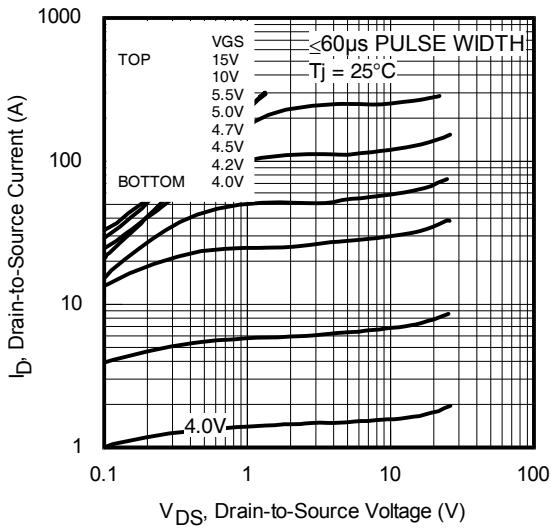
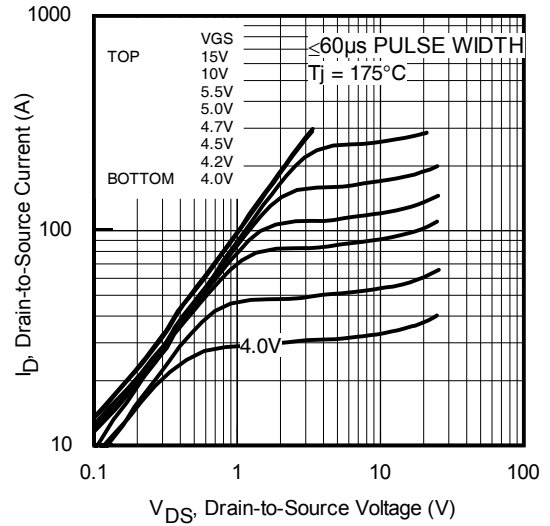
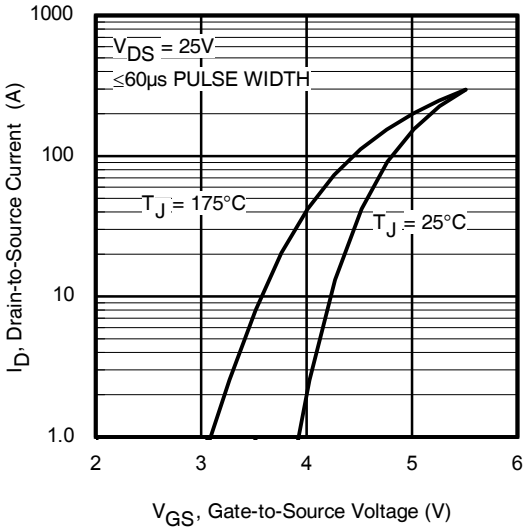
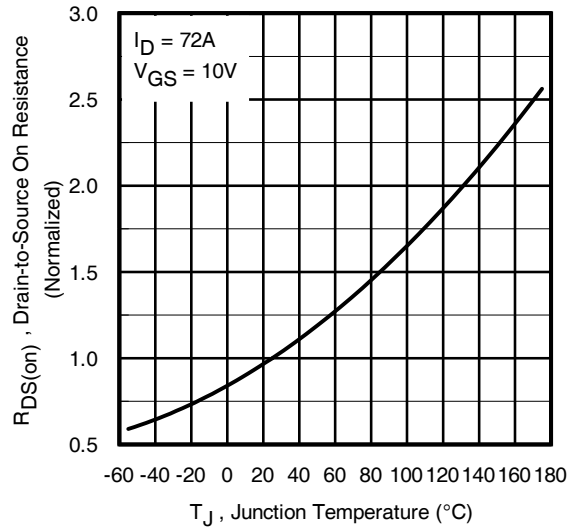
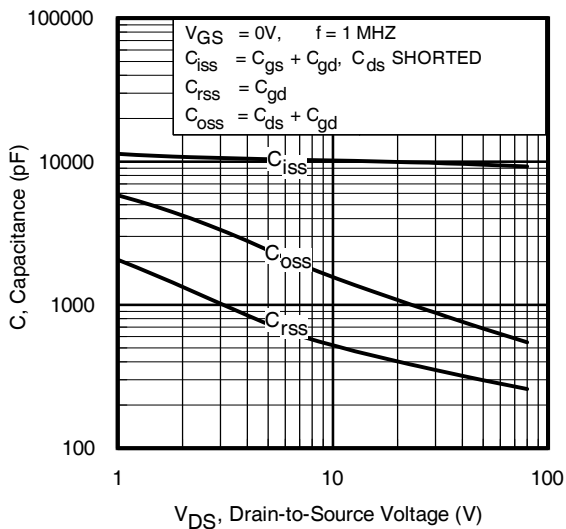
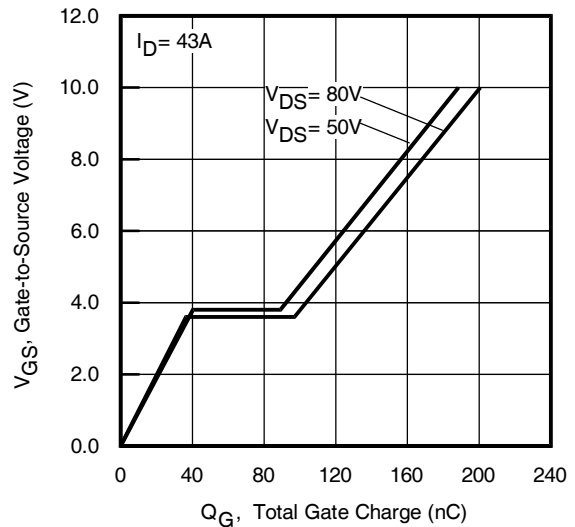
g <sub>fs</sub>	Forward Trans conductance	260	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 43A
Q <sub>g</sub>	Total Gate Charge	—	190	290	nC	I <sub>D</sub> = 43A
Q <sub>gs</sub>	Gate-to-Source Charge	—	40	—		V <sub>DS</sub> = 50V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	49	—		V <sub>GS</sub> = 10V ④
R <sub>G</sub>	Internal Gate Resistance	—	1.3	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	24	—	ns	V <sub>DD</sub> = 65V
t <sub>r</sub>	Rise Time	—	58	—		I <sub>D</sub> = 43A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	81	—		R <sub>G</sub> = 2.6Ω
t <sub>f</sub>	Fall Time	—	71	—		V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	—	9540	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	680	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	300	—		f = 1.0MHz
C <sub>oss eff. (ER)</sub>	Effective Output Capacitance (Energy Related)	—	760	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V ⑥
C <sub>oss eff. (TR)</sub>	Effective Output Capacitance (Time Related)	—	1120	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V ⑤

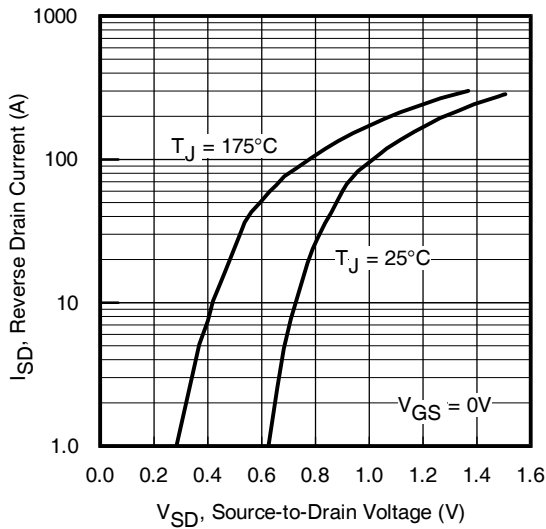
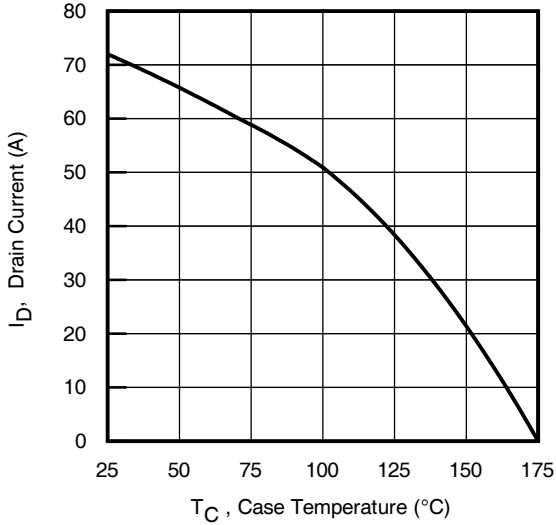
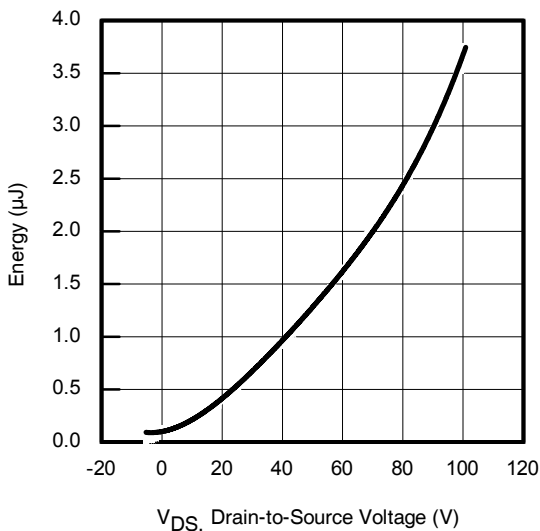
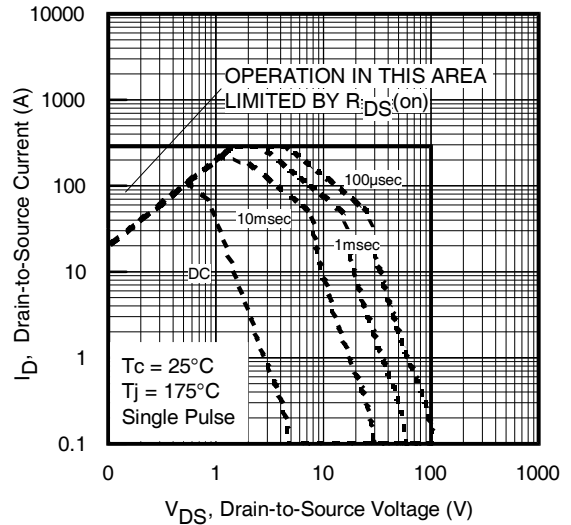
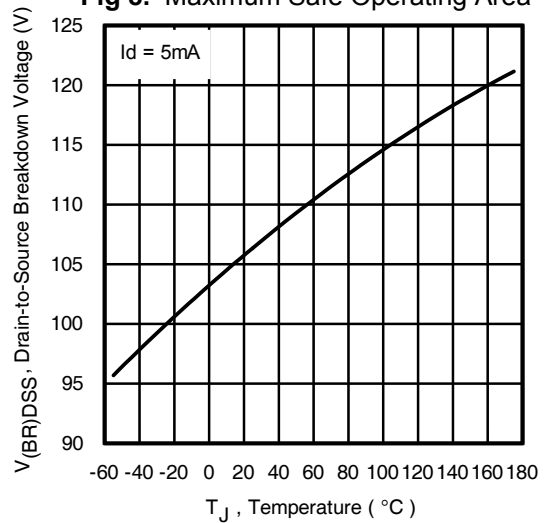
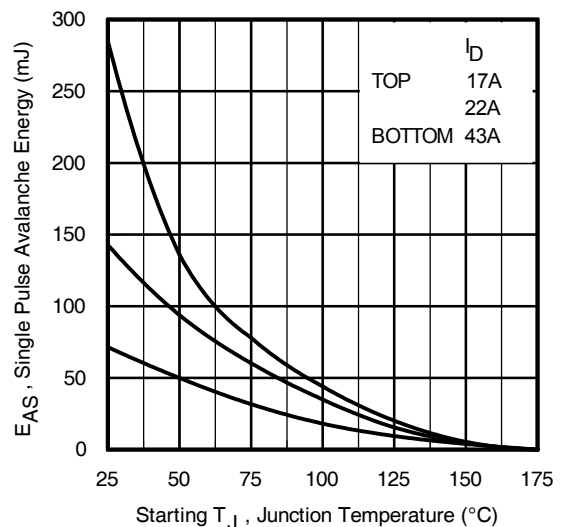
**Source-Drain Ratings and Characteristics**

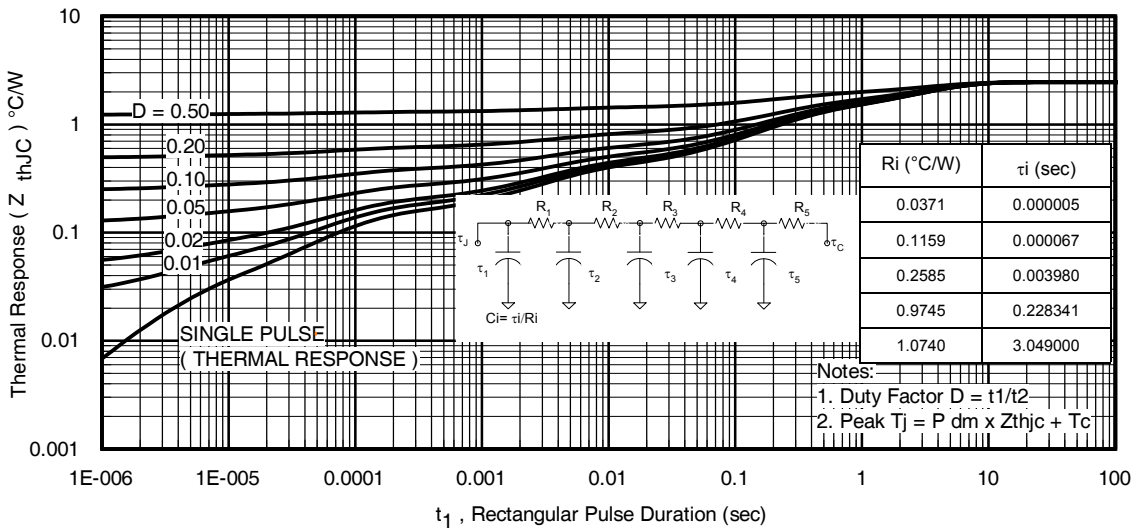
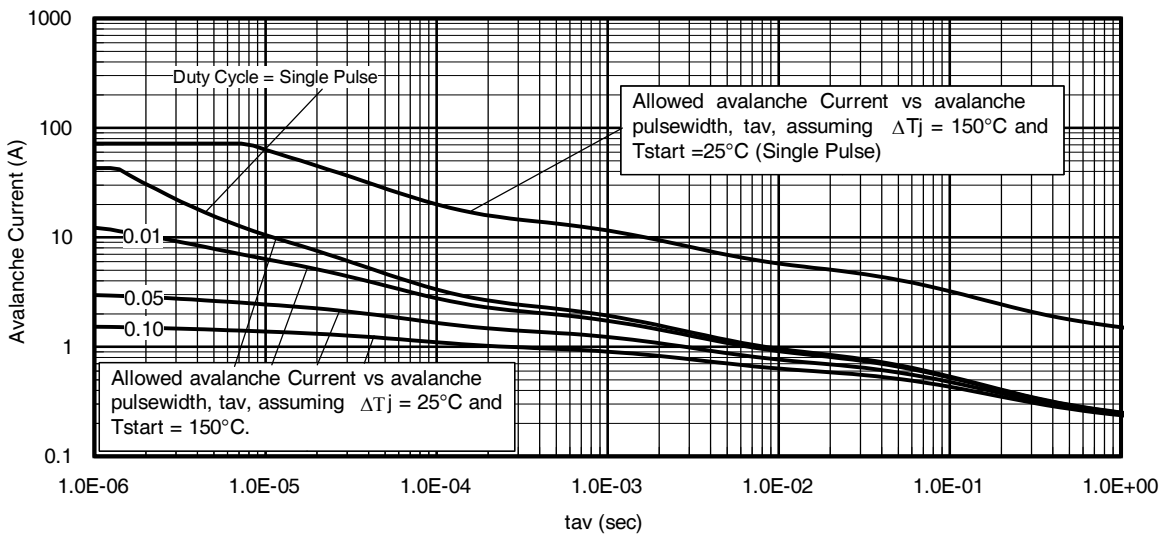
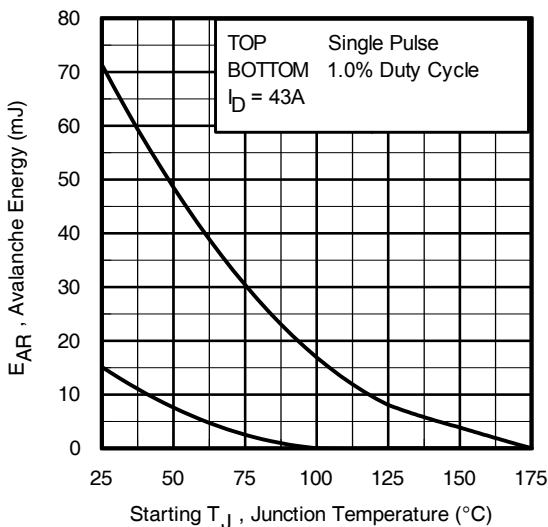
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	72	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	290		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 43A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	50	75	ns	T <sub>J</sub> = 25°C
		—	60	90		T <sub>J</sub> = 125°C
Q <sub>rr</sub>	Reverse Recovery Charge	—	100	150	nC	T <sub>J</sub> = 25°C — V <sub>R</sub> = 85V
		—	140	210		T <sub>J</sub> = 125°C — I <sub>F</sub> = 43A
I <sub>RRM</sub>	Reverse Recovery Current	—	3.5	—	A	T <sub>J</sub> = 25°C — di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.077mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 43A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 43A, di/dt ≤ 1600A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.


**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature

**Fig. 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig. 6.** Typical Gate Charge vs. Gate-to-Source Voltage

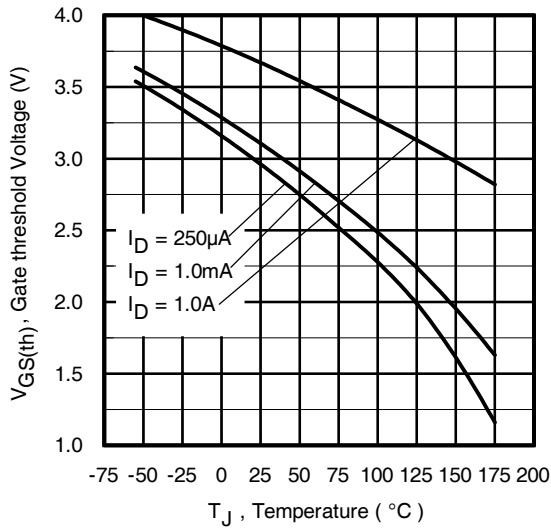
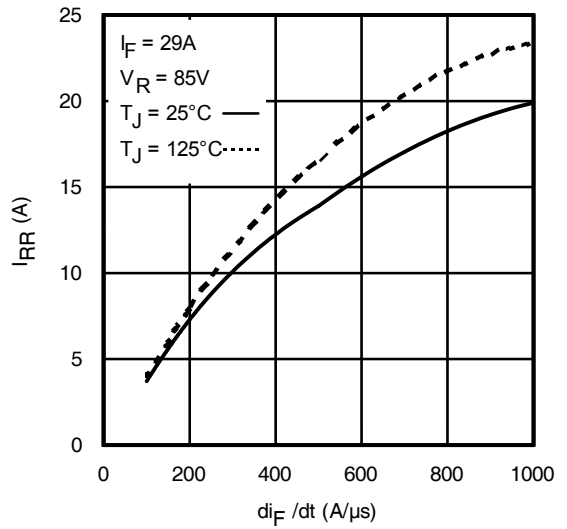
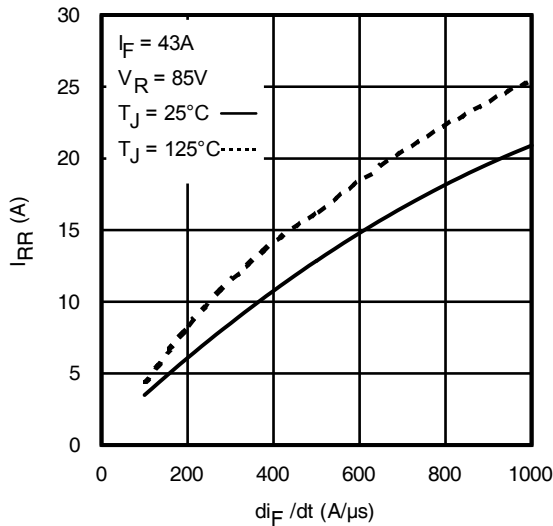
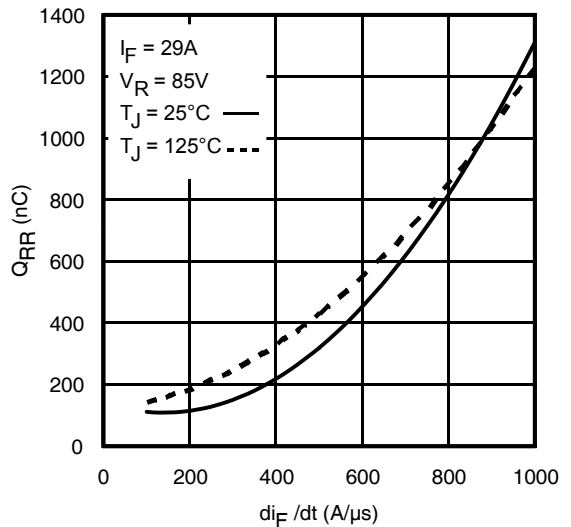
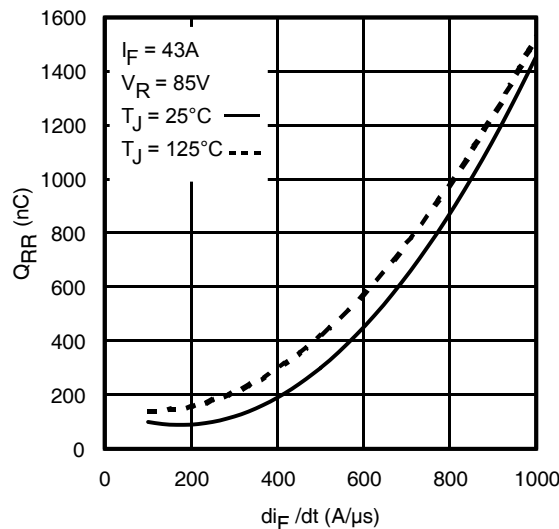

**Fig. 7.** Typical Source-to-Drain Diode Forward Voltage

**Fig. 9.** Maximum Drain Current vs. Case Temperature

**Fig. 11.** Typical  $C_{OSS}$  Stored Energy

**Fig 8.** Maximum Safe Operating Area

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 12.** Maximum Avalanche Energy vs. Drain Current

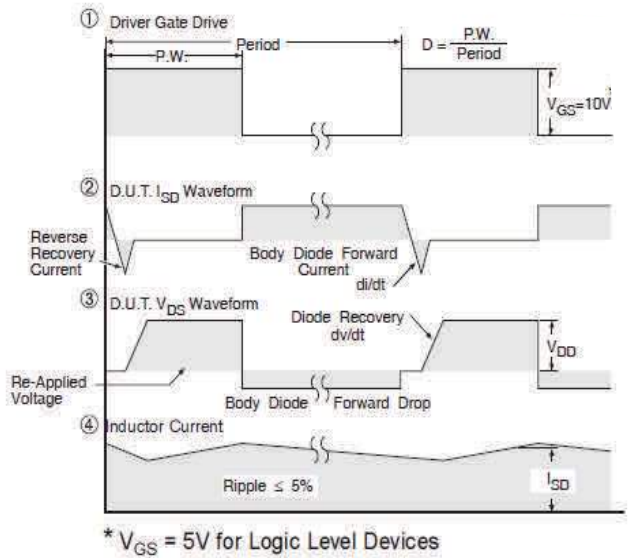
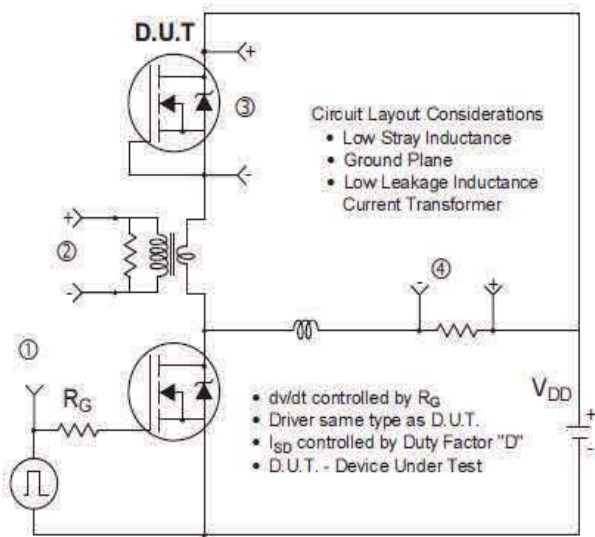
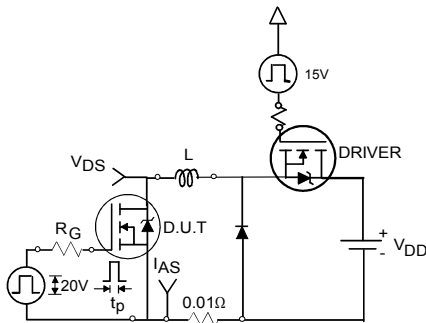
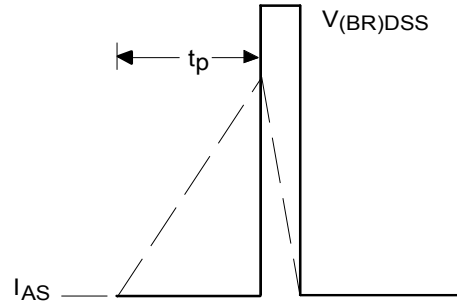
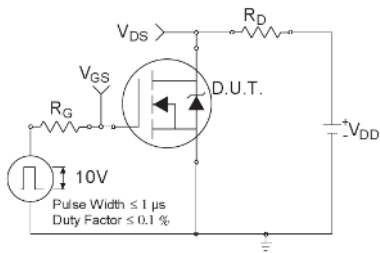
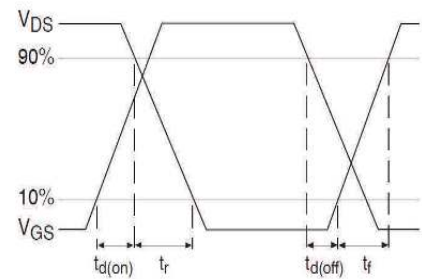
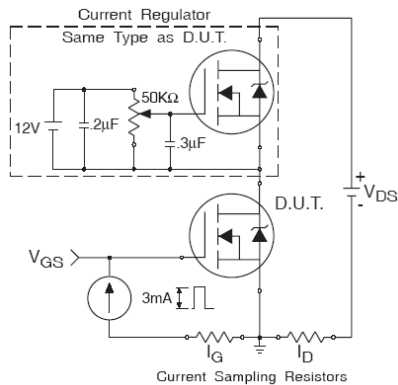
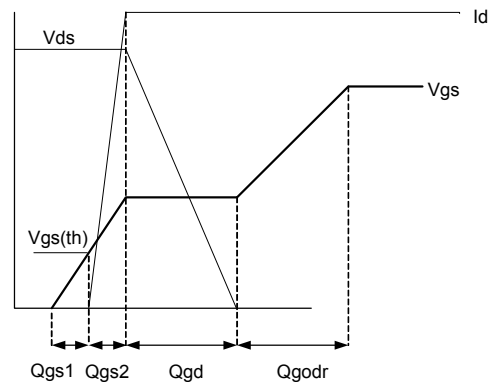

**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width**


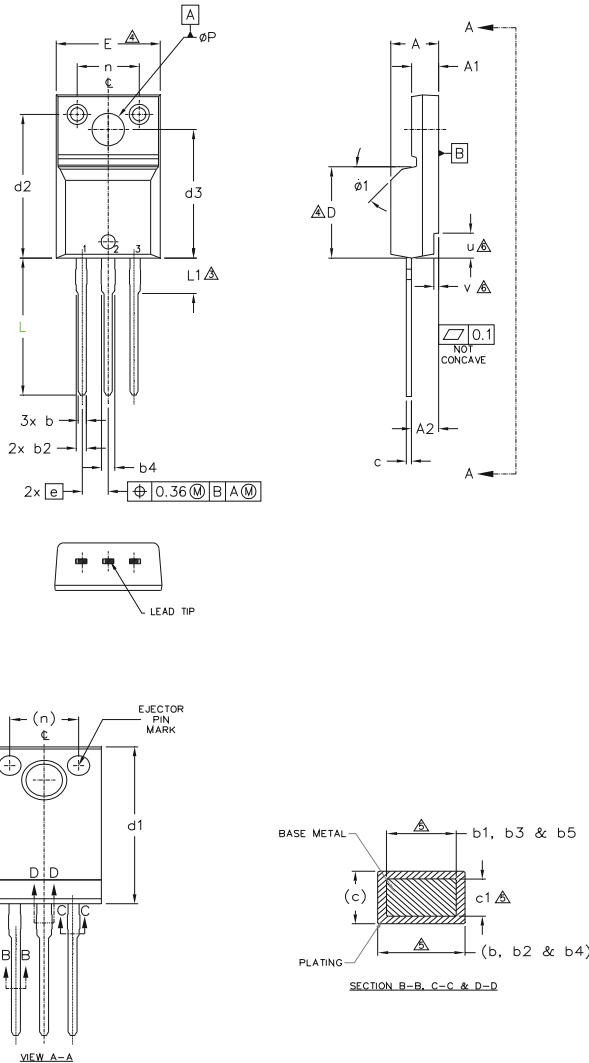
**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
**(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
  2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
  3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
  4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
  5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
  6.  $I_{av}$  = Allowable avalanche current.
  7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)
- $$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$
- $$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
- $$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

**Fig 15. Maximum Avalanche Energy vs. Temperature**


**Fig 16.** Threshold Voltage vs. Temperature

**Fig 17.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig 18.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig 19.** Typical Stored Charge vs.  $di_F/dt$ 

**Fig 20.** Typical Stored Charge vs.  $di_F/dt$


**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 22a. Unclamped Inductive Test Circuit**

**Fig 22b. Unclamped Inductive Waveforms**

**Fig 23a. Switching Time Test Circuit**

**Fig 23b. Switching Time Waveforms**

**Fig 24a. Gate Charge Test Circuit**

**Fig 24b. Gate Charge Waveform**

**TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

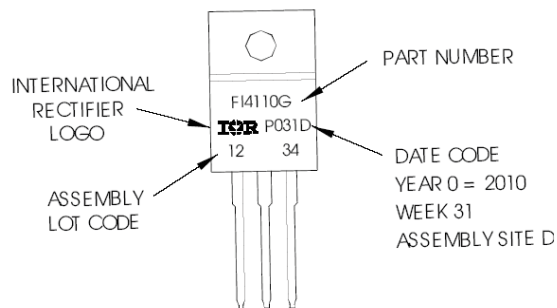
SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	.180	.190	LEAD ASSIGNMENTS  HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE	
A1	2.57	2.82	.101	.111		
A2	2.51	2.92	.099	.115		
b	0.61	0.94	.024	.037		
b1	0.61	0.89	.024	.035		5
b2	0.76	1.27	.030	.050		5
b3	0.76	1.22	.030	.048		
b4	1.02	1.52	.040	.060		5
b5	1.02	1.47	.040	.058		
c	0.33	0.63	.013	.025		4
c1	0.33	0.58	.013	.023		
D	8.66	9.80	.341	.386	4	
d1	15.80	16.13	.622	.635		
d2	13.97	14.22	.550	.560	4	
d3	12.29	12.93	.484	.509		
E	9.63	10.74	.379	.423	4	
e	2.54 BSC		.100 BSC			
L	13.21	13.72	.520	.540	3	
L1	3.10	3.68	.122	.145		
n	6.05	6.60	.238	.260	6	
phi P	3.05	3.45	.120	.136		
u	2.39	2.49	.094	.098	6	
v	0.41	0.51	.016	.020		
phi 1	-	45°	-	45°		

IGBTs, CoPACK  
1.- GATE  
2.- COLLECTOR  
3.- EMITTER

**TO-220 Full-Pak Part Marking Information**

EXAMPLE: THIS IS AN IRFI4110G  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW31, 2010

Notes: - "P" in assembly line position indicates "Lead-Free"  
- "G" suffix in part number indicates "Halogen-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>



**Qualification Information**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) †	
<b>Moisture Sensitivity Level</b>	TO-220 Full-Pak	N/A
<b>RoHS Compliant</b>	Yes	

† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
04/27/2017	<ul style="list-style-type: none"> <li>Changed datasheet with Infineon logo - all pages.</li> <li>Corrected Package Outline on page 8.</li> <li>Corrected fig 19 &amp; 20 –Y axis title from “A” to “nC” on page 6.</li> <li>Added disclaimer on last page.</li> </ul>

**Trademarks of Infineon Technologies AG**

µHVIC™, µIPM™, µPFC™, AU-ConvertIR™, AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolDP™, CoolGaN™, COOLiR™, CoolMOST™, CoolSET™, CoolSiC™, DAVE™, DI-POL™, DirectFET™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, GaNpowIR™, HEXFET™, HITFET™, HybridPACK™, iMOTION™, IRAM™, ISOFACE™, IsoPACK™, LEDrivIR™, LITIX™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OPTIGA™, OptiMOST™, ORIGA™, PowIRaudio™, PowIRStage™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SiL™, RASiC™, REAL3™, SmartLEWIS™, SOLID FLASH™, SPOC™, StrongIRFET™, SupIRBuck™, TEMPFET™, TRENCHSTOP™, TriCore™, UHVIC™, XHP™, XMC™

Trademarks updated November 2015

**Other Trademarks**

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2016-04-19**

**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

© 2016 Infineon Technologies AG.  
**All Rights Reserved.**

**Do you have a question about this document?**  
**Email:** [erratum@infineon.com](mailto:erratum@infineon.com)

**Document reference**  
**ifx1**

**IMPORTANT NOTICE**

The information given in this document shall in no event be regarded as a guarantee of conditions or **characteristics (“Beschaffenheitsgarantie”)**.

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document **is subject to customer’s compliance with its obligations** stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in **customer’s applications**.

The data contained in this document is exclusively intended for technically trained staff. It is the **responsibility of customer’s technical departments** to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office ([www.infineon.com](http://www.infineon.com)).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, **Infineon Technologies’ products may not be used** in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.