

## Fully integrated RF front-end receiver for GPS applications

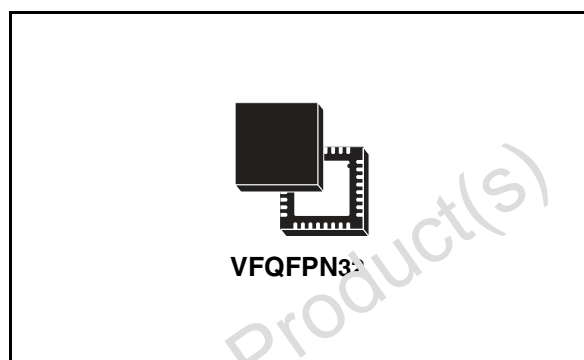
### Features

- Low IF architecture ( $f_{IF} = 4f_O$ )
- Minimum external components
- VGA gain internally regulated
- On chip programmable PLL
- Typ. 2.7 V supply voltage
- SPI interface
- 2 kV HBM ESD protected
- Compatible with GPS L1
- Standard QFN-32 package
- Low power for portable designs

### Description

The chip is a fully integrated RF front-end able to down-convert the GPS L1 signal from 1575.42 MHz to 4.092 MHz.

The IF signal is converted by a two bit ADC. Sign (SIGN), Magnitude (MAG) and the 16.368 MHz sampling clock (GPS\_CLK) are provided to the baseband.



The magnitude data is internally integrated in order to control the variable gain amplifiers in accordance to the RF input signal strength.

An excellent quality of reception in critical environments is ensured by the good noise figure and linearity of the receiver.

The on-chip oscillator supports crystal frequencies in the range of 10MHz to 40MHz. It is able to support TCXO providing also a buffered copy of the oscillator frequency.

The chip, using STMicroelectronics BiCMOS SiGe technology, is housed in a QFN-32 package.

**Table 1. Device summary**

| Order code | Marking | Package  | Packing     |
|------------|---------|----------|-------------|
| STA5620TR  | STA5620 | VFQFPN32 | Tape & reel |

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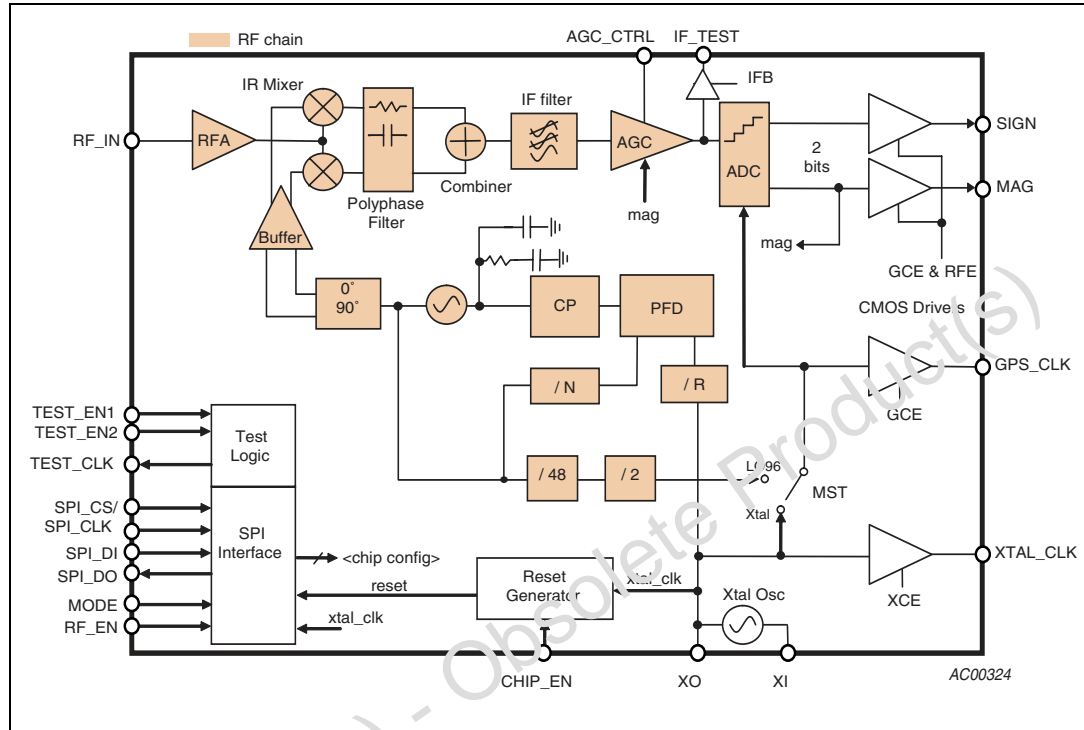
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Obsolete Product(s) - Obsolete Product(s)

# 1 Block diagram

Figure 1. Block diagram

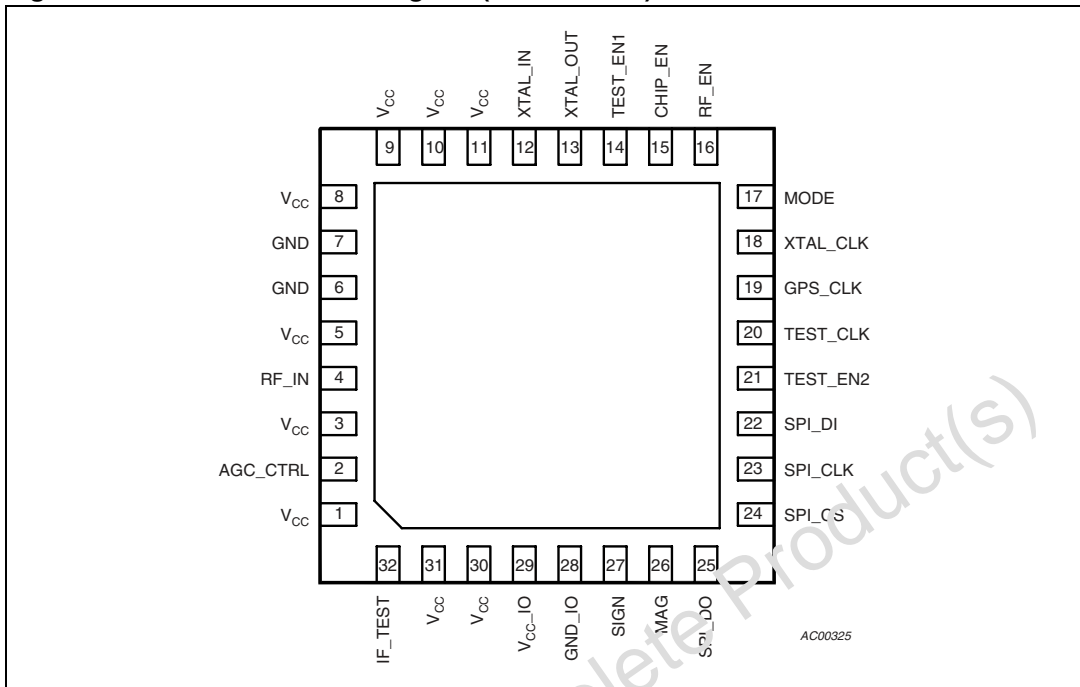


## 2 Pins description

**Table 2. Pins list description**

| PIN | Symbol             | Description  | Type              |
|-----|--------------------|--|-------------------|
| 1   | V <sub>CC</sub>    | IF section power supply                            | Supply pin        |
| 2   | AGC_CTRL           | Automatic Gain Control Pin                         | Analog – input    |
| 3   | V <sub>CC</sub>    | Mixer power supply                                 | Supply pin        |
| 4   | RF_IN              | RF section input                                   | Analog – RF input |
| 5   | V <sub>CC</sub>    | RF amplifier power supply                          | Supply pin        |
| 6   | GND                | Negative Supply Pin                                | Gnd               |
| 7   | GND                | Negative Supply Pin                                | Gnd               |
| 8   | V <sub>CC</sub>    | Charge pump power supply                           | Supply pin        |
| 9   | V <sub>CC</sub>    | Digital section power supply                       | Supply pin        |
| 10  | V <sub>CC</sub>    | VCO power supply                                   | Supply pin        |
| 11  | V <sub>CC</sub>    | Crystal oscillator power supply                    | Supply pin        |
| 12  | XTAL_IN            | Input Side of Crystal Oscillator or TCXO Input     | Analog – input    |
| 13  | XTAL_OUT           | Output Side of Crystal Oscillator                  | Analog – output   |
| 14  | TEST_EN1           | Test enable 1. Only for ST internal use            | Digital – input   |
| 15  | CHIP_EN            | Chip Enable  | Digital – input   |
| 16  | RF_EN              | RF/IF Receiver Chain Enable                        | Digital – input   |
| 17  | MODE               | Power-On Default Configuration Selector            | Digital – input   |
| 18  | XTAL_CLK           | Crystal Oscillator Buffered Output                 | Digital – output  |
| 19  | GPS_CLK            | GPS Reference Clock                                | Digital – output  |
| 20  | TEST_CLK           | Test Clock. Only for ST internal use               | Digital – output  |
| 21  | TEST_EN2           | Test enable 2. Only for ST internal use            | Digital – input   |
| 22  | SPI_DI             | Serial Parallel Interface Data Input               | Digital – input   |
| 23  | SPI_CLK            | Serial Parallel Interface Clock                    | Digital – input   |
| 24  | SPI_CS/            | Serial Parallel Interface Chip Select (Active Low) | Digital – input   |
| 25  | SPI_DO             | Serial Parallel Interface Data Output              | Digital – output  |
| 26  | MAG                | Magnitude Data                                     | Digital – output  |
| 27  | SIGN               | Sign Data  | Digital – output  |
| 28  | GND_IO             | Output Drivers Ground                              | Gnd               |
| 29  | V <sub>CC_IO</sub> | I/Os power supply                                  | Supply pin        |
| 30  | V <sub>CC</sub>    | SPI power supply                                   | Supply pin        |
| 31  | V <sub>CC</sub>    | A/D converter power supply                         | Supply pin        |
| 32  | IF_TEST            | RF/IF Receiver Chain Test Output                   | Analog – output   |

Figure 2. Pins connection diagram (bottom view)





## 3 Functional description

### 3.1 RFA and MIXER section

The 1575.42 MHz RF signal at the output of the external SAW filter is amplified by a RF amplifier (RFA) and then down converted by an image rejection mixer.

The good performances of the cascade configuration and the technology choice guarantee a noise figure better than 4.5 dB in typical conditions. In fact, the RFA gain is high enough to minimize the effects on the noise figure of the following integrated stages.

The linearity of the RFA and Mixer section ensures immunity to RF blockers close to the GPS signal. Then it allows the use of low quality external pre-selection filters.

Two ninety degrees out of phase signals are derived from the VCO and send to the input of the image rejection mixer. A minimum image rejection ratio of 20 dB is guaranteed.

The chosen IF frequency is  $4f_0 = 4.092$  MHz.

### 3.2 IF section

The output of the mixer combiner is processed through an integrated filter able to select the GPS L1 bands. The IF filter cuts any out-of-band signal including the mixer products. In addition it acts as an anti-aliasing filter for the A/D converter. An attenuation of 20 dB is guaranteed at  $12f_0 = 12.276$  MHz.

The IF filter characteristic is calibrated by an internal loop which compensates process, temperature and voltage variations.

In order to let the baseband reconstruct the received information, the IF filter must not introduce an excessive phase shift within the signal bandwidth.

### 3.3 Variable gain amplifiers

A cascade of variable gain amplifiers and the relevant control circuit balance the system gain in relationship to the RF input signal strength. In that way the signal level at the input of the A/D converter is suitably compensated.

The device is able to self-adjust the AGC gain by integrating the MAG output by a dedicated circuit in order to obtain 33 % of MAG bit duty cycle. The loop is compensated by an external capacitor connected to the AGC\_CTRL pin. The relevant voltage is used to control the variable gain amplifiers.

The internal loop can be by-passed by setting a voltage to the AGC\_CTRL input pin. A dynamic range of around 55 dB is typically achieved.

### 3.4 A/D converter

The task of the A/D converter is to determine the sign and the magnitude of the received signal. The A/D converter sampling frequency is  $16f_0 = 16.368$  MHz.

Those baseband chips with just one bit input will use only the sign bit. In that case the AGC\_CTRL pin must be connected to ground through an external capacitor ( $\sim 10 \mu\text{F}$ ).

### 3.5 PLL synthesizer and VCO

The PLL synthesizer is fully integrated on-chip, it is made by the voltage controlled oscillator (VCO), prescaler, dividers, phase-frequency detector (PFD), charge pump (CP) and loop filter. Both the reference divider R and the feedback divider N are programmable helping the user to choose the reference clock. The R divider ranges from 1 to 63 while the N divider from 56 to 4095.

In order to achieve good phase noise performances, a LC voltage controlled oscillator has been chosen. Quadrature signals are provided by means of a polyphase filter.

A programmable loop filter is integrated on-chip to reduce the number of external components. The loop stability is guaranteed for any of the supported crystals and comparison frequencies.

The charge pump is programmable and the output current can be selected among the following values: 50  $\mu\text{A}$ , 100  $\mu\text{A}$ , 150  $\mu\text{A}$  and 200  $\mu\text{A}$ .

### 3.6 Crystal oscillator

The reference oscillator circuit is a CMOS inverter able to work with external crystals up to 40 MHz. The crystal must be connected between the xtal input and the xtal output pins. The load capacitances must be chosen in accordance to the values specified by the crystal manufacturer. A limiting resistor can be placed at the output of the inverter in order to contain the power dissipated in the crystal within its specified maximum value.

When a TCXO is used the external reference clock must be applied to the XTAL\_IN terminal.

### 3.7 Output buffers

The RF front-end provides a set of four different signals to the baseband chip.

The S<sub>IG</sub>I and the MAG outputs are the sampled bit streams of the down-converted received signal.

CFC\_CLK, nominally equal to 16.368 MHz, is the clock signal used by the baseband. Its source can be chosen among the crystal oscillator signal and the VCO signal by means of a 96 divider.

XTAL\_CLK is the buffered copy of either the crystal oscillator or the TCXO signal.

In order to let the application find the best compromise between electro-magnetic interferences and the drivers speed, the output stages slew-rate can be programmed by SPI.

### 3.8 SPI interface

A SPI interface manages the communication between the baseband chip and the RF front-end. Four lines are required to accomplish this task: a data input line (SPI\_DI), a data output line (SPI\_DO), a clock line (SPI\_CLK) and a chip select line (SPI\_CS/) active low.

Any information can be passed to the RF receiver through the SPI interface depending on the CHIP\_EN and RF\_EN input pins status.

### 3.9 Power control modes

Three different power control modes can be chosen by means of the CHIP\_EN and the RF\_EN pins. If the CHIP\_EN pin is forced low the device goes to stand-by mode with very low power consumption. On the other hand, if CHIP\_EN is set high, two scenarios are possible:

1. If RF\_EN = 0 the crystal oscillator and only one output buffer are enabled, XTAL\_CLK if MODE = 1 or GPS\_CLK if MODE = 0;
2. If RF\_EN = 1 the whole chip is active and functional.  
Only if MODE = 0 the XTAL\_CLK output is disabled.

A logic reset of the SPI registers is generated by the low to high transitions of the CHIP\_EN pin. External pin strapping dominates until some SPI commands reverse the priority and overrides the strapping until next reset.

## 4 Electrical specifications

### 4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol      | Parameter                                       | Min  | Max | Unit |
|-------------|---|------|-----|------|
| $V_{CC}$    | All supply voltages                             | -0.3 | 3.6 | V    |
| $T_J$       | Junction operating temperature                  | -40  | 125 | °C   |
| $T_S$       | Storage temperature                             | -65  | 150 | °C   |
| $ESD_{HBM}$ | Electro static discharge – Human body model     | -    | 2   | kV   |
| $ESD_{MM}$  | Electro static discharge – Machine model        | -    | 200 | V    |
| $ESD_{CDM}$ | Electro static discharge - Charged device model | -    | 750 | V    |

### 4.2 Thermal data

Table 4. Thermal data

| Symbol         | Parameter                              | Value     | Unit |
|----------------|--|-----------|------|
| $T_{amb}$      | Ambient operating temperature          | -40 to 85 | °C   |
| $R_{th j-amb}$ | Thermal resistance junction to ambient | 40        | °C/W |

### 4.3 Electrical characteristics

Table 5. Electrical characteristics

( $V_{CC} = 2.7$  V,  $T_J = 25$  °C unless otherwise noted)

| Symbol                               | Parameter                    | Test conditions       | Min  | Typ     | Max | Unit |
|--------------------------------------|------------------------------|-----------------------|------|---------|-----|------|
| <b>Supply</b>                        |                              |                       |      |         |     |      |
| $V_{CC}$                             | Analog, Digital              |                       | 2.56 | 2.7     | 3.3 | V    |
| $V_{CC\_IO}$                         | I/O supply                   |                       | 1.7  |         | 3.3 | V    |
| $I_{CC}$                             | Total power consumption      | Internal blocks ON    |      | 15      | 19  | mA   |
| $I_{CC\_CLK}$                        | Clock only power consumption | Crystal oscillator ON |      | 1.5     | 1.8 | mA   |
| $I_{CC\_STB}$                        | Stand-by power consumption   | Internal blocks OFF   |      | 1       |     | µA   |
| <b>RFA – MIXER – IF FILTER – VGA</b> |                              |                       |      |         |     |      |
| $f_{IN}$                             | RFA Input frequency          |                       |      | 1575.42 |     | MHz  |
| $f_{IF}$                             | IF frequency                 |                       |      | 4.092   |     | MHz  |
| $G_C$                                | Conversion gain              | VGA at max gain       |      | 105     |     | dB   |
|                                      |                              | VGA at min gain       |      | 50      |     |      |

**Table 5. Electrical characteristics (continued)** $(V_{CC} = 2.7 \text{ V}, T_J = 25 \text{ }^\circ\text{C}$  unless otherwise noted)

| Symbol  | Parameter                             | Test conditions  | Min | Typ      | Max      | Unit          |
|---|---------------------------------------|--|-----|----------|----------|---------------|
| $\Delta G_C$  | VGA range                             | Set $V_{AGC\_CTRL} < 0.3 \text{ V}$ for maximum gain                     |     | 55       |          | dB            |
| $V_{AGC\_CTRL}$   | AGC Control Voltage Range             |  | 0   |          | $V_{CC}$ | V             |
| $G_{SENS}$  | VGA sensitivity                       |  |     |          | 36       | dB/V          |
| $NF_{RF-IF}$  | RF-IF-VGA noise figure                | $f = 4.092 \text{ MHz}$<br>VGA at max gain                               |     | 4.5      |          | dB            |
| $P_{-1dB}$  | RF-IF-VGA 1dB input compression point | VGA at min gain  |     | -57      |          | dBm           |
| IRR   | Mixer image rejection ratio           | $f = 2 \text{ to } 6 \text{ MHz}$  |     | 20       |          | dB            |
| $IFF_{3dB}$   | IF filter cut-off frequency           |  |     | 6        |          | MHz           |
| $IFF_{ATT}$   | IF filter out of band attenuation     | $f = 12.276 \text{ MHz}$   | 20  |          |          | dB            |
| $VSWR_{IN}$   | RFA Input voltage stat. wave ratio    | $Z_S = 50 \text{ } \Omega$   |     |          | 2:1      | -             |
| <b>Crystal oscillator – Integer-N synthesizer – VCO</b> |                                       |  |     |          |          |               |
| $F_{XTAL}$  | XTAL frequency                        |  | 10  |          | 40       | MHz           |
| $t_{START-UP}$  | XTAL oscillator start-up time         |  |     |          | 10       | msec          |
| $P_{XTAL\_IN}$  | Reference input signal sensitivity    | XTAL_IN pin, DC blocked.<br>No crystal mounted.<br>XTAL_OUT load <10 pF. |     | -20      |          | dBm           |
| $R_{DIV}$   | Reference divider range               |  | 1   |          | 63       | -             |
| $F_{LO}$  | LO operating frequency                |  |     | 1571.328 |          | MHz           |
| $N_{DIV}$   | VCO divider range                     |  | 56  |          | 4095     | -             |
| $K_V^{(1)}$   | VCO gain                              | $f = 1571.328 \text{ MHz}$   |     | 300      |          | MHz/V         |
| $PN_{VCO}^{(1)}$  | VCO phase noise                       | 100 kHz offset   |     |          | -80      | dBc/Hz        |
| $PN_{PLL}^{(1)}$  | PLL phase noise                       | 1 kHz offset   |     | -65      |          | dBc/Hz        |
| $I_{CP}^{(1)}$  | Charge pump current                   |  | 50  |          | 200      | $\mu\text{A}$ |
| $\Delta I_{CP}^{(1)}$                                   | Charge pump current steps             |  |     | 50       |          | $\mu\text{A}$ |
| <b>ADC – Output signals – GPS clock</b>                 |                                       |  |     |          |          |               |
| $f_{ADC}$   | ADC sampling frequency                |  |     | 16.368   |          | MHz           |
| $\tau_{MAG}$  | MAG duty cycle                        | Internally regulated   |     | 33       |          | %             |
| $\tau_{SIGN}$   | SIGN duty cycle                       |  |     | 50       |          | %             |
| $f_{CLOCK}$   | Output clock frequency                |  |     | 16.368   |          | MHz           |
| $\tau_{CLOCK}$  | Output clock duty cycle               |  |     | 50       |          | %             |

**Table 5. Electrical characteristics (continued)** $(V_{CC} = 2.7\text{ V}, T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted)

| Symbol                          | Parameter              | Test conditions   | Min                | Typ | Max                | Unit |
|---------------------------------|------------------------|---|--------------------|-----|--------------------|------|
| <b>Input and output buffers</b> |                        |   |                    |     |                    |      |
| $V_{IH}$                        | CMOS input high level  |   | $0.8 \cdot V_{CC}$ |     |                    | V    |
| $V_{IL}$                        | CMOS input low level   |   |                    |     | $0.2 \cdot V_{CC}$ | V    |
| $C_{IN}$                        | CMOS input capacitance |   |                    |     | 1                  | pF   |
| $V_{OH}$                        | CMOS output high level |   | $0.9 \cdot V_{CC}$ |     |                    | V    |
| $V_{OL}$                        | CMOS output low level  |   |                    |     | $0.1 \cdot V_{CC}$ | V    |
| $t_{RISE}^{(2)}$                | CMOS output rise time  | $C_L = 10\text{ pF}$ ,<br>from 10 % to 90 %<br>Slew-rate = fast |                    |     | 3                  | ns   |
|                                 |                        | $C_L = 10\text{ pF}$ ,<br>from 10 % to 90 %<br>Slew-rate = slow |                    |     | 6                  | ns   |
| $t_{FALL}^{(2)}$                | CMOS output fall time  | $C_L = 10\text{ pF}$ ,<br>from 10 % to 90 %<br>Slew-rate = fast |                    |     | 3                  | ns   |
|                                 |                        | $C_L = 10\text{ pF}$ ,<br>from 10 % to 90 %<br>Slew-rate = slow |                    |     | 6                  | ns   |

1. This value is guaranteed by design.
2. Simulation data.

## 5 Pin and I/O cells

### 5.1 Mode

This pin allows a choice of initial configuration of the registers at reset. This pin will always be an input. In application this pin will be connected either LO or HI.

When it is low the chip is configured to use 16.368 MHz as reference frequency, otherwise the reference frequency is 19.2 MHz. To use other reference frequencies the MODE bit must be overwritten by SPI.

### 5.2 RF\_EN

This pin provides control over the operating state of the RF and PLL sections. When it is low those blocks are off, when high the status of the blocks depends of CHIP\_EN. This pin will always be an input.

### 5.3 CHIP\_EN

This pin provides control over the operating state of the chip. When it is low the entire chip is disabled and only a leakage current is present ( $\sim 10 \mu\text{A}$ ). On the rising edge it provides the SPI with a reset signal, the SPI default status depends on MODE and RF\_EN pins status. When it is high the entire chip is enabled. This pin will always be an input.

### 5.4 TEST\_EN1, TEST\_EN2 and TEST\_CLK

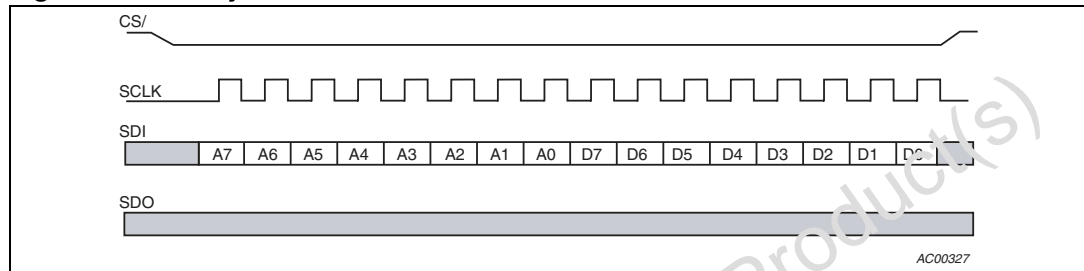
Those PINs are for ST test only. In the application TEST\_EN1 must be set LOW, TEST\_EN2 must be set HIGH ( $V_{CC\_IO}$ ) and TEST\_CLK must be not connected.

## 6 SPI bus protocol

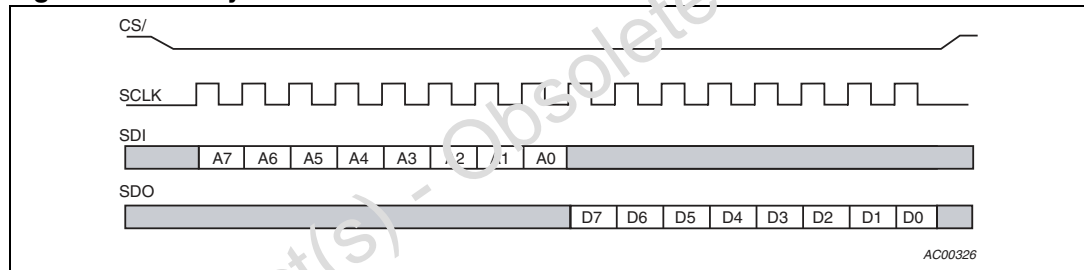
The SPI port is used for data exchange between STA5620 and a GPS base band. The SPI port is controlled by four pins SPI\_CLK, SPI\_DI, SPI\_DO and SPI\_CS/. These pins are inputs only, except for SPI\_DO, the data output. The SPI Bus protocol is based on a 2-phase transfer made of an address cycle and a data cycle.

The two functions in the bus interface layer are:

**Figure 3. SPI byte write**



**Figure 4. SPI byte read**



### 6.1 SPI\_CS/

This package pin provides the frame and CS/ connection for the serial interface (SPI). This pin will always be an input.

### 6.2 SPI\_CLK

This package pin provides the clock connection for the serial interface (SPI). This pin will always be an input.

### 6.3 SPI\_DI

This package pin provides the data input connection for the serial interface (SPI). This pin will always be an input.

### 6.4 SPI\_DO

This package pin provides the data output connection for the serial interface (SPI). This pin will always be an output.



## 7 Registers

### 7.1 Register map

Table 6. Register map

| Address R/W | Bit | 7                     | 6        | 5                     | 4                    | 3                      | 2   | 1                    | 0   |
|-------------|-----|-----------------------|----------|-----------------------|----------------------|------------------------|-----|----------------------|-----|
| 0xC0/40     |     | -                     | -        | -                     | -                    | ----- NDIV[11:8] ----- |     |                      |     |
| 0xC1/41     |     | ----- NDIV[7:0] ----- |          |                       |                      |                        |     |                      |     |
| 0xC2/42     |     | -                     | -        | ----- RDIV[5:0] ----- |                      |                        |     |                      |     |
| 0xC3/43     |     | Reserved              |          |                       |                      | GCE                    | XCE | LSR                  | MST |
| 0xD0/50     |     | -                     | Reserved |                       |                      |                        |     |                      | IFB |
| 0xD1/51     |     | ENM                   | Reserved | AGC                   | IF                   | MIX                    | RFA | PLL                  | VCO |
| 0xD2/52     |     | -                     | -        | -                     | ----- LFC[2:0] ----- |                        |     | ----- CPI[1,0] ----- |     |
| 0xE0/60     |     | RFE                   | -        | Reserved              |                      |                        |     |                      |     |

### 7.2 PLL N divider

Table 7. PLL N divider

| Register address | Name | Bit             | Default value MODE = 0 (decimal) | Default value MODE = 1 (decimal) | Description                         |
|------------------|------|-----------------|----------------------------------|----------------------------------|-------------------------------------|
| 0x40             | NDIV | XXXX nnnn [3:0] | 96                               | 1555                             | PLL Feedback Divider Division Ratio |
| 0x41             |      | nnnn nnnn [7:0] |                                  |                                  |                                     |

### 7.3 PLL R divider

Table 8. PLL R divider

| Register address | Name | Bit             | Default value MODE = 0 (decimal) | Default value MODE = 1 (decimal) | Description                      |
|------------------|------|-----------------|----------------------------------|----------------------------------|----------------------------------|
| 0x42             | RDIV | XXrr rrrr [5:0] | 1                                | 19                               | Reference Divider Division Ratio |

Note that registers 40, 41 and 42 are delivered on a single 24 bit bus. New register values are delivered synchronously to the bus only after register 42 is written.

## 7.4 Radio configuration register

Table 9. Radio configuration register

| Register address | Name            | Bit             | Default value<br>MODE = 0 | Default value<br>MODE = 1               | Description                                      |
|------------------|-----------------|-----------------|---------------------------|---|--|
| 0x43             | MST             | XXXX XXX y [0]  | 0                         | 1                                       | <b>MST = 0</b><br>GPS_CLK output equal to Xtal   |
|                  |                 |                 |                           |   | <b>MST = 1</b><br>GPS_CLK output equal to LO96   |
|                  | LSR             | XXXX XX y X [1] | 1                         | 1                                       | <b>LSR = 0</b><br>slow slew rate mode not active |
|                  |                 |                 |                           |   | <b>LSR = 1</b><br>slow slew rate mode active     |
|                  | XCE             | XXXX X y XX [2] | 0                         | 1                                       | <b>XCE = 0</b><br>XTAL_CLK buffer is OFF         |
|                  |                 |                 |                           |   | <b>XCE = 1</b><br>XTAL_CLK buffer is ON          |
| GCE              | XXXX y XXX [3]  | 1               | 1                         | <b>GCE = 0</b><br>GPS_CLK buffer is OFF |  |
|                  |                 |                 |                           | <b>GCE = 1</b><br>GPS_CLK buffer is ON  |  |
| Reserved         | yyyy XXXX [7:4] | 0100            | 0100                      | Reserved bits                           |  |

## 7.5 Test register

Table 10. Test register

| Register address | Name             | Bit            | Default value<br>MODE = 0 | Default value<br>MODE = 1 | Description                            |
|------------------|------------------|----------------|---------------------------|---------------------------|--|
| 0x50             | IFB              | XXXX XXX y [0] | 0                         | 0                         | <b>IFB = 0</b><br>The IF Buffer is OFF |
|                  |                  |                |                           |                           | <b>IFB = 1</b><br>The IF Buffer is ON  |
| Reserved         | X yyyyyy X [6:1] | 000000         | 000000                    | Reserved bits             |  |

## 7.6 Debug register (sub-circuit enables)

Table 11. Debug register (sub-circuit enables)

| Register address  | Name     | Bit             | Default value<br>MODE = 0 | Default value<br>MODE = 1 | Description   |
|---|----------|-----------------|---------------------------|---------------------------|---|
| 0x51  | VCO      | XXXX XXX y [0]  | 1                         | 1                         | <b>VCO = 0</b><br>The VCO block is OFF  |
|   |          |                 |                           |                           | <b>VCO = 1</b><br>The VCO block is ON   |
|   | PLL      | XXXX XX y X [1] | 1                         | 1                         | <b>PLL = 0</b><br>The PLL block is OFF  |
|   |          |                 |                           |                           | <b>PLL = 1</b><br>The PLL block is ON   |
|   | RFA      | XXXX X y XX [2] | 1                         | 1                         | <b>RFA = 0</b><br>The RF Amplifier is OFF   |
|   |          |                 |                           |                           | <b>RFA = 1</b><br>The RF Amplifier is ON  |
|   | MIX      | XXXX y XXX [3]  | 1                         | 1                         | <b>MIX = 0</b><br>The Mixer is OFF  |
|   |          |                 |                           |                           | <b>MIX = 1</b><br>The Mixer is ON   |
|   | IF       | XXX y XXXX [4]  | 1                         | 1                         | <b>IF = 0</b><br>The IF chain from Polyphase filter to ADC is OFF                                   |
|   |          |                 |                           |                           | <b>IF = 1</b><br>The IF chain from Polyphase filter to ADC is ON                                    |
|   | AGC      | XX y X XXXX [5] | 1                         | 1                         | <b>AGC = 0</b><br>The Automatic Gain Control is OFF   |
|   |          |                 |                           |                           | <b>AGC = 1</b><br>The Automatic Gain Control is ON  |
|   | Reserved | X y XXXXXX [6]  | 1                         | 1                         | Reserved bits   |
|   | ENM      | y XXX XXXX [7]  | 1                         | 1                         | <b>ENM = 0</b><br>The whole chip is OFF except the Xtal Osc and the GPS_CLK and/or XTAL_CLK buffers |
| <b>ENM = 1</b><br>RF chain is On<br>(If RFE bit or RF_EN pin = 1) |          |                 |                           |                           |   |

## 7.7 Radio trimming register

Table 12. Radio trimming register

| Register address | Name | Bit              | Default value<br>MODE = 0 | Default value<br>MODE = 1 | Description                                  |
|------------------|------|------------------|---------------------------|---------------------------|--|
| 0x52             | CPI  | XXXX XX yy [1:0] | 11                        | 11                        | <b>CPI = 00</b><br>50µA charge pump current  |
|                  |      |                  |                           |                           | <b>CPI = 01</b><br>100µA charge pump current |
|                  |      |                  |                           |                           | <b>CPI = 10</b><br>150µA charge pump current |
|                  |      |                  |                           |                           | <b>CPI = 11</b><br>200µA charge pump current |
|                  | LFC  | XXXy yyXX [4:2]  | 110                       | 110                       | Loop filter control                          |

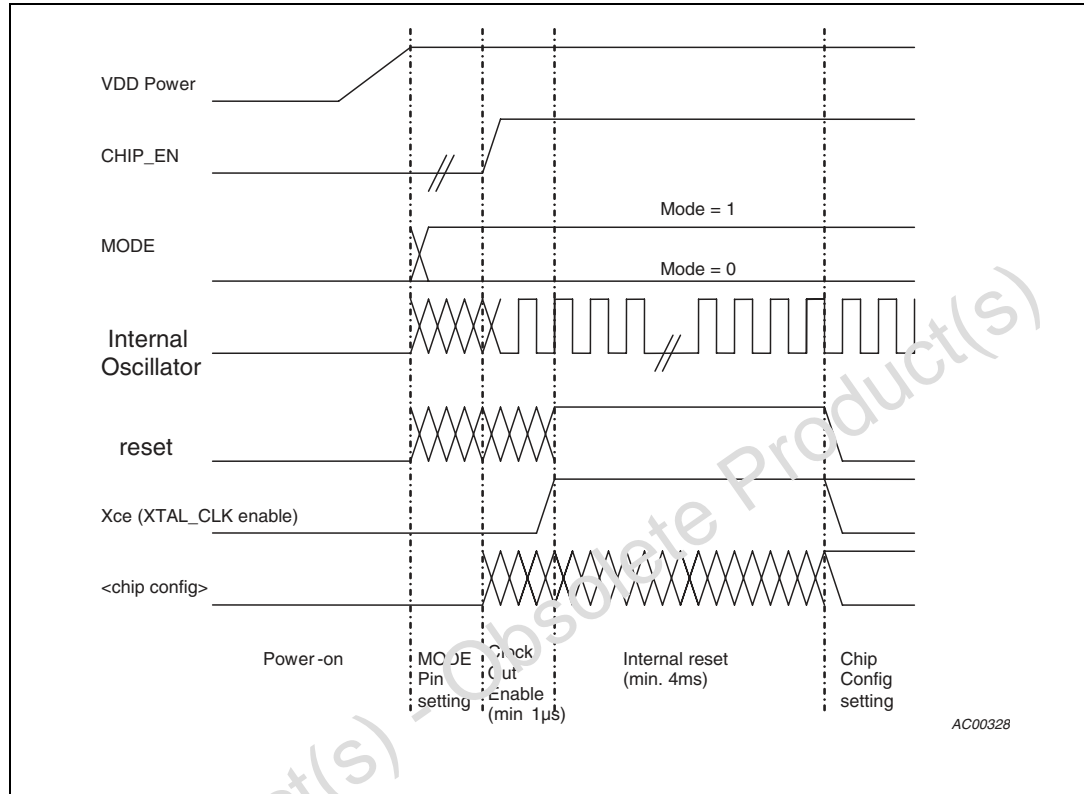
## 7.8 Receiver chain register (enable)

Table 13. Receiver chain register (enable)

| Register address | Name     | Bit             | Default value<br>MODE = 0 | Default value<br>MODE = 1 | Description   |
|------------------|----------|-----------------|---------------------------|---------------------------|---|
| 0x60             | Reserved | XX yyyyyy [5:0] | 110011                    | 110011                    | Reserved bits   |
|                  | RFE      | y XXX X'X'X [7] | 0                         | 0                         | <b>RFE = 0</b><br>The RF chain is controlled by RF_EN pin<br><b>RFE = 1</b><br>The RF chain is ON |

## 8 Chip enable and reset timing

Figure 5. Chip enable and reset timing



### 8.1 Principle of operation

With power supply applied and CHIP\_EN inactive the chip is in stand-by mode consuming just a minimal leakage current (<math><10 \mu A</math>). Applying CHIP\_EN High turns-on the chip and starts the Crystal oscillator. Two internal counters driven by the Oscillator output are used to create two timing periods to:

- The first time period (Clock Out Enable) is long enough to safely enable XTAL\_CLK as early as possible by default during oscillator startup.
- The second period (Internal reset) generates an internal reset pulse long enough to guarantee open-loop clock stabilization (driven either by internal oscillator or by off-chip TCXO) and be able to load the chip default configuration.

The default initial configurations depend on the state of the MODE input pin. After this phase, the chip configuration may be modified by the baseband unit with a set of SPI commands, allowing a more specific configuration to be set

### 8.1.1 Operating modes

The below table shows how select a particular default operating mode:

**Table 14. Operating modes**

| Operating modes                       |          | STA5620 current consumption | CHIP_EN | RF_EN | TEST_EN1 | TEST_EN2 |
|---------------------------------------|----------|-----------------------------|---------|-------|----------|----------|
| Fully operating                       | MODE = 0 | 15 mA                       | HIGH    | HIGH  | LOW      | HIGH     |
|                                       | MODE = 1 | 16 mA                       |         |       |          |          |
| RF Chain OFF<br>Crystal oscillator ON |          | 1.5 mA                      | HIGH    | LOW   | LOW      | HIGH     |
| Stand-by<br>All internal blocks OFF   |          | 1 $\mu$ A                   | LOW     | x     | LOW      | HIGH     |

HIGH = VCC\_IO; LOW = GND

#### MODE

LOW → sets the STA5620 internal dividers to work with 16.368 MHz reference and GPS\_CLK = ON and XTAL\_CLK = OFF;

HIGH → sets the STA5620 internal dividers to work with 19.2 MHz reference and GPS\_CLK = ON and XTAL\_CLK = ON;

In both cases GPS\_CLK pin provides 16.368 MHz clock to Base Band and SIGN pin provides the DATA to Base Band.

#### CHIP\_EN

LOW → the device goes to stand-by mode with very low power consumption.

HIGH → sets ON the internal blocks of the IC according to the RF\_EN status;

A logic reset of the SPI registers is generated by the low to high transitions of the CHIP\_EN pin while the RF\_EN is LOW.

#### RF\_EN

LOW → the crystal oscillator and only one output buffer are enabled, XTAL\_CLK if MODE = 1 or GPS\_CLK if MODE = 0;

HIGH → the whole chip is active and functional;

TEST\_EN1 → must be set LOW;

TEST\_EN2 → must be set HIGH (VCC\_IO);

## 8.2 Default configuration

This table describes the default configuration of the STA5620 internal registers.

**Table 15. Default configuration**

| Bit name                          | Description   | Values  | (MODE_EN=0) | (MODE_EN=1) |
|-----------------------------------|---|---|-------------|-------------|
| <b>Sample mode configuration</b>  |   |   |             |             |
| MST                               | Sample clock Source Selector                              | 0 = Xtal Osc<br>1 = VCO/96,   | 0           | 1           |
|                                   | Default xtal/TCXO frequency                               |   | 16.368 MHz  | 19.200 MHz  |
| <b>Power enable configuration</b> |   |   |             |             |
| ENM                               | RF Chain Enable<br>(From the RFA Input to the AGC Output) | 0 = RF chain OFF,<br>1 = RF chain On<br>If RFE bit or RF_EN pin = 1 | 1           | 1           |
| RFE                               | RF Chain Enable<br>(From the RFA Input to the AGC Output) | 0 = controlled by RF_EN pin,<br>1 = RF chain On                     | 0           | 0           |
| GCE                               | GPS Clock Enable  | 0 = GPS clock Off,<br>1 = GPS clock On                              | 1           | 1           |
| AGC                               | Automatic Control Gain Enable                             | 0 = AGC function Off,<br>1 = AGC function On                        | 1           | 1           |
| XCE                               | Xtal Clock Enable   | 0 = Off,<br>1 = On  | 0           | 1           |
| IFB                               | IF Output Buffer Enable                                   | 0 = Off,<br>1 = On  | 0           | 0           |
| VCO                               | Voltage Controlled Oscillator Enable                      | 0 = Off,<br>1 = On  | 1           | 1           |
| IF                                | IF enable   | 0 = Off,<br>1 = On  | 1           | 1           |
| MIX                               | Mixer enable  | 0 = Off,<br>1 = On  | 1           | 1           |
| RFA                               | RF Amplifier enable                                       | 0 = Off,<br>1 = On  | 1           | 1           |
| PLL                               | Phase Locked Loop Enable<br>(Dividers, PFD, Charge Pump). | 0 = Off,<br>1 = On  | 1           | 1           |

**Table 15. Default configuration (continued)**

| Bit name                            | Description   | Values  | (MODE_EN=0) | (MODE_EN=1) |
|-------------------------------------|---|---|-------------|-------------|
| <b>Divider configuration</b>        |   |   |             |             |
| NDIV[11:0]                          | PLL Feedback Divider Division Ratio<br>(mapped as 2 byte registers)                               | 56 to 4095  | 96          | 1555        |
| RDIV[5:0]                           | Reference Divider Division Ratio<br>(write of this register updates all of the ndiv, rdiv vector) | 1 to 63   | 1           | 19          |
| <b>Charge pump current selector</b> |   |   |             |             |
| CPI[1:0]                            | Charge Pump Current Selector  | 00 = 50 $\mu$ A<br>01 = 100 $\mu$ A<br>10 = 150 $\mu$ A<br>11 = 200 $\mu$ A | 11          | 11          |
| <b>Output slew rate control</b>     |   |   |             |             |
| LSR                                 | XTAL_CLK, GPS_CLK, TEST_CLK, SPI_DO, SIGN and MAG Output Drivers Slew Rate                        | 0 = Fast<br>1 = Slow  | 1           | 1           |

*Note: Disabling a digital output buffer means driving it low.*

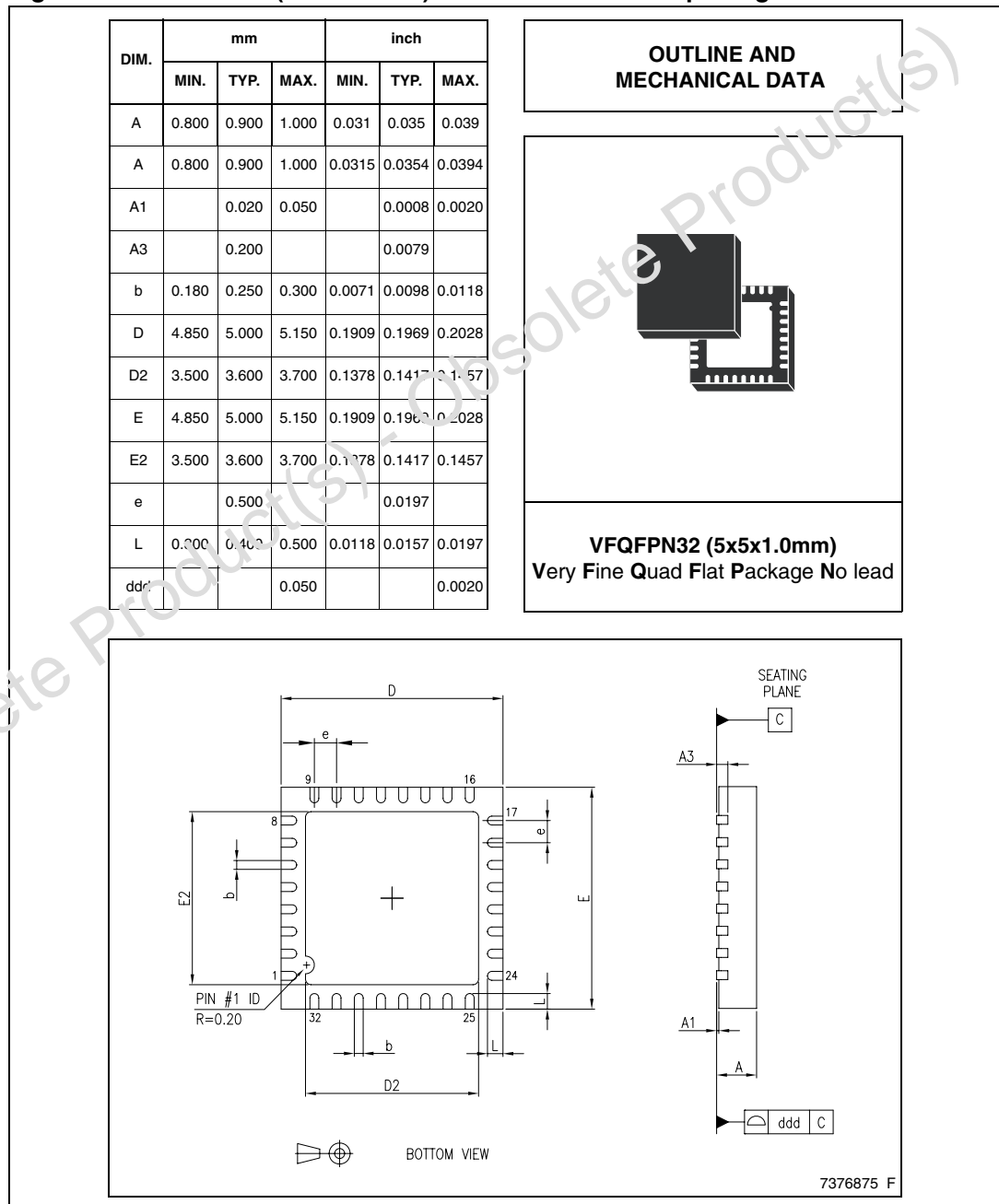


## 9 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 6. VFQFPN32 (5x5x1.0 mm) mechanical data and package dimensions**



# 10 Packing information

Figure 7. Reel, leader and trailer dimensions

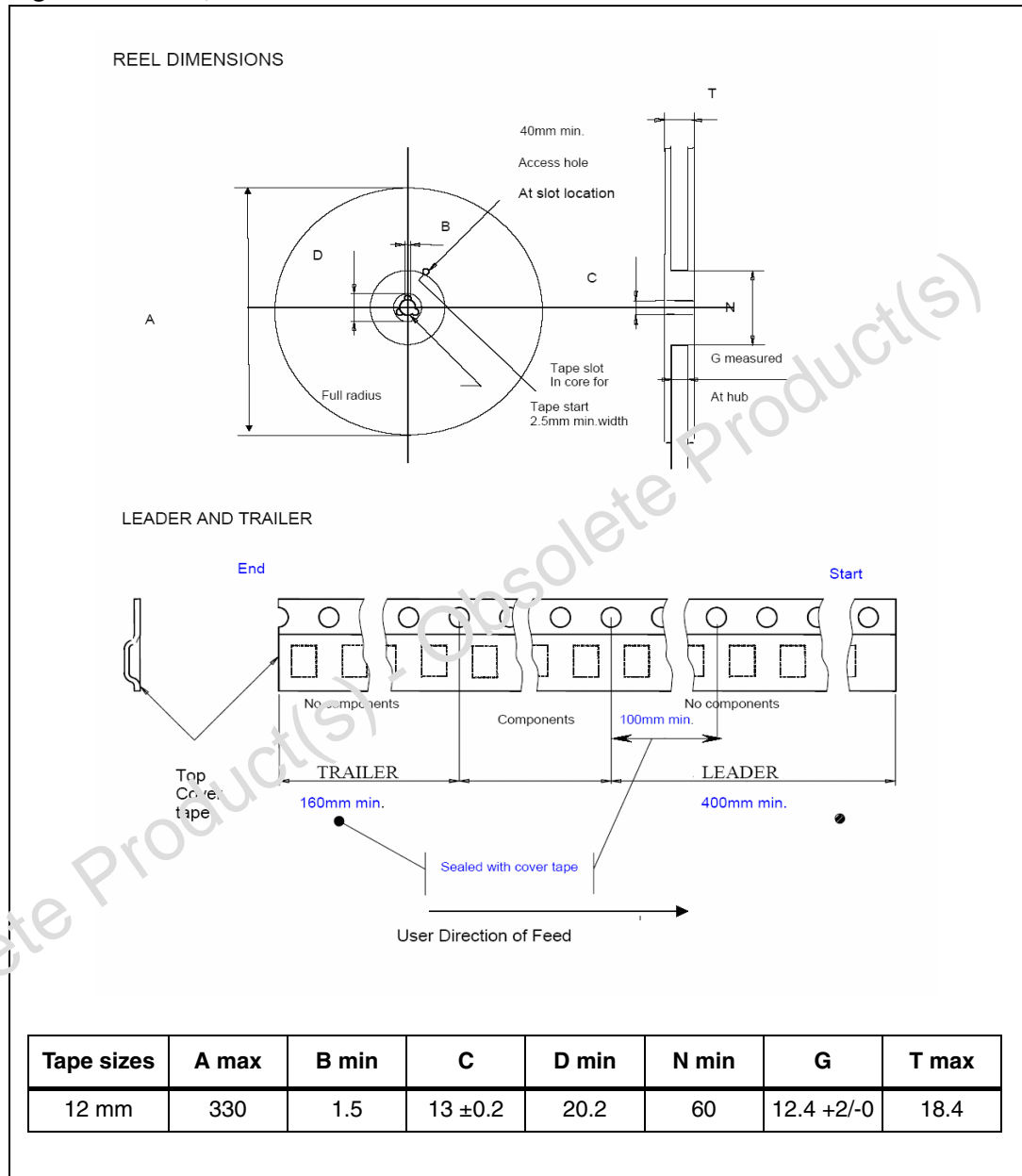


Figure 8. Carrier tape requirements

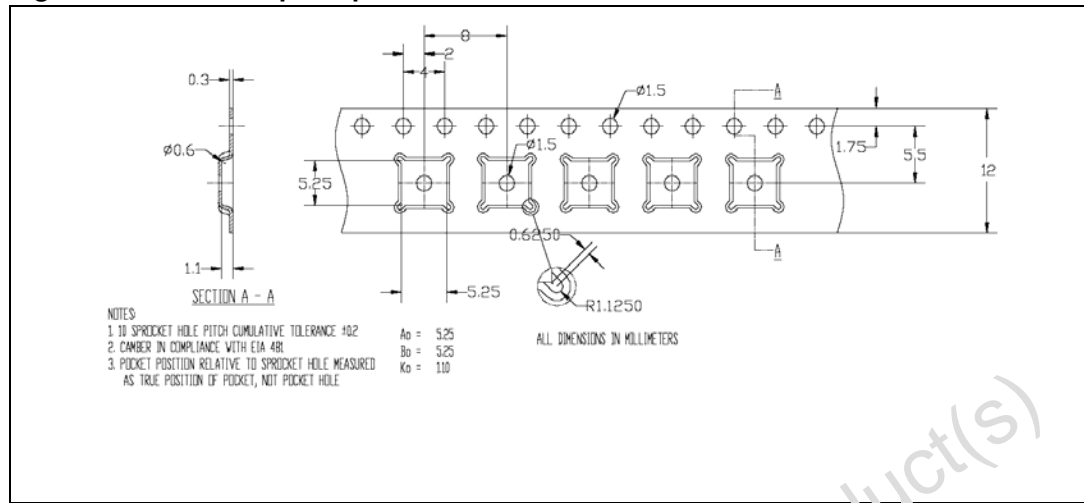
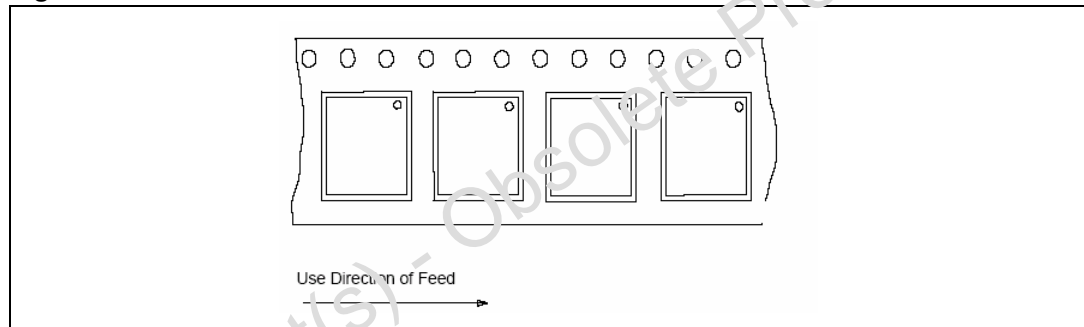


Figure 9. Orientation



## 11 Revision history

**Table 16. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 24-Jul-2007 | 1        | Initial release.   |
| 15-Nov-2007 | 2        | Modified the tables <a href="#">7</a> , <a href="#">8</a> , <a href="#">10</a> , <a href="#">12</a> and <a href="#">13</a> .<br>Updated <a href="#">Figure 3</a> and <a href="#">4</a> . |
| 14-Jan-2008 | 3        | Updated the following tables: <a href="#">9</a> , <a href="#">10</a> , <a href="#">11</a> and <a href="#">13</a> .<br>Updated the <a href="#">Figure 3 on page 16</a> .                  |
| 18-Feb-2008 | 4        | Document status promoted from preliminary data to datasheet.<br>Updated the <a href="#">Section 3.4: A/D converter</a> .   |

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