User's Guide
SLUUBX2B–October 2018–Revised June 2020

UCC217XX Family Driving and Protecting SiC and IGBT Power Modules and Transistors

This User's Guide describes the characteristics, operation and use of the UCC21732QDWEVM-025 Evaluation Module (EVM). This TI EVM provides driving and protection for popular Silicon Carbide (SiC) MOSFETs and Si IGBTs both in discrete and Power Module implementations. The EVM is using feature rich isolated driver device UCC21732 that is part of family of UCC217XX drivers. A complete schematic diagram, printed-circuit board layouts, and bill of materials are included in this document.

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1 Overview

The UCC217XXQDWEVM-025 is a compact, single channel isolated gate driver board providing drive, bias voltages, protection and monitoring needed for SiC MOSFET and Si IGBT Power Modules housed in 150 x 62 x 17 mm and 106 x 62 x 30 mm packages. The board can be used with the UCC21710, UCC21732, UCC21750, or UCC21736 drivers of the UCC217XX family. This TI EVM is based on 5.7-kVrms reinforced isolation drivers UCC217XX in SOIC-16DW package with 8.0 mm creepage and clearance. The EVM includes SN6505B based isolated DC-DC transformer bias supplies. Isolated temperature and input rail monitoring is provided using analog sensor and PWM output integrated into UCC217XX. Compact form factor 62 x 48 x 6.6 mm allows direct connection of two boards to drive and protect standard half-bridge modules with up to 1700 V rail.

1.1 Features

- 10-A peak split sink/source drive current for fast turn ON and turn OFF time
- 2-W bias supply with UVLO and OVLO protection set by default at 4.5 V to 5.5 V
- Drive voltages by default are 17/-5 V with single 5-V input supply
- Drive voltages can be also programmed independently from 11 V to 19 V for turn ON and from -3.3 V to -6 V for turn OFF by using two input supplies from 3.3 V to 5.5 V
- Noise-immune design with CMTI >150 V/ns
- 5.7-kVrms reinforced isolation
- OC short-circuit shunt resistor sensing with two-level (UCC21732) or single level (UCC21710) soft turn-OFF protection
- OC signal setting either for positive or negative polarity
- Desat short-circuit sensing for UCC21750
- Active Miller clamp using external FET (UCC21732) or internal (UCC21710)
- Output short circuit clamp
- Fault feedback with reset
- Isolated temperature and input rail monitoring

1.2 Applications

- Solar inverters
- Motor drives
- HEV/EV chargers
- HEV/EV traction Inverters

1.3 Description

1.3.1 Specification

High voltage SiC and IGBT power modules in the popular 150-mm and 106-mm packages are the building blocks of various power systems at power levels up to megawatts. Recently, wide bandgap SiC FET based power modules are introduced in power electronics instead of Si IGBT because of their excellent conduction and switching performance. Compact driver board UCC21732QDWEVM-025 supports SiC modules by reducing parasitics, minimizing switching loss, EMI and providing full required protection and diagnostics features. Electrical parameters of the board are shown in Table 1.

Table 1. Electrical Specifications

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS						
VCC	Primary supply voltage		4.5	5.0	5.5	V
IVCCQ	Primary quiescent current	IN+, IN- low		5		mA
IVCCS	Primary supply current	FSW = 10kHz, CLOAD = 10nF		50		mA
VCCUR	Vcc rising UVLO threshold			4.5	4.6	V
VCCUF	Vcc falling UVLO threshold		4.2	4.3		V
VCCUH	Vcc UVLO hysteresis			0.2		V
VCCOR	Vcc rising OVLO threshold			5.7	5.8	V
VCCOF	Vcc falling OVLO threshold		5.4	5.5		V
VCCOH	Vcc UVLO hysteresis			0.2		V
VCC2U, VCC2L	Drive voltages	Transformer 750342879	15	17	19	V
VCC2U, VCC2L	Drive voltages	Transformer 750313734	-5.9	-5	-4.7	V
DRIVE CURRENT AND POWER						
IOH	Peak source current	CLOAD = 10nF		10		A
IOL	Peak sink current	CLOAD = 10nF		10		A
PDRV	Drive power	At 25ºC			2.0	W
INPUT/OUTPUT SIGNALS						
VINR, VRSTR	IN+, IN-, RST/EN rising threshold				0.7 x VCC	V
VINF, VRSTF	IN+, IN-, RST/EN falling threshold		0.3 x VCC			V
VINH, VRSTH	INL+, INU+, RST hysteresis			0.1 x VCC		V
TIMING PARAMETERS						
TRISE	Drive output rise time	CLOAD = 10 nF, Rg = 0.4 Ω		27		ns
TFALL	Drive output fall time	CLOAD = 10 nF, Rg = 0.4 Ω		21		ns
TPROP	Propagation delay	CLOAD = 100 pF		90		ns
TGLITCH	Input glitch filter		28	40		ns
SHORT CIRCUIT PROTECTION						
VOC	Nominal overcurrent threshold		0.63	0.7	0.77	V
TDEGLITCH	Blanking time			150		ns
TSR90	Response time to 90% VDR	CLOAD = 10nF		200		ns
V2LOFF	2LOFF voltage			11.0		V
T2LOFF	2LOFF voltage time			2.5		µs
ITL3	Soft turn OFF pull down current			100		mA
VCLAMP	Miller clamp threshold		1.5	2.0	2.5	V
ICLAMP	Miller clamp current			4		A

Table 1. Electrical Specifications (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ISOLATION						
CMTI		CMTI	150			V/ns
VISO	Withstand isolation voltage	Reinforced, 60s	5.7			kVrms
CIO	Barrier capacitance				20	pF
TA	Operating Ambient Temperature		-40	25	125	°C
SIZE						
Board size					62 x 48 x 6.6	mm

1.3.2 Block Diagram

The block diagram shown in Figure 1 details the UCC217XXQDWEVM-025 EVM. The EVM core is an isolated driver device, UCC217XX, providing optimal drive protection and diagnostic of IGBT and SiC power devices. The isolated drive and control voltages on the secondary side are provided by push-pull transformer drivers SN6505B supplied by a 5-V power source on primary side. The EVM provides either temperature, or input voltage bus monitoring using analog an isolated channel available from UCC217XX. There is also board level logic block providing diagnostic and overlapping protection when two EVMs operate together to drive the FETs in half-bridge power stage configurations. The input and output signals and voltages are provided through miniature 2 x 10 connector. The EVM also includes numerous test points and 2 x 6 header to allow access to key signals during evaluation.

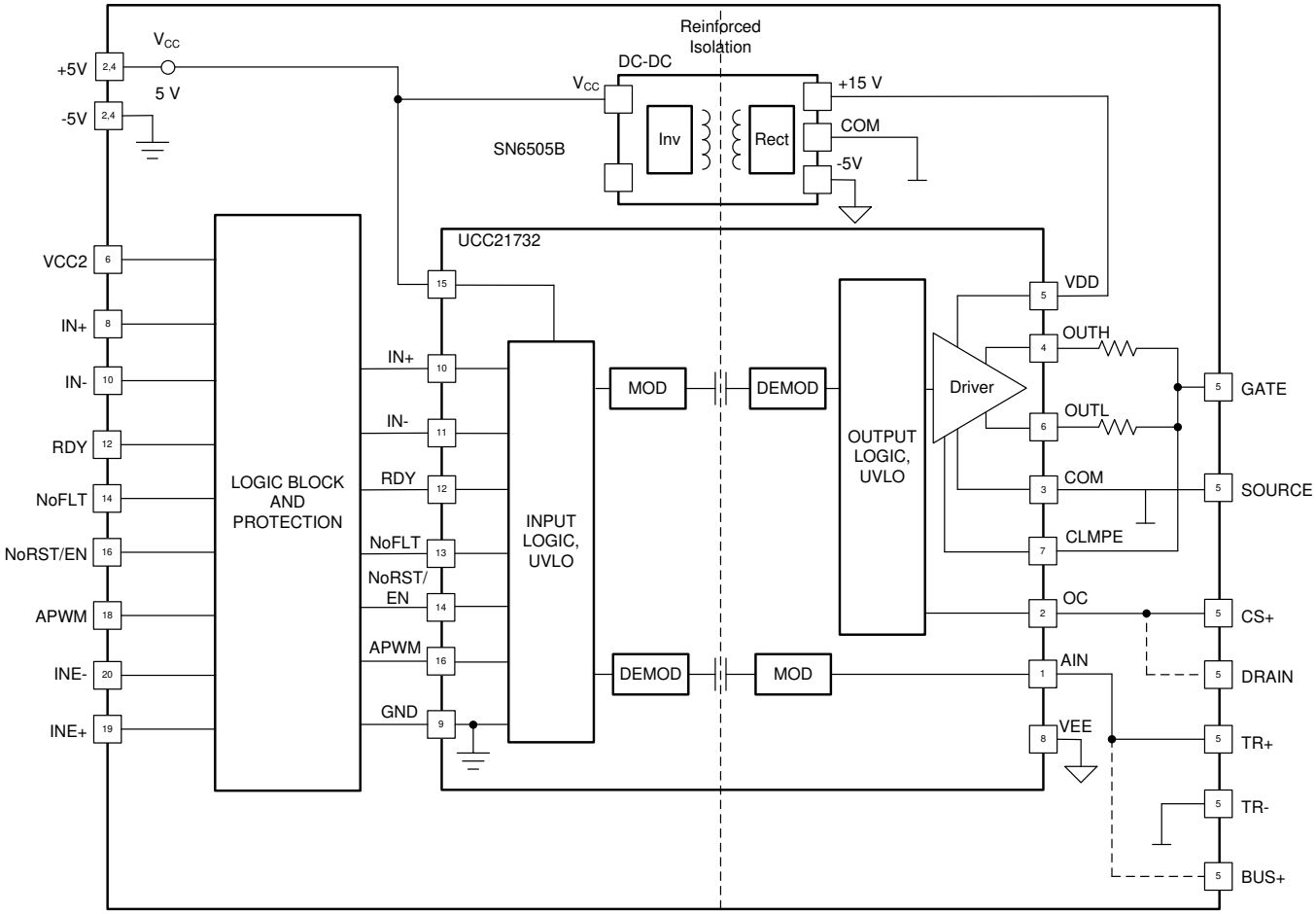


Figure 1. UCC21732QDWEVM-025 Block Diagram

The UCC217XXQDWEVM-025 EVM includes the following key functional blocks shown in schematic in Figure 2.

1. B1: Split rail bias supply using 424 kHz transformer drivers SN6505B to generate separately +17-V rail for turn ON and –5-V rail for turn OFF
2. B2: Input diagnostic, protection and logic block
3. B3: 10-A source/sink 5.0-kVrms Isolated driver using UCC217XX driver device with short circuit protection and Miller clamp circuits
4. B4: Isolated temperature or input voltage rail monitoring block
5. B4 (UCC21736-Q1): Active Short Circuit input

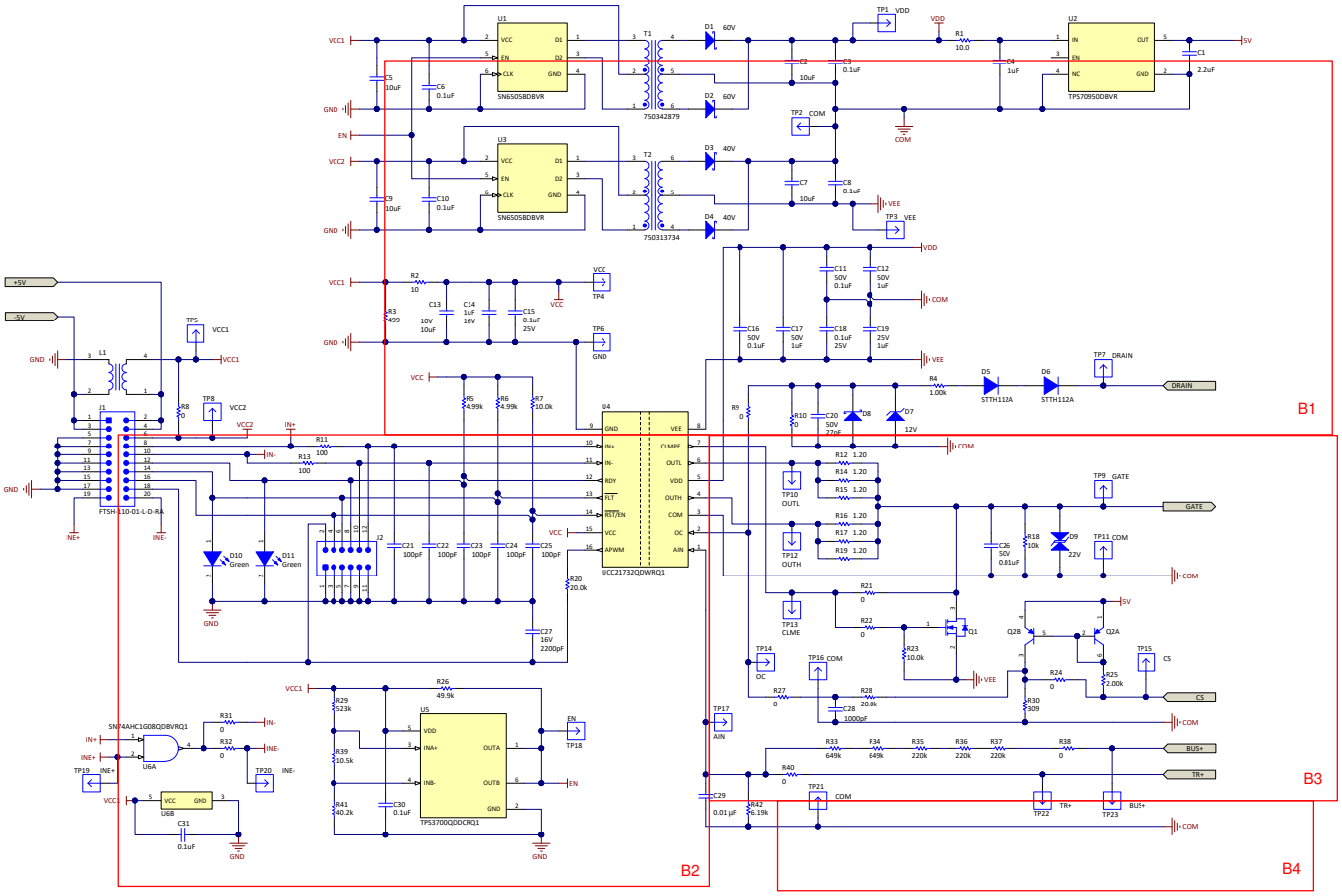


Figure 2. UCC21732QDWEVM-025 Functional Blocks

The location of key functional blocks on the board view are shown in Figure 3.

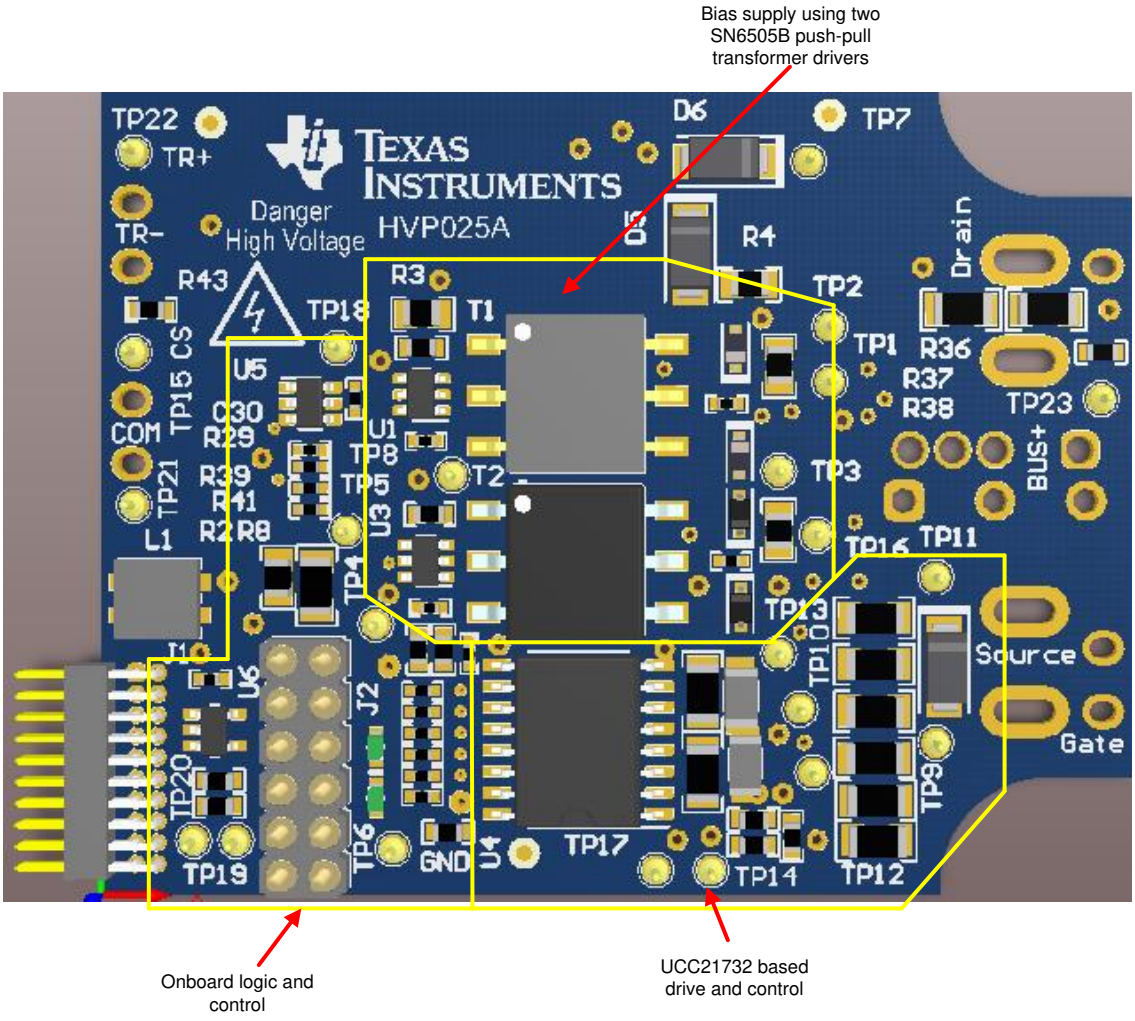


Figure 3. Location of Key Functional Blocks on Board View

1.3.3 Isolated Gate Driver Family UCC217XX

The UCC217XX family of isolated drivers in SOIC-16 DW package with 8.0-mm creepage and clearance providing 5.7-kVrms reinforced isolation, includes all main short circuit protection features for driving SiC and IGBT modules along with discrete power transistors. The UCC217XX family employs TI proprietary high voltage, low propagation delay, CMTI immune capacitive isolation technology. The list of isolation safety certifications from agencies like VDE, CSA, UL and CQC is provided in related datasheet. Table 2 lists UCC217XX family members UCC21710, UCC21732, UCC21750 and their differences, while related block diagrams are shown in Figure 4.

UCC21736-Q1, not shown in the block diagrams below, can be placed on the UCC21732 EVM for evaluation. This device replaces AIN with ASC.

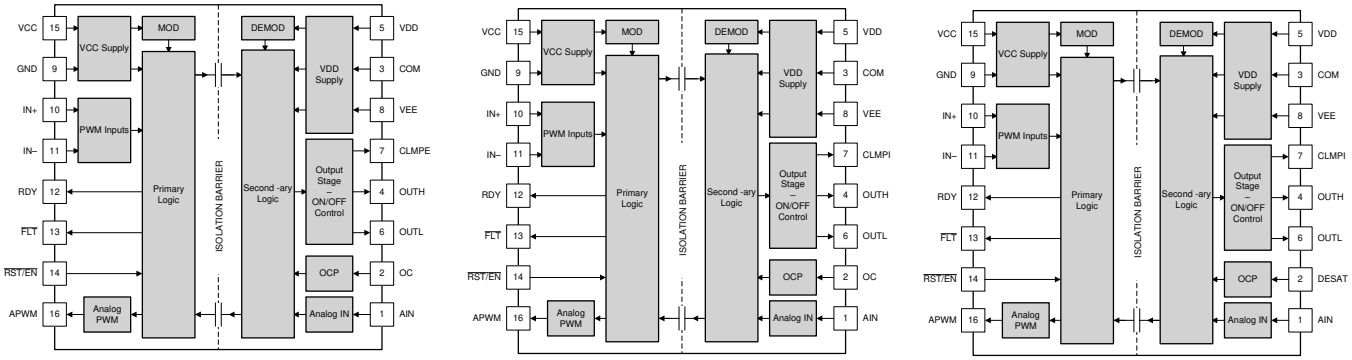


Figure 4. Simplified Block Diagrams of the UCC21732, UCC21710 and UCC21750

Table 2. UCC217XX Isolated Driver Family

DEVICE OPTIONS	AIN-APWM	±PEAK IO	OC/DESAT	MILLER CLAMP	FLT SHUTDOWN	OUTPUT
UCC21710	YES	10 A	OC	Internal	Int. Soft OFF	Split
UCC21732	YES	10 A	OC	External	2-level Int. Soft OFF	Split
UCC21750	YES	10 A	DESAT	Internal	Int. Soft OFF	Split
UCC21736	No (ASC Function)	10 A	OC	External	2-level Int. Soft OFF	Split

The UCC217XX family demonstrates short and accurate 90-ns propagation delay allowing accurate control of power devices. Primary side voltage VCC is controlled by UVLO1 circuit with 2.95 Vmax rising threshold and 2.5 Vtyp falling threshold. Inverting and non-inverting input signals IN+ and IN- have CMOS thresholds derived from Vcc voltage: 0.7 x VCC max rising and 0.3 x VCC min falling accordingly. Secondary side voltage VDD can go up to 36 Vabs. max. Turn ON drive voltage between VDD and COM pins is controlled by UVLO2 circuit with 12.8 Vmax rising threshold and 10.4 Vmin falling threshold. The split sink/source ±10-A output allows setting optimal turn ON and turn OFF time by selecting gate resistors between driver output and power device. This family has all necessary short circuit protection features using OC current sensing with 0.7-V tripping threshold and either, soft two-level short circuit turn OFF with external Miller gate clamp, like UCC21732, or single level soft turn OFF with internal Miller clamp, like UCC21710 or DESAT Vds sensing method used in UCC21750. All family provides “Fault”, “Power Ready” and accepts “Reset/Enable” signals.

1.3.4 Split Rail Bias Supply using SN6505B

Split rail bias supply generates 17 V turn ON, and -5V turn OFF voltages using two push-pull transformer drivers SN6505B operating at 424kHz and housed in 6-pin small SOT-23 package. Functional block diagram of SN6505B is shown in Figure 5.

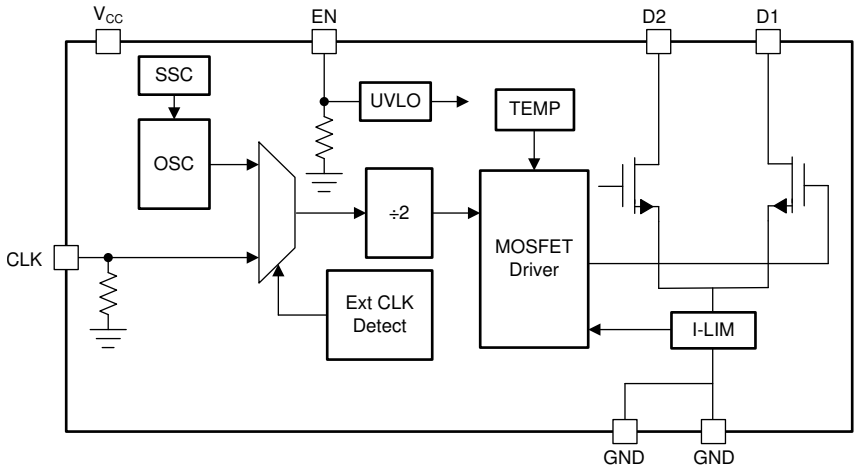


Figure 5. SN6505B Block Diagram

The SN6505B is supplied through Vcc terminal from external source in the range from 2.25 to 5.5V. Input voltage is controlled by UVLO circuit having rising threshold 2.25Vmax and falling threshold 1.7V min. Internal oscillator operates at 424kHz typical frequency within range from 363 kHz min. to 517 kHz max. It can be synchronized by external logic level clock signal from 100 kHz min to 1600 kHz max. The SN6505 employs spread spectrum clocking technique to minimize EMI. The output stage includes 1A push-pull switches rated up to 16 V abs. max. The switches are protected by current limit circuit tripped at 1.7 A typ. level. The device also protected by thermal shutdown circuit triggered at 168°C typical threshold and returning back to normal operation at 150°C typical. Additional features include soft start and Enable signal. Because there is no closed feedback loop in this inexpensive bias solution, it operates like DC-DC transformer and requires low tolerance primary voltage to maintain output voltages within ±10% range.

1.3.5 Input Diagnostics, Protection and Logic Block

Input diagnostic, protection and logic block fulfills the following functions:

1. Provides additional UVLO and OVLO protection of secondary side drive voltages using sensing on primary side. This approach is accurate enough because the bias supply operates as DC-DC transformer. This UVLO/OVLO circuit is based on window comparator TPS3700
2. Provides optional overlapping protection for two boards driving half-bridge power module using CMOS logic AND SN74AHC1G08QDBVRQ1
3. Provides isolated filtered signal using APWM output coming from temperature or input rail monitoring circuits using AIN input

1.3.6 Output Protection and Diagnostics

The output protection and diagnostic blocks fulfill the following functions:

1. Determine short circuit conditions using OC shunt resistor sensing programmable for either positive, or negative OC signal when using UCC21732 or UCC21710, and DESAT detection when using UCC21750
2. Analog isolated sensing APWM signal using AIN input for either temperature monitoring using thermistor inside the module, or input rail sensing
3. Includes external active Miller clamp circuit

In the case of UCC21736-Q1 placed on the UCC12732 EVM, AIN is now replaced with the ASC function. ASC or Active Short Circuit is used in three phase motor drive applications to re-direct short current through the phases in order to avoid over-voltage at the battery input. ASC, when pulled high, will force the UCC21736-Q1 output high. ASC takes precedence over a VCC UVLO fault. However, OC detection and VDD UVLO will take precedence over ASC. APWM output on the primary side is used to monitor the status of the ASC pin. The EVM configuration for UCC21736-Q1 is given in Section 3.1.

Either OC detection or DESAT detection may be used with this EVM. For positive OC detection, a shunt resistor is connected between the CS pin and COM, where the voltage across R_{SHUNT} is the over-current threshold, I_{OC}, times R_{SHUNT}. The OC pin detection threshold voltage is 0.7 V.

Negative OC detection is used in cases where the IGBT or SiC MOSFET has a split emitter. In this case, the Kelvin Emitter/Source must be connected to COM of UCC21732 and the current sense OC pin is connected to the power Emitter/Source path, so the measured current is negative. The shunt resistor value, R_{SHUNT}, must correspond to the voltage across R30, which is connected to the OC pin. When the desired OC detection current, I_{OC}, is reached then the voltage across R30 should be 0.7V. The voltage across the shunt resistor is given in Equation 1, where I_{OC} is negative.

$$V_{Shunt} = I_{OC} * R_{Shunt} \tag{1}$$

The value of R_{Shunt} must be designed so that the voltage at the OC pin, V_{OC}, is 0.7 V.

$$V_{OC} = 0.7V = \frac{R30 * (5 - I_{OC} * R_{Shunt} - V_{BE})}{R25} \tag{2}$$

R30 is 309 Ω, R25 is 2 kΩ, V_{BE} is the BJT base to emitter voltage estimated as 0.7 V, and I_{OC} is the over current threshold and is a negative value.

This equation is rearranged to find R_{Shunt} in Equation 3:

$$R_{Shunt} = \frac{0.7 * (R25 / R30) - 5 + V_{BE}}{-I_{OC}} \tag{3}$$

The current through R30 is found using V_{Shunt} in Equation 4.

$$I_{R25} = \frac{(5 - V_{Shunt} - V_{BE})}{R25} = I_{R30} \tag{4}$$

The voltage across R30 is then found using Equation 5, and is equal to the OC detection threshold voltage.

$$V_{OC} = 0.7 = I_{R30} * R30 \tag{5}$$

Finally, when using DESAT detection with UCC21750, the resistor R27 and R10 are not populated and R9 is populated. The DESAT threshold is 9 V, where 9 V corresponds to the saturation voltage of the IGBT or SiC MOSFET during a short circuit event. The blanking time is set by C20 in order to prevent false triggering while the power device is turning on.

2 Quick Initial Evaluation

Quick initial evaluation is starting point before using the board to drive power modules as part of power system.To start evaluation, nominal 5V is applied through terminals J1:2,4 (positive) and J1:1,3(GND). Input signal IN+ not exceeding VCC level is applied through J1:8 terminal. The 5-V VCC voltage generates +17 V turn ON drive voltage and -5.3 V turn OFF voltage on secondary side. The switching frequency range is limited by maximum power dissipated on board and should not exceed 2 W at room temperature if no forced cooling is available. Thus, if the supply current exceeds 400 mA, the IN+ signal must be stopped by bringing it to low level and supply power source turned OFF.

By default the EVM includes capacitive load C26 for drive switching waveforms evaluation, but it also has footprints for standard TO-247 package and for 4-pin package with separate source terminal available for SiC FETs. When evaluating with power device, the capacitor C26 has to be removed.

2.1 Equipment

Below is the list of needed equipment

- Power Supplies
  - At least up to 6-V and 1-A two power supplies for powering EVM, for example: BK Precision, series 1715
- Function Generator and accessories
  - One 2-channel function generator, for example: Tektronix AFG3102

  - Two standard 50-Ω BNC coaxial cables
  - Two 50-Ω BNC male to female feed-thru terminators, for example: Tektronix 011-0049-02
- Oscilloscope and accessories
  - Oscilloscope 500-MHz or higher with at least 4 channels, for example: Tektronix DPO7104
  - At least 500-MHz bandwidth four passive voltage probes, for example: P6139A
- Digital Multi-Meters
  - Four DMMs, for example Fluke 187
- Other
  - Connection wires of various length with Pomona clips and connectors

2.2 Test Setups and Procedures

List of initial tests include:

- Power up and bias supply voltages test
- Input and output pulse switching waveforms test
- Overcurrent and two-level soft turn OFF test
- Isolated analog input/output test

NOTE: Before start testing make sure to follow all electrical safety and ESD protection requirements implemented at your company!

2.2.1 Power Up and Bias Supply Voltages Test

Test setup is shown in Figure 6. Additionally, connect TP15 to TP21.

Figure 6. Power Up and Bias Supply Voltages Test Setup

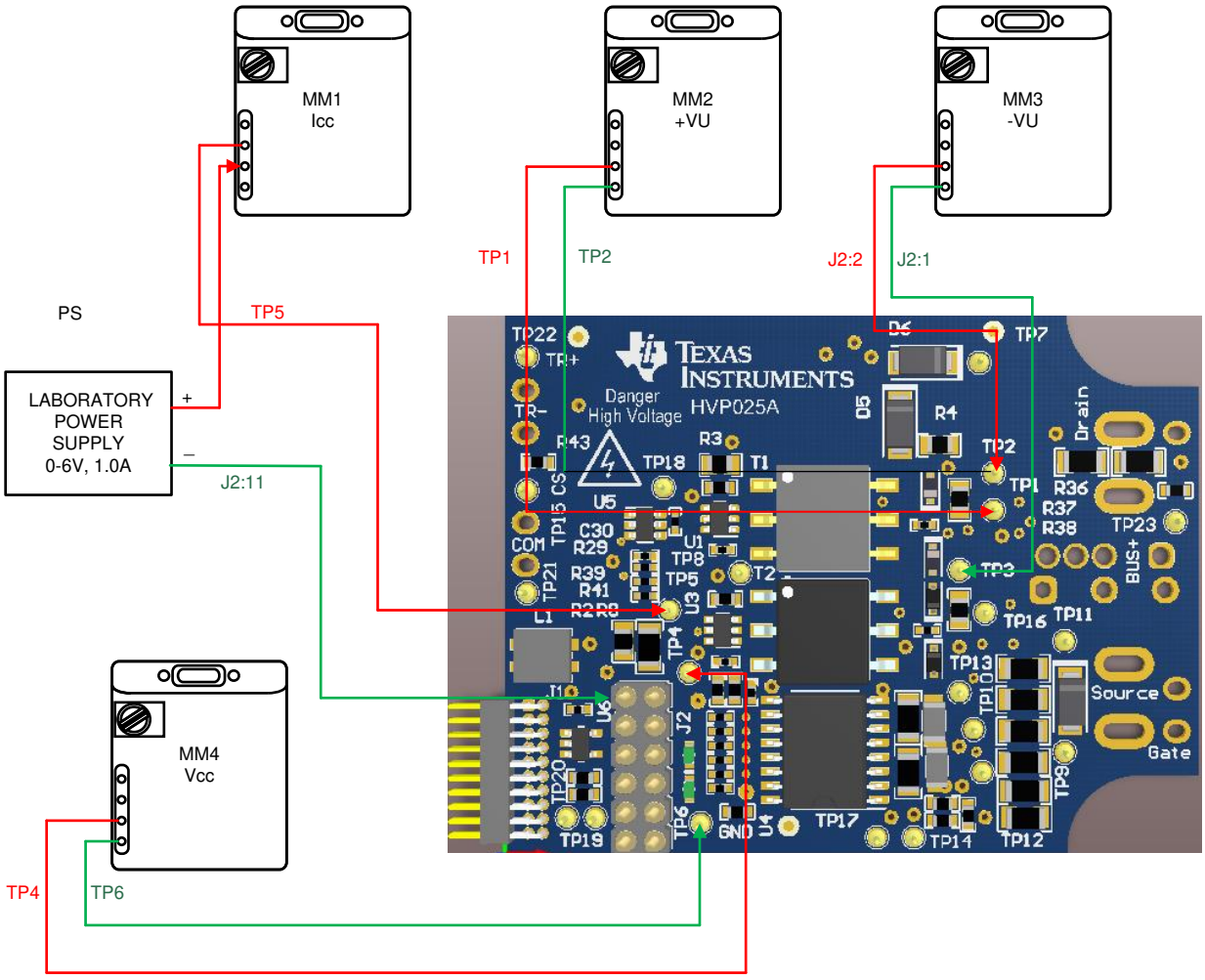


Figure 7.

Because of small size of EVM board it must be fixed on bench area using either standard clamp, or simply the sticking isolation tape.

Digital Multi-meter settings

MM2, MM3, MM4 are set for DC voltage measurements, auto-range.

MM1 is set for DC current measurements with expected range up to 500 mA

The following is power up and bias supply voltages test procedure.

1. Enable power supply PS
2. Gradually increase the voltage at PS and monitor voltage using MM4 and current using MM1
3. Verify measured voltage and current in accordance to Table 3. If current or voltage is outside of the specified range, stop increasing the voltage at PS and return to initial stage
4. Gradually reduce the voltage at PS1 to 0 V and disable it

Table 3. Voltages and Currents During Power Up Test

MM4	MM1	MM2	MM3	LED D10 (NoFLT)	LED D11 (RDY)
2.95 V-3.05 V	<4 mA	<±0.1 V	<±0.1 V	Starts illuminating	Dark
4.65 V-4.75 V	35 mA-72 mA	15.7 V-16.7 V	4.5 V-5.2 V	Light	Light
4.95 V-5.05 V	38 mA-75 mA	16.8 V-17.7 V	5.0 V-5.6 V	Light	Light

Table 3. Voltages and Currents During Power Up Test (continued)

MM4	MM1	MM2	MM3	LED D10 (NoFLT)	LED D11 (RDY)
5.4 V-5.45 V	40 mA-77 mA	17.7 V-19.2 V	5.5 V-6.2 V	Light	Light
>5.7 V,but <6 V	<6 mA	<±0.1 V	<±0.1 V	Light	Dark

2.2.2 Input and Output Switching Waveforms Test

Test setup for input and output switching waveforms is shown in Figure 8. The EVM by default includes 10-nF load capacitor C26. Connect TP7 to SOURCE terminal for UCC21750 only.

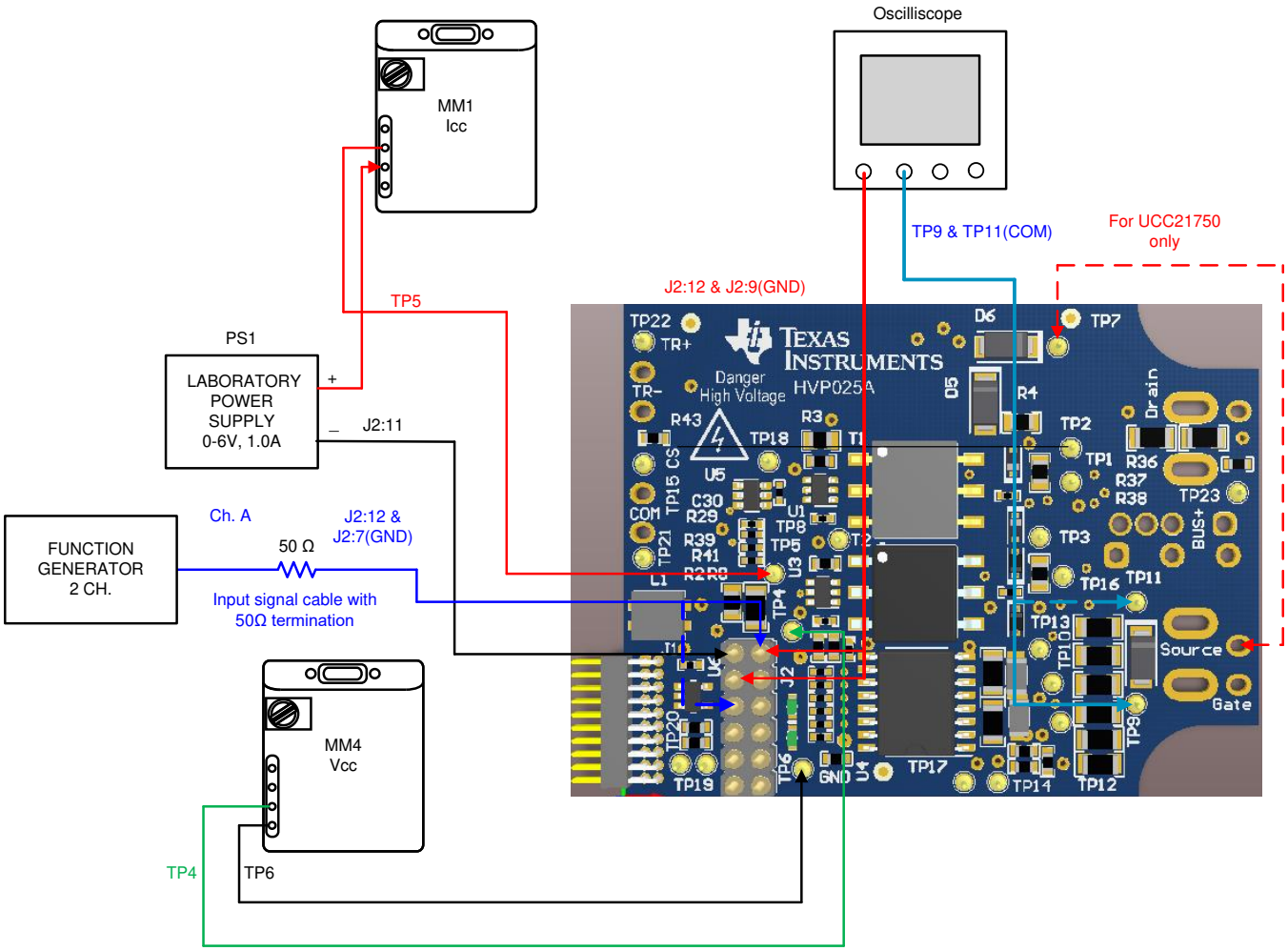


Figure 8. Input and Output Switching Waveforms Test Setup

Function generator settings are shown in Table 4.

Table 4. Function Generator Settings

CHANNEL	MODE	FREQ.	WIDTH	DELAY	AMPL.	OFFSET	LOAD IMPED.
A (Ch.1)	Pulse	10 kHz	50 µs	0	4 Vpp	2.0 V	50 Ω

Oscilloscope settings are shown in Table 5. See also waveforms and settings in .

Table 5. Oscilloscope Settings

CHANNEL	VERTICAL SCALE	HORIZONTAL SCALE	BANDWIDTH	COUPL.	TERMINATION	SYNC.	RESOLUTION
Ch. 1(yellow)	3 V/div	20 µs/div	500 MHz or above	DC	1 MΩ	Ch. 1	High
Ch. 2(blue)	10 V/div						

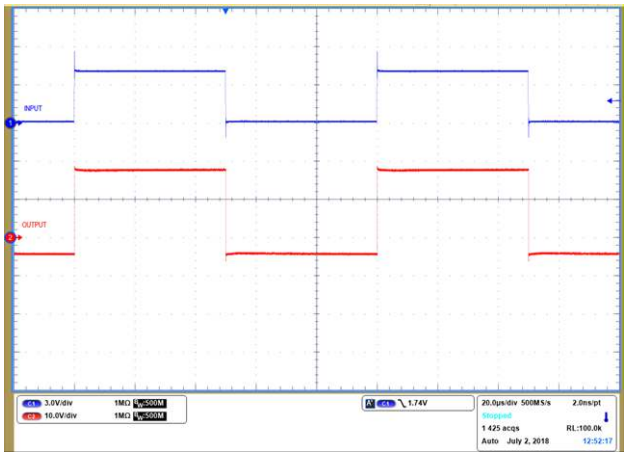


Figure 9. Input and Output Switching Waveforms with C_{LOAD} = 10 nF

The following is input and output switching waveforms test procedure.

1. Enable power supply PS
2. Gradually increase the voltage at PS into 4.95 V to 5.05 V range and monitor current using MM1 that should not exceed 75 mA
3. Enable channel A (ch.1) of function generator
4. Monitor current increase at MM1 but does not exceed 90 mA
5. Compare waveforms with typical screen shot shown in Figure 9
6. Disable function generator channels
7. Gradually reduce voltage at PS down to 0 and disable it (Make sure function generator outputs are disabled before this action!)

2.2.3 Overcurrent and Short Circuit Soft Turn OFF Test

The test setup is shown in Figure 10. For UCC21750 there is no need to connect channel B (Ch.2) of function generator. The hardware settings for using either OC detection or DESAT detection for the versions of UCC217xx are shown in Section 3.1.

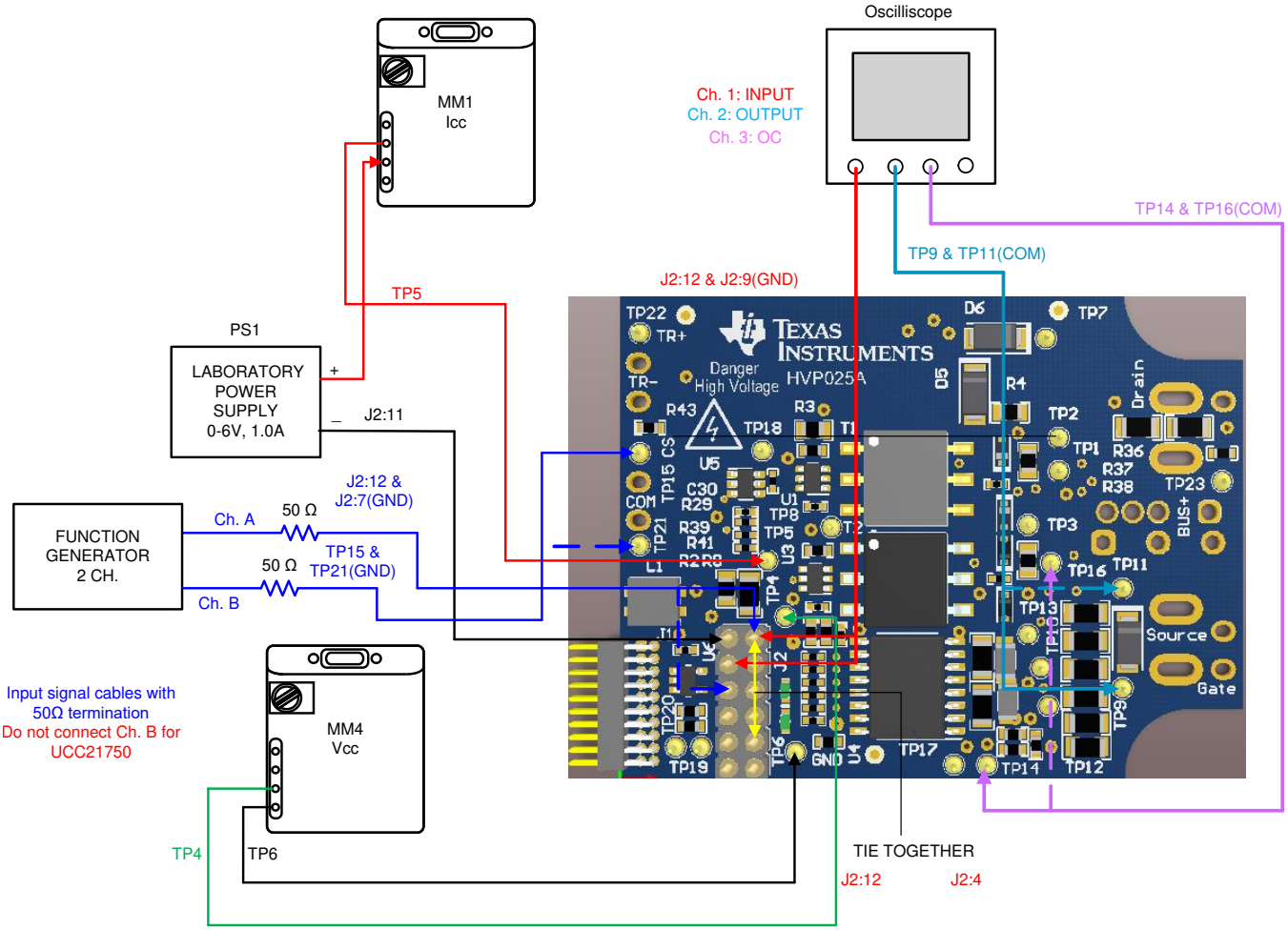


Figure 10. Overcurrent and Short Circuit Test Setup

Function generator settings are shown in Table 6.

Table 6. Function Generator Settings

Channel	Mode	Freq. kHz	Duty	Delay	Ampl. V	Offset, V	Load Imped.	Frequency set	Comment
A (Ch.1)	Pulse	10	50%	0	4	2.0	50 Ω		
B (Ch.2)	Ramp	10	50%	270 µs	1.2	0.6	50 Ω	Ch1=Ch2, ON	N/A for UCC21750

Oscilloscope settings for UCC21710 and UCC21732 based EVMs are shown in Table 7 and in Figures 10 through 12.

Table 7. Oscilloscope Settings for UCC21710 and UCC21732 EVMs

Channel	Vertical scale	Horizontal scale	Bandwidth	Coupling	Termination	Sync.	Resolution
Ch. 1(yellow)	10 V/div	200 µs/div	500 MHz or above	DC	1 MΩ		High
Ch. 2(blue)	2 V/div					Ch. 2	
Ch. 3(pink)	500 mV/div						

Figure 11. Short Circuit Test Waveforms

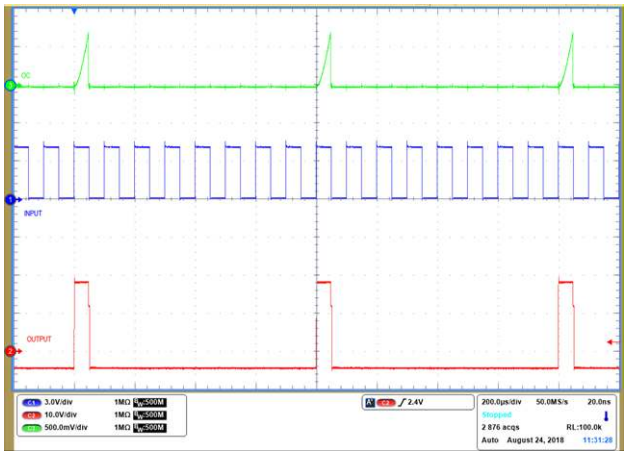


Figure 12. Expanded Short Circuit Waveforms for UCC21732

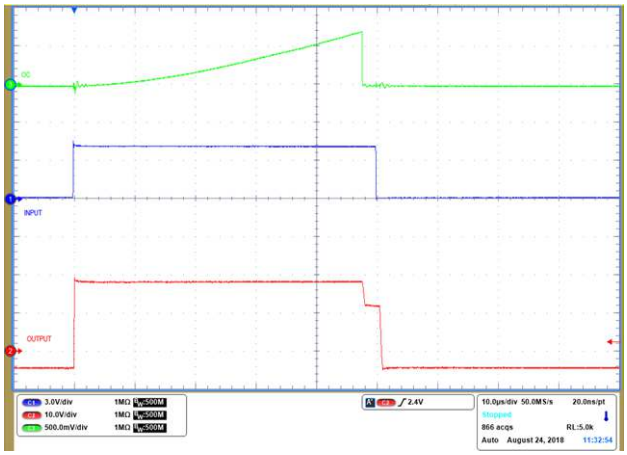


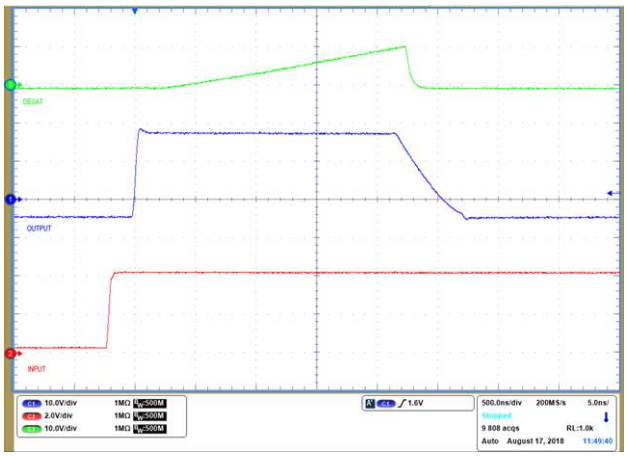
Figure 13. Expanded Short Circuit Waveforms for UCC21710

Oscilloscope settings for UCC21750 based EVM are shown in Table 8 and in Figure 13.

Table 8. Oscilloscope Settings for UCC21750 EVM

Channel	Vertical scale	Horizontal scale	Bandwidth	Coupling	Termination	Sync.	Resolution
Ch. 1(yellow)	10 V/div	500 ns/div	500 MHz or above	DC	1 MΩ	Ch. 1	High
Ch. 2(blue)	2 V/div						
Ch. 3(pink)	10 V/div						

Figure 14. Expanded Short Circuit Waveforms for UCC21750



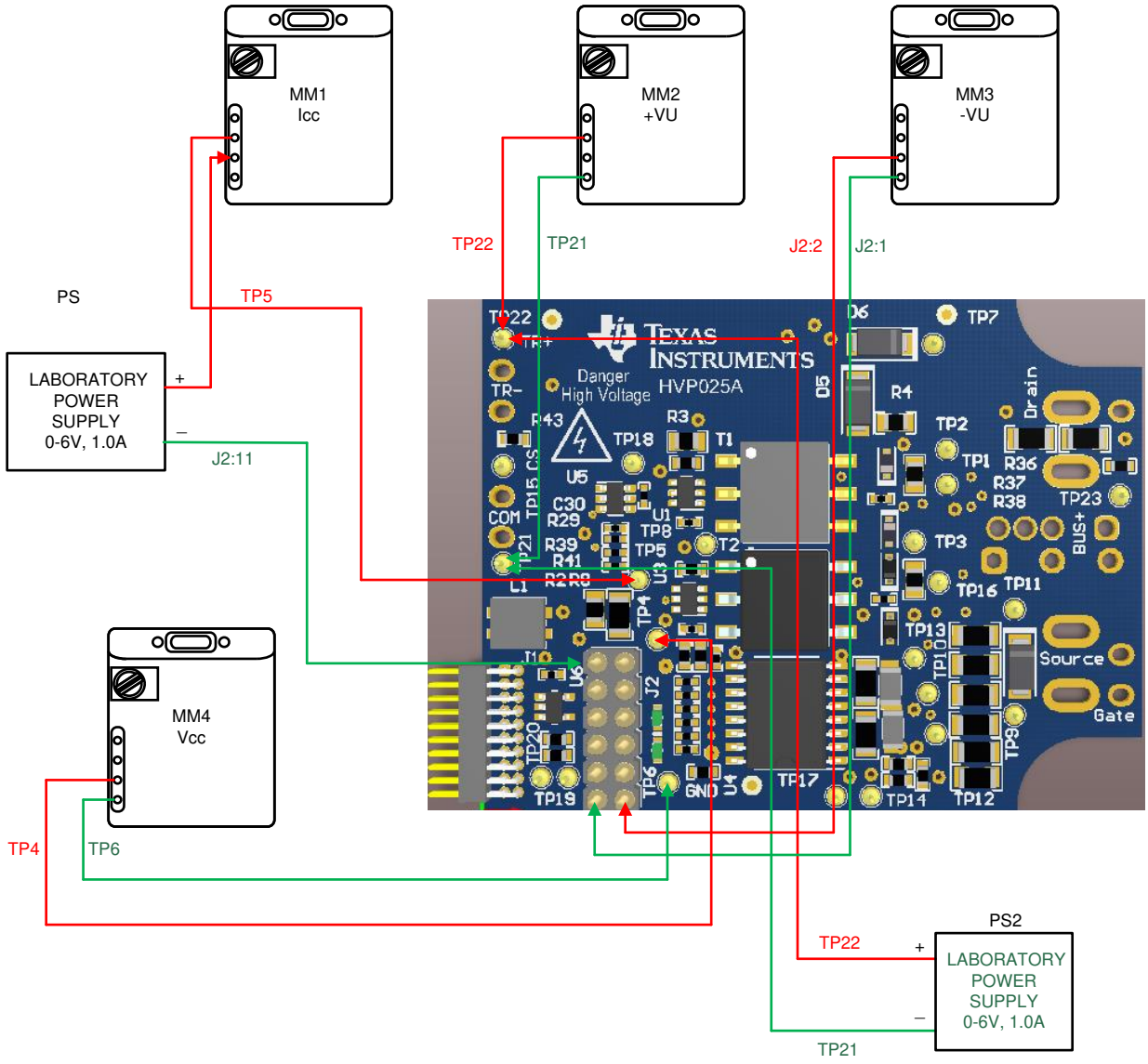
The following is overcurrent and short circuit turn OFF test procedure.

1. Enable power supply PS
2. Gradually increase the voltage at PS into 4.95 V to 5.05 V range and monitor current using MM1 that should not exceed 6075 mA
3. Enable channel A (ch.1) and channel B (ch.2) of function generator
4. LED D10 should go dark indicating fault
5. Compare waveforms with typical screen shot shown in Fig. 10
6. Expand waveforms into scale 10 µs/div and compare with Fig. 11 for UCC21732, Fig. 12 for UCC21710 and with scale 500 ns/div in Fig. 13 for UCC21750
7. Disable function generator channels
8. Gradually reduce voltage at PS down to 0 and disable it (Make sure function generator outputs are disabled before this action!)

2.2.4 Isolated Analog Input and Output Test

The test setup is shown in Figure 14. Additionally, connect TP15 to TP21.

Figure 15. Isolated Analog Input and Output Test Setup



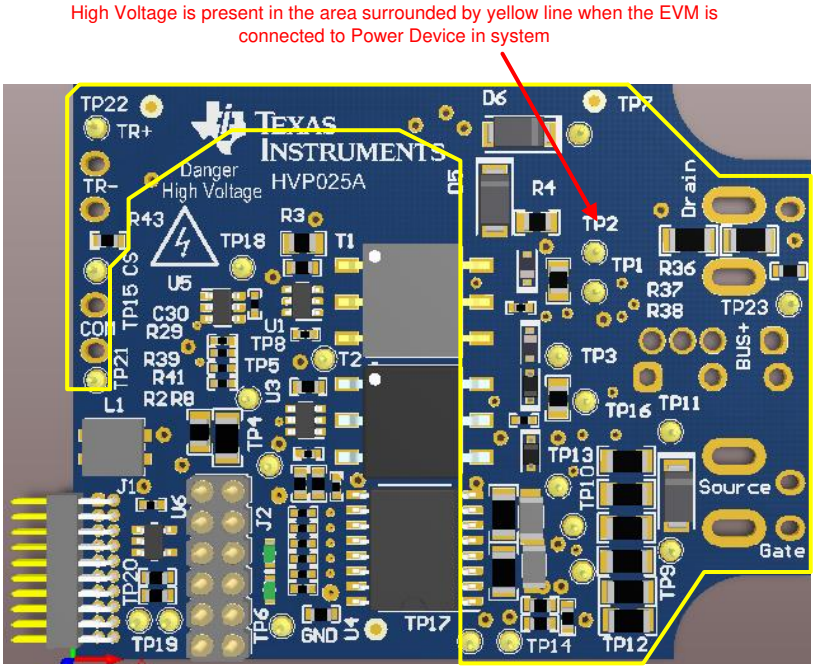
The following is isolated analog input/output test procedure.

1. Enable power supply PS1
2. Gradually increase the voltage at PS1 into 4.95 V to 5.05 V range and monitor current using MM1 that should not exceed 75 mA
3. Enable power supply PS2
4. Gradually increase the voltage of power supply PS2 from 0 V up to 4.5 V and monitor voltage at multi-meter MM3. The voltage at MM3 is gradually reducing from 4.4 V-4.8 V to 0.1 V-0.7 V, while the voltage at multi-meter MM2 is increasing following power supply PS2
5. Gradually decrease the voltage of power supply PS2 down to 0 and disable it
6. Gradually reduce the voltage of power supply PS1 down to 0 V and disable it

3 Advanced Evaluation with Power Modules

The board view is shown in Figure 15. For evaluation with power device, the 5-V nominal input voltage is supplied through 0.05” pitch connector J1 on the left side. The user has to use proper receptacle and design input/output cable based on own needs. All signals on primary side are available through header J2.

Figure 16. The Board View with Potential High Voltage Area



NOTE: The area oulined by yellow line in Figure 15 has high voltage present when the EVM is connected to power device in system. Depending on power system, this high voltage can be up to 1500 V.

To minimize risk of electric shock hazard always follow safety practices normally followed in a development laboratory. Refer to TI's EVM High Voltage guideline accompmanying this EVM.

All critical voltage signals are accessible through numerous test points shown in the schematic and assembly top and bottom views (Figures 16 through 18).

Figure 17. Electrical Schematic

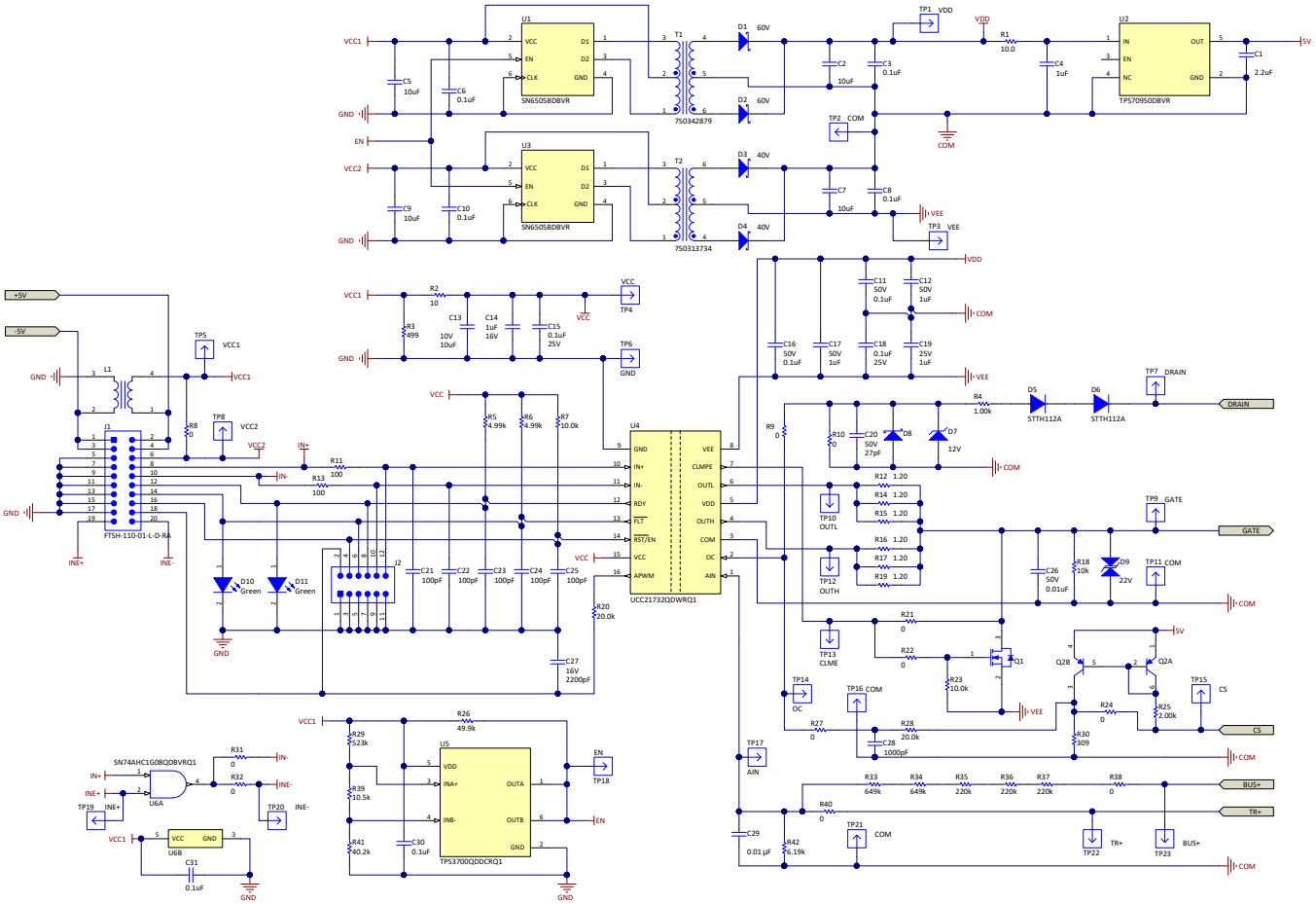


Figure 18. EVM Top View

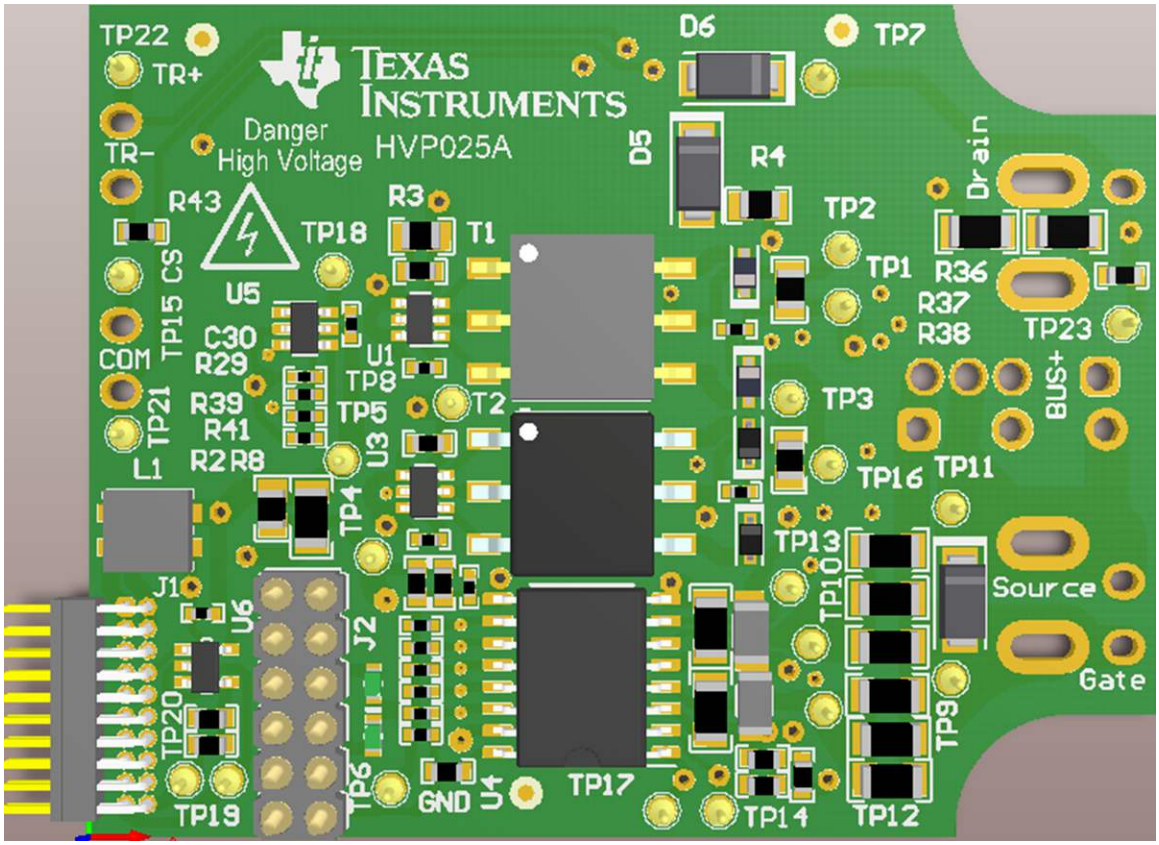
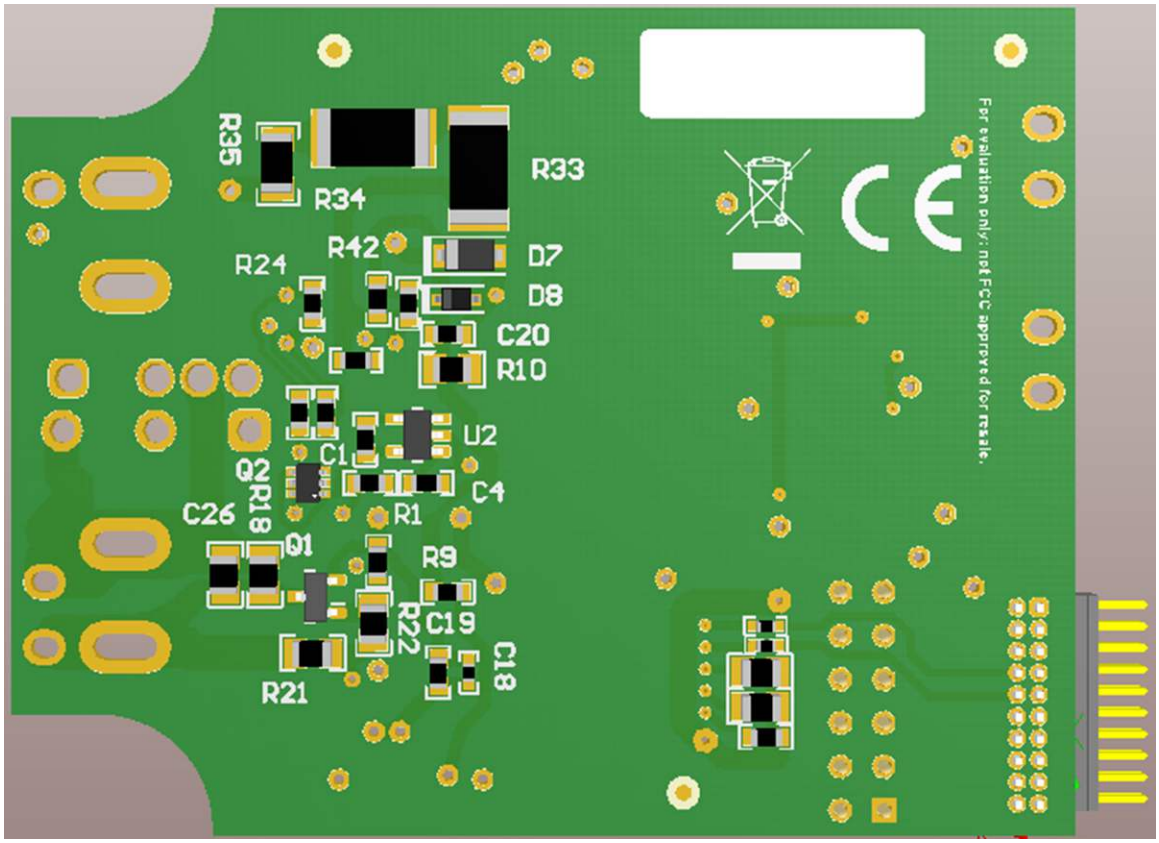


Figure 19. EVM Bottom View



3.1 EVM Default Settings and Recommendations

Most drive, protection and diagnostic functions are integrated within TI ICs used in the board. The board setting can be either for isolated driver UCC21710, UCC21732, or UCC21750 as it is shown on board label and on its bag.

The default settings for UCC21732 driver are shown in Figures 19 and 20.

Figure 20. UCC21732QDWEVM-025 Top Assembly View

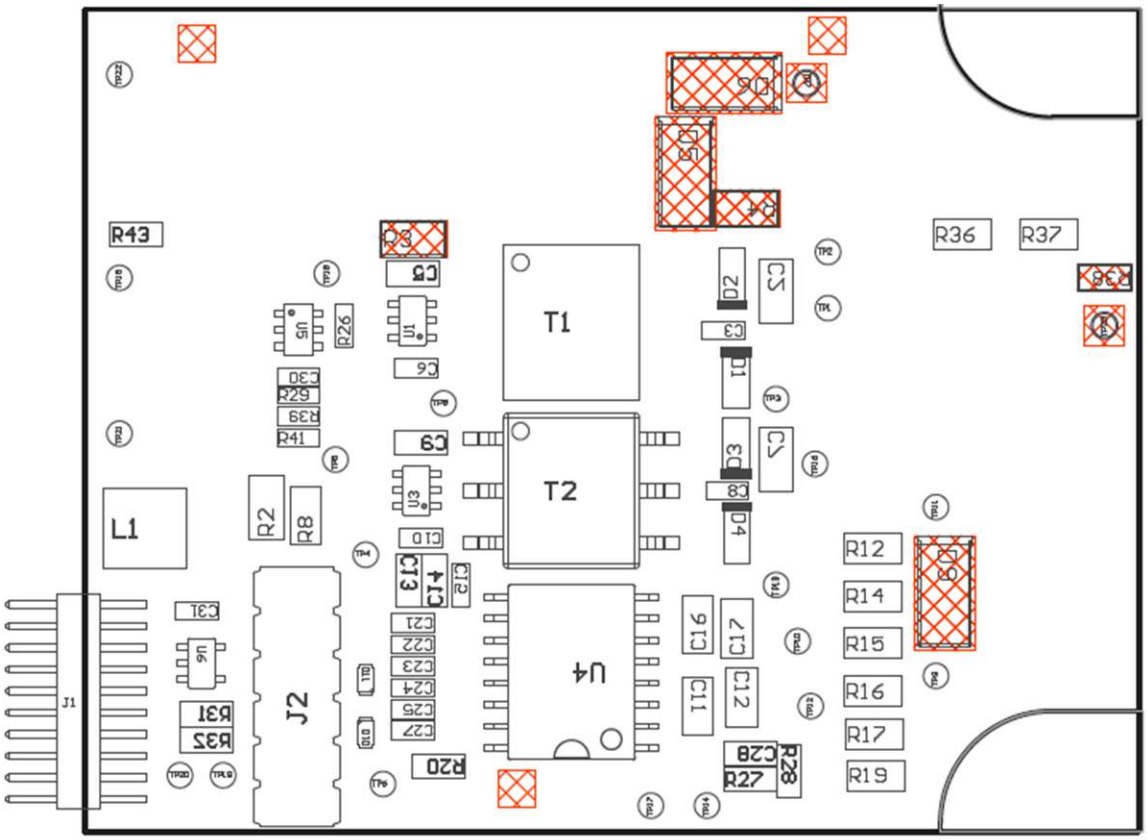
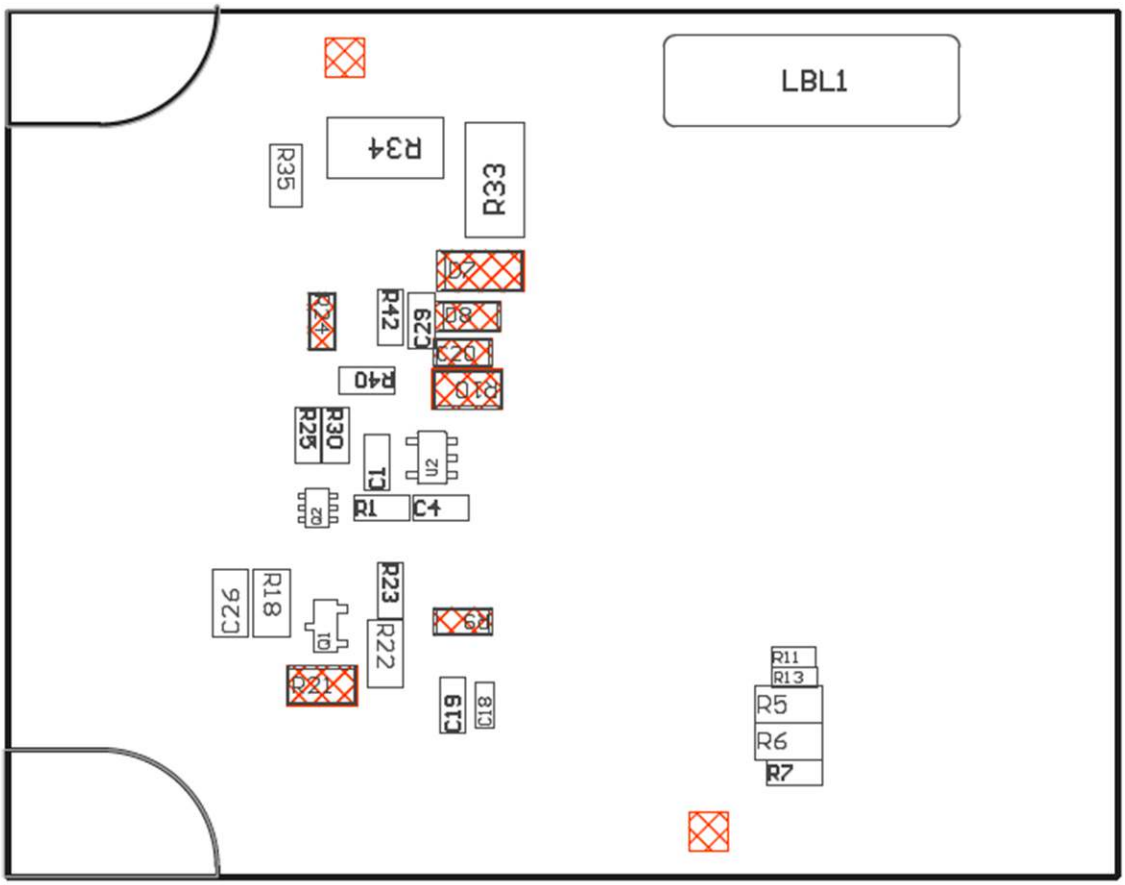


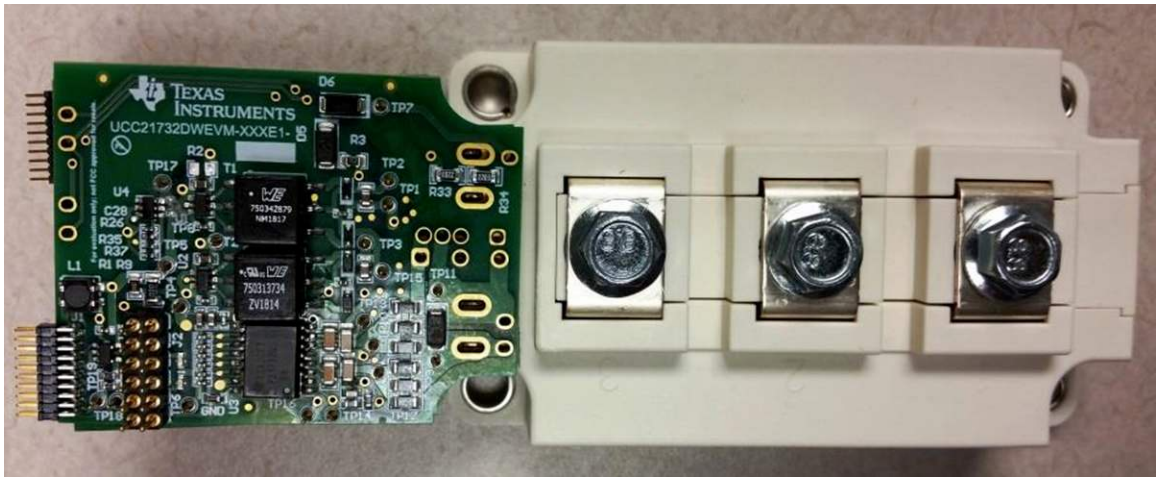
Figure 21. UCC21732QDWEVM-025 Bottom Assembly View



- Remove R9 – to disable desaturation protection feature and allow OC protection provided by UCC21710 and UCC21732, but leave R9 and remove R27 and R10 for UCC21750
- Remove R21 – to disable internal Miller clamp and allow external FET Miller clamp for UCC21732
- Keep R21 and remove R22 and Q1 to allow internal Miller clamp for UCC21710 and UCC21750
- Remove R38 – to allow temperature monitoring using thermistor inside the power module. Putting back R38 and removing R40 allows input voltage rail monitoring and disables temperature monitoring
- Remove R30, R25 and Q2 and use R24 to connect directly to CS+. This setting by default allows positive OC signal sensing. Resistor R28 is used for high frequency OC noise rejection and its value depends on system needs and can be selected differently
- For negative OC signal sensing, keep R30, R25 and Q2 and remove R24
- C26 is 10 nF capacitor to emulate Cgs charge of power module. When connecting to power module this capacitor must be removed
- By default R3 is not populated. This resistor is used in the systems where the driver is turned OFF at some conditions by external switch in series with VCC. In this case R3 provides relatively fast discharge path for input VCC capacitances
- In order to use UCC21736 on the EVM, which has the ASC input instead of AIN input, the IC must be replaced manually onto the UCC21732 EVM with the same configurations aside from the following: R40 and R38 should be removed. TP17 may be used as the test point to enable ASC for evaluation of this function.

In many systems half-bridge power stage is used as key functional block for power conversion. Thus, two EVMs can be used to drive standard half-bridge power modules as shown in Figures 21 and 22.

Figure 22. EVM Boards with Standard 106 mm Half-Bridge Module



In 106-mm half-bridge module configuration two boards are placed one on top of another and the bottom board is flipped over. The supply voltage and input signals are provided through connectors J1 on each board. By connecting IN+ and INE- terminals on one board to INE+ and IN- terminals accordingly on another board, the overlapping protection circuit using logic U5 is engaged. This circuit could be disabled by removing resistors R31 and R32 in case of overlapping is required in the system.

Figure 23. EVM Boards with Standard 150 mm Half-Bridge Module

In 150-mm half-bridge module configuration two boards are placed one next to another but one board rotated 180°. The vias for Vgs drive and temperature and input rail sensing will be aligned based on boards form factor. If the power module has standard terminals for shunt resistor current sensing, these terminals also will be aligned with CS+ and COM inputs of driver board. Isolated analog input of driver IC is referenced to COM pin. Thus, input voltage rail sensing requires to be used by the EVM on right side in Figure 22, because it shares the same reference as input voltage rail. The connection of VIN+ terminal to Drain via needs to be done by wire. The thermistor for temperature sensing in power moduls is usually electrically isolated. Thus, analog isolated input of left side EVM can be used for temperature sensing. The connection of thermistor pins to TR+ and TR- vias needs to be done by using twisted wires.

NOTE: While operating with power modules as part of power system, the input supply current limit 400mA to each driver board, the isolation working voltage 1500V, and voltage and temperature limits, set by power module vendors to the module, should never been exceeded!

3.2 PCB Board Design

The 4-layer PCB board is used for EVM to minimize EMI by using ground planes in internal layers. The layout of all 4 layers is shown in Figures 23 through 26.

Figure 24. Top Layer

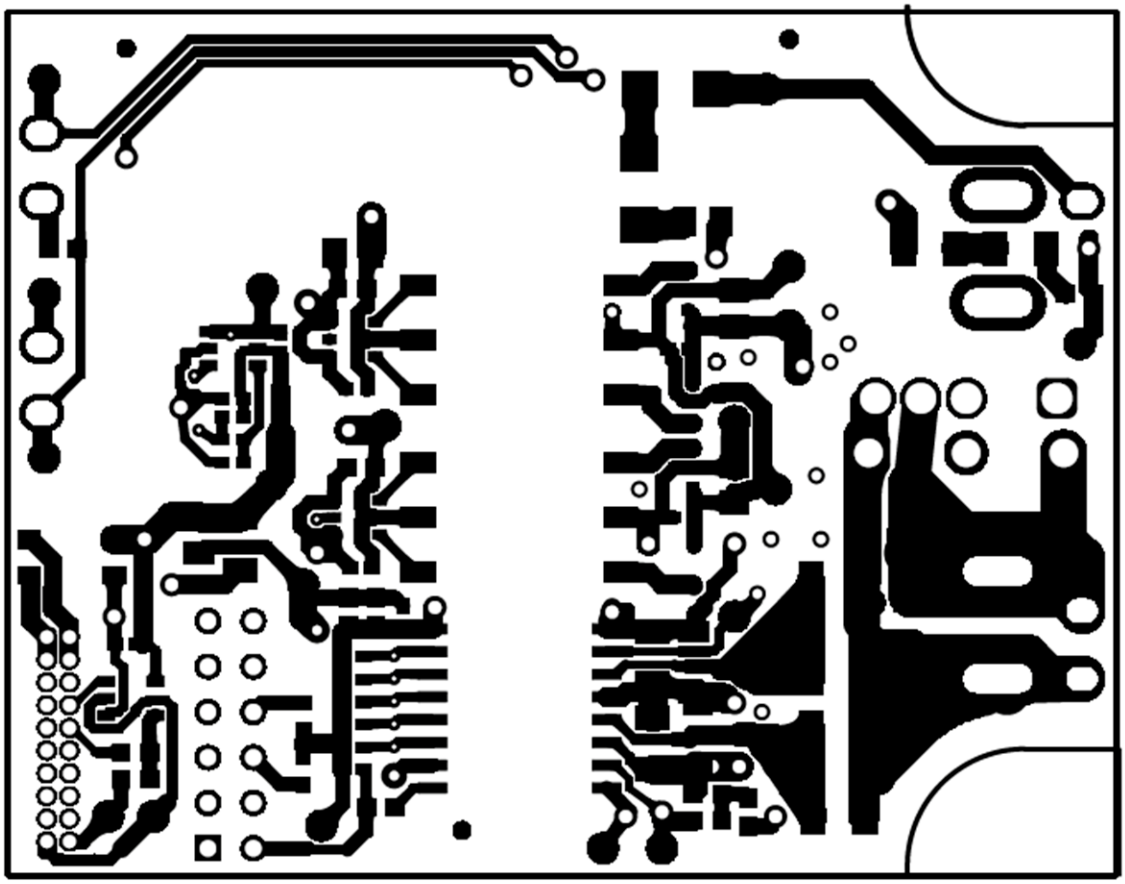


Figure 25. Internal Signal Layer 1

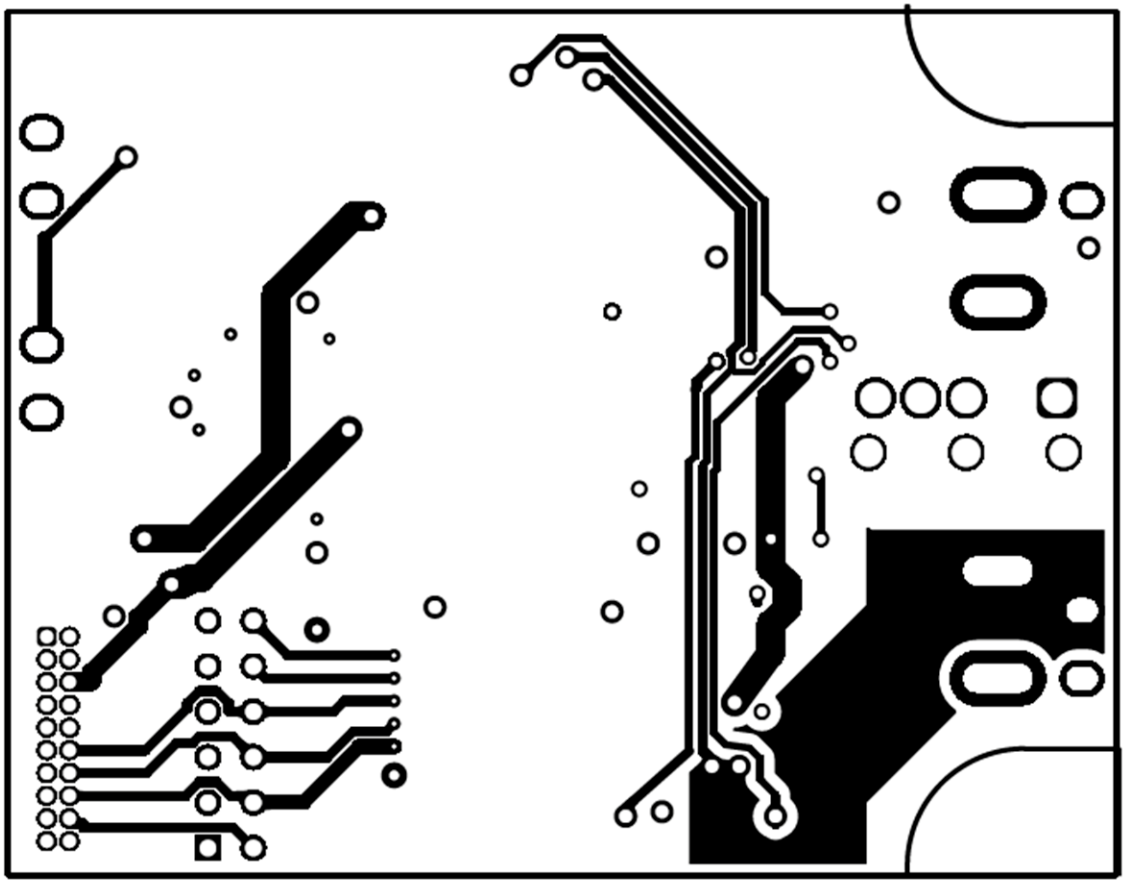


Figure 26. Internal Singal Layer 2

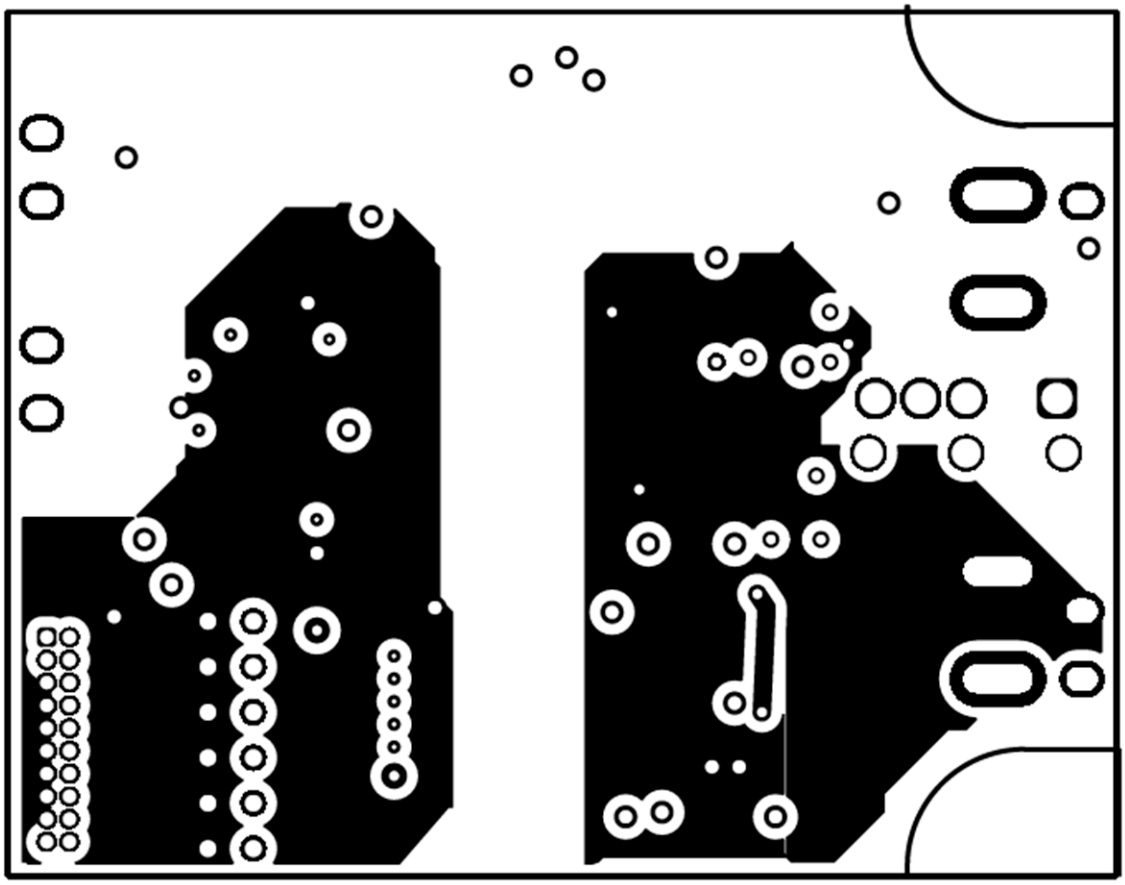
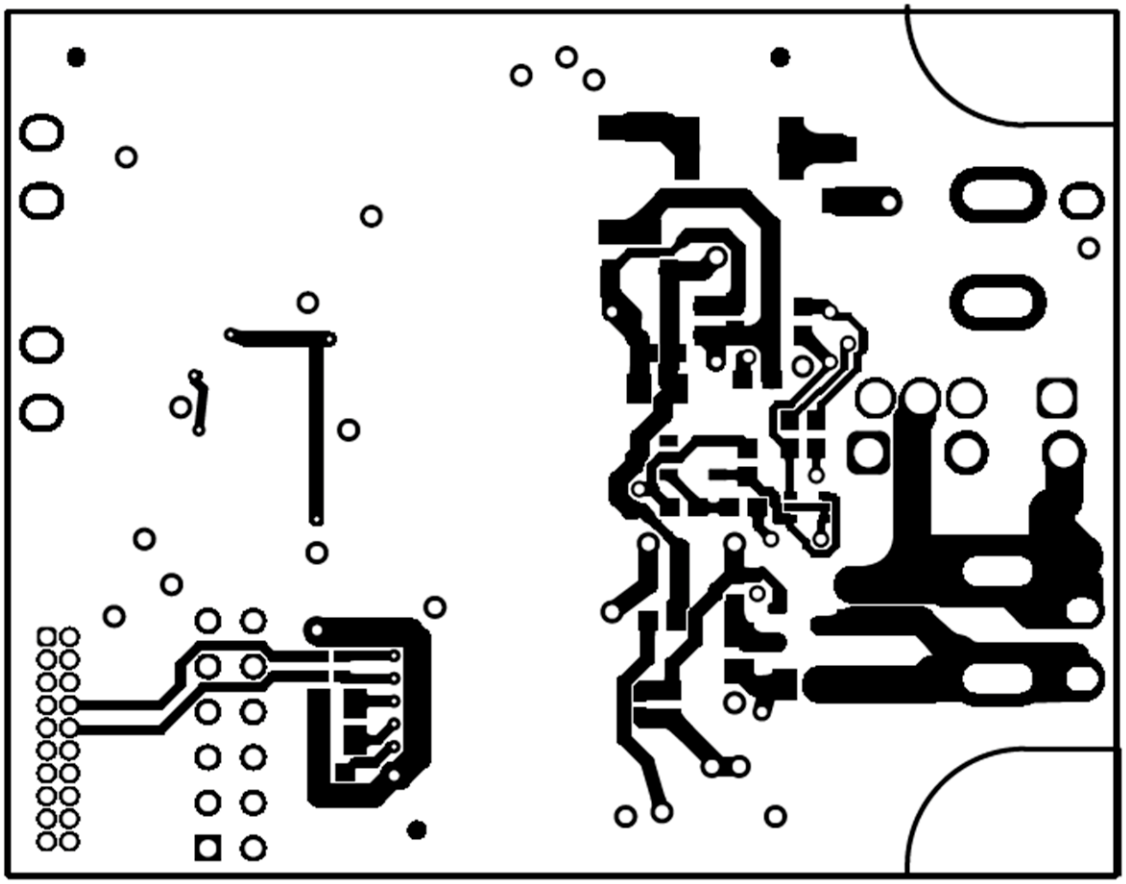


Figure 27. Bottom Layer



3.3 List of Materials

List of materials for the UCC21732QDWEVM-025.

Table 9. UCC21732QDWEVM-025 List of Materials

DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
!PCB1	1	Printed Circuit Board	Any	HVP025
C1	1	Capacitor, ceramic, 2.2 uF, 16 V,+/- 10%, X7R, 0603	Taiyo Yuden	EMK107BB7225MA-T
C2, C7	2	Capacitor, ceramic, 10 uF, 25 V, +/- 10%, X5R, 0805	TDK	C2012X5R1E106K125AB
C3, C8	2	Capacitor, ceramic, 0.1 uF, 50 V, +/- 10%, X7R, 0402	TDK	C1005X7R1H104K050BB
C4	1	Capacitor, ceramic, 1 uF, 50 V, +/- 10%, X7R, 0603	Taiyo Yuden	UMK107AB7105KA-T
C5, C9, C13	3	Capacitor, ceramic, 10 uF, 10 V,+/- 20%, X5R, 0603	MuRata	GRM188R61A106MAALD
C6, C10, C30, C31	4	Capacitor, ceramic, 0.1 uF, 10 V, +/- 10%, X5R, 0402	MuRata	GRM155R61A104KA01D
C11, C16	2	Capacitor, ceramic, 0.1 uF, 50 V, +/- 5%, X7R, 1206	Kemet	C1206C104J5RACTU
C12, C17	2	Capacitor, ceramic, 1 uF, 50 V, +/- 10%, X7R, 1206	TDK	C3216X7R1H105K160AB
C14	1	Capacitor, ceramic, 1.5 uF, 10 V, +/- 10%, X7R, 0603	TDK	C1608X7R1A155K080AC
C15	1	Capacitor, ceramic, 0.1 uF, 25 V, +/- 10%, X7R, 0402	MuRata	GRM155R71E104KE14D

Table 9. UCC21732QDWEVM-025 List of Materials (continued)

DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
C18	1	Capacitor, ceramic, 0.1 uF, 16 V, +/- 10%, X7R, 0402	MuRata	GCM155R71C104KA55D
C19	1	Capacitor, ceramic, 1 uF, 25 V, +/- 10%, X7R, 0603	Kemet	C0603C105K3RACTU
C21, C22, C23, C24, C25	5	Capacitor, ceramic, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	Yageo America	CC0402JRNPO9BN101
C26	1	Capacitor, ceramic, 0.01 uF, 50 V, +/- 10%, X7R, 0805	Wurth Elektronik	885012207092
C27	1	Capacitor, ceramic, 2200 pF, 16 V, +/- 10%, X7R, 0402	MuRata	GRM155R71C222KA01D
C28	1	Capacitor, ceramic, 1000 pF, 50 V, +/- 5%, X7R, AEC-Q200 Grade 1, 0603	Kemet	C0603C102J5RACAUTO
C29	1	Capacitor, ceramic, 0.01 µF, 25 V,+/- 10%, X7R, 0603	Presidio Components	SR0603X7R103K1NT95(F)#M123A
D1, D2	2	Diode, Schottky, 60 V, 1 A, SOD-323F	Nexperia	PMEG6010CEJ,115
D3, D4	2	Diode, Schottky, 40 V, 0.5 A, SOD-323	Diodes Inc.	B0540WS-7
D10, D11	2	LED, Green, SMD	OSRAM	LG L29K-G2J1-24-Z
FID4	1	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
J1	1	Header, 1.27mm, 10x2, Gold with Tin tail, R/A, TH	Samtec	FTSH-110-01-L-D-RA
J2	1	Header, 2.54 mm, 6x2, Gold, TH	Mill-Max	802-10-012-10-001000
L1	1	Coupled inductor, 2.8 A, 0.055 ohm, SMD	TDK	ACM4520-421-2P-T000
LBL1	1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10
Q1	1	MOSFET, N-CH, 40 V, 5.6 A, SOT-23	Vishay-Siliconix	SI2318CDS-T1-GE3
Q2	1	Transistor, Dual PNP, 60 V, 0.6 A, SOT-363	Diodes Inc.	MMDT2907A-7-F
R1	1	Resistor, 10.0, 1%, 0.1 W, 0603	Yageo	RC0603FR-0710RL
R2	1	Resistor, 10, 5%, 0.125 W, 0805	Vishay-Dale	CRCW080510R0JNEA
R5, R6	2	Resistor, 4.99 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW08054K99FKEA
R7	1	Resistor, 10.0 k, 1%, 0.1 W, 0603	Panasonic	ERJ-3EKF1002V
R8	1	Resistor, 0, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12060000Z0EA
R11, R13	2	Resistor, 100, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402100RFKED
R12, R14, R15, R16, R17, R19	6	Resistor, 1.20, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW12061R20FKEA
R18	1	Resistor, 10 k, 5%, 0.125 W, 0805	Panasonic	ERJ-6GEYJ103V
R20	1	Resistor, 20.0 k, 0.5%, 0.1 W, 0603	Yageo America	RT0603DRE0720KL
R22	1	Resistor, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW08050000Z0EA
R23	1	Resistor, 10.0 k, 1%, 0.1 W, 0603	TT Electronics/IRC	M55342K12B10E0T
R25, R28	2	Resistor, 2.00 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-072KL
R26	1	Resistor, 49.9 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249K9FKED
R24, R27, R40, R43	3	Resistor, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Stackpole Electronics Inc	RMCF0603ZT0R00
R29	1	Resistor, 523 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402523KFKED
R30	1	Resistor, 309, 1%, 0.1 W, 0603	Yageo	RC0603FR-07309RL
R31, R32	2	Resistor, 0, 5%, 0.1 W, 0603	Panasonic	ERJ-3GEY0R00V
R33, R34	2	Resistor, 649 k, 1%, 1 W, AEC-Q200 Grade 0, 2512	Vishay-Dale	CRCW2512649KFKEG
R35, R36, R37	3	Resistor, 220 k, 1%, 0.25 W, 1206	Yageo America	RC1206FR-07220KL

Table 9. UCC21732QDWEVM-025 List of Materials (continued)

DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
R39	1	Resistor, 10.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040210K5FKED
R41	1	Resistor, 40.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040240K2FKED
R42	1	Resistor, 6.19 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06036K19FKEA
T1	1	Transformer, 50 uH, SMT	Wurth Elektronik	750342879
T2	1	Transformer, 340 uH, TH	Wurth Elektronik	750313734
TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22	21	PCB Pin, 20mil Dia, Gold, TH	Mill-Max	0508-0-00-15-00-00-03-0
U1, U3	2	Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)	Texas Instruments	SN6505BDBVR
U2	1	150-mA, 30-V, Ultra-Low IQ, Wide Input Low-Dropout Regulator with Reverse Current Protection, DBV0005A (SOT-23-5)	Texas Instruments	TPS70950DBVR
U4	1	Single Channel Isolated Gate Driver for SiC/IGBT with Advanced Protection and High-CMTI, DW0016B (SOIC-16)	Texas Instruments	UCC21732QDWRQ1
U5	1	Automotive, High-Voltage (18V) Window Comparator with Over- and Undervoltage Detection, DDC0006A (SOT-23-T-6)	Texas Instruments	TPS3700QDDCRQ1
U6	1	Automotive Catalog Single 2-Input Positive-AND Gate, DBV0005A, LARGE T&R	Texas Instruments	
C20	0	Capacitor, ceramic, 27 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C270J5GACTU
D5, D6	0	Diode, Ultrafast, 1200 V, 1 A, SMA	STMicroelectronics	STTH112A
D7	0	Diode, Zener, 12 V, 500 mW, SOD-123	Diodes Inc.	MMSZ5242B-7-F
D8	0	Diode, Schottky, 30 V, 0.2 A, SOD-323	Diodes Inc.	BAT54WS-7-F
D9	0	Diode, TVS, Bi, 22 V, SMA	Littelfuse	SMAJ22CA
FID1, FID2, FID3, FID5, FID6	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
R3	0	Resistor, 499, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805499RFKEA
R4	0	Resistor, 1.00 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08051K00FKEA
R9, R24, R38	0	Resistor, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Stackpole Electronics Inc	RMCF0603ZT0R00
R10, R21	0	Resistor, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW08050000Z0EA
TP7, TP23	0	PCB Pin, 20mil Dia, Gold, TH	Mill-Max	0508-0-00-15-00-00-03-0

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2019) to B Revision	Page
• Added note on UCC21736-Q1	6
• Added ASC function description	8
• Added negative current sensing functional description	9
• Added EVM configuration for using UCC21736-Q1 IC on UCC21732 EVM	23

Changes from Original (October 2018) to A Revision	Page
• Changed marketing status from select disclosure to catalog.	2

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