

BLF0910H6L500; BLF0910H6LS500

Power LDMOS transistor

Rev. 2 — 13 April 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 500 W LDMOS power transistor for industrial applications at frequency of 915 MHz.

The BLF0910H6L500 and BLF0910H6LS500 are designed for high-power CW applications and are assembled in high performance ceramic packages.

Table 1. Typical performance

RF performance at $V_{DS} = 50\text{ V}$; $I_{Dq} = 90\text{ mA}$ in a class-AB application circuit.

Test signal	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW [1]	915	50	500	18	61
CW pulsed [2][3]	915	50	500	19.5	62.5

[1] $T_{case} = 65\text{ °C}$.

[2] $T_{case} = 25\text{ °C}$.

[3] $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$.

1.2 Features and benefits

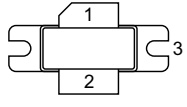
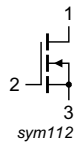
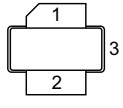
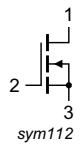
- High efficiency
- Easy power control
- Excellent ruggedness
- Integrated ESD protection
- Designed for broadband operation (900 MHz to 930 MHz)
- Internally input matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial applications in the 915 MHz ISM band

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF0910H6L500 (SOT502A)			
1	drain		 sym112
2	gate		
3	source ^[1]		
BLF0910H6LS500 (SOT502B)			
1	drain		 sym112
2	gate		
3	source ^[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF0910H6L500	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF0910H6LS500	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	114.5	V
V_{GS}	gate-source voltage	-6	+11	V
T_{stg}	storage temperature	-65	+150	°C
T_j	junction temperature ^[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 500\text{ W}$	0.2	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 4\text{ mA}$	114.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 400\text{ mA}$	1.25	1.9	2.35	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	60	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 20\text{ A}$	-	29	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 14\text{ A}$	-	0.078	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\%$; $f = 915\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$; $I_{Dq} = 90\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 500\text{ W}$	15	19	-	dB
RL_{in}	input return loss	$P_L = 500\text{ W}$	-	-18	-7	dB
η_D	drain efficiency	$P_L = 500\text{ W}$	59	63.5	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF0910H6L500 and BLF0910H6LS500 are capable of withstanding a load mismatch corresponding to $V_{SWR} = 30 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{Dq} = 90\text{ mA}$; $P_L = 500\text{ W}$ (CW); $f = 915\text{ MHz}$.

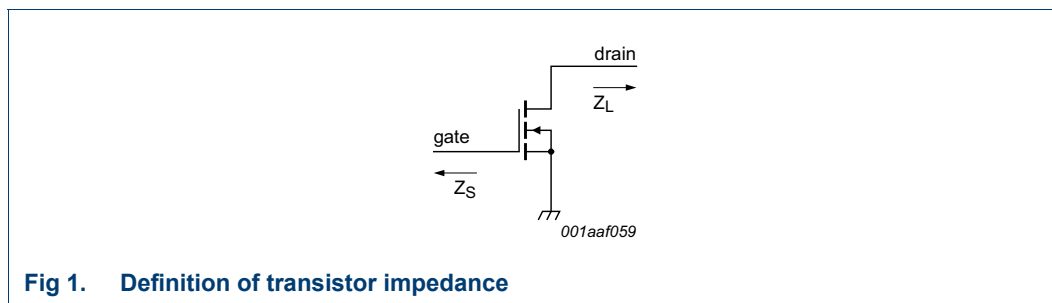
7.2 Impedance information

Table 8. Typical impedance

Measured load-pull Z_S and Z_L device impedances; $I_{Dq} = 90\text{ mA}$; $V_{DS} = 50\text{ V}$; typical values unless otherwise specified.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)
915	$1.8 - 1.4j$	$0.6 + 0.35j$

[1] Z_S and Z_L defined in [Figure 1](#).



7.3 Test circuit

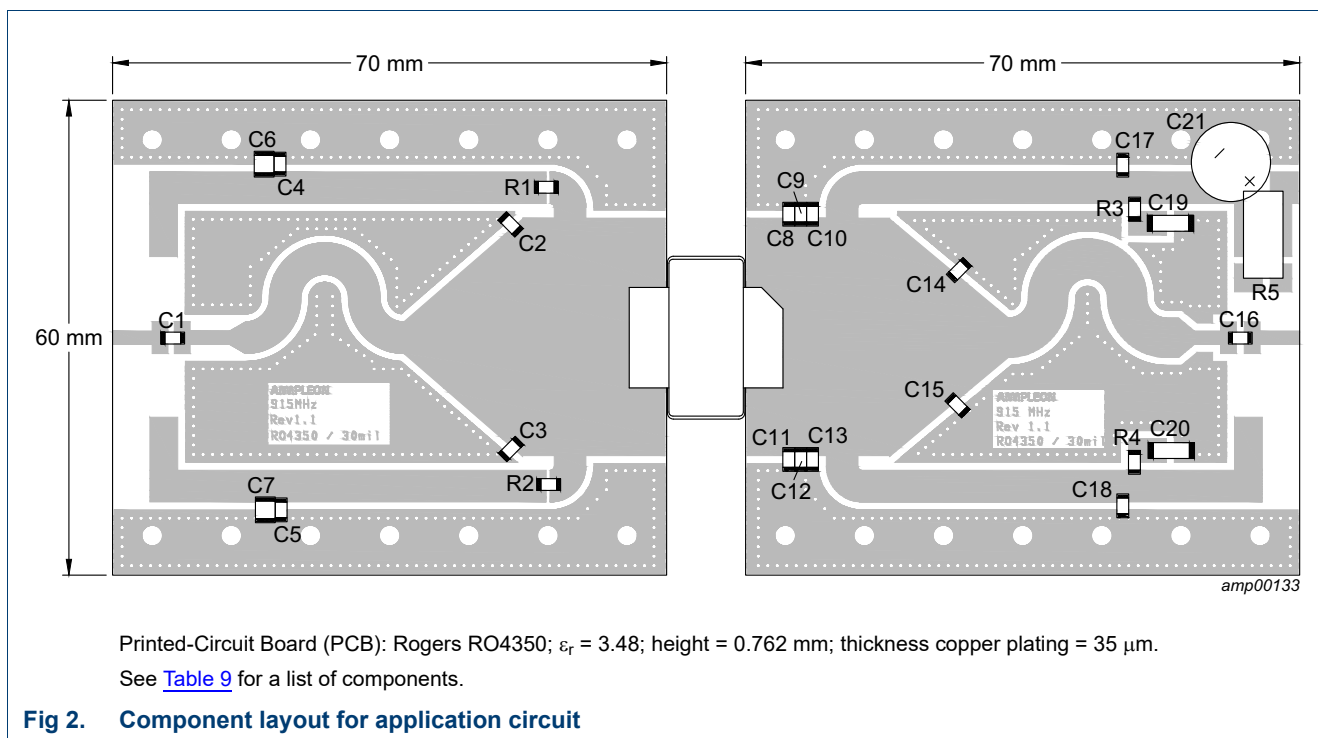


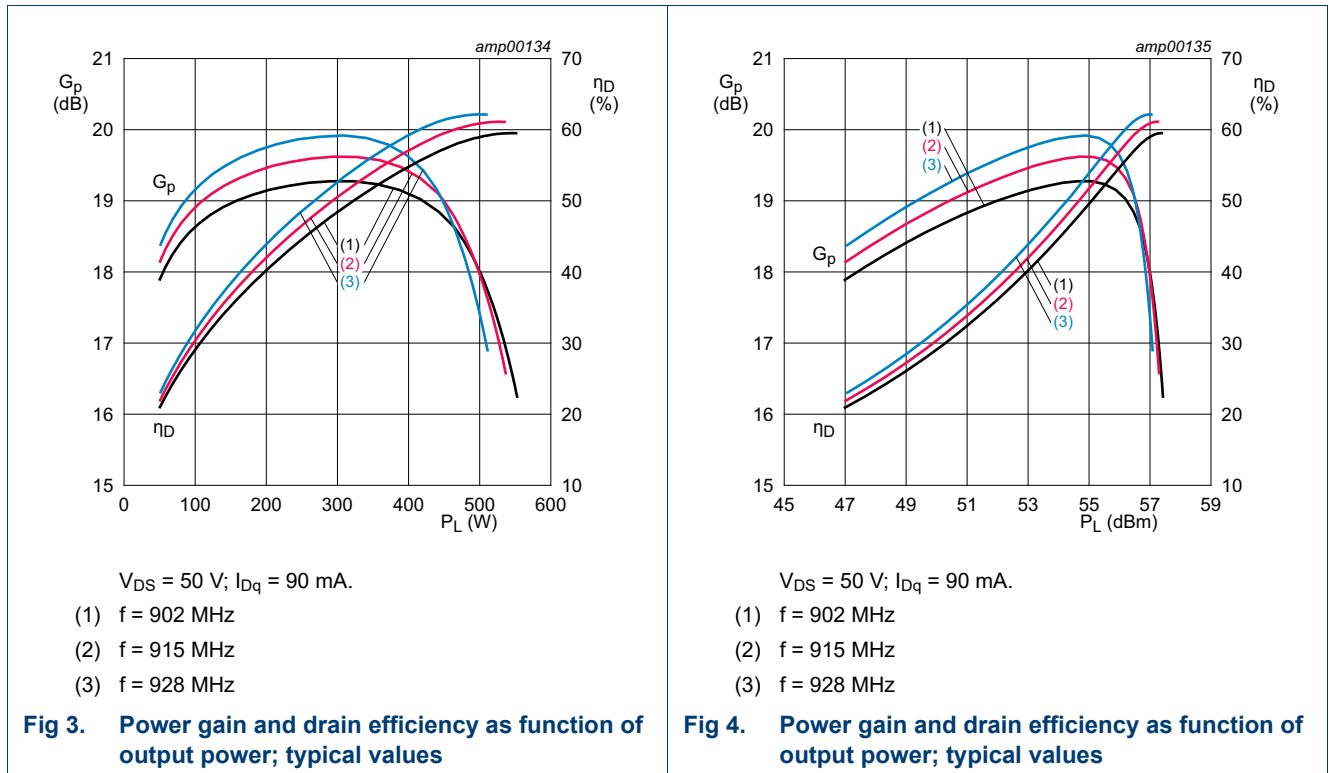
Table 9. List of components
See [Figure 2](#) for component layout.

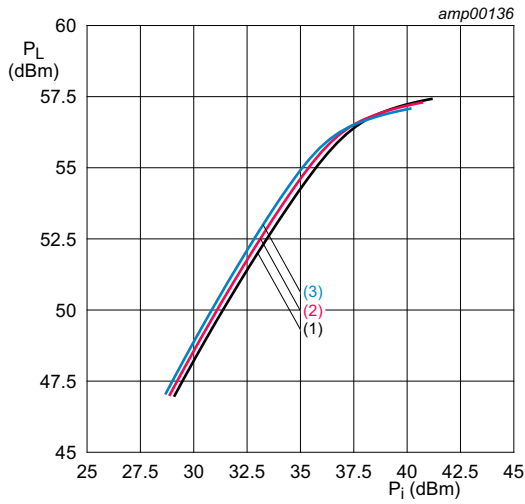
Component	Description	Value	Remarks
C1, C16	multilayer ceramic chip capacitor	470 pF	ATC 800B
C2, C3	multilayer ceramic chip capacitor	2.4 pF	ATC 800B
C4, C5, C17, C18	multilayer ceramic chip capacitor	100 pF	ATC 800B
C6, C7	multilayer ceramic chip capacitor	4.7 μF , 50 V	Murata: GRM32ER71H475KA88L
C8, C11	multilayer ceramic chip capacitor	5.6 pF	ATC 800B
C9, C10, C12, C13	multilayer ceramic chip capacitor	4.7 pF	ATC 800B
C14, C15	multilayer ceramic chip capacitor	0.9 pF	ATC 800B
C19, C20	multilayer ceramic chip capacitor	4.7 μF , 100 V	TDK: C5750X7R2A475KT/A
C21	electrolytic capacitor	470 μF , 63 V	

Table 9. List of components ...continued
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
R1, R2	resistor	10 Ω	SMD1206
R3, R4	resistor	3 Ω	SMD1206
R5	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER

7.4 Graphical data

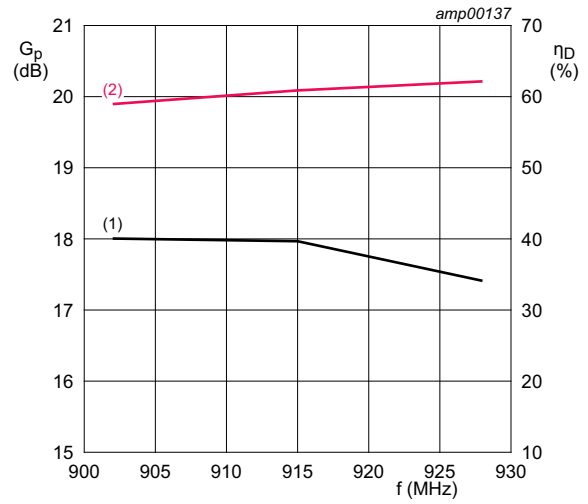




$V_{DS} = 50\text{ V}; I_{Dq} = 90\text{ mA}.$

- (1) $f = 902\text{ MHz}$
- (2) $f = 915\text{ MHz}$
- (3) $f = 928\text{ MHz}$

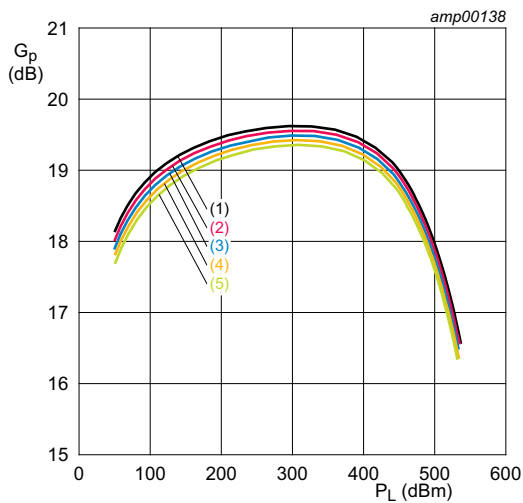
Fig 5. Output power as a function of input power; typical values



$V_{DS} = 50\text{ V}; I_{Dq} = 90\text{ mA}; P_L = 500\text{ W}.$

- (1) G_p
- (2) η_D

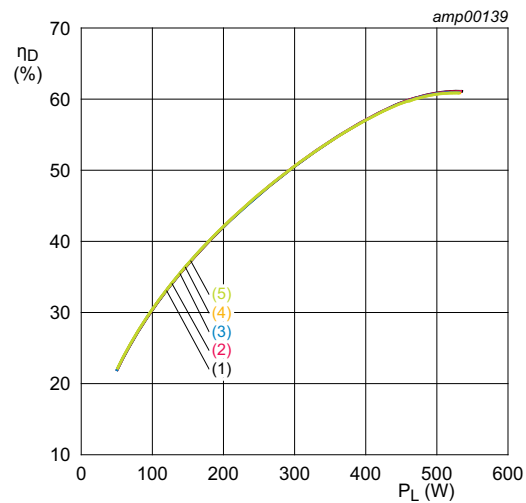
Fig 6. Power gain and drain efficiency as a function of frequency; typical values



$V_{DS} = 50\text{ V}; f = 915\text{ MHz}.$

- (1) $I_{Dq} = 90\text{ mA}$
- (2) $I_{Dq} = 80\text{ mA}$
- (3) $I_{Dq} = 70\text{ mA}$
- (4) $I_{Dq} = 60\text{ mA}$
- (5) $I_{Dq} = 50\text{ mA}$

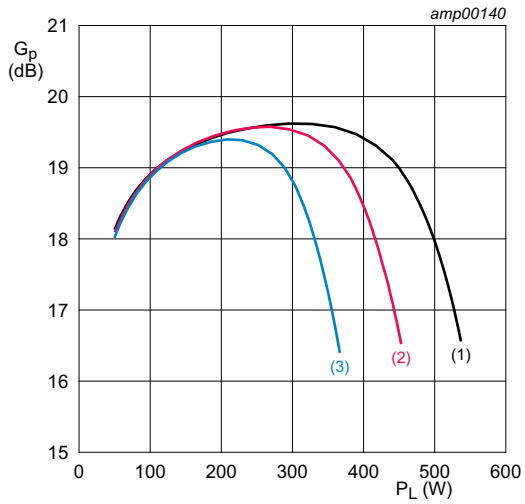
Fig 7. Power gain as a function of output power; typical values



$V_{DS} = 50\text{ V}; f = 915\text{ MHz}.$

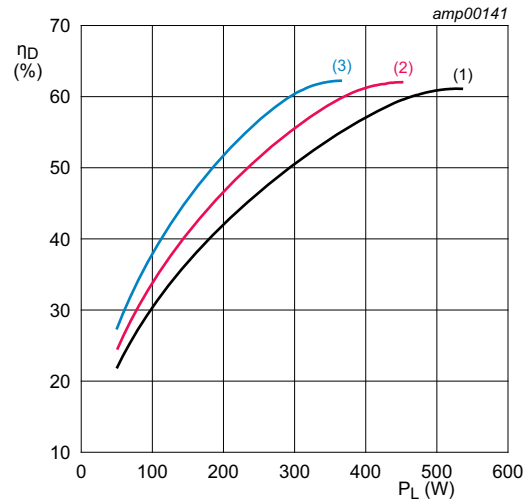
- (1) $I_{Dq} = 90\text{ mA}$
- (2) $I_{Dq} = 80\text{ mA}$
- (3) $I_{Dq} = 70\text{ mA}$
- (4) $I_{Dq} = 60\text{ mA}$
- (5) $I_{Dq} = 50\text{ mA}$

Fig 8. Drain efficiency as a function of output power; typical values



$I_{Dq} = 90 \text{ mA}; f = 915 \text{ MHz}.$
 (1) $V_{DS} = 50 \text{ V}$
 (2) $V_{DS} = 45 \text{ V}$
 (3) $V_{DS} = 40 \text{ V}$

Fig 9. Power gain as a function of output power; typical values



$I_{Dq} = 90 \text{ mA}; f = 915 \text{ MHz}.$
 (1) $V_{DS} = 50 \text{ V}$
 (2) $V_{DS} = 45 \text{ V}$
 (3) $V_{DS} = 40 \text{ V}$

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

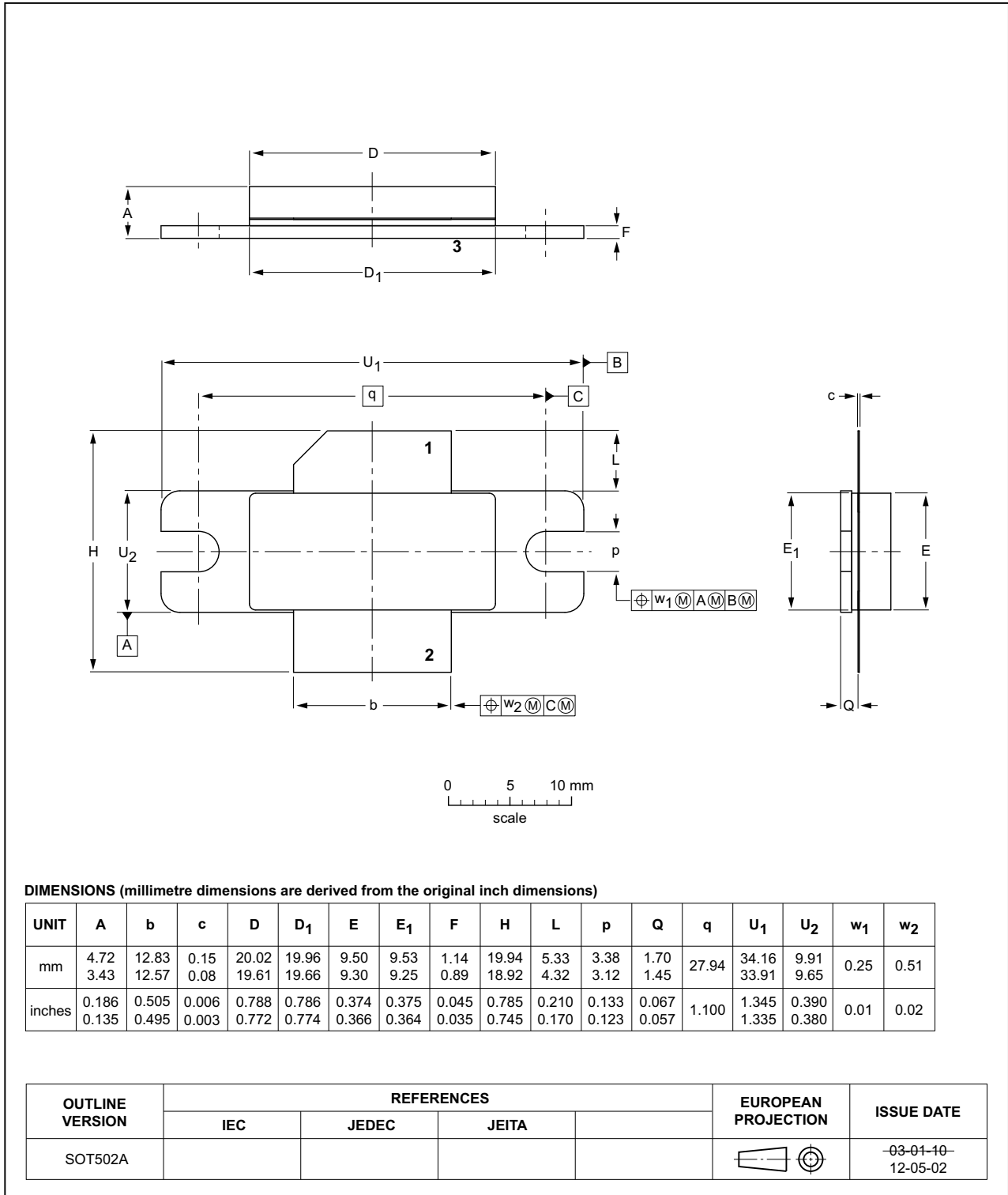


Fig 11. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

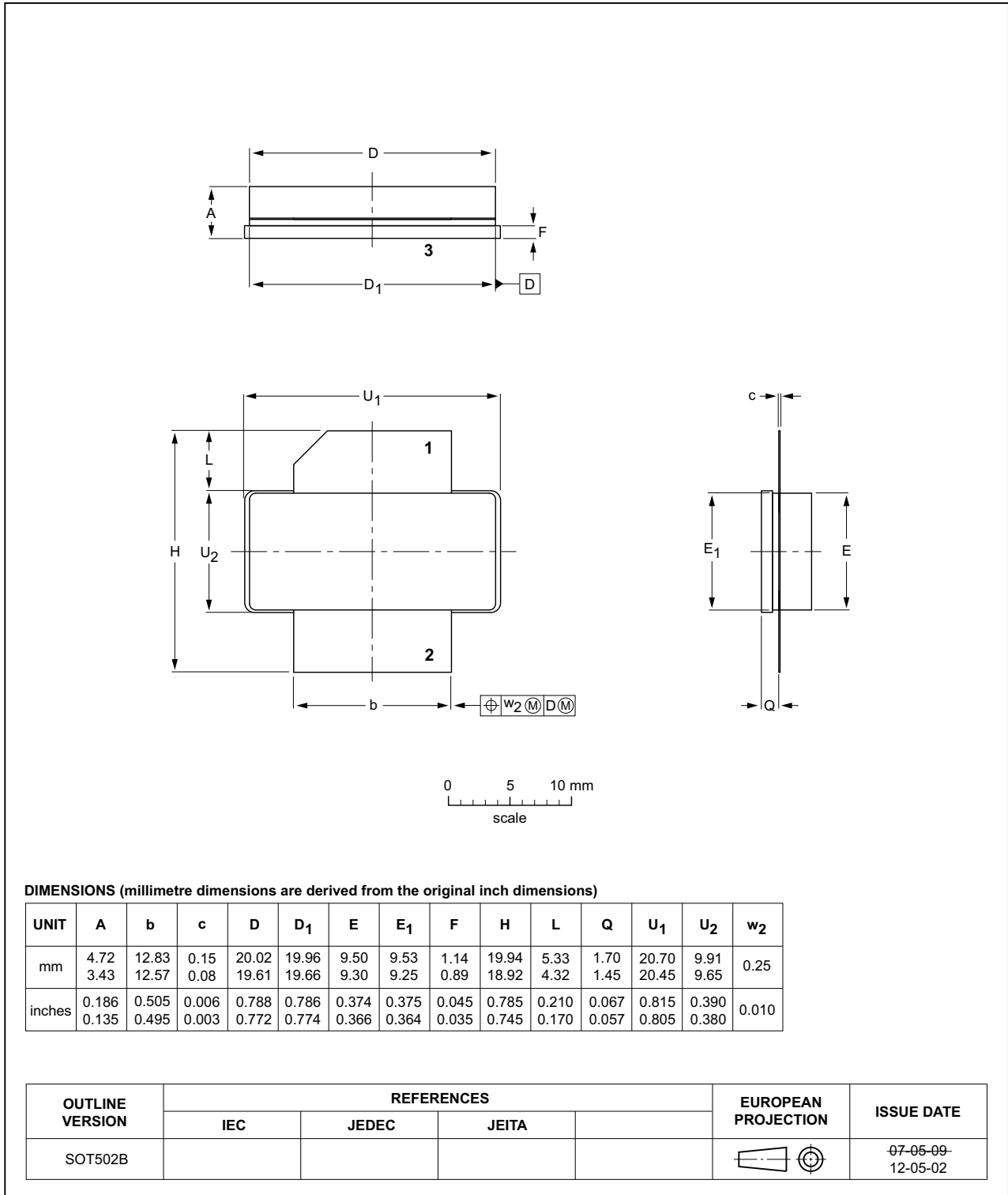


Fig 12. Package outline SOT502B

9. Handling information


CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

- [1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V, but fails after exposure to an ESD pulse of 500 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF0910H6L500_H6LS500 v.2	20170413	Product data sheet	-	BLF0910H6L500_H6LS500 v.1
Modifications:	<ul style="list-style-type: none"> • Table 8 on page 3: corrected GHz to MHz 			
BLF0910H6L500_H6LS500 v.1	20161202	Product data sheet	-	-

12. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1 **Product profile** 1

1.1 General description 1

1.2 Features and benefits 1

1.3 Applications 1

2 **Pinning information** 2

3 **Ordering information** 2

4 **Limiting values** 2

5 **Thermal characteristics** 2

6 **Characteristics** 3

7 **Test information** 3

7.1 Ruggedness in class-AB operation 3

7.2 Impedance information 3

7.3 Test circuit 4

7.4 Graphical data 5

8 **Package outline** 8

9 **Handling information** 10

10 **Abbreviations** 10

11 **Revision history** 10

12 **Legal information** 11

12.1 Data sheet status 11

12.2 Definitions 11

12.3 Disclaimers 11

12.4 Trademarks 12

13 **Contact information** 12

14 **Contents** 13

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