



Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 250mW (max)
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SETTLING TIME:** 10 μ s to 0.012%
- **12-BIT LINEARITY AND MONOTONICITY:** -40°C to $+85^{\circ}\text{C}$
- **DOUBLE-BUFFERED DATA INPUTS**
- **SMALL SO-16 PACKAGE**

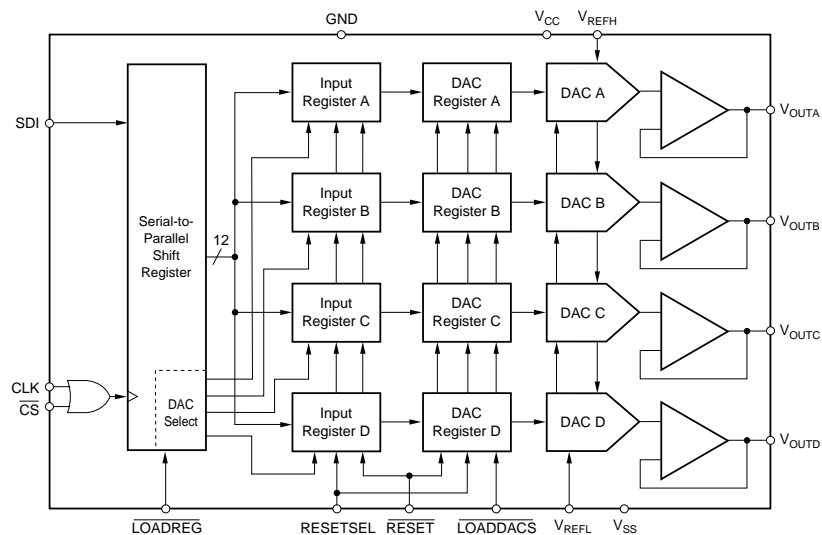
APPLICATIONS

- **PROCESS CONTROL**
- **ATE PIN ELECTRONICS**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7715 is a quad, serial input, 12-bit, voltage output Digital-to-Analog Converter (DAC) with guaranteed 12-bit monotonic performance over the -40°C to $+85^{\circ}\text{C}$ temperature range. An asynchronous reset clears all registers to either mid-scale (800_{H}) or zero-scale (000_{H}), selectable via the RESETSEL pin. The individual DAC inputs are double buffered to allow for simultaneous update of all DAC outputs. The device can be powered from a single $+15\text{V}$ supply or from dual $+15\text{V}$ and -15V supplies.

Low power and small size makes the DAC7715 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The device is available in a SO-16 package and is guaranteed over the -40°C to $+85^{\circ}\text{C}$ temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

<http://www.burr-brown.com/>  <http://www.ti.com/>

SPECIFICATIONS (Dual Supply)

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, $V_{REFL} = -10\text{V}$, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC7715U | | | DAC7715UB | | | UNITS |
|------------------------------------|------------------------------------|-------------------|-----------------|-------------------|-----------|-----|---------|------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| ACCURACY | | | | | | | | |
| Linearity Error | | | | ± 2 | | | ± 1 | LSB ⁽¹⁾ |
| Linearity Matching ⁽²⁾ | | | | ± 2 | | | ± 1 | LSB |
| Differential Linearity Error | | | | ± 1 | | | ± 1 | LSB |
| Monotonicity | T_{MIN} to T_{MAX} | 12 | | | * | | | Bits |
| Zero-Scale Error | Code = 000 _H | | | ± 2 | | | * | LSB |
| Zero-Scale Drift | | | 1 | | | * | | ppm/ $^\circ\text{C}$ |
| Zero-Scale Matching ⁽²⁾ | | | | ± 2 | | | ± 1 | LSB |
| Full-Scale Error | Code = FFF _H | | | ± 2 | | | * | LSB |
| Full-Scale Matching ⁽²⁾ | | | | ± 2 | | | ± 1 | LSB |
| Power Supply Sensitivity | At Full Scale | | 10 | | | * | | ppm/V |
| ANALOG OUTPUT | | | | | | | | |
| Voltage Output ⁽³⁾ | | V_{REFL} | | V_{REFH} | * | | * | V |
| Output Current | | -5 | | +5 | * | | * | mA |
| Load Capacitance | No Oscillation | | 500 | | | * | | pF |
| Short-Circuit Current | | | ± 20 | | | * | | mA |
| Short-Circuit Duration | To V_{SS} , V_{CC} , or GND | | Indefinite | | | * | | |
| REFERENCE INPUT | | | | | | | | |
| V_{REFH} Input Range | | $V_{REFL} + 1.25$ | | +10 | * | | * | V |
| V_{REFL} Input Range | | -10 | | $V_{REFH} - 1.25$ | * | | * | V |
| Ref High Input Current | | -0.5 | | 3.0 | * | | * | mA |
| Ref Low Input Current | | -3.5 | | 0 | * | | * | mA |
| DYNAMIC PERFORMANCE | | | | | | | | |
| Settling Time | To $\pm 0.012\%$, 20V Output Step | | 8 | 10 | | * | * | μs |
| Channel-to-Channel Crosstalk | Full-Scale Step | | 0.25 | | | * | | LSB |
| Digital Feedthrough | | | 2 | | | | * | nV-s |
| Output Noise Voltage | $f = 10\text{kHz}$ | | 65 | | | * | | $\text{nV}/\sqrt{\text{Hz}}$ |
| DIGITAL INPUT | | | | | | | | |
| Logic Levels | | | | | | | | |
| V_{IH} | $I_{IH} \leq \pm 10\mu\text{A}$ | 3.325 | | | * | | | V |
| V_{IL} | $I_{IL} \leq \pm 10\mu\text{A}$ | | | 1.575 | | | * | V |
| Data Format | | | Straight Binary | | | * | | |
| POWER SUPPLY REQUIREMENTS | | | | | | | | |
| V_{CC} | | +14.25 | | +15.75 | * | | * | V |
| V_{SS} | | -15.75 | | -14.25 | * | | * | V |
| I_{CC} | | | 6 | 8.5 | | * | * | mA |
| I_{SS} | | -8 | -6 | | * | * | * | mA |
| Power Dissipation | | | 180 | 250 | | * | * | mW |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | -40 | | +85 | * | | * | $^\circ\text{C}$ |

NOTES: (1) LSB means Least Significant Bit; if V_{REFH} equals +10V and V_{REFL} equals -10V, then one LSB equals 4.88mV. (2) All DAC outputs will match within the specified error band. (3) Ideal output voltage does not take into account zero or full-scale error.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS (Single Supply)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +15\text{V}$, $V_{SS} = \text{GND}$, $V_{REFH} = +10\text{V}$, $V_{REFL} = 0\text{V}$, unless otherwise noted.

| PARAMETER | CONDITIONS | DAC7715U | | | DAC7715UB | | | UNITS |
|------------------------------------|---------------------------------|-------------------|------------|-------------------|-----------|-----|-----|--------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| ACCURACY | | | | | | | | |
| Linearity Error ⁽¹⁾ | | | | ±2 | | | ±1 | LSB ⁽²⁾ |
| Linearity Matching ⁽³⁾ | | | | ±2 | | | ±1 | LSB |
| Differential Linearity Error | | | | ±1 | | | ±1 | LSB |
| Monotonicity | T_{MIN} to T_{MAX} | 12 | | | * | | | Bits |
| Zero-Scale Error | Code = 004 _H | | | ±4 | | | * | LSB |
| Zero-Scale Drift | | | 2 | | | * | | ppm/°C |
| Zero-Scale Matching ⁽³⁾ | | | | ±4 | | | ±2 | LSB |
| Full-Scale Error | Code = FFF _H | | | ±4 | | | * | LSB |
| Full-Scale Matching ⁽³⁾ | | | | ±4 | | | ±2 | LSB |
| Power Supply Sensitivity | At Full Scale | | 20 | | | * | | ppm/V |
| ANALOG OUTPUT | | | | | | | | |
| Voltage Output ⁽⁴⁾ | | V_{REFL} | | V_{REFH} | * | | * | V |
| Output Current | | -5 | | +5 | * | | * | mA |
| Load Capacitance | No Oscillation | | 500 | | | * | | pF |
| Short-Circuit Current | | | ±20 | | | * | | mA |
| Short-Circuit Duration | To V_{CC} or GND | | Indefinite | | | * | | |
| REFERENCE INPUT | | | | | | | | |
| V_{REFH} Input Range | | $V_{REFL} + 1.25$ | | +10 | * | | * | V |
| V_{REFL} Input Range | | 0 | | $V_{REFH} - 1.25$ | * | | * | V |
| Ref High Input Current | | -0.3 | | 1.5 | * | | * | mA |
| Ref Low Input Current | | -2.0 | | 0 | * | | * | mA |
| DYNAMIC PERFORMANCE | | | | | | | | |
| Settling Time ⁽⁵⁾ | To ±0.012%, 10V Output Step | | 8 | 10 | | * | * | µs |
| Channel-to-Channel Crosstalk | | | 0.25 | | | * | * | LSB |
| Digital Feedthrough | | | 2 | | | | * | nV-s |
| Output Noise Voltage | f = 10kHz | | 65 | | | * | | nV/√Hz |
| DIGITAL INPUT | | | | | | | | |
| Logic Levels | | | | | | | | |
| V_{IH} | $I_{IH} \leq \pm 10\mu\text{A}$ | 3.325 | | | * | | | V |
| V_{IL} | $I_{IL} \leq \pm 10\mu\text{A}$ | | | 1.575 | | | * | V |
| Data Format | | Straight Binary | | | | * | | |
| POWER SUPPLY REQUIREMENTS | | | | | | | | |
| V_{CC} | | 14.25 | | 15.75 | * | | * | V |
| I_{CC} | | | 3.0 | | | * | * | mA |
| Power Dissipation | | | 45 | | | * | | mW |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | -40 | | +85 | * | | * | °C |

NOTES: (1) If $V_{SS} = 0\text{V}$, specification applies at code 004_H and above. (2) LSB means Least Significant Bit; if V_{REFH} equals +10V and V_{REFL} equals 0V, then one LSB equals 2.44mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage does not take into account zero or full-scale error. (5) Full-scale positive 10V step and negative step from code FFF_H to 020_H.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|-----------------|
| V_{CC} to V_{SS} | -0.3V to +32V |
| V_{CC} to GND | -0.3V to +16V |
| V_{SS} to GND | +0.3V to -16V |
| V_{REFH} to GND | -9V to +11V |
| V_{REFL} to GND ($V_{SS} = -15V$) | -11V to +9V |
| V_{REFL} to GND ($V_{SS} = 0V$) | -0.3V to +9V |
| V_{REFH} to V_{REFL} | -1V to +22V |
| Digital Input Voltage to GND | -0.3V to 5.8V |
| Digital Output Voltage to GND | -0.3V to 5.8V |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

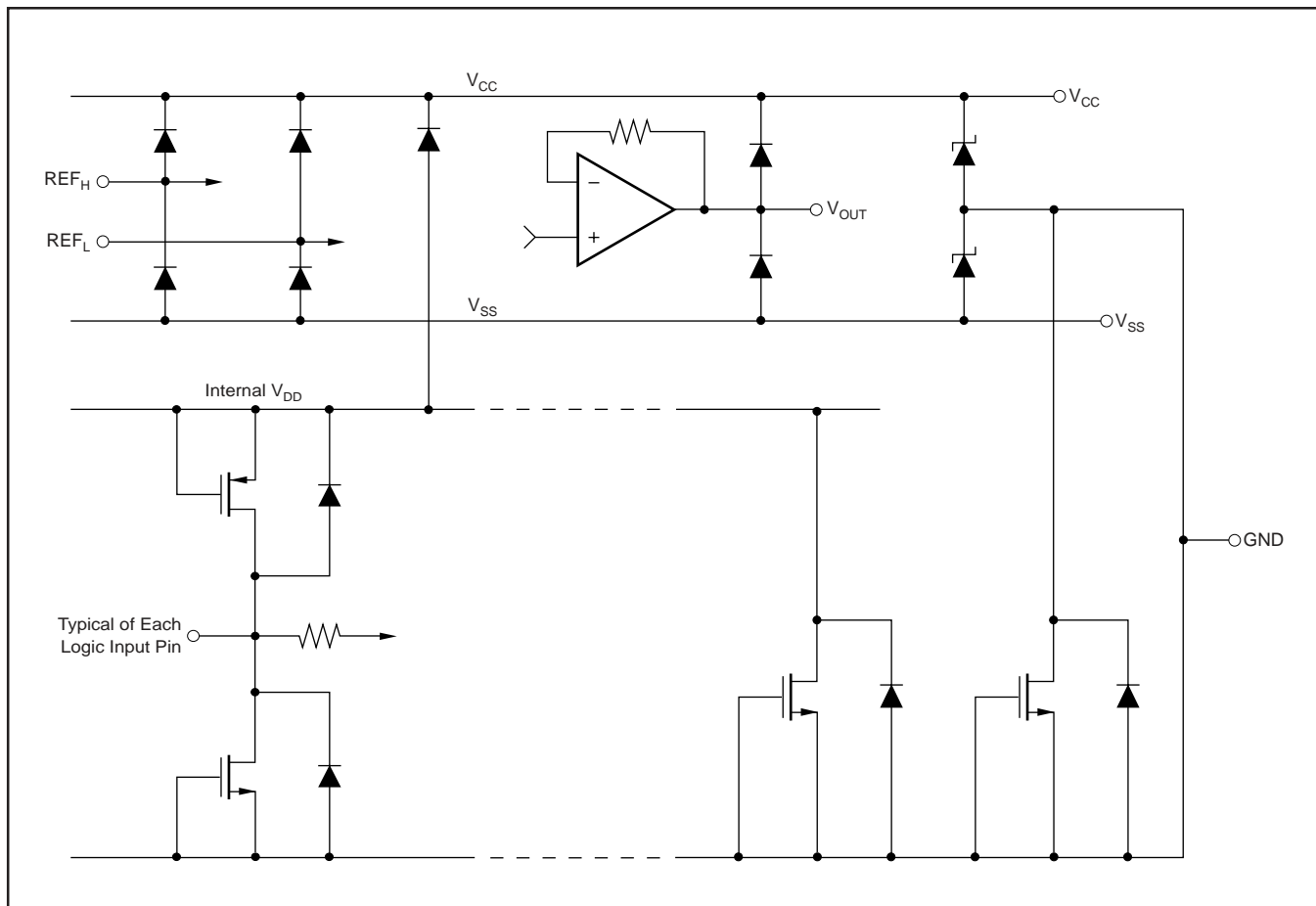
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

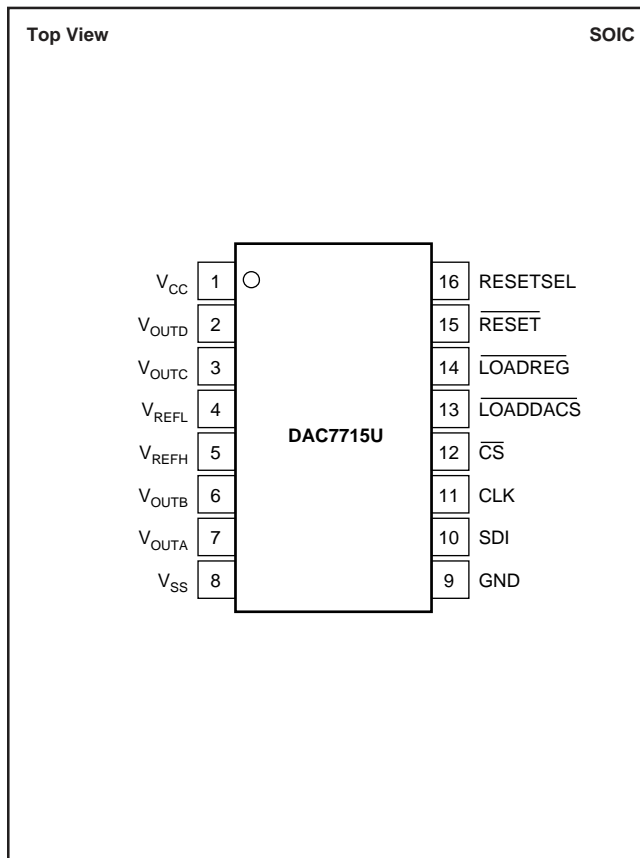
| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFICATION TEMPERATURE RANGE | ORDERING NUMBER ⁽¹⁾ | TRANSPORT MEDIA |
|-----------|-------------------------------|--------------------------------------|---------|------------------------|---------------------------------|--------------------------------|-----------------|
| DAC7715U | ±2 | ±1 | SOIC-16 | 211 | -40°C to +85°C | DAC7715U | Rails |
| " | " | " | " | " | " | DAC7715U/1K | Tape and Reel |
| DAC7715UB | ±1 | ±1 | SOIC-16 | 211 | -40°C to +85°C | DAC7715UB | Rails |
| " | " | " | " | " | " | DAC7715UB/1K | Tape and Reel |

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7715UB/1K" will get a single 1000-piece Tape and Reel.

ESD PROTECTION CIRCUITS



PIN CONFIGURATION—U Package



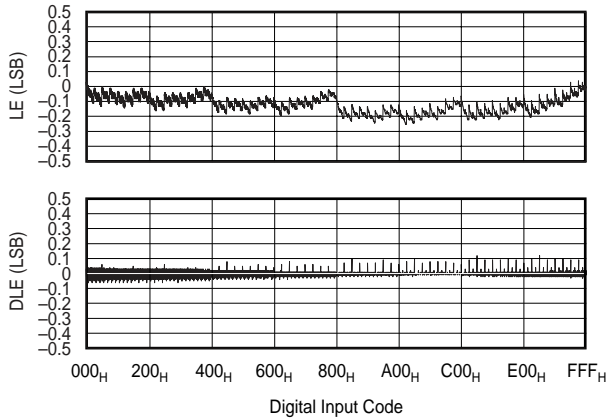
PIN DESCRIPTIONS—U Package

| PIN | LABEL | DESCRIPTION |
|-----|------------------------------|--|
| 1 | V _{CC} | Positive Supply Voltage, +15V nominal. |
| 2 | V _{OUTD} | DAC D Voltage Output |
| 3 | V _{OUTC} | DAC C Voltage Output |
| 4 | V _{REFL} | Reference Input Voltage Low. Sets minimum output voltage for all DACs. |
| 5 | V _{REFH} | Reference Input Voltage High. Sets maximum output voltage for all DACs. |
| 6 | V _{OUTB} | DAC B Voltage Output |
| 7 | V _{OUTA} | DAC A Voltage Output |
| 8 | V _{SS} | Negative Supply Voltage, 0V or -15V nominal. |
| 9 | GND | Ground |
| 10 | SDI | Serial Data Input |
| 11 | CLK | Serial Data Clock |
| 12 | $\overline{\text{CS}}$ | Chip Select Input |
| 13 | $\overline{\text{LOADDACS}}$ | All DAC registers become transparent when $\overline{\text{LOADDACS}}$ is LOW. They are in the latched state when $\overline{\text{LOADDACS}}$ is HIGH. |
| 14 | $\overline{\text{LOADREG}}$ | The selected input register becomes transparent when $\overline{\text{LOADREG}}$ is LOW. It is in the latched state when $\overline{\text{LOADREG}}$ is HIGH. |
| 15 | $\overline{\text{RESET}}$ | Asynchronous Reset Input. Sets DAC and input registers to either zero-scale (000 _H) or mid-scale (800 _H) when LOW. RESETSEL determines which code is active. |
| 16 | RESETSEL | When LOW, a LOW on $\overline{\text{RESET}}$ will cause the DAC and input registers to be set to code 000 _H . When RESETSEL is HIGH, a LOW on $\overline{\text{RESET}}$ will set the registers to code 800 _H . |

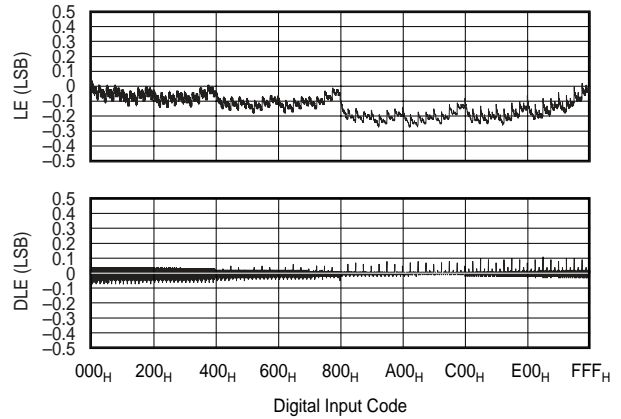
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.

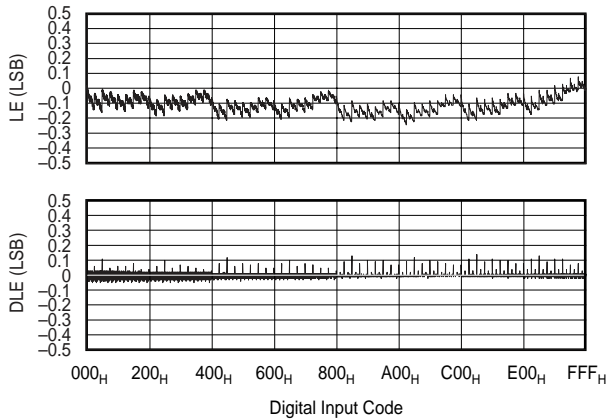
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



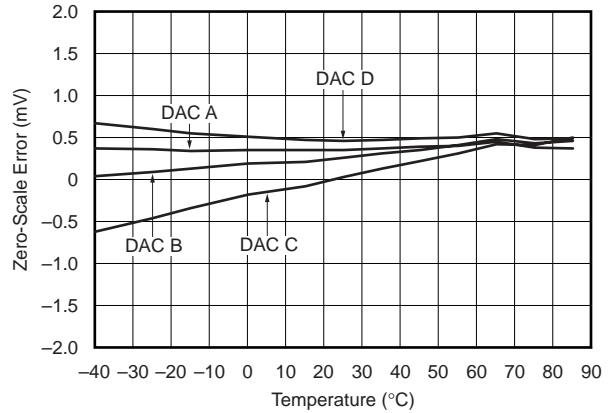
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



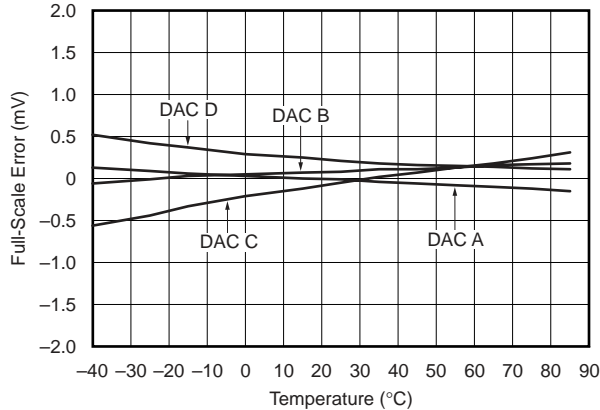
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel -40°C
(Typical of Each Output Channel)



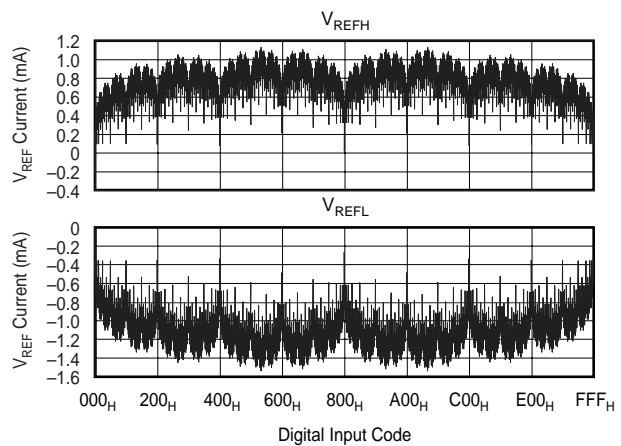
ZERO-SCALE ERROR vs TEMPERATURE
(Code 004_H)



FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)

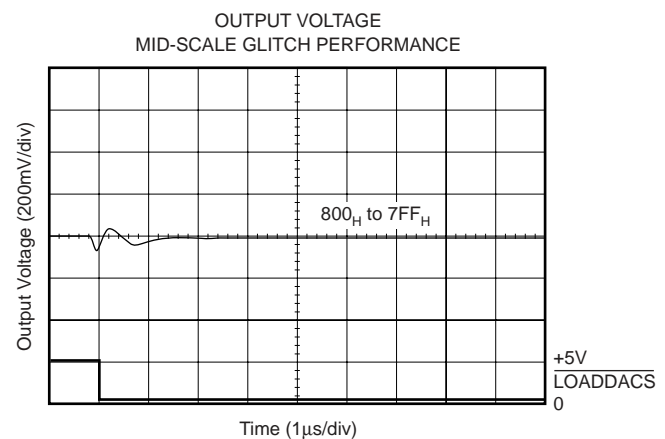
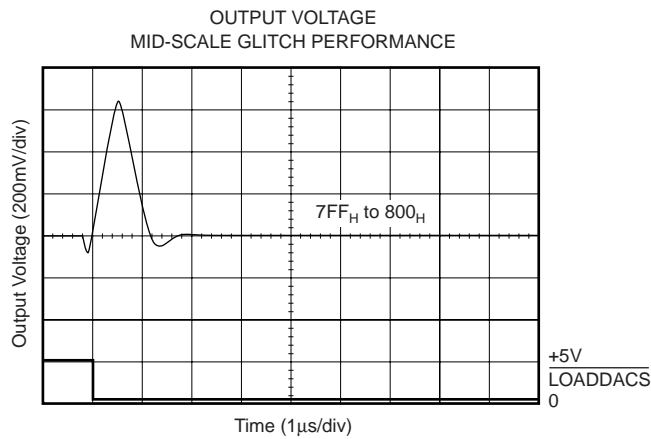
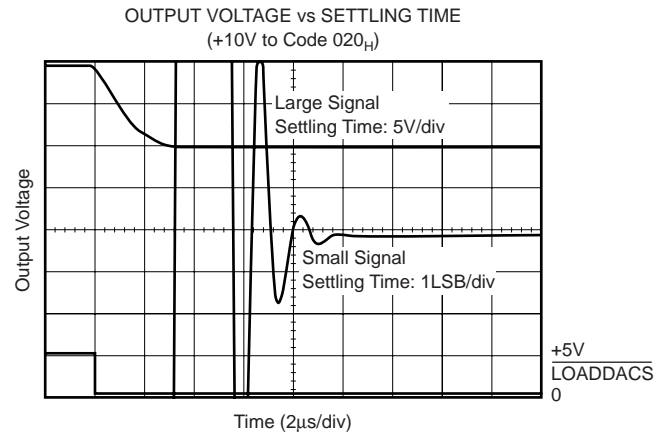
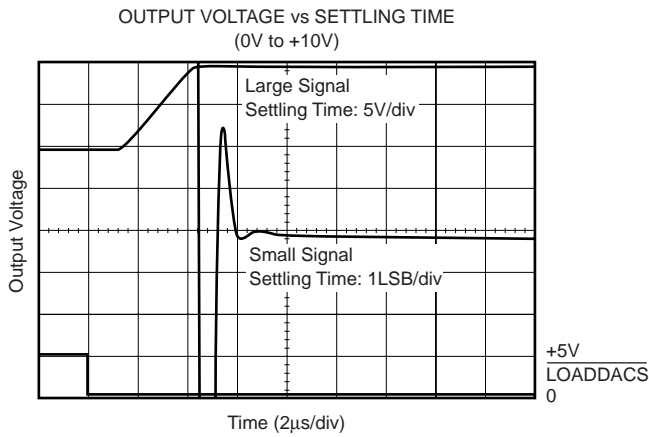
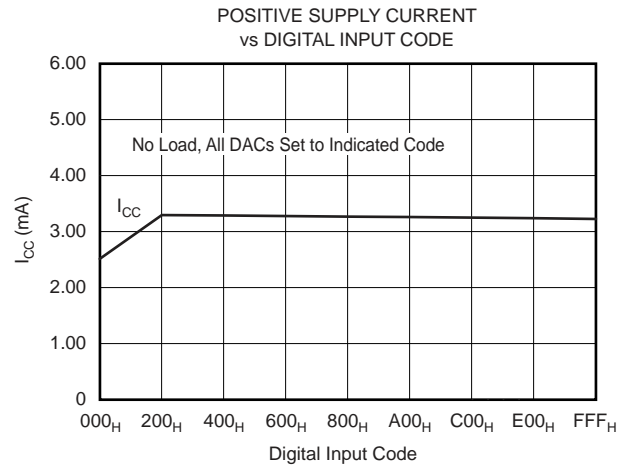
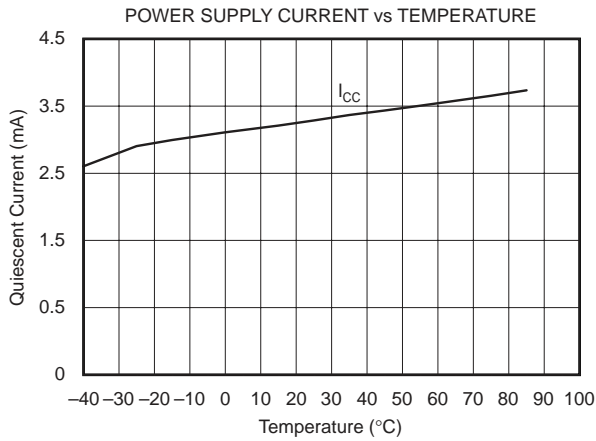


CURRENT vs CODE
All DACs Set to Indicated Code



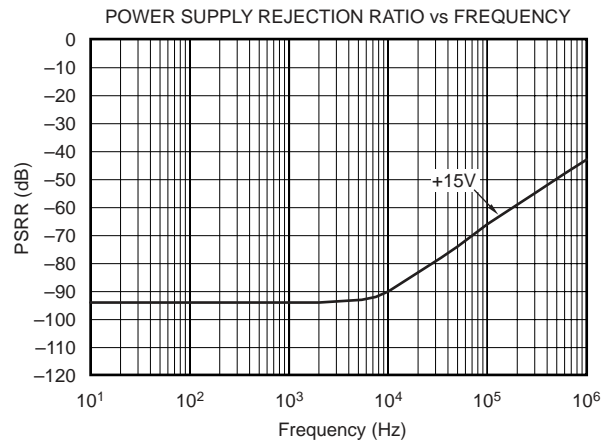
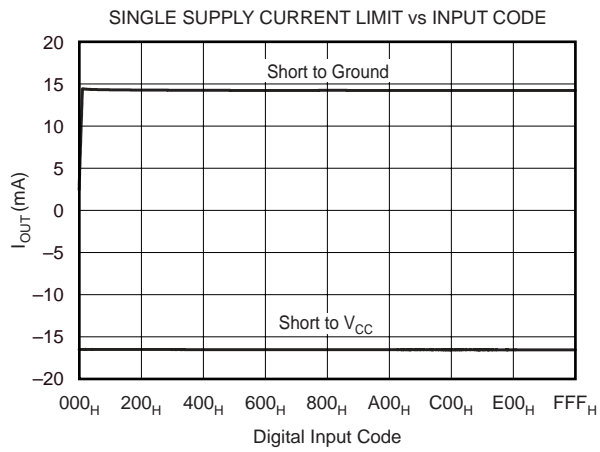
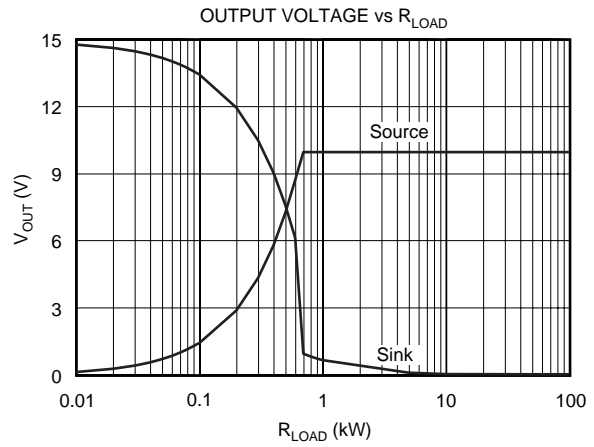
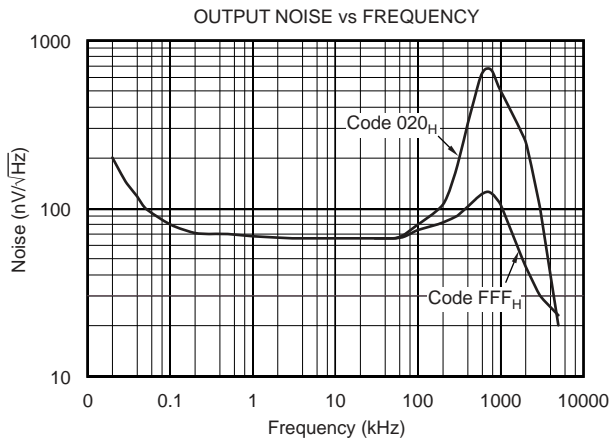
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

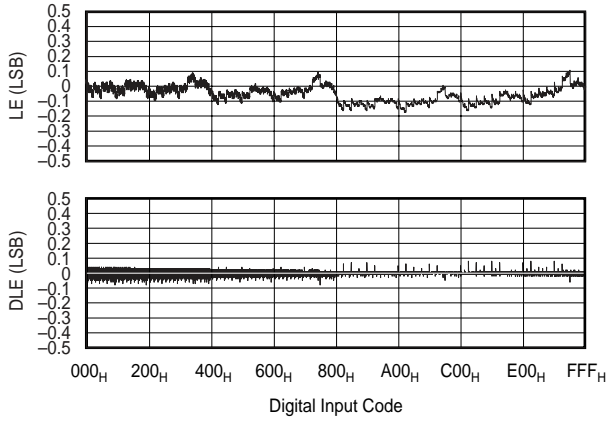
At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



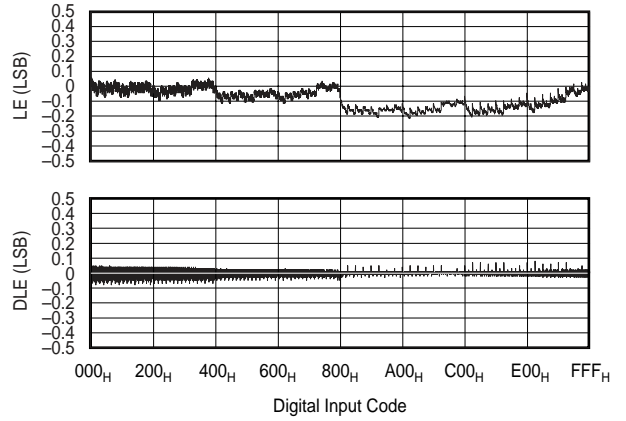
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.

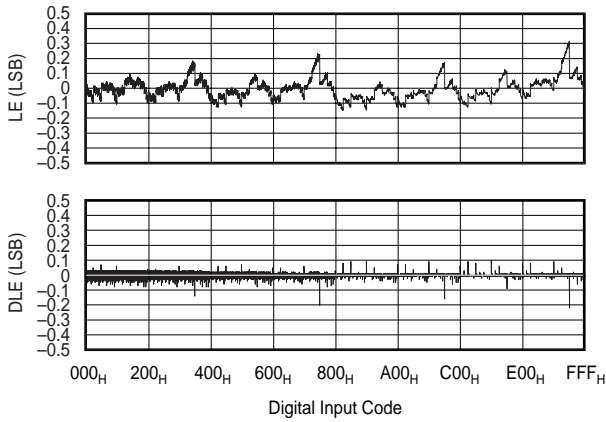
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



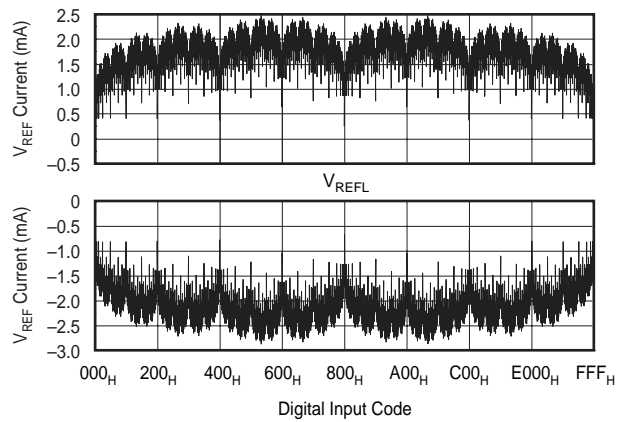
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



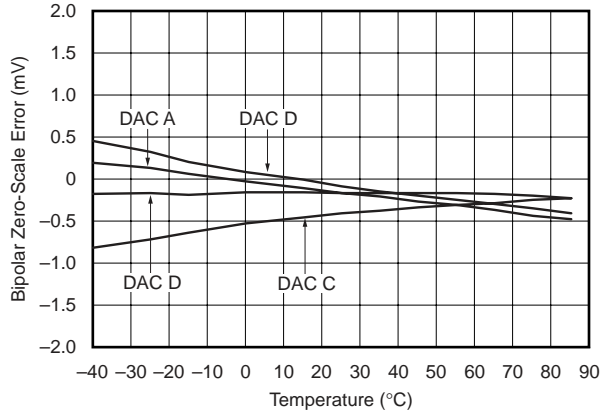
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel -40°C
(Typical of Each Output Channel)



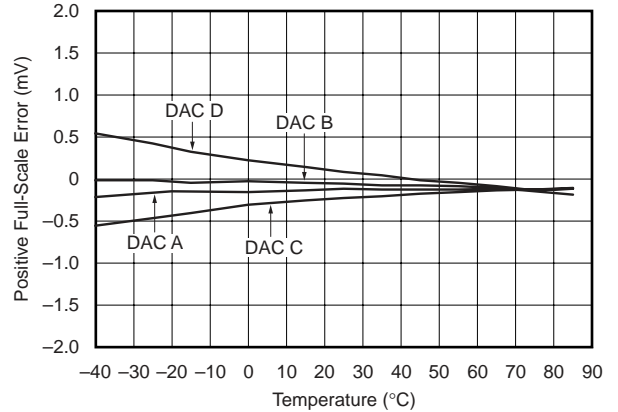
CURRENT vs CODE
All DACs Set to Indicated Code



BIPOLAR ZERO-SCALE ERROR vs TEMPERATURE
(Code 800H)

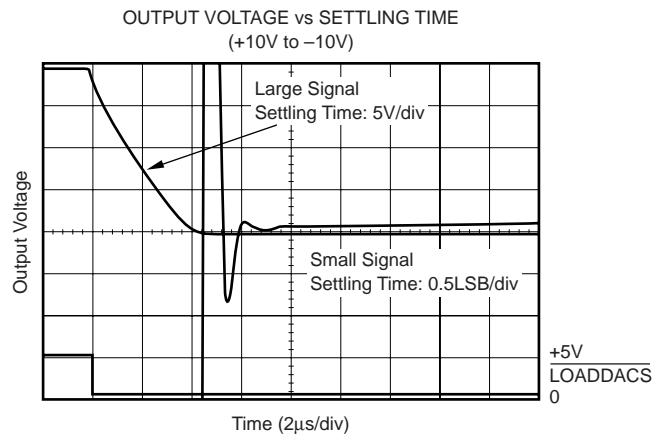
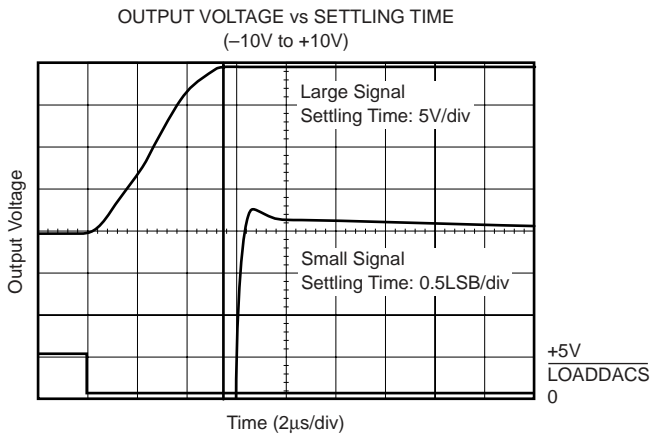
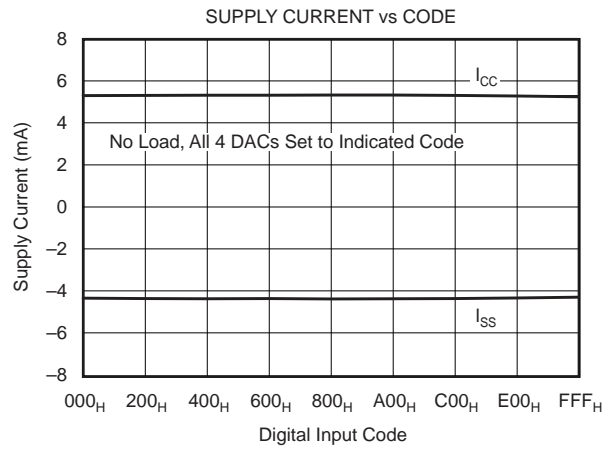
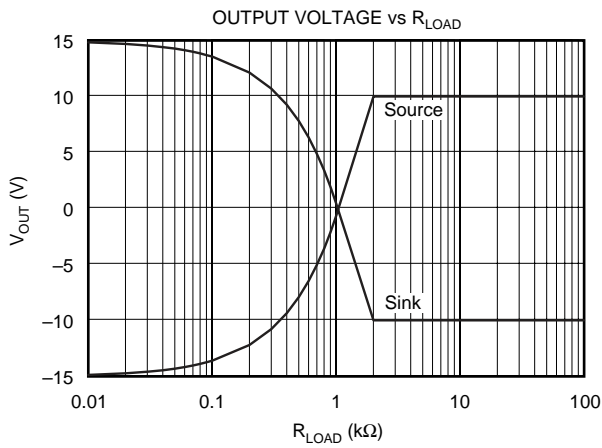
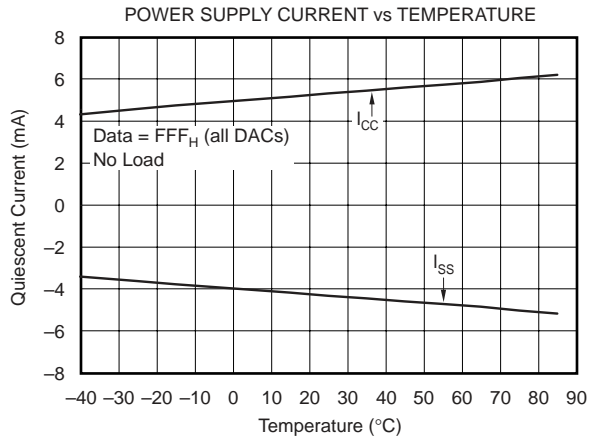
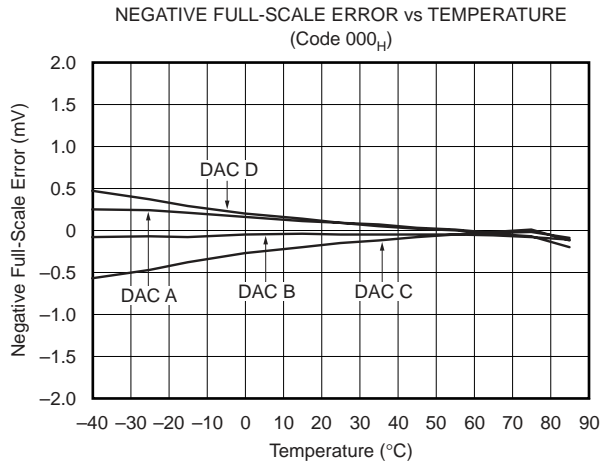


POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code FFFH)



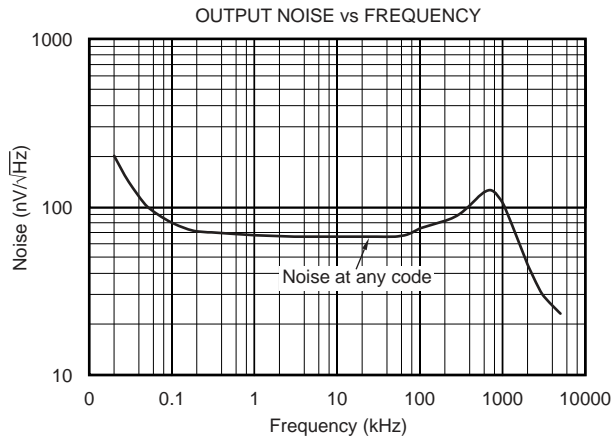
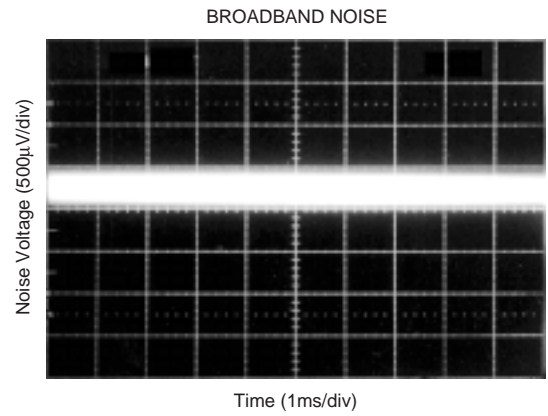
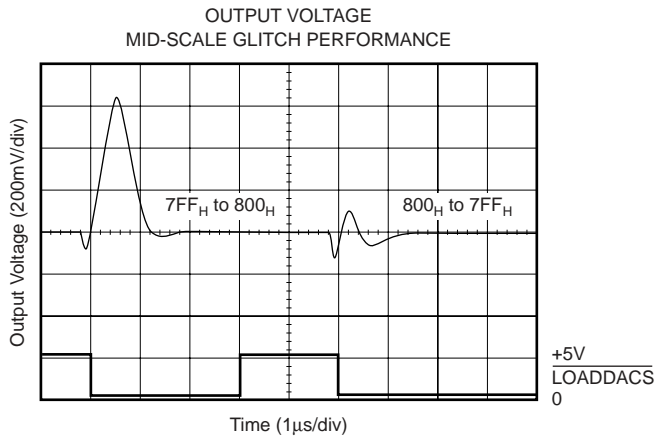
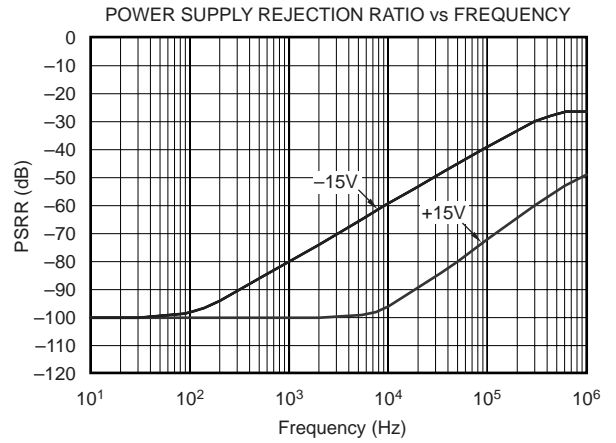
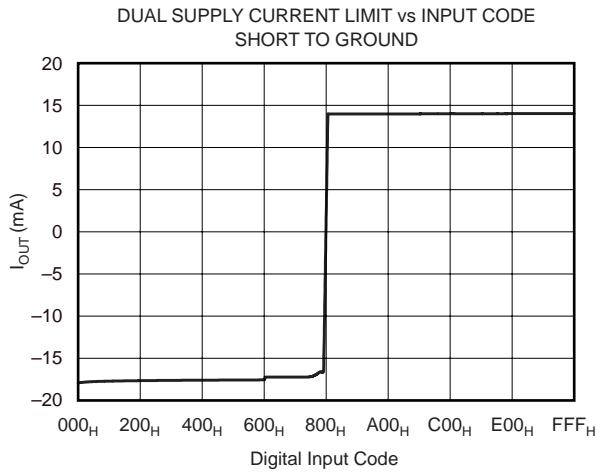
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7715 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer, as shown in Figure 1. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs. The minimum voltage output (“zero-scale”) and maximum voltage output (“full-scale”) are set by external voltage references (V_{REFL} and V_{REFH} , respectively). The

digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +15V supply or a dual ±15V supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000_H) or mid-scale (code 800_H). The reset code is selected by the state of the RESETSEL pin (LOW = 000_H, HIGH = 800_H). See Figures 2 and 3 for the basic operation of the DAC7715.

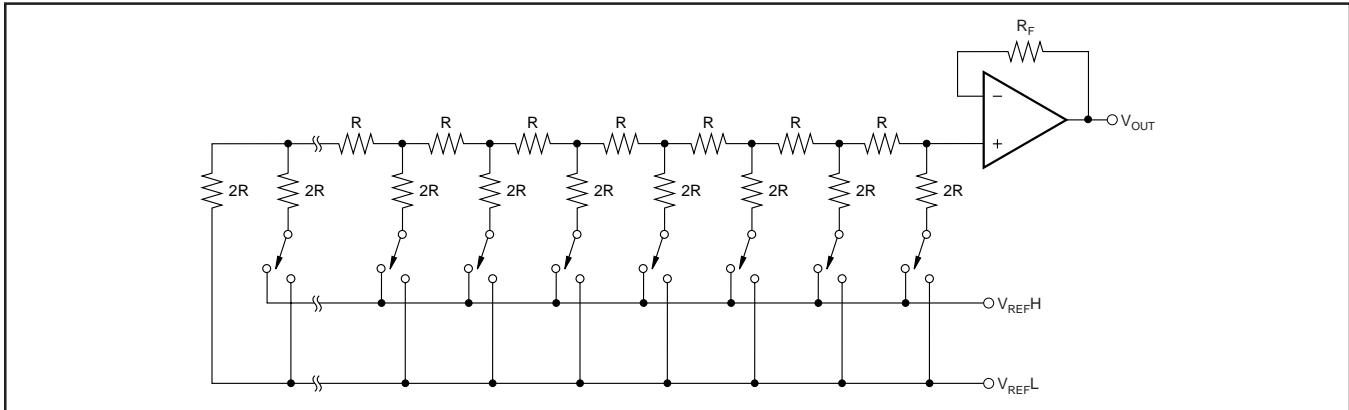


FIGURE 1. DAC7715 Architecture.

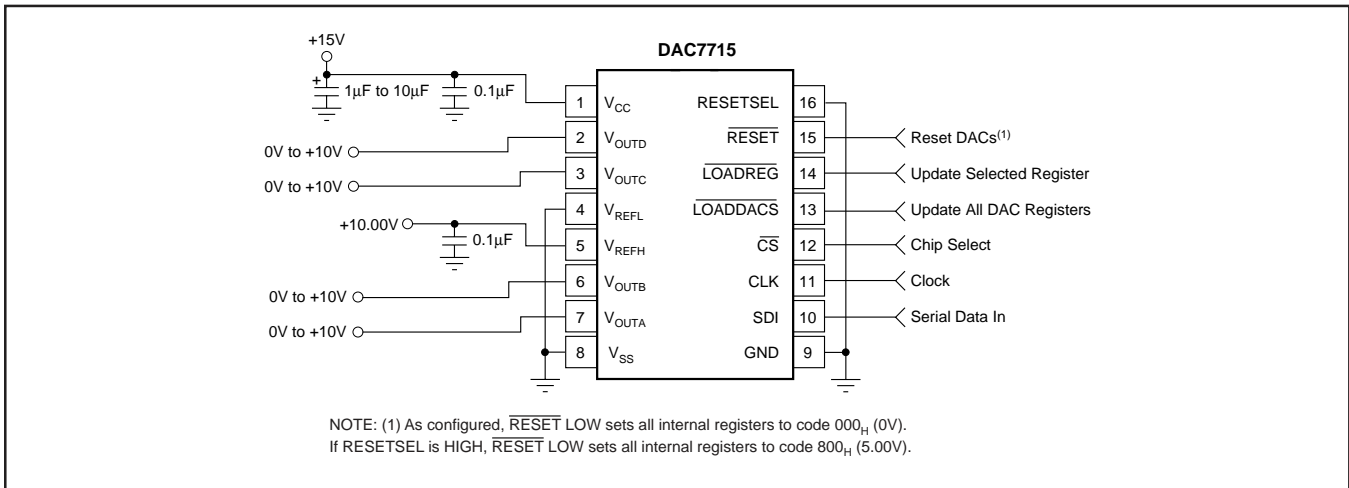


FIGURE 2. Basic Single-Supply Operation of the DAC7715.

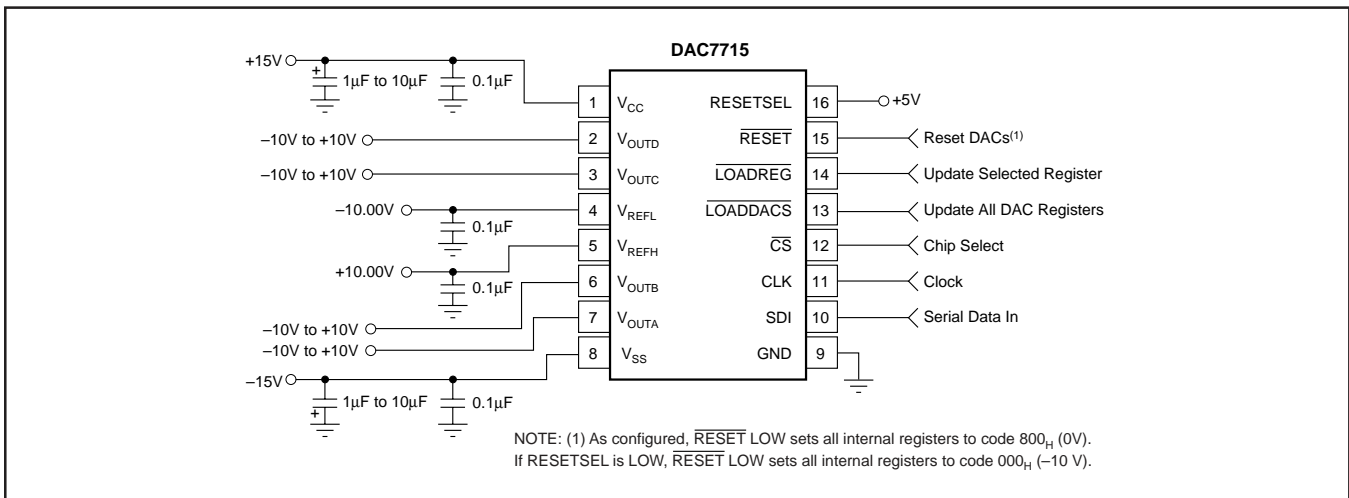


FIGURE 3. Basic Dual-Supply Operation of the DAC7715.

ANALOG OUTPUTS

When $V_{SS} = -15V$ (dual supply operation), the output amplifier can swing to within 4V of the supply rails, over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range. With $V_{SS} = 0V$ (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Also, care must be taken when measuring the zero-scale error when $V_{SS} = 0V$. If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) since the output voltage cannot swing below ground.

At the negative offset limit of $-4LSB$ ($-9.76mV$), for the single-supply case, the first specified output starts at code 004_H.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 4V$ and $V_{CC} - 4V$ provided that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to $V_{REFL} - 1LSB$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or be in the range of $-14.75V$ to $-15.25V$. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to

approximately 3mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. See "Reference Current vs Code" in the Typical Performance Curves.

The analog supplies must come up before the reference power supplies, if they are separate. If the power supplies for the references come up first, then the V_{CC} and V_{SS} supplies will be powered from the reference via the ESD protection diodes (see page 4).

DIGITAL INTERFACE

Figure 4 and Table I provide the basic timing for the DAC7715. The interface consists of a serial clock (CLK), serial data (SDI), a load register signal ($\overline{LOADREG}$), and a

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|------------|---|-----|-----|-----|---------|
| t_{DS} | Data Valid to CLK Rising | 25 | | | ns |
| t_{DH} | Data Held Valid after CLK Rises | 20 | | | ns |
| t_{CH} | CLK HIGH | 30 | | | ns |
| t_{CL} | CLK LOW | 50 | | | ns |
| t_{CSS} | \overline{CS} LOW to CLK Rising | 55 | | | ns |
| t_{CSH} | CLK HIGH to \overline{CS} Rising | 15 | | | ns |
| t_{LD1} | $\overline{LOADREG}$ HIGH to CLK Rising | 40 | | | ns |
| t_{LD2} | CLK Rising to $\overline{LOADREG}$ LOW | 15 | | | ns |
| t_{LDRW} | $\overline{LOADREG}$ LOW Time | 45 | | | ns |
| t_{LDDW} | $\overline{LOADDACS}$ LOW Time | 45 | | | ns |
| t_{RSSH} | RESETSEL Valid to RESET LOW | 25 | | | ns |
| t_{RSTW} | RESET LOW Time | 70 | | | ns |
| t_s | Settling Time | 10 | | | μs |

TABLE I. Timing Specifications ($T_A = -40^{\circ}C$ to $+85^{\circ}C$).

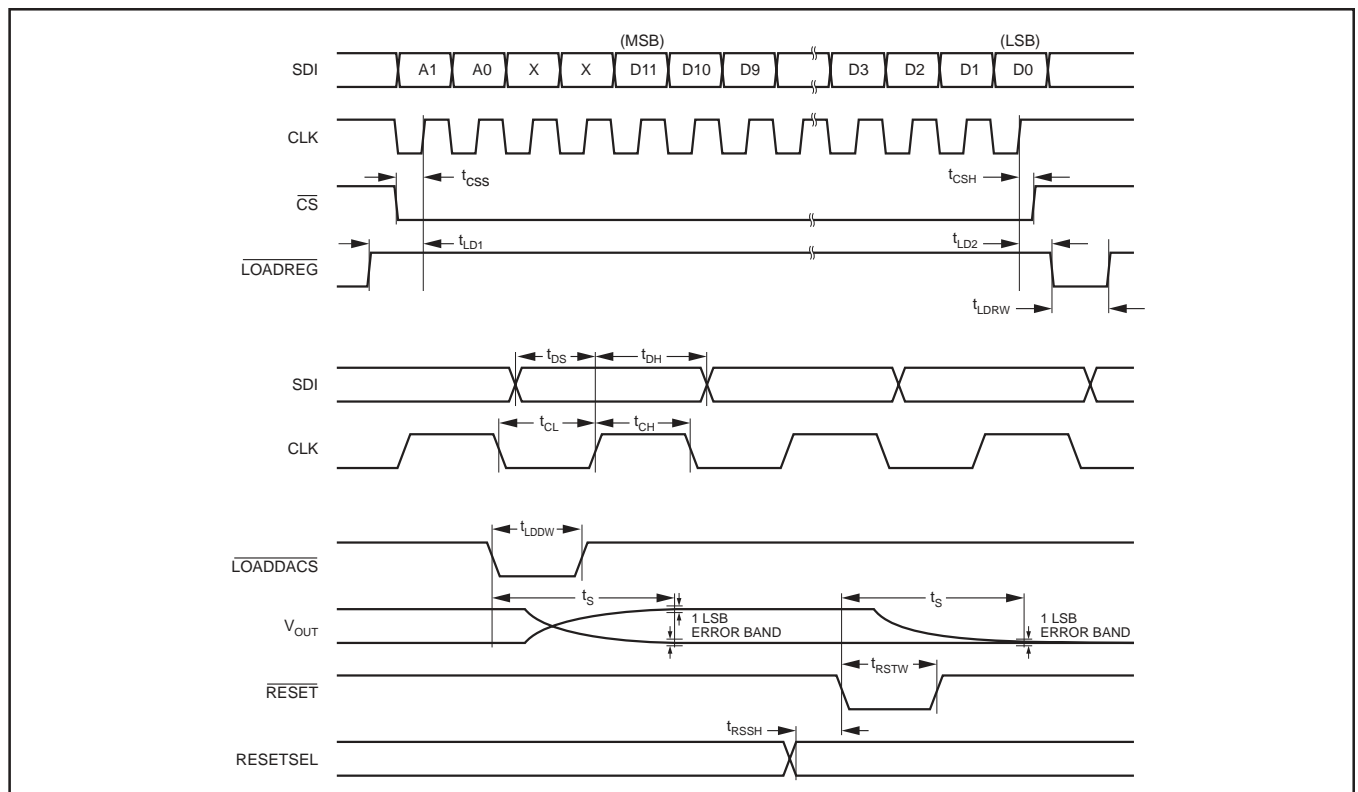


FIGURE 4. DAC7715 Timing.

| A1 | A0 | $\overline{\text{LOADREG}}$ | $\overline{\text{LOADDACS}}$ | $\overline{\text{RESET}}$ | SELECTED INPUT REGISTER | STATE OF SELECTED INPUT REGISTER | STATE OF ALL DAC REGISTERS |
|------------------|----|-----------------------------|------------------------------|---------------------------|-------------------------|----------------------------------|----------------------------|
| L ⁽¹⁾ | L | L | H ⁽²⁾ | H | A | Transparent | Latched |
| L | H | L | H | H | B | Transparent | Latched |
| H | L | L | H | H | C | Transparent | Latched |
| H | H | L | H | H | D | Transparent | Latched |
| X ⁽³⁾ | X | H | L | H | NONE | (All Latched) | Transparent |
| X | X | H | H | H | NONE | (All Latched) | Latched |
| X | X | X | X | L | ALL | Reset ⁽⁴⁾ | Reset ⁽⁴⁾ |

NOTES: (1) L = Logic LOW. (2) H = Logic HIGH. (3) X = Don't Care. (4) Resets to either 000H or 800_H, per the RESESEL state (LOW = 000_H, HIGH = 800_H). When $\overline{\text{RESET}}$ rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

| $\overline{\text{CS}}$ ⁽¹⁾ | CLK ⁽¹⁾ | $\overline{\text{LOADREG}}$ | $\overline{\text{RESET}}$ | SERIAL SHIFT REGISTER |
|---------------------------------------|--------------------|-----------------------------|---------------------------|-----------------------|
| H ⁽²⁾ | X ⁽³⁾ | H | H | No Change |
| L ⁽⁴⁾ | L | H | H | No Change |
| L | ↑ ⁽⁵⁾ | H | H | Advanced One Bit |
| ↑ | L | H | H | Advanced One Bit |
| H ⁽⁶⁾ | X | L ⁽⁷⁾ | H | No Change |
| H ⁽⁶⁾ | X | H | L ⁽⁸⁾ | No Change |

NOTES: (1) $\overline{\text{CS}}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{\text{LOADREG}}$ is LOW, the selected input register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each input register that has been erroneously selected. (8) $\overline{\text{RESET}}$ LOW causes no change in the contents of the serial shift register.

TABLE III. Serial Shift Register Truth Table.

"load all DAC registers" signal ($\overline{\text{LOADDACS}}$). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset input ($\overline{\text{RESET}}$) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

The DAC code and address are provided via a 16-bit serial interface as shown in Figure 4. The first two bits select the input register that will be updated when $\overline{\text{LOADREG}}$ goes LOW, as shown in Table II. The next two bits are not used. The last 12 bits are the DAC code which is provided, most significant bit first.

Note that $\overline{\text{CS}}$ and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7715 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of

CLK when $\overline{\text{CS}}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{\text{CS}}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register.

If both $\overline{\text{CS}}$ and CLK are used, then $\overline{\text{CS}}$ should rise only when CLK is HIGH. If not, then either $\overline{\text{CS}}$ or CLK can be used to operate the shift register. See Table III for more information.

The digital data into the DAC7715 is double-buffered. This allows new data to be entered for each DAC without disturbing the analog outputs. When the new settings have been entered into the device, all of the DAC outputs can be updated simultaneously. The transfer from the input registers to the DAC registers is accomplished with a HIGH to LOW transition on the $\overline{\text{LOADDACS}}$ input.

Because the DAC registers become transparent when $\overline{\text{LOADDACS}}$ is LOW, it is possible to keep this pin LOW and update each DAC via $\overline{\text{LOADREG}}$. However, as each new data word is entered into the device, the corresponding output will update immediately when $\overline{\text{LOADREG}}$ is taken LOW.

Digital Input Coding

The DAC7715 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{\text{OUT}} = V_{\text{REFL}} + \frac{(V_{\text{REFH}} - V_{\text{REFL}}) \cdot N}{4096}$$

where N is the digital input code (in decimal). This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As the DAC7715 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

Because the DAC7715 has a single ground pin, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would

be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to V_{DD} (as well as V_{SS} , if not grounded) should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DAC7715U | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC7715U | Samples |
| DAC7715U/1K | ACTIVE | SOIC | DW | 16 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC7715U | Samples |
| DAC7715UB | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC7715U B | Samples |
| DAC7715UB/1K | ACTIVE | SOIC | DW | 16 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC7715U B | Samples |
| DAC7715UG4 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | DAC7715U | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

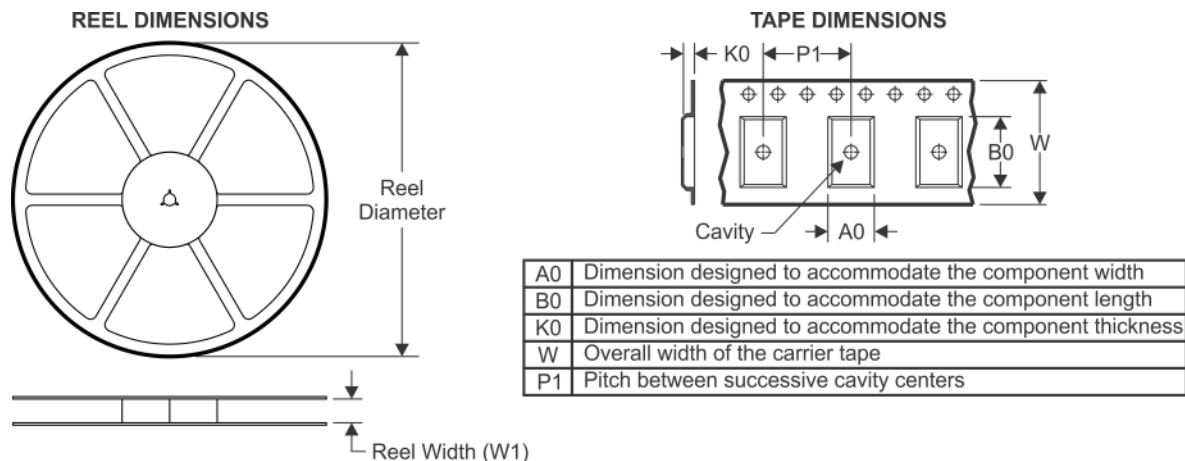
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

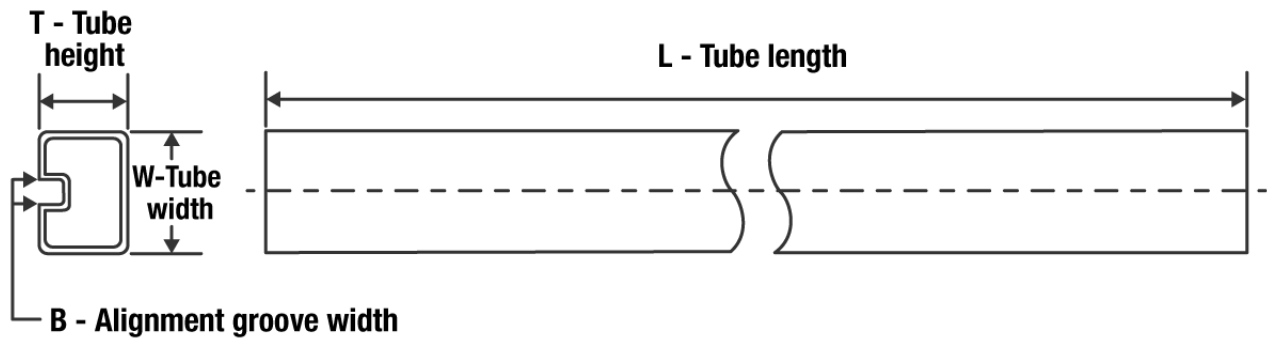

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DAC7715U/1K | SOIC | DW | 16 | 1000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| DAC7715UB/1K | SOIC | DW | 16 | 1000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DAC7715U/1K | SOIC | DW | 16 | 1000 | 350.0 | 350.0 | 43.0 |
| DAC7715UB/1K | SOIC | DW | 16 | 1000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DAC7715U | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| DAC7715UB | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| DAC7715UG4 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated