

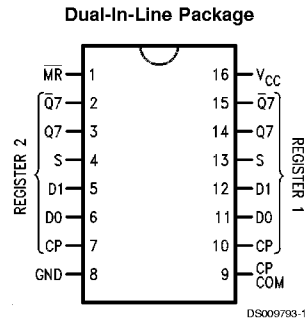
9328/DM9328 Dual 8-Bit Shift Register

General Description

The '9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both

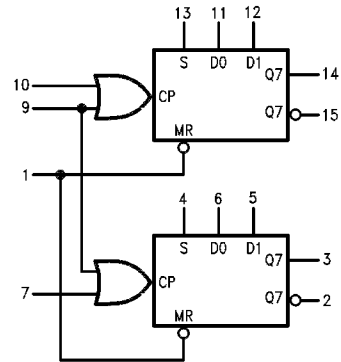
shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

Connection Diagram



Order Number 9328DMQB, 9328FMQB or DM9328N
See Package Number J16A, N16E or W16A

Logic Symbol



VCC = Pin 16
GND = Pin 8

| Pin Names | Description |
|-----------------|---|
| S | Data Select Input |
| D0, D1 | Data Inputs |
| CP | Clock Pulse Input (Active HIGH) Common (Pin 9) Separate (Pins 7 and 10) |
| \overline{MR} | Master Reset Input (Active LOW) |
| Q7 | Last Stage Output |
| $\overline{Q7}$ | Complementary Output |

Absolute Maximum Ratings (Note 1)

| | | | |
|--------------------------------------|------|---------------------------|-----------------|
| Supply Voltage | 7V | Military | -55°C to +125°C |
| Input Voltage | 5.5V | Commercial | 0°C to +70°C |
| Operating Free Air Temperature Range | | Storage Temperature Range | -65°C to +150°C |

Recommended Operating Conditions

| Symbol | Parameter | Military | | | Commercial | | | Units |
|--------------------|--------------------------------|----------|-----|------|------------|-----|------|-------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High Level Input Voltage | 2 | | | 2 | | | V |
| V _{IL} | Low Level Input Voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High Level Output Current | | | -0.4 | | | -0.4 | mA |
| I _{OL} | Low Level Output Current | | | 16 | | | 16 | mA |
| T _A | Free Air Operating Temperature | -55 | | 125 | 0 | | 70 | °C |
| t _s (H) | Setup Time HIGH or LOW | 20 | | | 20 | | | ns |
| t _s (L) | D _n to CP | 20 | | | 20 | | | ns |
| t _h (H) | Hold Time HIGH or LOW | 0 | | | 0 | | | ns |
| t _h (L) | D _n to CP | 0 | | | 0 | | | ns |
| t _w (H) | Clock Pulse Width HIGH | 25 | | | 25 | | | ns |
| t _w (L) | or LOW | 25 | | | 25 | | | ns |
| t _w (L) | MR Pulse Width with CP HIGH | 30 | | | 30 | | | ns |
| t _w (L) | MR Pulse Width with CP LOW | 40 | | | 40 | | | ns |
| t _{rec} | Recovery Time MR to CP | 33 | | | 33 | | | ns |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|-----------------|-----------------------------------|---|-----|-----------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -12 mA | | | -1.5 | V |
| V _{OH} | High Level Output Voltage | V _{CC} = Min, I _{OH} = Max V _{IL} = Max | 2.4 | 3.4 | | V |
| V _{OL} | Low Level Output Voltage | V _{CC} = Min, I _{OL} = Max V _{IH} = Min | | 0.2 | 0.4 | V |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 5.5V | | | 1 | mA |
| I _{IH} | High Level Input Current | V _{CC} = Max, V _I = 2.4V MR, D _n Inputs | | | 40 | μA |
| | | CP Inputs | | | 60 | |
| | | S Inputs | | | 80 | |
| | | CP (COM) Inputs | | | 120 | |
| I _{IL} | Low Level Input Current | V _{CC} = Max, V _I = 0.4V MR, D _n Inputs | | | -1.6 | mA |
| | | CP Inputs | | | -2.4 | |
| | | S Inputs | | | -3.2 | |
| | | CP (COM) Input | | | -4.8 | |

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted) (Continued)

| Symbol | Parameter | Conditions | | Min | Typ (Note 2) | Max | Units |
|-----------------|----------------|-----------------------------------|------|-----|-----------------|-----|-------|
| I _{OS} | Short Circuit | V _{CC} = Max (Note 3) | MIL | -20 | | -70 | mA |
| | Output Current | | COMM | -20 | | -70 | |
| I _{CC} | Supply Current | V _{CC} = Max | | | | 77 | mA |

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

| Symbol | Parameter | C _L = 15 pF R _L = 400Ω | | Units |
|------------------|---|---|-----|-------|
| | | Min | Max | |
| f _{max} | Maximum Shift Right Frequency | 20 | | MHz |
| t _{PLH} | Propagation Delay | | 20 | ns |
| t _{PHL} | CP to Q7 or $\overline{Q7}$ | | 35 | |
| t _{PHL} | Propagation Delay \overline{MR} to Q7 | | 50 | ns |

Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register

has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: S_D = SD0 + SD1

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table

| INPUTS | | | OUTPUT |
|--------|----|----|-------------------------|
| S | D0 | D1 | Q7 (t _n + δ) |
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

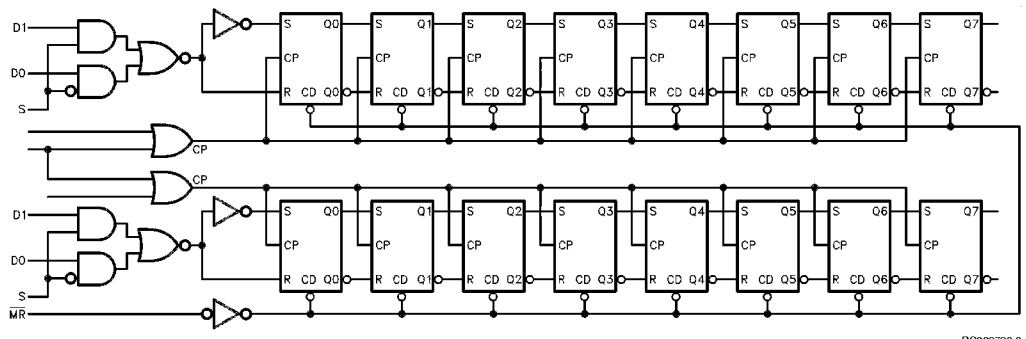
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

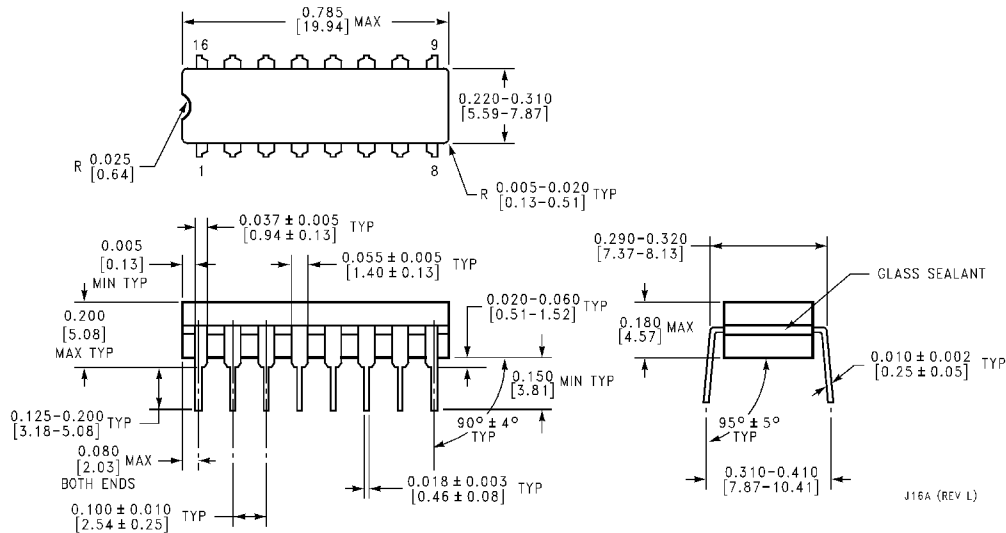
n + 8 = indicates state after eight clock pulse

Logic Diagram

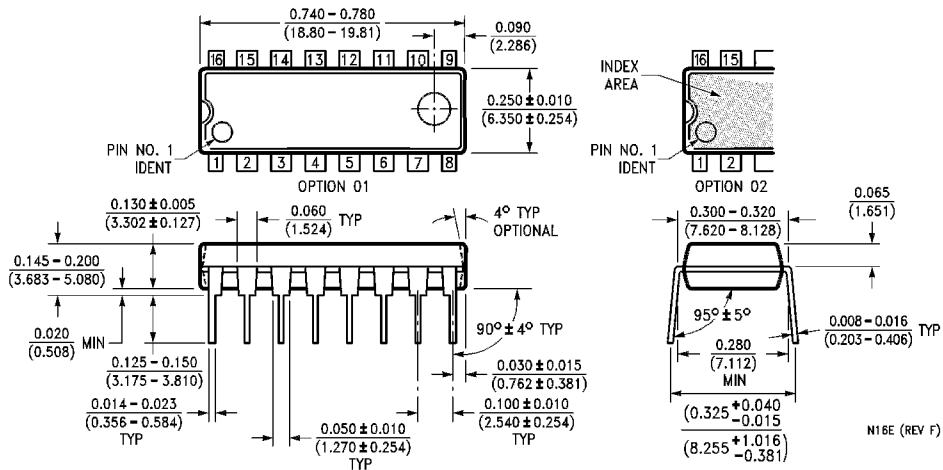


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Physical Dimensions inches (millimeters) unless otherwise noted

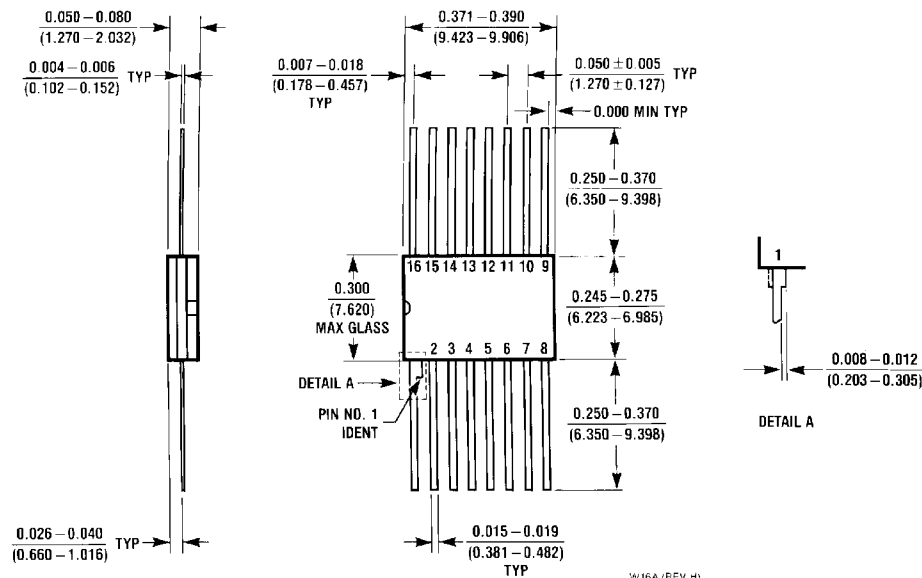


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 9328DMQB
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM9328N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 9328FMQB
Package Number W16A

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