

## Dual N-Channel 30-V (D-S) MOSFET

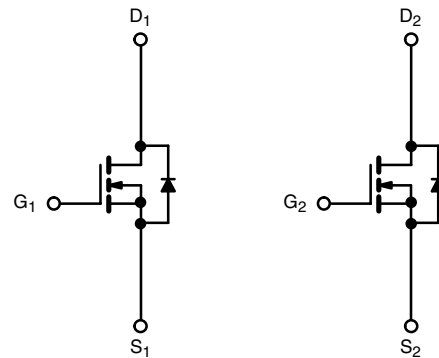
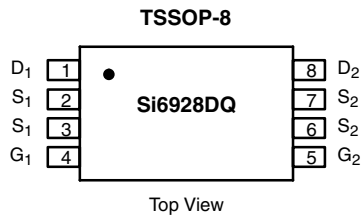
PRODUCT SUMMARY		
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.035 at $V_{GS} = 10$ V	$\pm 4.0$
	0.050 at $V_{GS} = 4.5$ V	$\pm 3.4$

### FEATURES

- Halogen-free Option Available



**RoHS\***  
COMPLIANT



N-Channel MOSFET

N-Channel MOSFET

**Ordering Information:** Si6928DQ-T1  
Si6928DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	30	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	$T_A = 25$ °C	$\pm 4.0$	A
		$T_A = 70$ °C	$\pm 3.2$	
Pulsed Drain Current	$I_{DM}$	$\pm 20$		
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.25		
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25$ °C	1.0	W
		$T_A = 70$ °C	0.64	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	125	°C/W	

Notes:

a. Surface Mounted on FR4 board,  $t \leq 10$  s.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

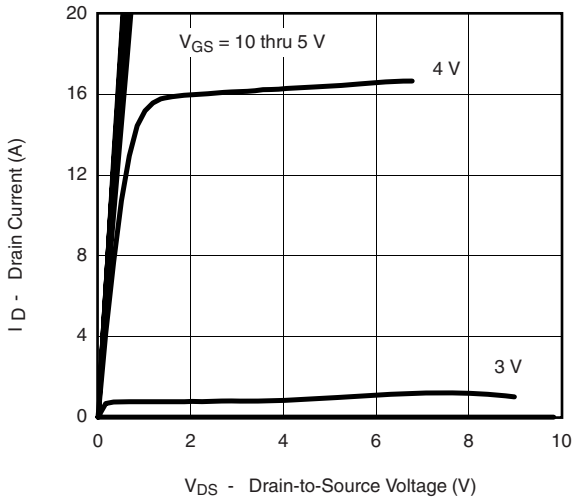
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 4.0\text{ A}$		0.027	0.035	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 3.4\text{ A}$		0.038	0.050	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 4.0\text{ A}$		13		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.25\text{ A}$ , $V_{GS} = 0\text{ V}$		0.73	1.2	V
<b>Dynamic<sup>b</sup></b>						
Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}$ , $V_{GS} = 5\text{ V}$ , $I_D = 4.0\text{ A}$		9	14	nC
Total Gate Charge	$Q_{gt}$	$V_{DS} = 15\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 4.0\text{ A}$		17.5	30	
Gate-Source Charge	$Q_{gs}$			4.0		
Gate-Drain Charge	$Q_{gd}$			2.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$ , $R_L = 6\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$		12	20	ns
Rise Time	$t_r$			9	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	$t_f$			20	40	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		25	60	

## Notes:

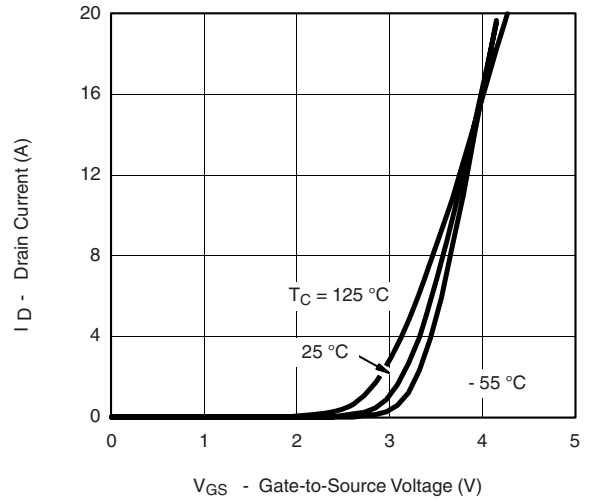
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

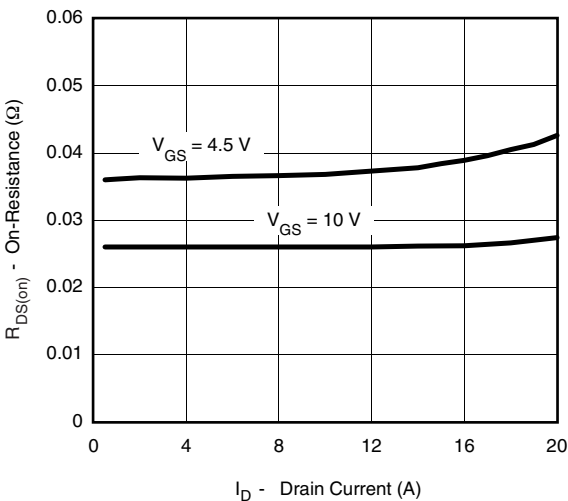
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



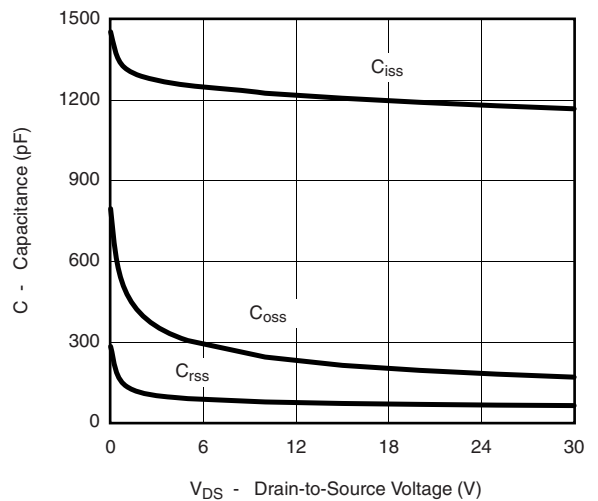
**Output Characteristics**



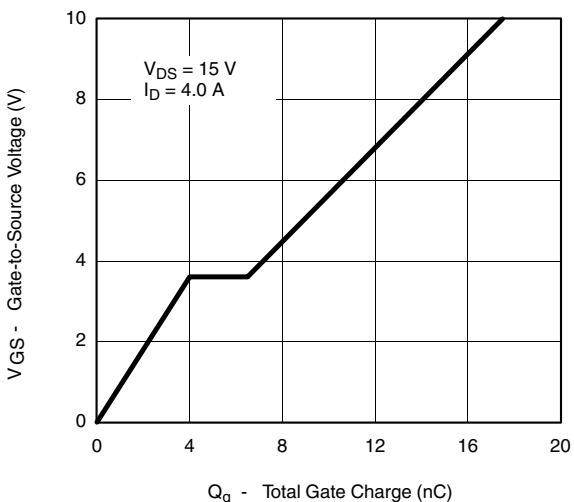
**Transfer Characteristics**



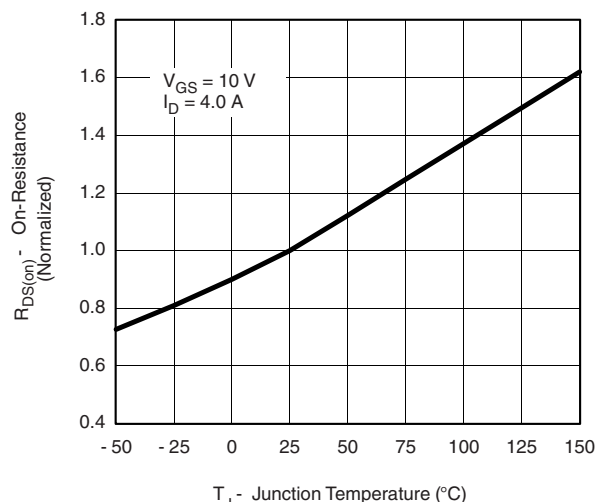
**On-Resistance vs. Drain Current**



**Capacitance**

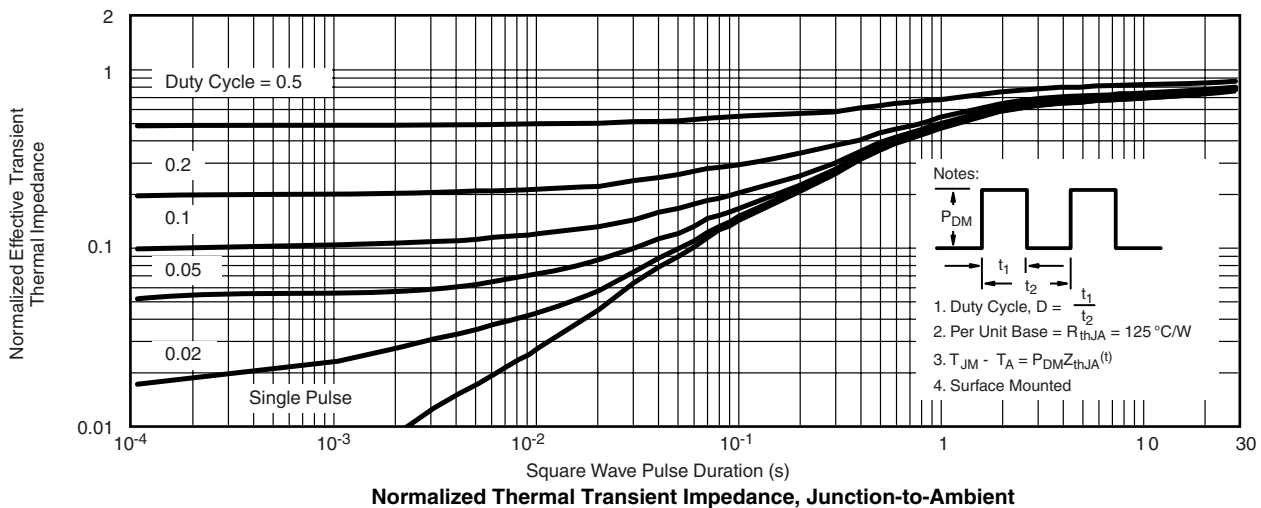
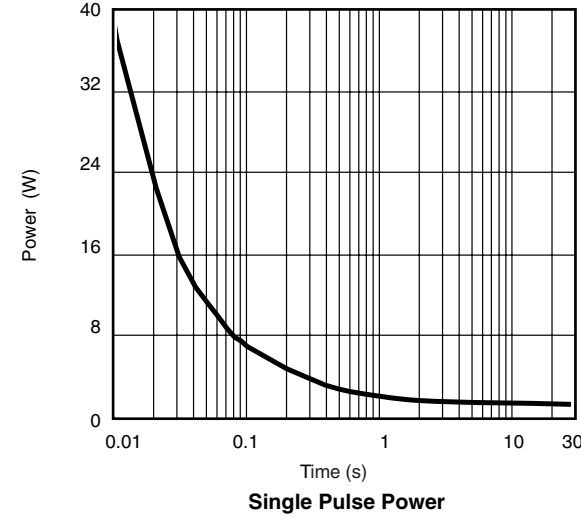
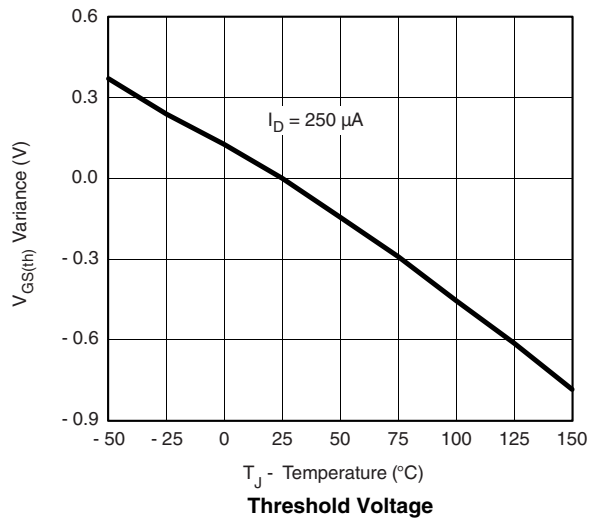
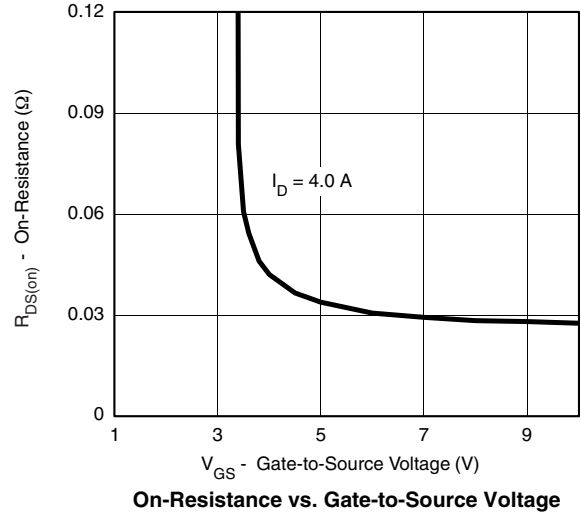
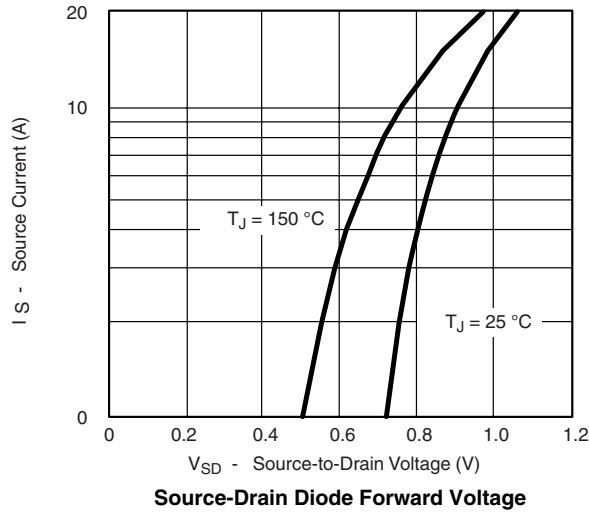


**Gate Charge**



**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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