

***TPS54610/810/910
Evaluation Module With
Ceramic Output Capacitors***

User's Guide

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Contents

1	Introduction	1-1
1.1	Background	1-2
1.2	Performance Specification Summary	1-3
1.3	Modifications	1-5
2	Test Setup and Results	2-1
2.1	Input/Output Connections	2-2
2.2	Efficiency	2-3
2.3	Power Dissipation	2-4
2.4	Output Voltage Regulation	2-5
2.5	Load Transients	2-6
2.6	Loop Characteristics	2-7
2.7	Output Voltage Ripple	2-10
2.8	Input Voltage Ripple	2-12
2.9	Start-Up	2-13
3	Board Layout	3-1
3.1	Layout	3-2
4	Schematic and Bill of Materials	4-1
4.1	Schematic	4-2
4.2	Bill of Materials	4-3

Figures

1-1	Frequency Trimming Resistor Selection	1-5
2-1	Connection Diagram	2-2
2-2	Measured Efficiency	2-3
2-3	Measured Board Losses	2-4
2-4	Load Regulation	2-5
2-5	Line Regulation	2-5
2-6	Load Transient Response, TPS54610	2-6
2-7	Load Transient Response, TPS54810	2-6
2-8	Load Transient Response, TPS54910	2-7
2-9	Measured Loop Response, TPS54610, $V_{IN} = 3\text{ V}$	2-7
2-10	Measured Loop Response, TPS54610, $V_{IN} = 6\text{ V}$	2-8
2-11	Measured Loop Response, TPS54810, $V_{IN} = 4\text{ V}$	2-8
2-12	Measured Loop Response, TPS54810, $V_{IN} = 6\text{ V}$	2-9
2-13	Measured Loop Response, TPS54910, $V_{IN} = 3\text{ V}$	2-9
2-14	Measured Loop Response, TPS54910, $V_{IN} = 3.6\text{ V}$	2-10
2-15	Measured Output Voltage Ripple, TPS54610	2-10
2-16	Measured Output Voltage Ripple, TPS54810	2-11
2-17	Measured Output Voltage Ripple, TPS54910	2-11
2-18	Input Voltage Ripple, TPS54610	2-12
2-19	Input Voltage Ripple, TPS54810	2-12
2-20	Input Voltage Ripple, TPS54910	2-13
2-21	Measured Start-Up Waveform, TPS54610	2-13
2-22	Measured Start-Up Waveform, TPS54810	2-14
2-23	Measured Start-Up Waveform, TPS54910	2-14
3-1	Top-Side Layout	3-2
3-2	Internal Layer 1 Layout	3-3
3-3	Internal Layer 2 Layout	3-3
3-4	Bottom-Side Layout (looking from top side)	3-4
3-5	Top-Side Assembly	3-4
4-1	SLVP213 Schematic	4-2

Tables

1-1	Input Voltage and Output Current Summary	1-2
1-2	TPS54610EVM-213 Performance Specification Summary	1-3
1-3	TPS54810EVM-213 Performance Specification Summary	1-4
1-4	TPS54910EVM-213 Performance Specification Summary	1-4
1-5	Output Voltage Programming	1-5
4-1	SLVP213 Bill of Materials	4-3



Introduction

This chapter contains background information for the TPS54610, TPS54810, and TPS54910 as well as support documentation for the TPS54610EVM-213, TPS54810EVM-213, and TPS54910EVM-213 evaluation modules. Performance specifications for the EVMs are given, as well as modification information.

Topic	Page
1.1 Background	1-2
1.2 Performance Specification Summary	1-3
1.3 Modifications	1-5

1.1 Background

The SLVP213 evaluation modules use the TPS54610, TPS54810, or TPS54910 synchronous buck regulators to provide an output voltage of 1.8 V from a nominal 3.3-V or 5-V input. Rated input voltage range and output current range are listed in Table 1–1. These evaluation modules are designed to demonstrate the small PCB areas that can be achieved when designing with the TPS54x10 family of regulators. The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.65- μ H output inductor. The MOSFETs of the TPS54x10 are incorporated inside the TPS54x10 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on-resistance of the MOSFETs provides the TPS54x10 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC and allow for an adjustable output voltage and an application specific loop response.

Table 1–1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54610EVM–213	3 V to 6 V	0 A to 6 A
TPS54810EVM–213	4 V to 6 V	0 A to 8 A
TPS54910EVM–213	3 V to 4 V	0 A to 9 A

1.2 Performance Specification Summary

A summary of the SLVP213 performance specifications is listed in Table 1–2, Table 1–3, and Table 1–4. All specifications are for an ambient temperature of 25°C, unless otherwise noted.

Table 1–2. TPS54610EVM-213 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		3	3.3 or 5	6	V
Output voltage set point		0.9	1.8	†	V
Output current range	$V_{IN} = 5\text{ V}$	0		6	A
Line regulation	$I_O = 0\text{ A to }6\text{ A}$	-0.2		0.2	mV
Load regulation	$V_{IN} = 5\text{ V}$	-4		4	mV
Load transient response	$I_O = 1.5\text{ A to }4.5\text{ A}$ $t_r = 1\text{ }\mu\text{s}$		-65		mV _{PK}
			20		μs
	$I_O = 4.5\text{ A to }1.5\text{ A}$ $t_f = 1\text{ }\mu\text{s}$		65		mV _{PK}
			20		μs
Loop bandwidth	$V_{IN} = 3\text{ V}$		74		kHz
Phase margin	$V_{IN} = 3\text{ V}$		43		degrees
Loop bandwidth	$V_{IN} = 6\text{ V}$		118		kHz
Phase margin	$V_{IN} = 6\text{ V}$		46		degrees
Input ripple voltage			150	250	mV _{PP}
Output ripple voltage			7	10	mV _{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	$V_{IN} = 5\text{ V}, I_O = 2.5\text{ A}$		89.7%		

† 3.3 V at V_{IN} greater than 3.8 V.

Table 1–3. TPS54810EVM-213 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4	5	6	V
Output voltage set point		0.9	1.8	3.3	V
Output current range	$V_{IN} = 5\text{ V}$	0		8	A
Line regulation	$I_O = 0\text{ A to }8\text{ A}$	-0.4		0.4	mV
Load regulation	$V_{IN} = 5\text{ V}$	-1.5		1.5	mV
Load transient response	$I_O = 2\text{ A to }6\text{ A}$ $t_r = 1\text{ }\mu\text{s}$		-85		mV _{PK}
			20		μs
	$I_O = 6\text{ A to }2\text{ A}$ $t_f = 1\text{ }\mu\text{s}$		85		mV _{PK}
			20		μs
Loop bandwidth	$V_{IN} = 4\text{ V}$		85		kHz
Phase margin	$V_{IN} = 4\text{ V}$		47		degrees
Loop bandwidth	$V_{IN} = 6\text{ V}$		112		kHz
Phase margin	$V_{IN} = 6\text{ V}$		48		degrees
Input ripple voltage			160	250	mV _{PP}
Output ripple voltage			7	10	mV _{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	$V_{IN} = 5\text{ V}, I_O = 2\text{ A}$		89.4%		

Table 1–4. TPS54910EVM-213 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		3	3.3	4	V
Output voltage set point		0.9	1.8	2.5	V
Output current range	$V_{IN} = 3.3\text{ V}$	0		9	A
Line regulation	$I_O = 0\text{ A to }9\text{ A}$	-0.2		0.2	mV
Load regulation	$V_{IN} = 5\text{ V}$	-1		1	mV
Load transient response	$I_O = 1\text{ A to }5\text{ A}$ $t_r = 10\text{ }\mu\text{s}$		-50		mV _{PK}
			100		μs
	$I_O = 5\text{ A to }1\text{ A}$ $t_f = 10\text{ }\mu\text{s}$		50		mV _{PK}
			150		μs
Loop bandwidth	$V_{IN} = 3\text{ V}$		72		kHz
Phase margin	$V_{IN} = 3\text{ V}$		40		degrees
Loop bandwidth	$V_{IN} = 3.6\text{ V}$		85		kHz
Phase margin	$V_{IN} = 3.6\text{ V}$		42		degrees
Input ripple voltage			160	250	mV _{PP}
Output ripple voltage			7	10	mV _{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	$V_{IN} = 3.3\text{ V}, I_O = 2\text{ A}$		92.4%		

1.3 Modifications

The SLVP213 is designed to demonstrate the small size that can be attained when designing with the TPS54x10, so many of the features which allow for extensive modifications have been omitted from this EVM. The output voltage can be changed in the range of 0.9 V to 3.3 V (2.5 V for the TPS54910) by changing the value of R4. The value of R4 for a specific output voltage can be calculated by using the following equation. Table 1–5 lists the values of R4 for some common output voltages.

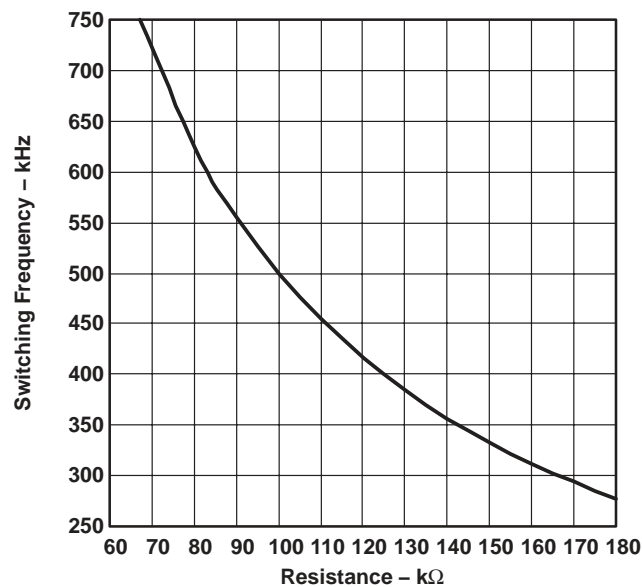
$$R4 = 10 \text{ k}\Omega \times \frac{0.891 \text{ V}}{V_O - 0.891 \text{ V}}$$

Table 1–5. Output Voltage Programming

Output Voltage (V)	R4 Value (kΩ)
0.9	1000
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49
3.3	3.74

The switching frequency can be trimmed to any value between 280 kHz and 700 kHz by changing the value of R5. Decreasing the switching frequency results in increased output ripple unless the value of L1 is also increased. A plot of the value of R5 versus the switching frequency is shown in Figure 1–1.

Figure 1–1. Frequency Trimming Resistor Selection



Modifying the value of C6 can change the slow start time of the SLVP213. Use the following equation to calculate the required value of C6 for a specific slow start time. With C6 left open, the slow start time is typically 3.6 ms. The slow start time cannot be made faster than 3.6 ms.

$$R6 = \frac{T_{SS} \times 5 \mu A}{0.891 V}$$

Test Setup and Results

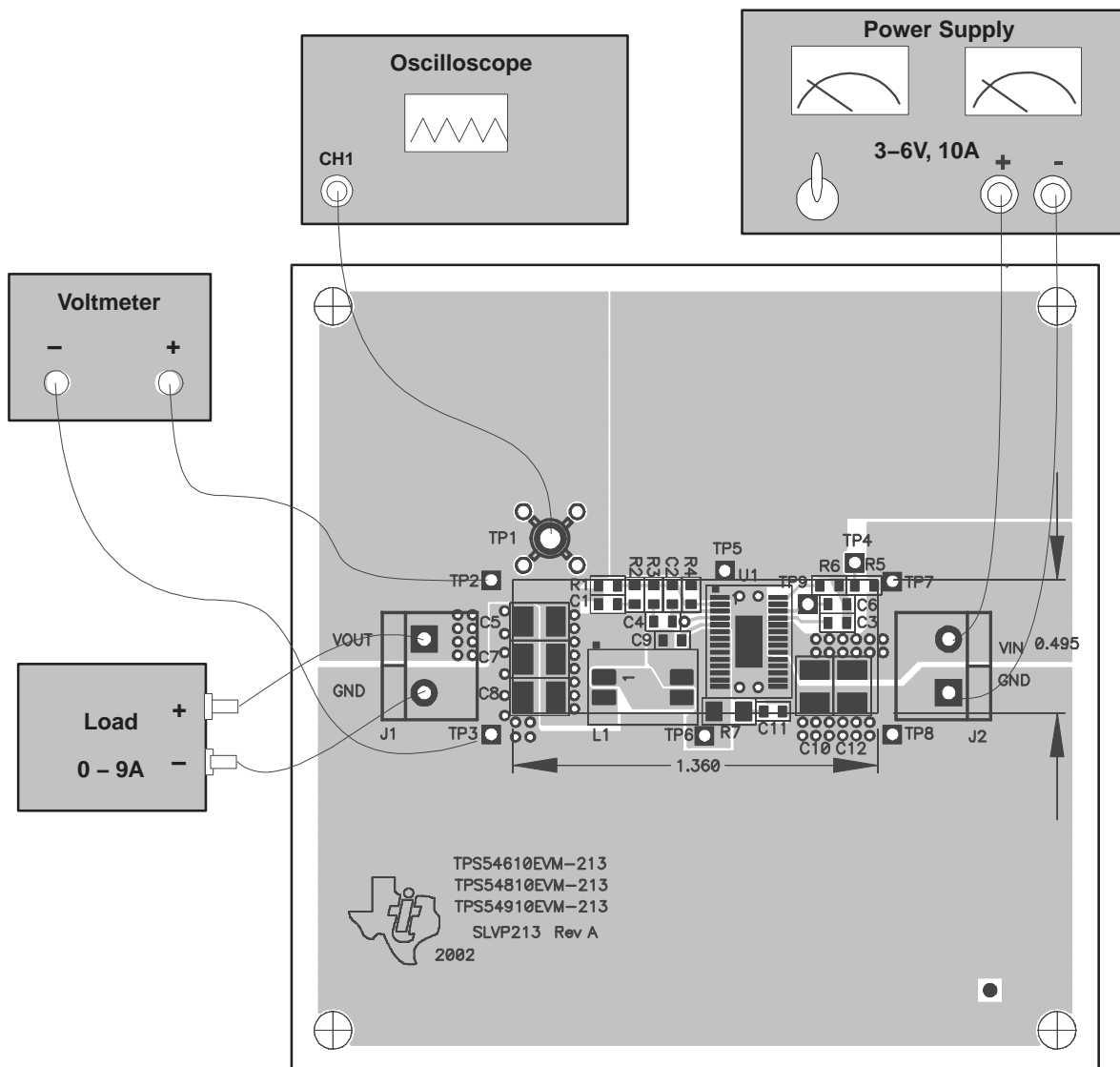
This chapter describes how to properly connect, set up, and use the SLVP213 evaluation module. The chapter also includes test results typical for the SLVP213 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

Topic	Page
2.1 Input/Output Connections	2-2
2.2 Efficiency	2-3
2.3 Power Dissipation	2-4
2.4 Output Voltage Regulation	2-5
2.5 Load Transients	2-6
2.6 Loop Characteristics	2-7
2.7 Output Voltage Ripple	2-10
2.8 Input Voltage Ripple	2-12
2.9 Start-Up	2-13

2.1 Input/Output Connections

The SLVP213 has the following four input/output connections: input, input return, output, and output return. A diagram showing the connection points is shown in Figure 2–1. A power supply capable of supplying 10 A should be connected to J2 through a pair of 20 AWG wires. The load should be connected to J1 through a pair of 16 AWG wires. The maximum load current can be reduced from 9 A if 6 A or 8 A versions of the SLVP213 are used. Wire lengths should be minimized to reduce losses in the wires. Test point TP1 provides a location to easily connect an oscilloscope voltage probe to monitor the output voltage.

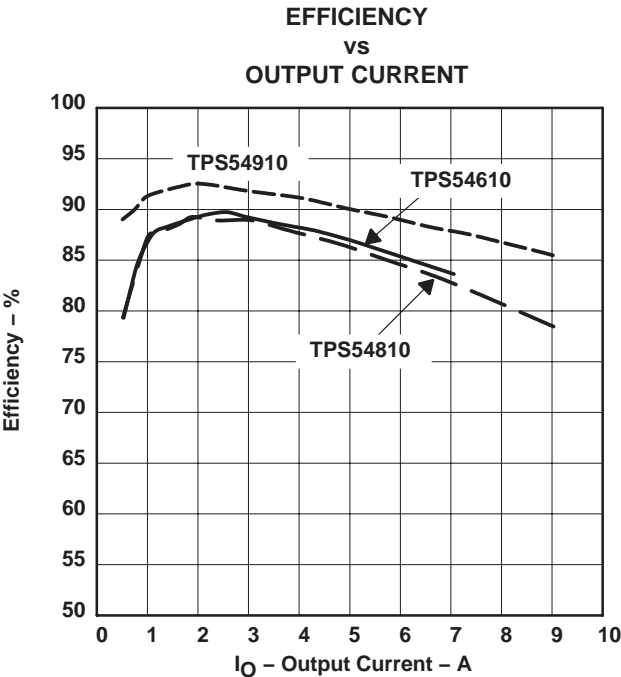
Figure 2–1. Connection Diagram



2.2 Efficiency

The SLVP213 efficiency peaks at a load current of about 2 A and then decreases as the load current increases to full load. The efficiency shown in Figure 2–2 is for 5-V (TPS54610, TPS54810) and 3.3-V (TPS54910) inputs at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

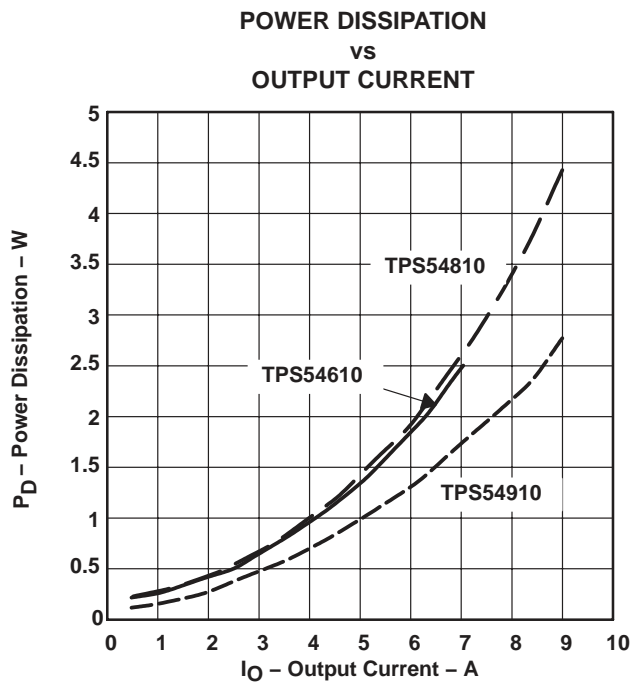
Figure 2–2. Measured Efficiency



2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a well-designed board layout, allows the SLVP213 EVMs to output full rated load current while maintaining safe junction temperatures. For the TPS54610 with a 5-V input source and a 6-A load, the junction temperature is approximately 60°C while the case temperature is approximately 55°C. The total board losses at 25°C are shown in Figure 2–3. The input voltage for the TPS54910 is 3.3 V and for the TPS54610 and TPS54810 is 5 V. Note that for a given output current the TPS54910 dissipates less power due to the lower drain-to-source on- resistance of the MOSFETs. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2–3. Measured Board Losses



2.4 Output Voltage Regulation

The output voltage load regulation of the SLVP213 is shown in Figure 2–4 while the output voltage line regulation is shown in Figure 2–5. Measurements are shown for an ambient temperature of 25°C.

Figure 2–4. Load Regulation

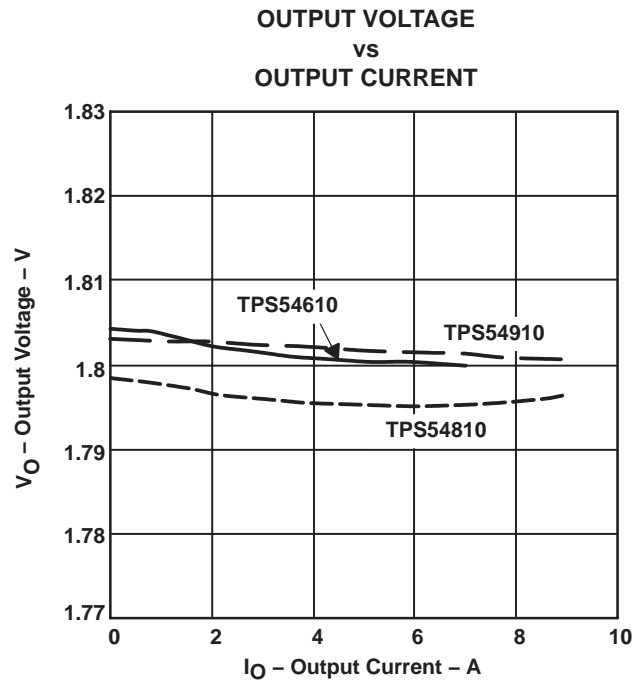
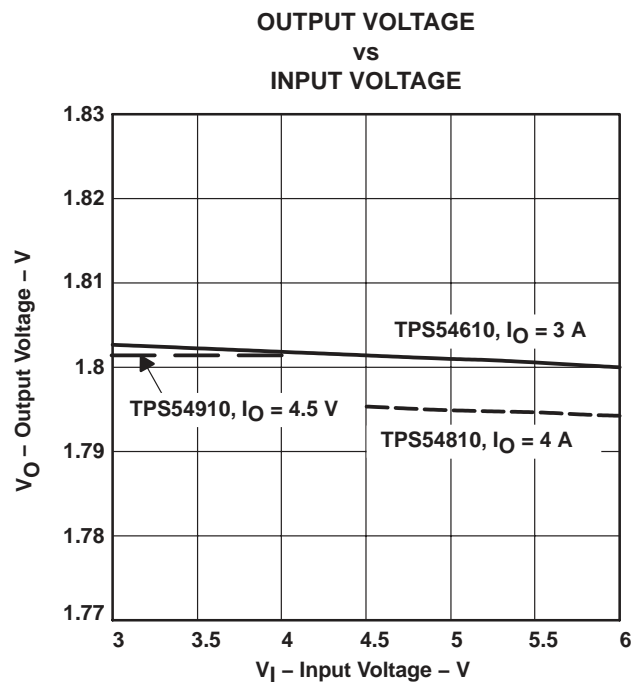


Figure 2–5. Line Regulation



2.5 Load Transients

The SLVP213 response-to-load transients are shown in Figure 2–6, Figure 2–7, and Figure 2–8. The current step is from 25% to 75% of the maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2–6. Load Transient Response, TPS54610

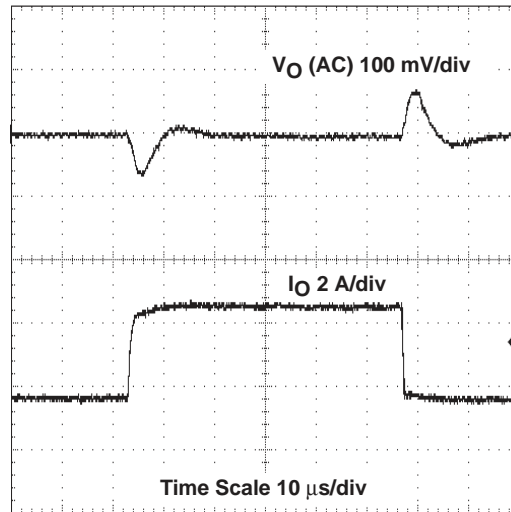


Figure 2–7. Load Transient Response, TPS54810

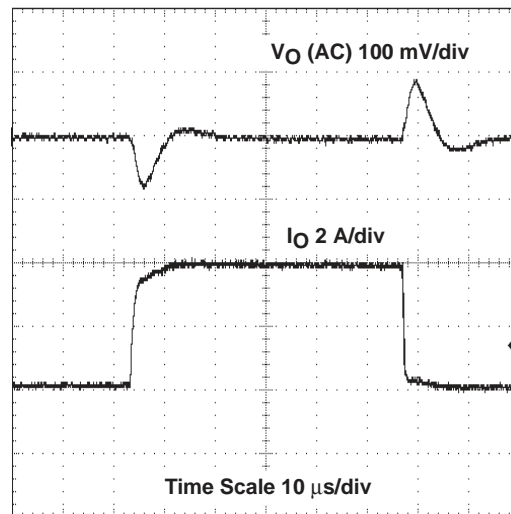
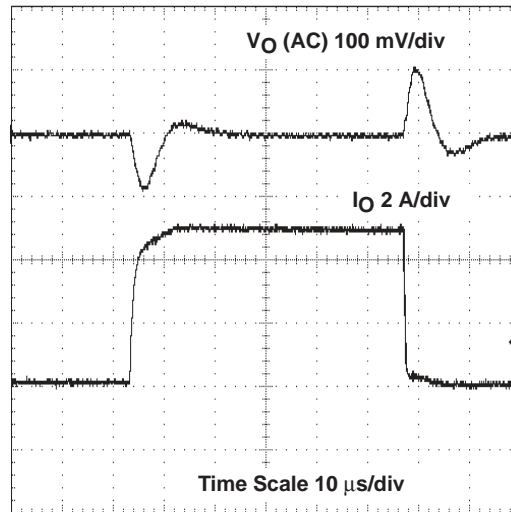


Figure 2–8. Load Transient Response, TPS54910



2.6 Loop Characteristics

The SLVP213 loop response characteristics are shown in Figure 2–9 through Figure 2–14. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

Figure 2–9. Measured Loop Response, TPS54610, $V_{IN} = 3$ V

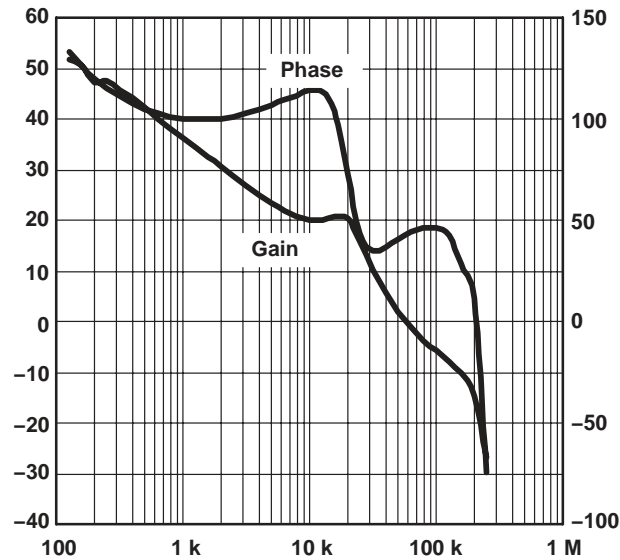


Figure 2-10. Measured Loop Response, TPS54610, $V_{IN} = 6\text{ V}$

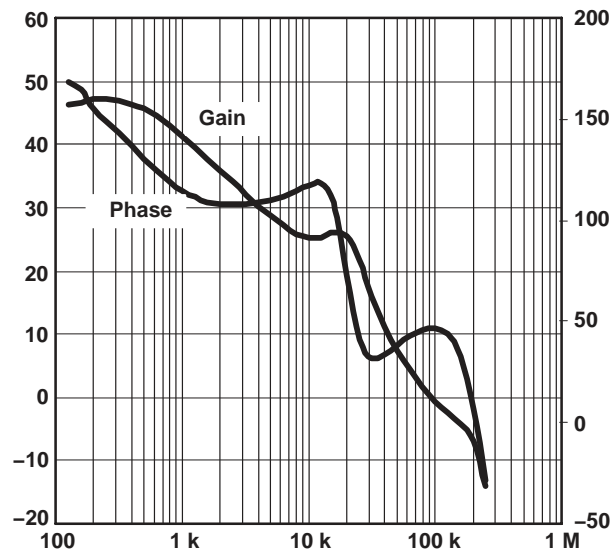


Figure 2-11. Measured Loop Response, TPS54810, $V_{IN} = 4\text{ V}$

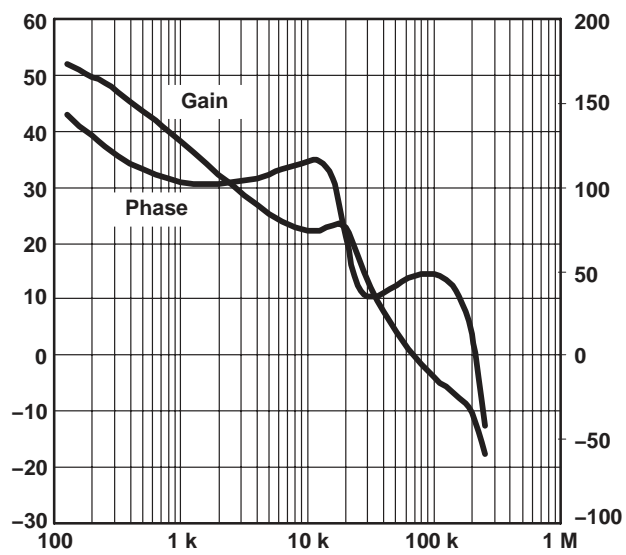


Figure 2–12. Measured Loop Response, TPS54810, $V_{IN} = 6\text{ V}$

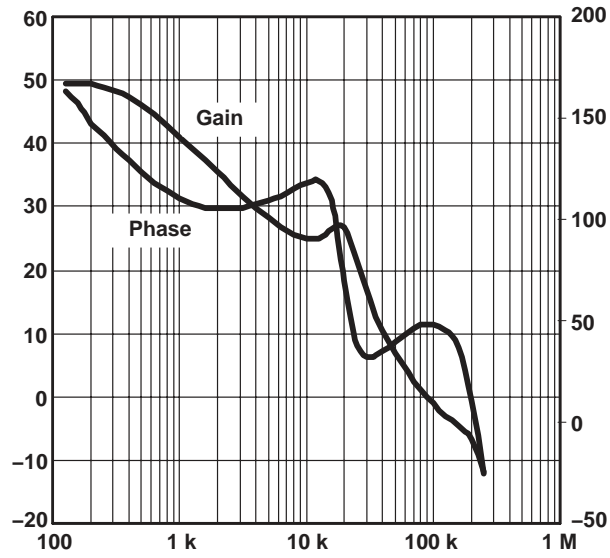


Figure 2–13. Measured Loop Response, TPS54910, $V_{IN} = 3\text{ V}$

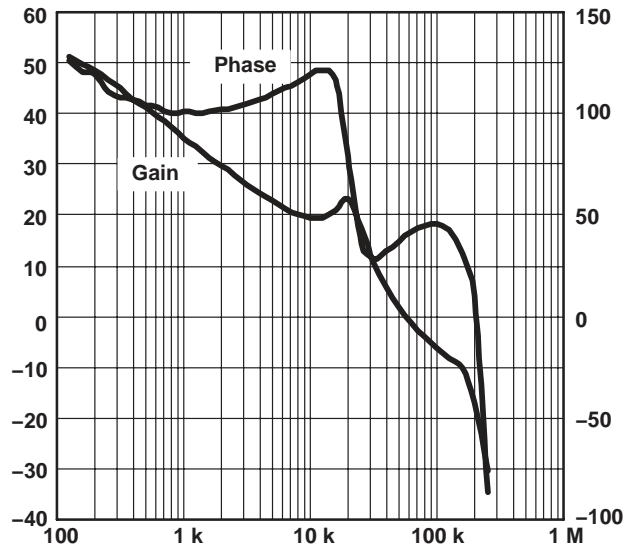
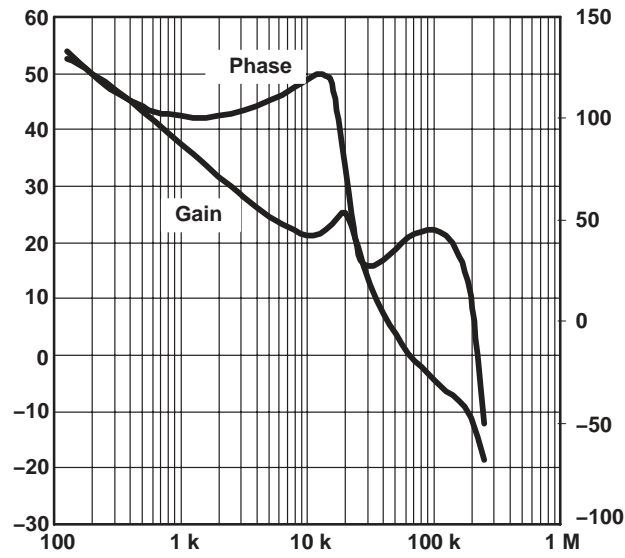


Figure 2–14. Measured Loop Response, TPS54910, $V_{IN} = 3.6\text{ V}$



2.7 Output Voltage Ripple

The SLVP213 output voltage ripple are shown in Figure 2–15, Figure 2–16, and Figure 2–17 for each device type. The input voltage is 3.3 V for the TPS54610 and TPS54910. The input voltage is 5 V for the TPS54810. Output current for each device is 50% of rated full load.

Figure 2–15. Measured Output Voltage Ripple, TPS54610

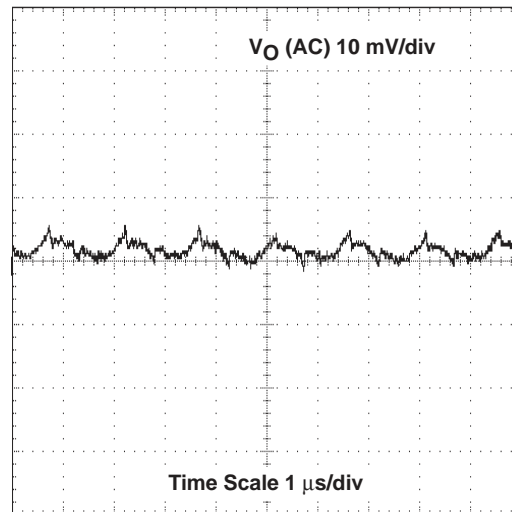


Figure 2–16. Measured Output Voltage Ripple, TPS54810

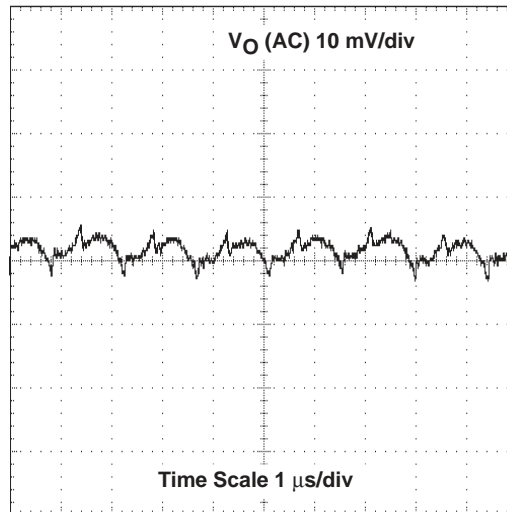
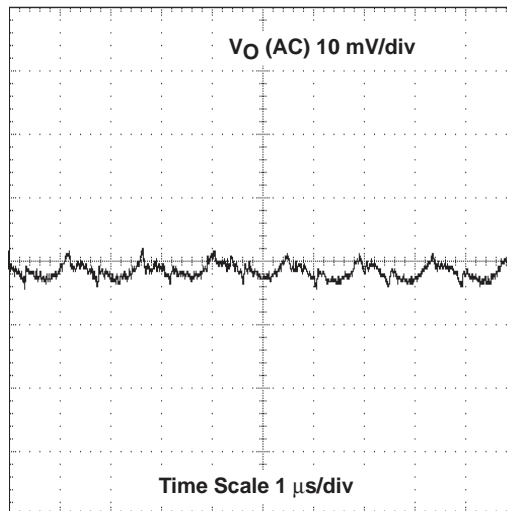


Figure 2–17. Measured Output Voltage Ripple, TPS54910



2.8 Input Voltage Ripple

The SLVP213 output voltage ripple is shown in Figure 2–18, Figure 2–19, and Figure 2–20 for each device type. The input voltage is 3.3 V for the TPS54610 and TPS54910. The input voltage is 5 V for the TPS54810. Output current for each device is 50% of rated full load.

Figure 2–18. Input Voltage Ripple, TPS54610

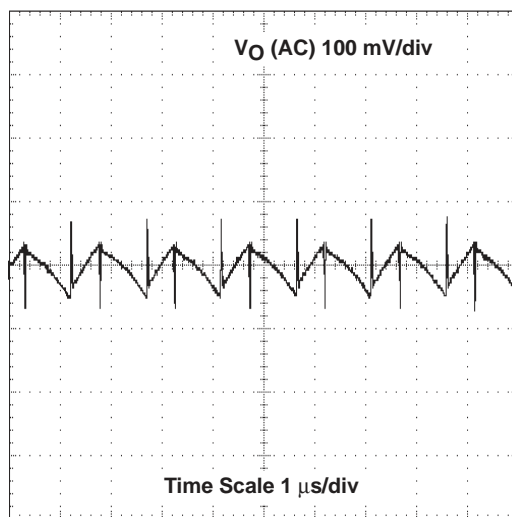


Figure 2–19. Input Voltage Ripple, TPS54810

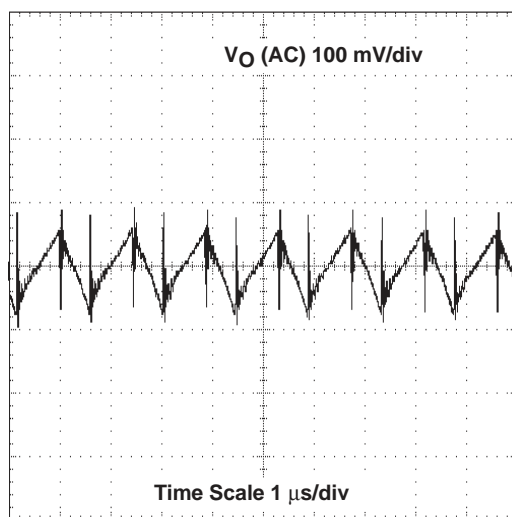
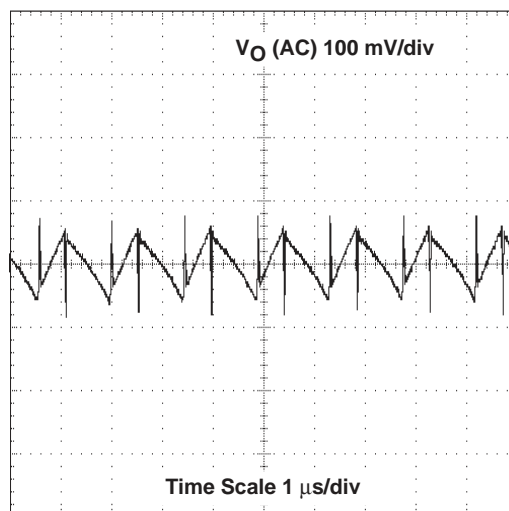


Figure 2–20. Input Voltage Ripple, TPS54910



2.9 Start-Up

The start-up voltage waveforms of the SLVP213 are shown in Figure 2–21, Figure 2–22, and Figure 2–23. There is approximately a 9-ms delay after the input voltage rises above the 2.9-V (3.8 V for the TPS54810) startup voltage threshold until the output voltage begins to ramp up to the final value of 1.8 V. The output voltage tracks the greater of the internal and external slow start voltages, accounting for the change in ramp rates.

Figure 2–21. Measured Start-Up Waveform, TPS54610

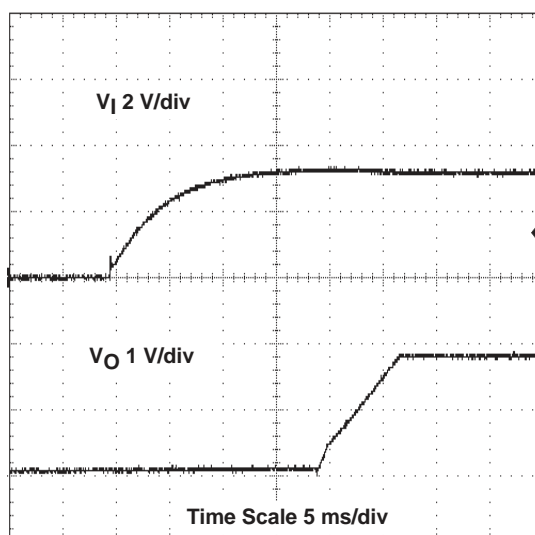


Figure 2–22. Measured Start-Up Waveform, TPS54810

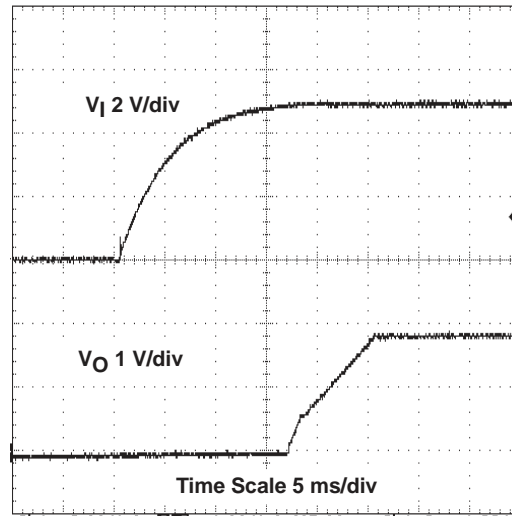
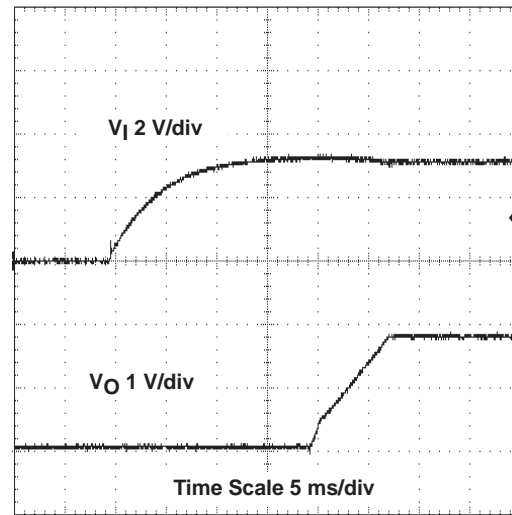


Figure 2–23. Measured Start-Up Waveform, TPS54910



Board Layout

This chapter provides a description of the SLVP213 board layout and layer illustrations.

Topic	Page
3.1 Layout	3-2

3.1 Layout

The board layouts and assembly for the SLVP213 are shown in Figure 3–1 through Figure 3–5. The SLVP213 is laid out in a fashion to resemble a layer stack-up that could be encountered in a typical application. The top and bottom layers are 1.5 oz. copper, while the two internal layers are 0.5 oz. copper.

The top layer contains the main power traces for V_{IN} , V_{OUT} , and V_{phase} . Also on the top layer are connections for the remaining pins of the TPS54x10 and a large area filled with a ground plane. The two internal layers are identical and are dedicated ground planes. The bottom layer contains the compensation network circuitry as well as additional V_{IN} , V_{OUT} , and ground traces. The top and bottom ground traces are connected to the internal ground planes with 45 vias placed around the board including 12 directly under the TPS54x10 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C4 and C8), bias decoupling capacitor (C9), and boot strap capacitor (C6) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC on the backside of the PCB. The compensation circuit ties to the output voltage at the point of regulation, which is a wide trace to the output connector (J2).

Figure 3–1. Top-Side Layout

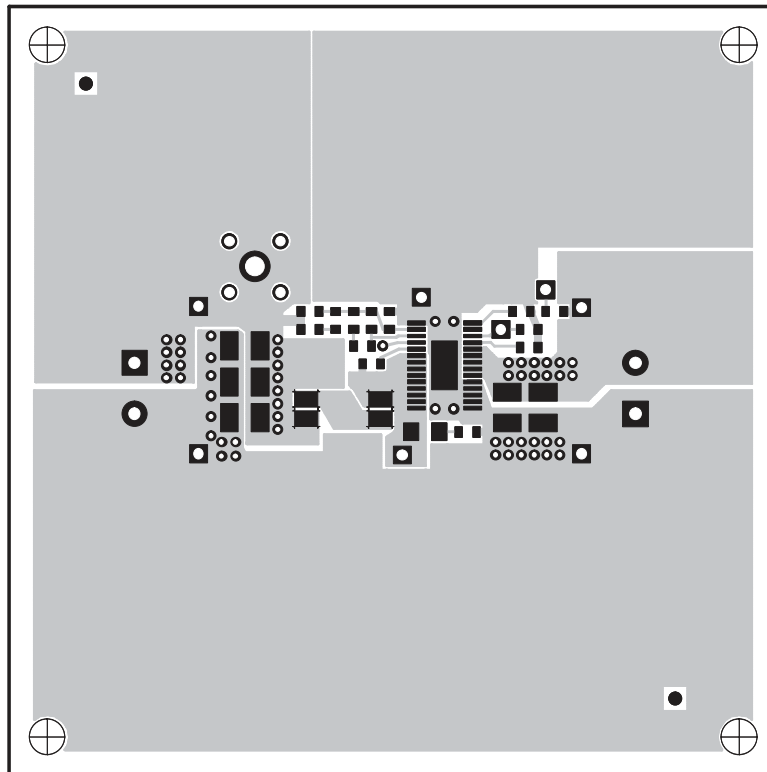


Figure 3–2. Internal Layer 1 Layout

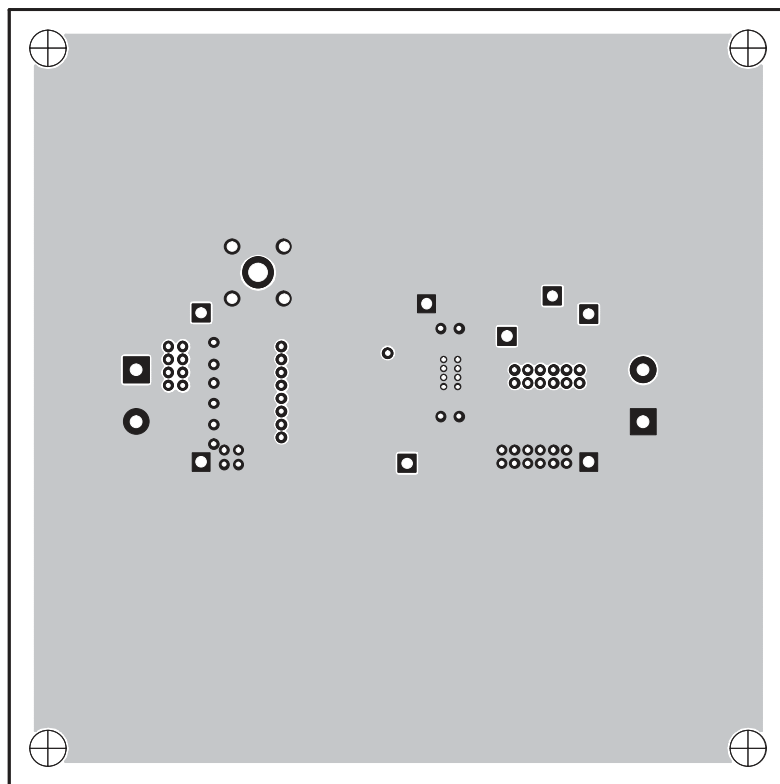


Figure 3–3. Internal Layer 2 Layout

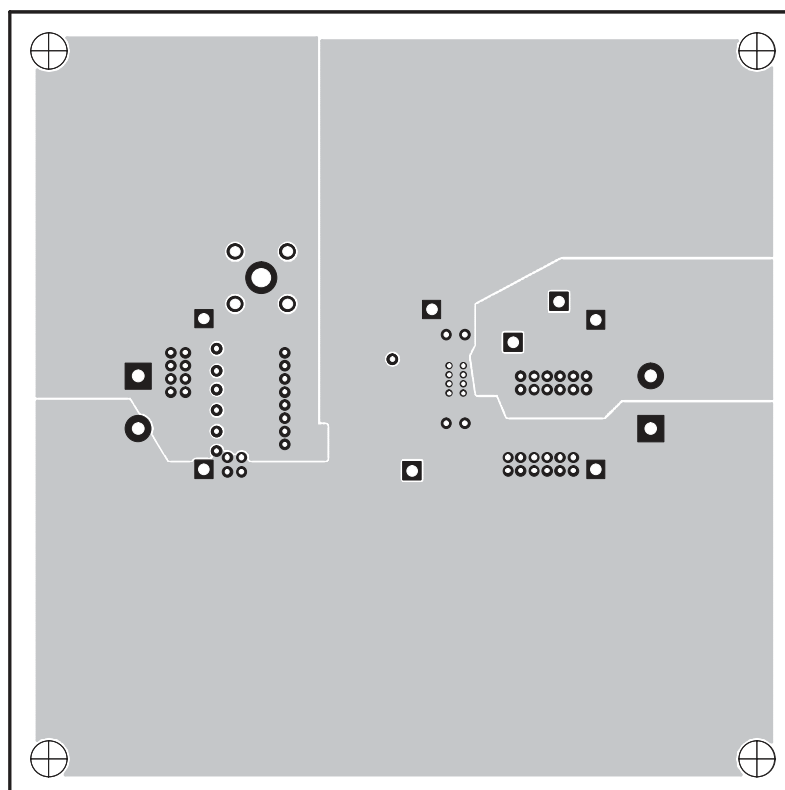


Figure 3–4. Bottom-Side Layout (looking from top side)

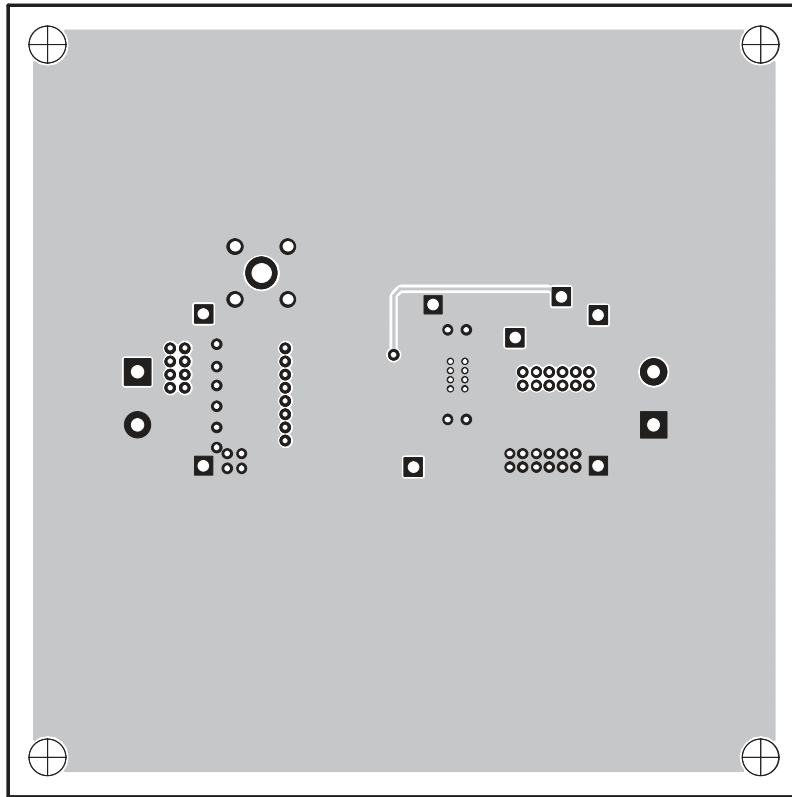
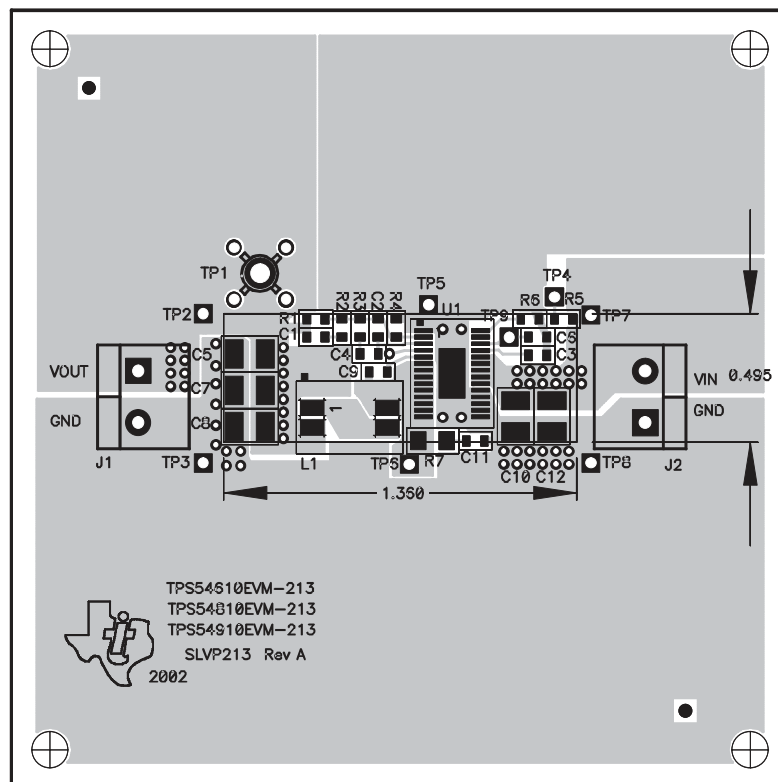


Figure 3–5. Top-Side Assembly



Schematic and Bill of Materials

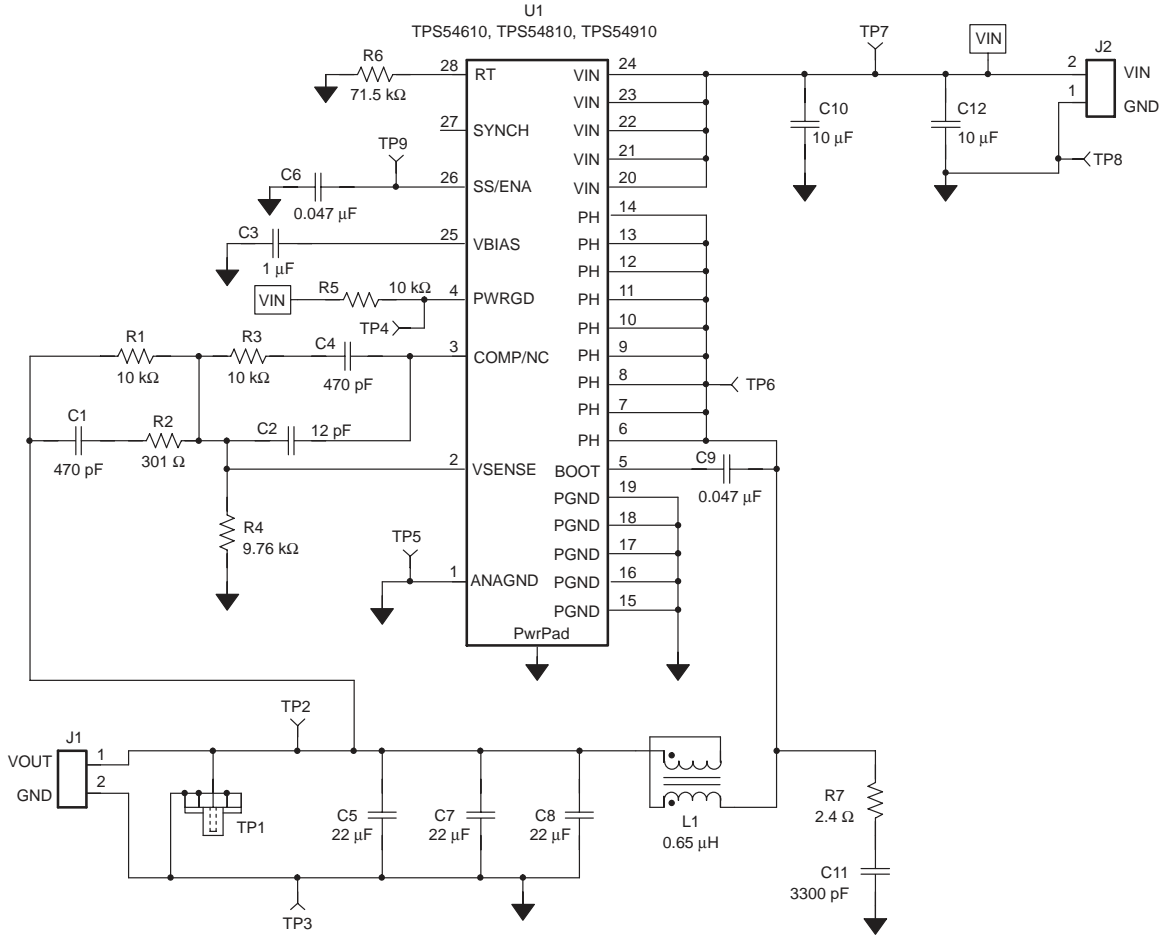
The SLVP213 schematic and bill of materials are presented in this chapter.

Topic	Page
4.1 Schematic	4-2
4.2 Bill of Materials	4-3

4.1 Schematic

The schematic for the SLVP213 is shown in Figure 4–1.

Figure 4–1. SLVP213 Schematic



The analog and power grounds are tied to the PowerPAD under the package of the IC.

4.2 Bill of Materials

The bill of materials for the SLVP213 is listed in Table 4–1.

Table 4–1. SLVP213 Bill of Materials

COUNT			REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
-1	-2	-3					
2	2	2	C1, C4	Capacitor, ceramic, 470 pF, 50 V, C0G, 5%	603	Panasonic	GRM1885C1H471JA01
2	2	2	C10, C12	Capacitor, ceramic, 10 μ F, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	1	1	C11	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Panasonic	ECJ-1VB1H332K
1	1	1	C2	Capacitor, ceramic, 12 pF, 50 V, C0G, 5%	603	Murata	GRM1885C1H120JZ01
1	1	1	C3	Capacitor, ceramic, 1 μ F, 10 V, X5R, 10%	603	TDK	C1608X5R1A105M
3	3	3	C5, C7, C8	Capacitor, ceramic, 22 μ F, 6.3 V, X5R, 20%	1210	Taiyo Yuden	JMK325BJ226MN
2	2	2	C6, C9	Capacitor, ceramic, 0.047 μ F, 25 V, X7R, 10%	603	Murata	GRM188R71E473KA01
2	2	2	J1, J2	Terminal block, 2 pin, 15 A, 5,1 mm	148830	OST	ED1609
1	1	1	L1	Inductor, 0.65 μ H, 12 A	0.340x0.250	Pulse	PA0277
2	2	2	R1, R5	Resistor, chip, 10.0 k Ω , 1/16 W, 1%	603	Panasonic	ERJ-3EKF1002
1	1	1	R2	Resistor, chip, 301 Ω , 1/16 W, 1%	603	Panasonic	ERJ-3EKF301
1	1	1	R3	Resistor, chip, 10.0 k Ω , 1/16 W, 1%	603	Panasonic	ERJ-3EKF1002
1	1	1	R4	Resistor, chip, 9.76 k Ω , 1/16 W, 1%	603	Std	Std
1	1	1	R6	Resistor, chip, 71.5 k Ω , 1/16 W, 1%	603	Std	Std
1	1	1	R7	Resistor, chip, 2.4 Ω , 1/8 W, 1%	1206	Panasonic	ERJ-8RQF2R4
1	1	1	TP1	Adaptor, 3.5-mm probe clip (or 131-5031-00)	72900	Tektronix	131-4244-00
5	5	5	TP2, TP4, TP6, TP7, TP9	Test point, red, 1 mm	0.038"	Farnell	240-345
3	3	3	TP3, TP5, TP8	Test point, black, 1 mm	0.038"	Farnell	240-333
1			U1	IC, IFET power controller, 3 V to 6 V, 6 A	PWP28	TI	TPS54610PWP
	1			IC, IFET power controller, 4 V to 6 V, 8 A	PWP28	TI	TPS54810PWP
		1		IC, IFET power controller, 3 V to 3.6 V, 9 A	PWP28	TI	TPS54910PWP
1	1	1	--	PCB, 3 in \times 3 in \times 0.062 in		Any	SLVP213

