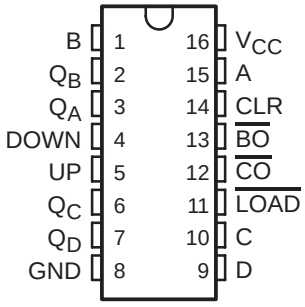
- **High-Speed f_{max} of 100 MHz Typical**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74F193A is a synchronous, 4-bit binary up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count/clock (UP or DOWN) input. The direction of the count is determined by which count input is pulsed while the other count input is high.

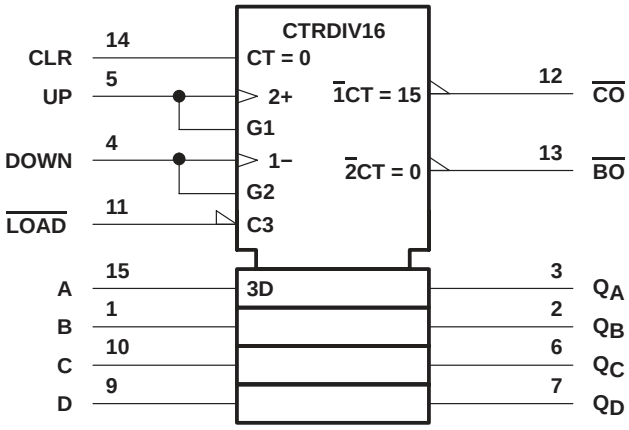
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the $\overline{LOAD}$ input and entering the desired data at the data (D) inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A high level applied to the clear (CLR) input forces all outputs to the low level. The clear function is independent of the count and load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ($\overline{BO}$) output produces a low-level pulse while the count is zero (all Q outputs low) and the DOWN input is low. Similarily, the carry ($\overline{CO}$) output produces a low-level pulse while the count is 15 (all Q outputs high) and the UP input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

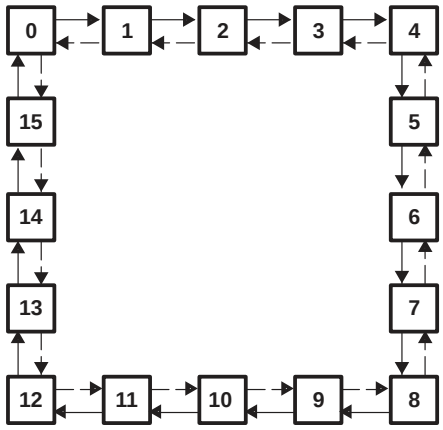
The SN74F193A is characterized for operation from 0°C to 70°C.

logic symbol†



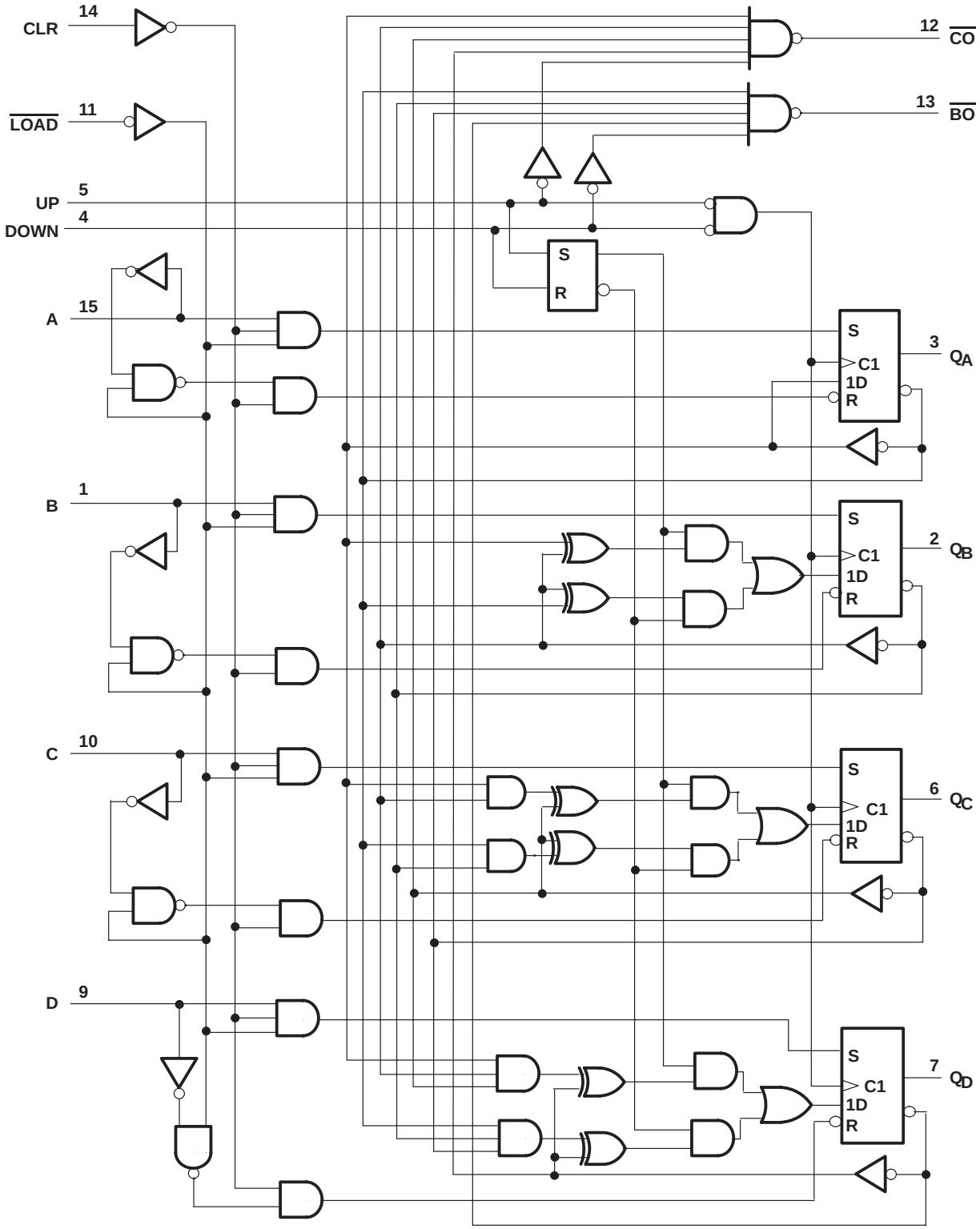
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

state diagram



Count up →
Count down ⇢

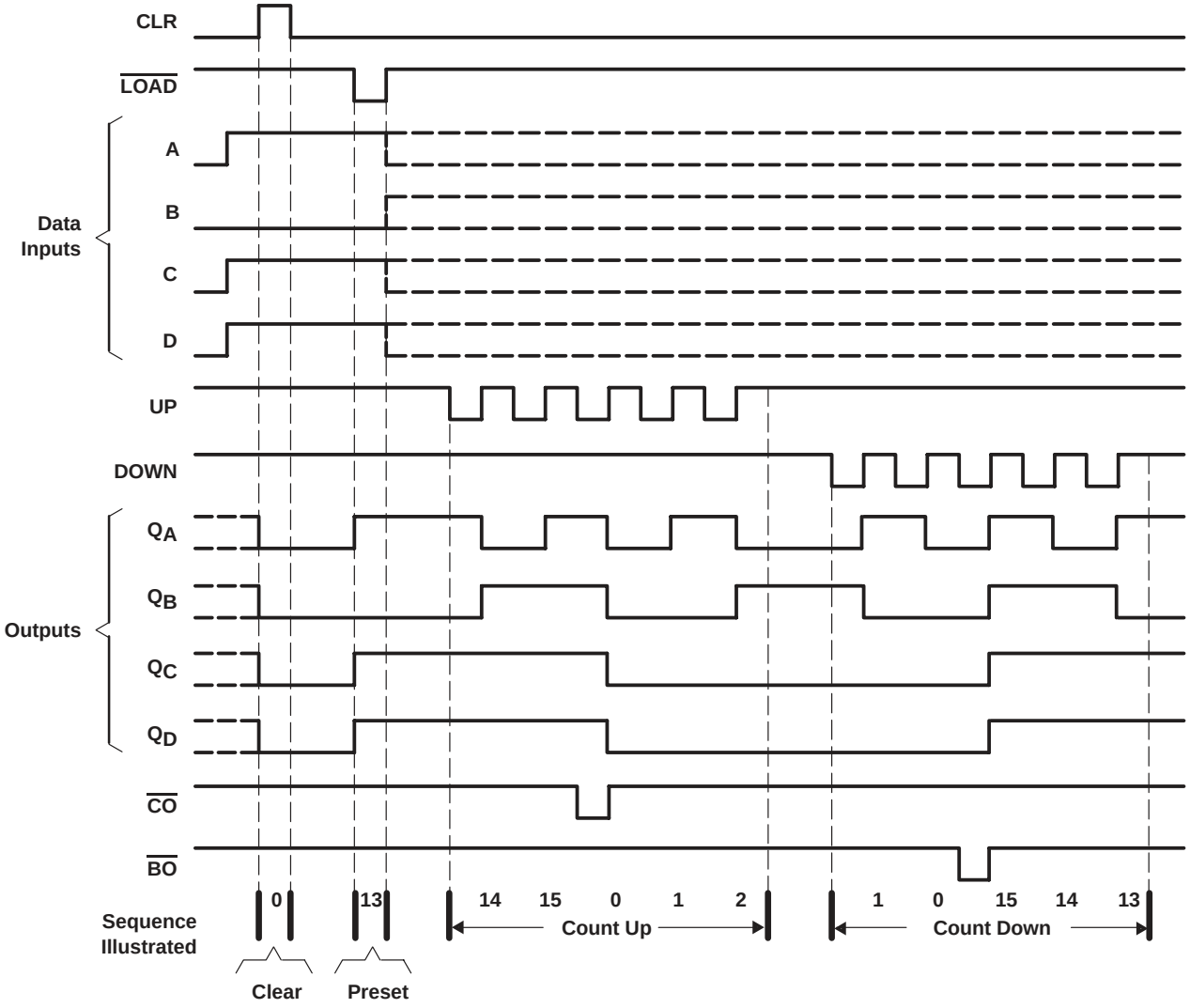
logic diagram (positive logic)



typical clear, load, and count sequence

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen (carry), zero, one, and two
4. Count down to one, zero (borrow), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . − 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . − 30 mA to 5 mA
Voltage applied to any output in the high state . . . . . − 0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . − 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded if the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			18	mA
I_{OH}	High-level output current			− 1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = − 18 mA				− 1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 1 mA		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = − 1 mA to 3 mA		2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V	UP			− 1.8	mA
			Others			− 0.6	
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0		− 60		− 150	mA
I_{CC}	V_{CC} = 5.5 V,	Outputs open			34	54	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	85	0	85	MHz
t_w	Pulse duration	CLR high	4		4		ns
		$\overline{LOAD}$ low	5.5		5.5		
		UP or DOWN high	4		4		
		UP or DOWN low	6		6		
t_{su}	Setup time	Data before $\overline{LOAD}$ inactive	3.5		3.5		ns
		CLR inactive before UP↑ or DOWN↑	5		5		
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑	7.5		7.5		
t_h	Hold time	Data after $\overline{LOAD}$ inactive	2.5		2.5		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			85	100		85		MHz
t_{PLH}	UP or DOWN	$\overline{CO}$ or $\overline{BO}$	2.5		8.5	2.5	9	ns
t_{PHL}			3		8	3	9	
t_{PLH}	UP or DOWN	Any Q	2.5		8.5	2.5	9	ns
t_{PHL}			5		12	5	13	
t_{PLH}	A, B, C, or D	Any Q	2		7	1.5	8	ns
t_{PHL}			6		13.5	5	15	
t_{PLH}	$\overline{LOAD}$	Any Q	4.5		10	4	11	ns
t_{PHL}			5.5		12	5	13	
t_{PHL}	CLR	Any Q	5		11	5	12	ns
t_{PLH}		$\overline{CO}$	6		12	5.5	13	
t_{PHL}	CLR	$\overline{BO}$	5		11	5	12	ns
t_{PLH}	$\overline{LOAD}$	$\overline{CO}$ or $\overline{BO}$	6		13.5	6	15	ns
t_{PHL}			6		12.6	6	13.8	
t_{PLH}	A, B, C, or D	$\overline{CO}$ or $\overline{BO}$	5.5		13	5	14	ns
t_{PHL}			4.5		12.5	4.5	13.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74F193AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74F193ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74F193AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

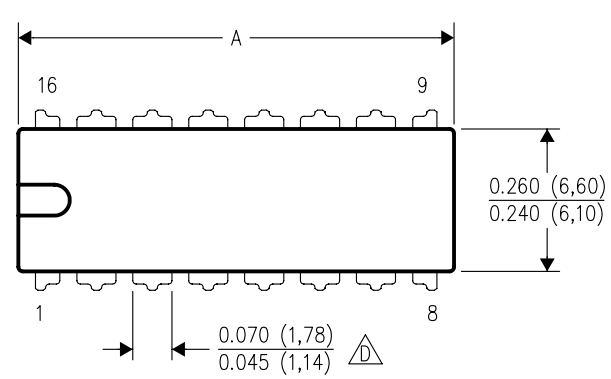
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

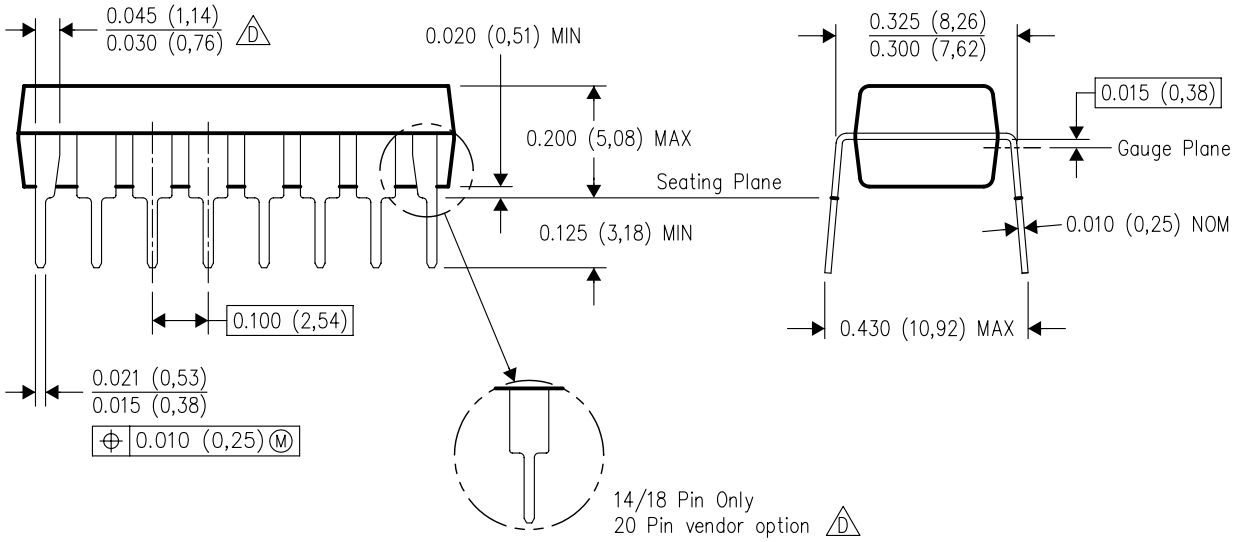
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



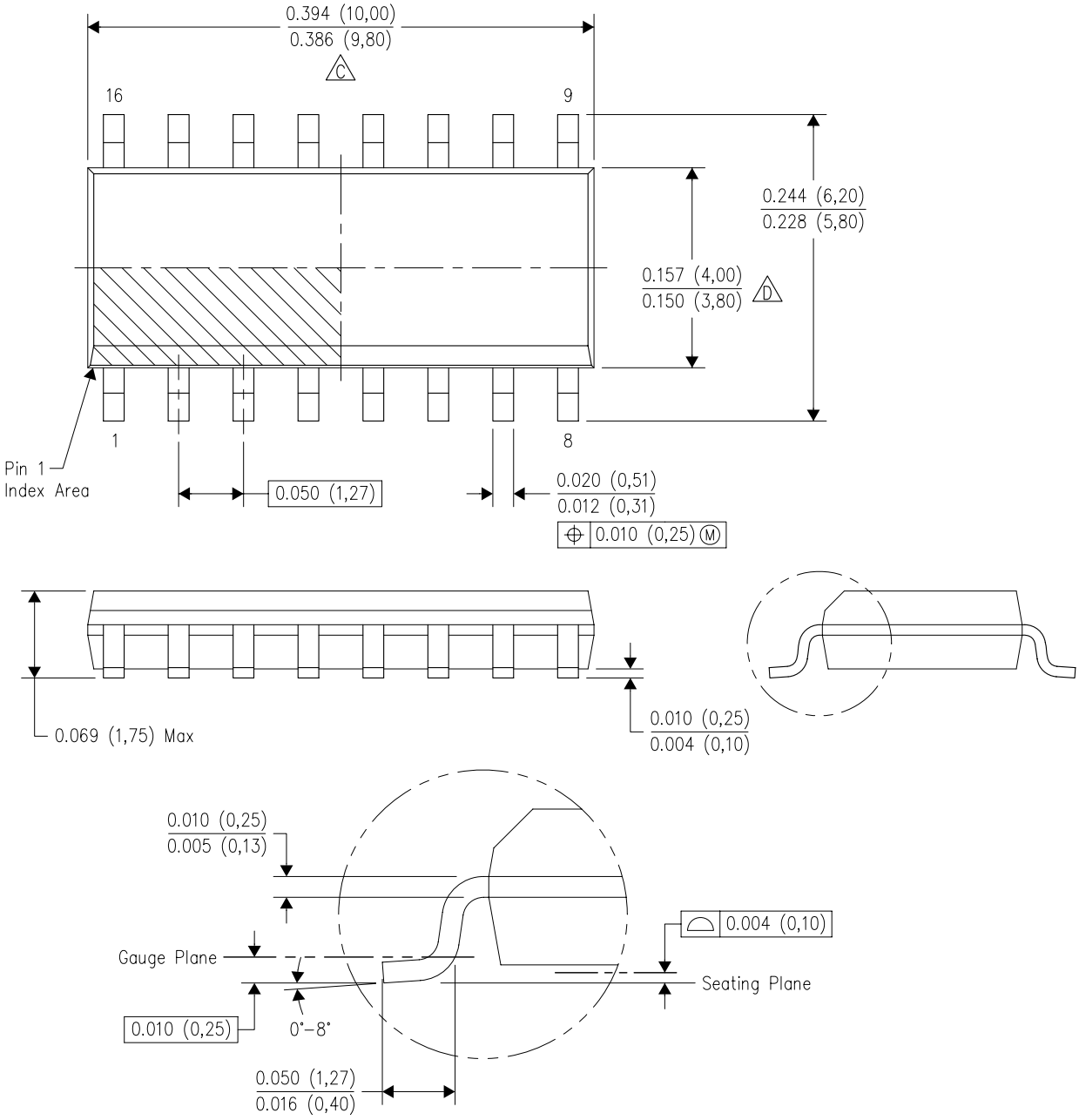
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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