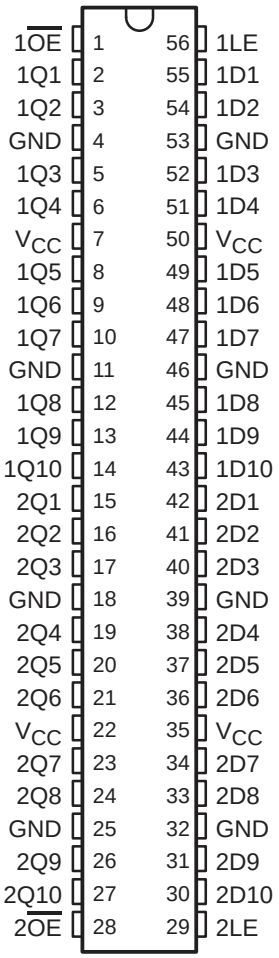
- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Provide Extra Bus Driving/Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) Packages, 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

**54ACT16841 . . . WD PACKAGE**
**74ACT16841 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ’ACT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OE}$ does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

## description (continued)

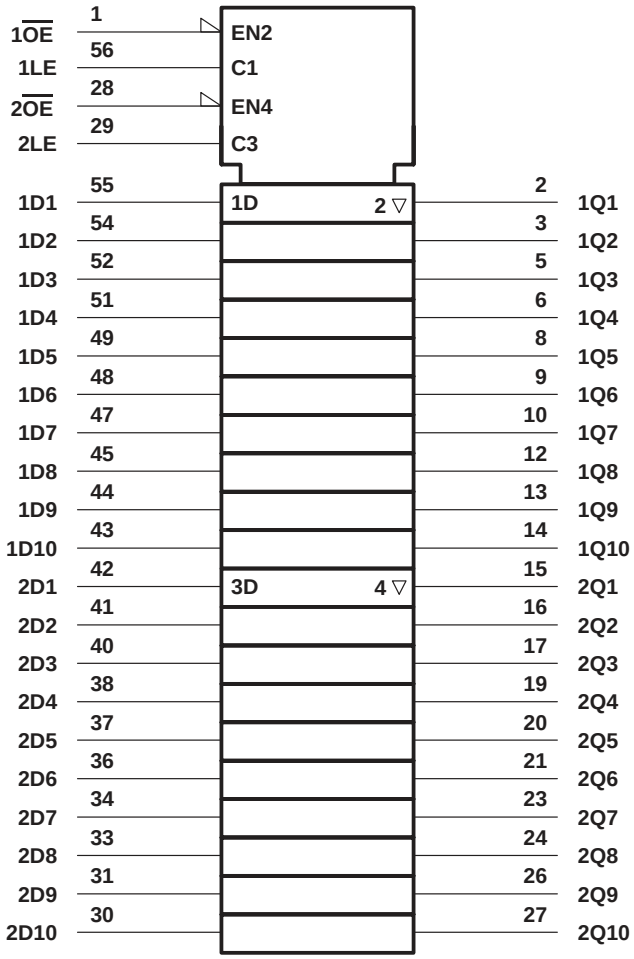
The 74ACT16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16841 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16841 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each 10-bit latch)**

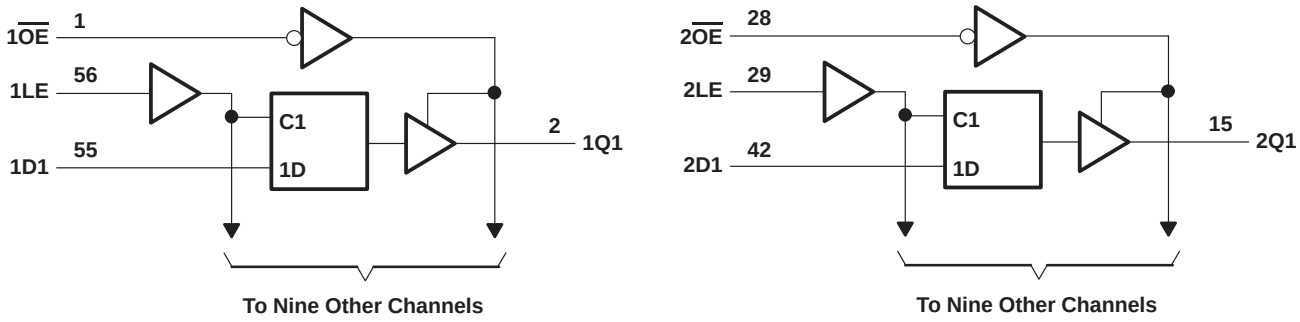
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±500 mA
Maximum package power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DGG package . . . . . 1 W
DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

| | | 54ACT16841 | | | 74ACT16841 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | 54ACT16841 | | 74ACT16841 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | 4.8 | | |
| | $I_{OH}$ = –75 mA† | 5.5 V | | | | 3.85 | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.44 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.44 | | 0.44 | |
| | $I_{OL}$ = 75 mA† | 5.5 V | | | | | 1.65 | | 1.65 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±5 | | ±5 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 80 | | 80 | µA |
| $\Delta I_{CC}$‡ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V | | | 0.9 | | 1 | | 1 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 3 | | | | | | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | 5 V | | 11 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | 54ACT16841 | | 74ACT16841 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | | 4 | | 4 | | 4 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | | 1.5 | | 1.5 | | 1.5 | | ns |
| $t_h$ | Hold time, data after LE↓ | High | 3 | | 3 | | 3 | | ns |
| | | Low | 4.5 | | 4.5 | | 4.5 | | |

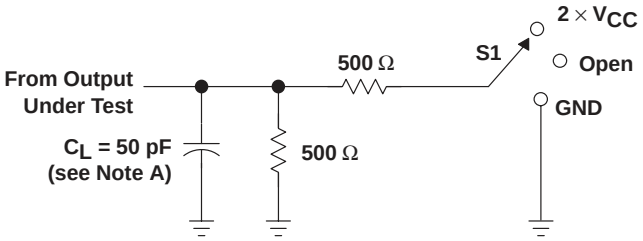
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | 54ACT16841 | | 74ACT16841 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 4 | 7.1 | 10.3 | 4 | 11.8 | 4 | 11.8 | ns |
| $t_{PHL}$ | | | 3.2 | 6.9 | 11 | 3.2 | 12.2 | 3.2 | 12.2 | |
| $t_{PLH}$ | LE | Q | 4.5 | 7.7 | 11.3 | 4.5 | 12.7 | 4.5 | 12.7 | ns |
| $t_{PHL}$ | | | 4.3 | 7.8 | 11.4 | 4.3 | 12.7 | 4.3 | 12.7 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 3.1 | 6.4 | 10.1 | 3.1 | 11.3 | 3.1 | 11.3 | ns |
| $t_{PZL}$ | | | 3.8 | 7.6 | 12.1 | 3.8 | 13.7 | 3.8 | 13.7 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 4 | 7.3 | 9.5 | 4 | 10.2 | 4 | 10.2 | ns |
| $t_{PLZ}$ | | | 4 | 6.8 | 8.9 | 4 | 9.6 | 4 | 9.6 | |

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

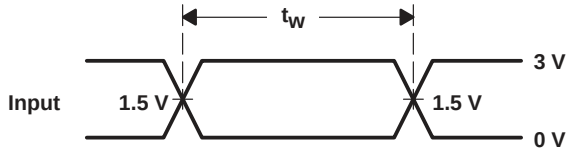
| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, | f = 1 MHz | 41 | pF |
| | | Outputs disabled | | | 10 | |

## PARAMETER MEASUREMENT INFORMATION

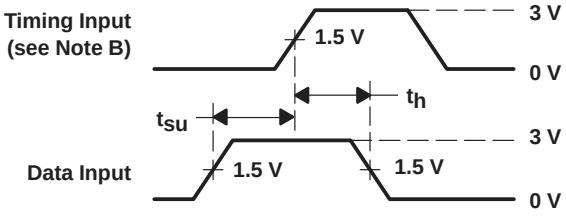



LOAD CIRCUIT

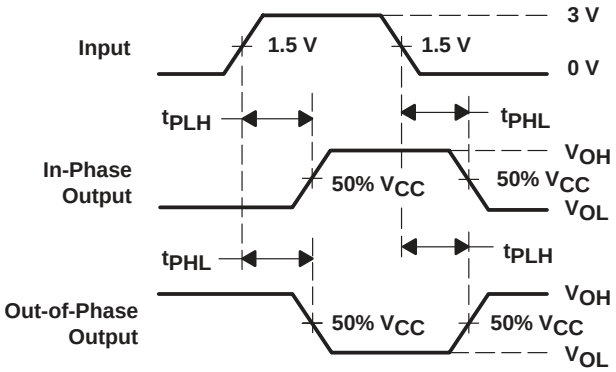
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



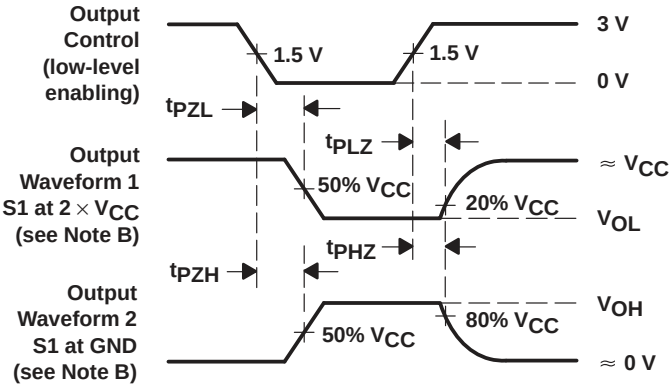

VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74ACT16841DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT16841 | Samples |
| 74ACT16841DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT16841 | Samples |
| 74ACT16841DLR | ACTIVE | SSOP | DL | 56 | | TBD | Call TI | Call TI | -40 to 85 | ACT16841 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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