# CS2001

# 1.2 A Switching Regulator, and 5.0 V, 100 mA Linear Regulator with $\overline{\text{RESET}}$

The CS2001 is a smart power supply ASIC utilized in automotive airbag systems. It contains a current−mode switching regulator with a 1.2 A on−chip switch and a 5.0 V, 100 mA linear regulator. The linear output capacitor must be 3.3 μF or greater with an ESR in the range of 100 mΩ to 1.0 Ω. If the ESR of the cap is less than 100 mΩ, a series resistor must be used. The switcher can be configured in either a boost or flyback topology. The boost topology produces energy reserve the resistor divider connected to the $V_{FB}$ pin. In the event of fault voltage VER which is externally adjustable (25 V maximum) through conditions that produce $V_{FB}$ either open or shorted, the switcher is shut down.

Under normal operating conditions ($V_{BAT}$ > 8.0 V), the current loading on the linear regulator is directed through $V_{BAT}$. A low battery or loss of battery condition switches the supply for the linear regulator from $V_{BAT}$ to VER and shuts down the switcher using the ASIC's internal smart switch. This switchover feature minimizes the power dissipation in both the linear and switcher output devices and saves the cost of using a larger inductor.

The NERD (No Energy Reserve Detected) pin is a dual function output. If $V_{OUT}$ is not in regulation, it provides a Power On Reset function whose time interval is externally adjustable with the capacitor. This interval can be seen on the RESETB pin, which allows for clean power−up and power−down of the microprocessor. Once $V_{OUT}$ is in regulation, the logic level of the NERD output (usually low) indicates to the microprocessor whether or not the VER pin is connected.

A switched−capacitor voltage tripler accepts input voltage VER and produces output voltage $V_{CHG}$ (typically VER + 8.0 V). This voltage is used in the system to drive high−side FETs.

This part is capable of withstanding a 50 V peak transient voltage. The linear regulator will not shut down during this event.

### Features

- Linear Regulator 5.0 V ±2% @ 100 mA
- Switching Regulator 1.2 A Peak Internal Switch
- Voltage Tripler
- Smart Functions
  - Smartswitch
  - RESET
  - Energy Reserve Status
- Protection
  - Overtemperature
  - Current Limit
  - 50 V Peak Transient Capability
- Internally Fused Leads in SO−20L Package

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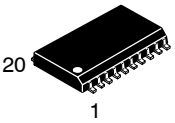
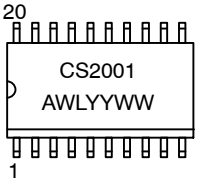


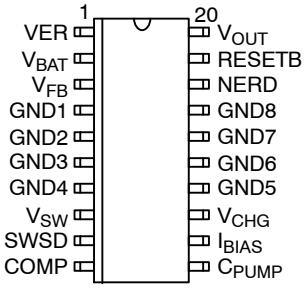

**SO−20L**
**DWF SUFFIX**
**CASE 751D**

### MARKING DIAGRAM




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

### PIN CONNECTIONS




### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| CS2001YDWF20 | SO−20L | 37 Units/Rail |
| CS2001YDWFR20 | SO−20L | 1000 Tape & Reel |

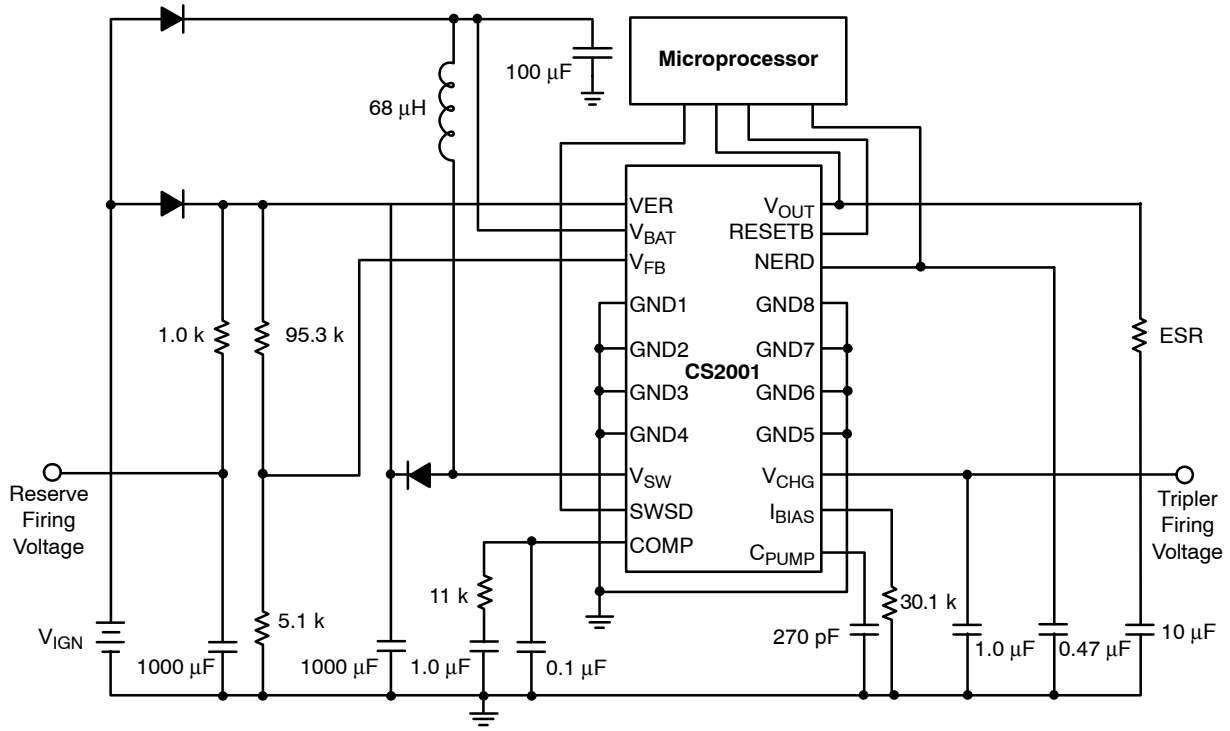



**Figure 1. Application Diagram**

## ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
|---|---|---|
| $V_{BAT}$ | −0.5 to 25 | V |
| VER | −0.5 to 25 | V |
| $V_{OUT}$ | −0.5 to 7.0 | V |
| Digital Input/Output Voltage | −0.5 to 7.0 | V |
| Peak Transient Voltage (36 V Load Dump @ 14 V Battery Voltage) | 50 | V |
| Storage Temperature Range | −55 to 150 | °C |
| Junction to Free Air Thermal Impedance | 55 | °C/W |
| ESD Susceptibility (Human Body Model) | 4.0 | kV |
| Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1) | 230 peak | °C |
| $T_A$ | −40 to 85 | °C |
| $T_J$ | −40 to 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

**ELECTRICAL CHARACTERISTICS** (8.0 V ≤ $V_{BAT}$ ≤ 16 V, 8.0 V ≤ VER ≤ 25 V, 1.0 mA ≤ $I_{V(OUT)}$ ≤ 100 mA, $T_{TEST}$ = −40°C to 125°C; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Linear Regulator** | | | | | |
| Output Voltage | Output Driven from $V_{BAT}$, VER = 25 V<br>Output Driven from VER, $V_{BAT}$ = 0 V | 4.9<br>4.9 | –<br>– | 5.1<br>5.1 | V<br>V |
| Regulator Bias Current (from $V_{BAT}$) | $I_{V(BAT)}$ @ $I_{V(OUT)}$ = −100 mA, SWSD = 4.0 V, $V_{BAT}$ = 16 V, VER = 25 V<br>T = −40°C<br>T = 25°C<br>T = 125°C | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>8.0<br>7.0<br>6.0 | <br>mA<br>mA<br>mA |
| Regulator Bias Current (from VER) | $I_{VER}$ @ $I_{V(OUT)}$ = −100 mA, SWSD = 4.0 V, $V_{BAT}$ = 0 V, VER = 25 V<br>T = −40°C<br>T = 25°C<br>T = 125°C | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>11<br>9.0<br>8.0 | <br>mA<br>mA<br>mA |
| Dropout Voltage $V_{BAT}$ – $V_{OUT}$ | VER = 25 V, $I_{V(OUT)}$ = −100 mA (Probe Only) | – | – | 1.5 | V |
| Dropout Voltage VER – $V_{OUT}$ | $V_{BAT}$ = 0 V, $I_{V(OUT)}$ = −100 mA | – | – | 1.5 | V |
| Smart Switch Threshold $V_{BAT}$ to VER | VER = 25 V, $I_{V(OUT)}$ = −50 mA | 6.5 | – | 8.0 | V |
| Smart Switch Threshold Hysteresis | VER = 25 V, $I_{V(OUT)}$ = −50 mA | 0.5 | – | 1.0 | V |
| $V_{OUT}$ Output Noise | $V_{BAT}$ = 16 V, VER = 25 V, $I_{V(OUT)}$ = − 1.0 mA, C = 10 μF, ESR = 0.5 Ω | – | – | 0.05 | V |
| Line Regulation | – | – | – | 0.025 | V |
| Load Regulation | – | – | – | 0.025 | V |
| Output Current Limit | – | 120 | – | – | mA |
| **Switching Regulator** | **VER = 25V, $I_{V(OUT)}$ = −1.0 mA** | | | | |
| Switching Frequency | $C_{PUMP}$ 270 pF, $R_{I(BIAS)}$ = 30.1 kΩ | 135 | 150 | 165 | kHz |
| Pump Drive Current | $\Delta I_{V(BAT)}$ for 0 A ≤ $I_{V(SW)}$ ≤ 1.2 A | – | – | 50 | mA |
| Switch Saturation Voltage | $I_{V(SW)}$ = 1.2 A | – | – | 1.6 | V |
| Output Current Limit | – | 1.2 | – | 2.4 | A |
| $V_{FB}$ Regulation | – | 1.238 | 1.27 | 1.303 | V |
| $V_{FB}$ Input Current | $V_{FB}$ Above Short Low Detection Level | – | – | 1.0 | μA |
| $V_{FB}$ Input Shorted Low Detection Level | – | 200 | 250 | 300 | mV |
| $C_{PUMP}$ Short Detection Threshold | – | 200 | 250 | 300 | mV |
| Maximum Duty Cycle | – | 80 | – | 95 | % |
| $V_{SW}$ Leakage Current | $I_{V(SW)}$ @ $V_{SW}$ = 50 V, SWSD = $V_{OUT}$ | – | – | 100 | μA |
| **Voltage Tripler** | **$V_{BAT}$ = 16 V, $I_{V(OUT)}$ = −1.0 mA, $C_{CHG}$ = 1.5 μF** | | | | |
| Output Voltage Clamp $V_{CHG}$ – VER | VER = 8.0 V, $I_{V(CHG)}$ = −30 μA<br>VER = 12 V, $I_{V(CHG)}$ = −90 μA | 6.25<br>6.25 | 8.0<br>8.0 | 13<br>13 | V<br>V |
| Initial Charge Time | $C_{CHG}$ = 0.15 μF, VER = 8.0 V, $V_{CHG}$ = 14.25 V | – | – | 30 | ms |
| Maximum Output Voltage Clamp $V_{CHG}$ | – | 25 | 32.5 | 40 | V |
| Output Voltage Clamp $V_{CHG}$ | VER = 28 V, $I_{V(CHG)}$ = 0 μA | 25 | 32.5 | 40 | V |
| Short Circuit Path Current Limit VER to $V_{CHG}$ | – | – | – | 3.0 | mA |

**ELECTRICAL CHARACTERISTICS (continued)** (8.0 V ≤ $V_{BAT}$ ≤ 16 V, 8.0 V ≤ VER ≤ 25 V, 1.0 mA ≤ $I_{V(OUT)}$ ≤ 100 mA, $T_{TEST}$ = −40°C to 125°C; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **RESETB OUTPUT** | **$V_{BAT}$ = 0 V** | | | | |
| High Threshold | $V_{OUT}$ Increasing | 4.525 | 4.75 | 4.85 | V |
| Low Threshold | $V_{OUT}$ Decreasing | 4.5 | 4.65 | 4.825 | V |
| Hysteresis | – | 25 | 100 | 200 | mV |
| Output Low Voltage | $V_{OUT}$ = 1.0 V, $I_{RESETB}$ = 100 μA<br>$I_{RESETB}$ = 1.0 mA, $V_{OUT}$ = 4.5 V | –<br>– | –<br>– | 0.5<br>0.5 | V<br>V |
| Pull−Up Resistor | RESETB = 1.0 V | 25 | 50 | 100 | kΩ |
| **SWSD Input** | **$V_{BAT}$ = 16 V, VER = 25 V, $I_{V(OUT)}$ = −1.0 mA** | | | | |
| High Threshold | – | – | – | 0.7 × $V_{OUT}$ | V |
| Low Threshold | – | 0.3 × $V_{OUT}$ | – | – | V |
| Input Impedance | Referenced to Ground | 10 | 20 | 40 | kΩ |
| **NERD OUTPUT** | **$V_{BAT}$ = 16 V, $I_{V(OUT)}$ = −1.0 mA, $C_{NERD}$ = 0.47 μF** | | | | |
| VER Detection Voltage | – | 1.5 | – | 6.5 | V |
| Output Low Voltage | $I_{NERD}$ = 1.0 mA, $V_{OUT}$ = 4.5 V | – | – | 0.5 | V |
| Pull−Up Current | NERD = 0.5 V | 30 | 40 | 50 | μA |
| Power On Delay | – | 6.25 | 8.5 | 11 | ms |
| Clamping Voltage (Low) | VER Present | 1.0 | 1.25 | 1.5 | V |
| Clamping Voltage (High) | VER Not Present | 3.5 | 3.75 | 4.0 | V |
| **General** | | | | | |
| VER Load Current | VER = 25 V, $V_{BAT}$ = 16 V, $I_{V(OUT)}$ = −100 mA<br>T = −40°C<br>T = 25°C<br>T = 125°C | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>5.0<br>5.0<br>4.0 | <br>mA<br>mA<br>mA |
| Thermal Shutdown | (Guaranteed by Design) | 160 | – | 210 | °C |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN # SO−20L | PIN SYMBOL | FUNCTION |
|---|---|---|
| 1 | VER | Energy reserve input. |
| 2 | $V_{BAT}$ | Battery input. |
| 3 | $V_{FB}$ | Charge PUMP control voltage input. |
| 4 | GND1 | Ground. |
| 5 | GND2 | Ground. |
| 6 | GND3 | Ground. |
| 7 | GND4 | Ground. |
| 8 | $V_{SW}$ | Charge PUMP switch collector. |
| 9 | SWSD | Charge PUMP shutdown input. |
| 10 | COMP | Charge PUMP compensation pin. |
| 11 | $C_{PUMP}$ | Charge PUMP timing cap input. |
| 12 | $I_{BIAS}$ | Reference current resistor pin. |

**PACKAGE PIN DESCRIPTION (continued)**

| PACKAGE PIN # SO−20L | PIN SYMBOL | FUNCTION |
|---|---|---|
| 13 | $V_{CHG}$ | Switched cap voltage tripler output. |
| 14 | GND5 | Ground. |
| 15 | GND6 | Ground. |
| 16 | GND7 | Ground. |
| 17 | GND8 | Ground. |
| 18 | NERD | No energy reserve detected output. |
| 19 | RESETB | Reset output. |
| 20 | $V_{OUT}$ | Linear regulator output. |

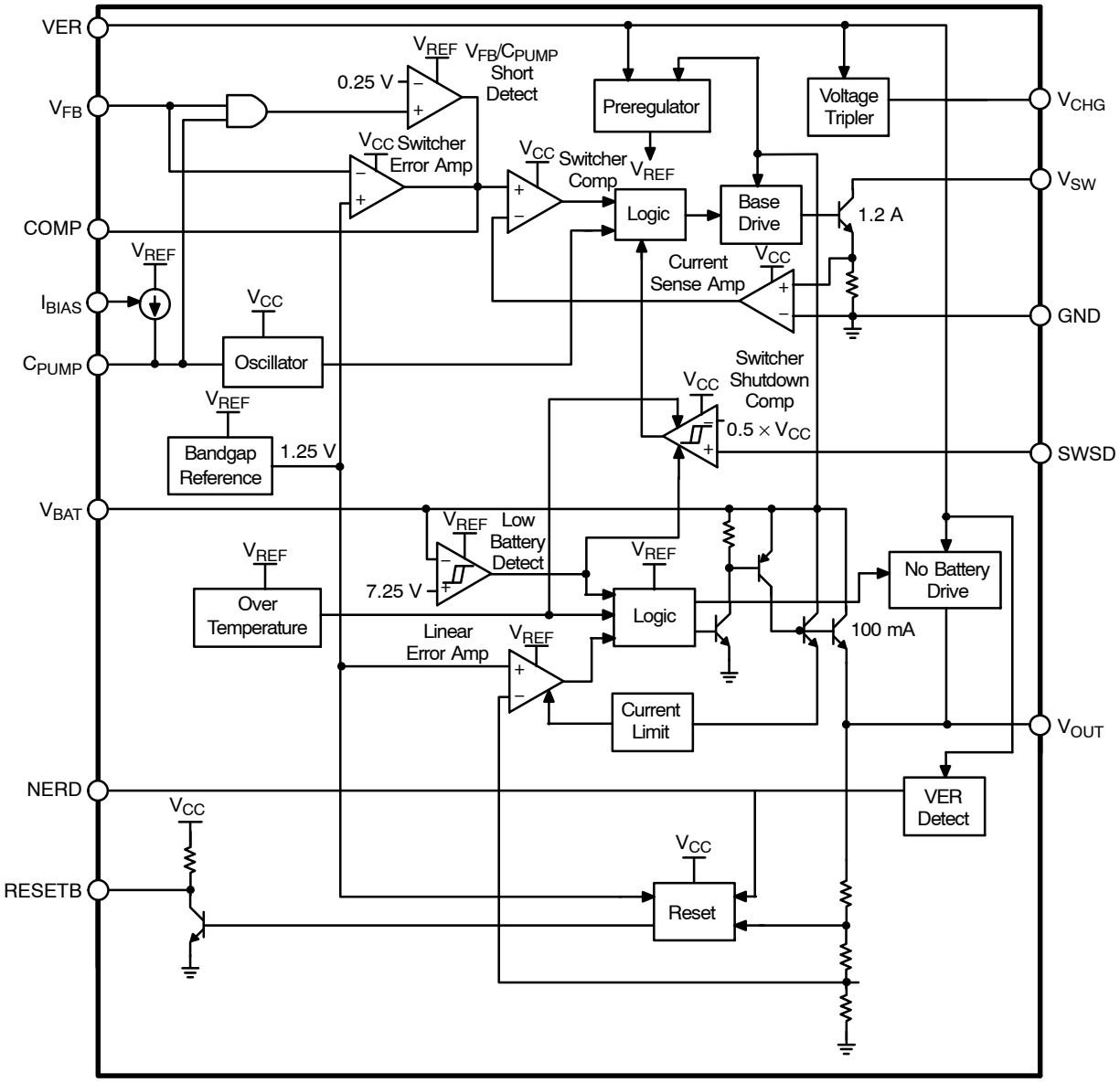



**Figure 2. Block Diagram**

## CIRCUIT DESCRIPTION

Figure 3 is an oscilloscope waveform showing the charge pump collector voltage, collector current and the charge pump timing capacitor during normal operation with $I_{VER}$ = 30mA.

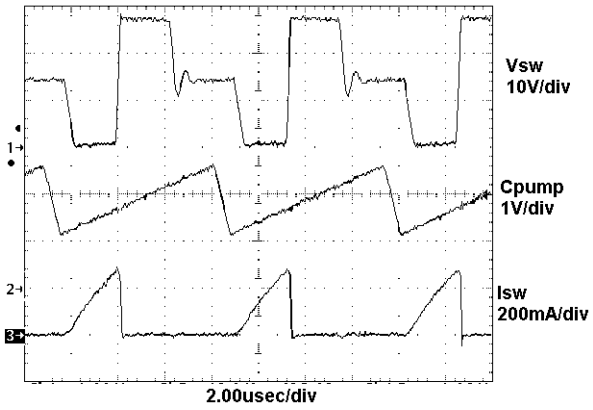



**Figure 3. Typical Operation with $I_{VER}$ = 30 mA**

Figure 4 is an oscilloscope waveform showing the voltage tripler output and the energy reserve input during power up.

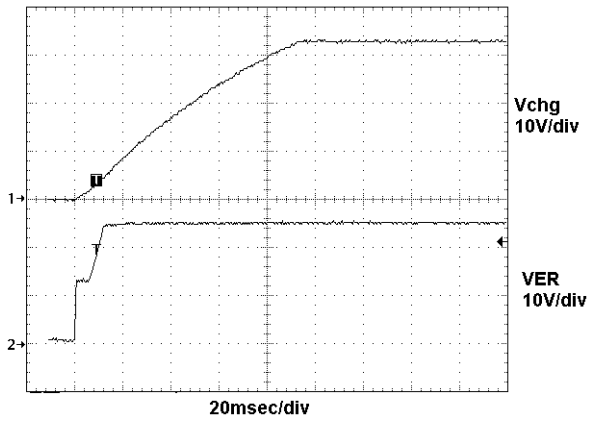
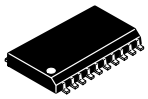



**Figure 4. Startup with $R_{V(CHG)}$ = 510 k**

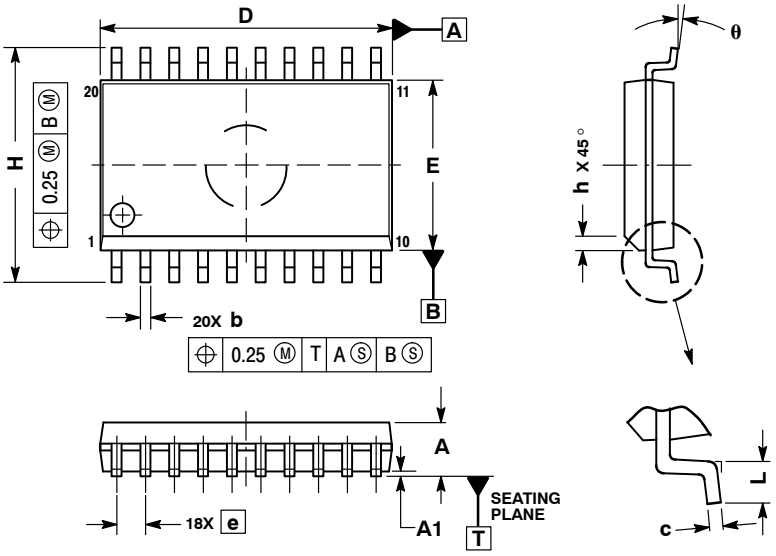
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



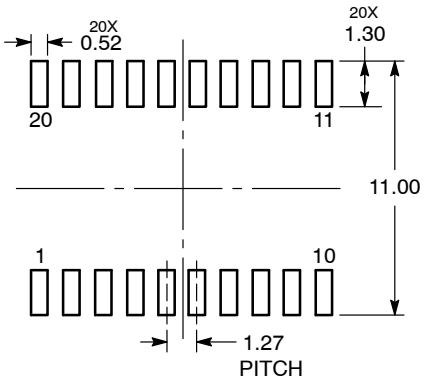
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

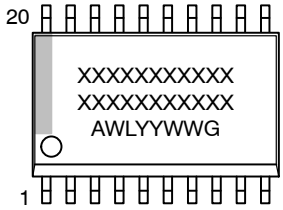
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC−20 WB** | **PAGE 1 OF 1** |

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