MPQ2484

75V, Multi-Topology LED Controller with Multiple Dimming Modes, AEC-Q100 Qualified

DESCRIPTION

The MPQ2484 is a flexible, multi-topology, asynchronous controller for LED lights with a high brightness. The device supports buck, boost, and buck-boost configurations, which makes it well-suited for multi-purpose applications. The MPQ2484 features a wide 4.5V to 45V input voltage (V_{IN}) range, with a maximum boost voltage up to 75V. Peak current mode operation provides fast transient response and eases loop stabilization.

The switching frequency (f_{SW}) can be set by the FSET pin, or it can be synchronized by a 100kHz to 2.2MHz external clock signal. The configurable frequency spread spectrum (FSS) function can periodically enable dither switching to improve EMI.

The MPQ2484 provides dimming switch mode with a P-channel MOSFET. During normal operation without a P-channel MOSFET, two-step dimming or PWM dimming can be selected.

Robust fault protections include thermal shutdown, cycle-by-cycle peak current limiting, output over-voltage protection (OVP), output short-circuit protection (SCP), LED open protection, and LED short protection. The fault indicator outputs an active logic low signal if a fault occurs.

The MPQ2484 is available in a TSSOP-28EP package.

FEATURES

- **Built to Handle Automotive Lighting:**
    - Load Dump Up to 45V
    - Cold Crank Down to 4.5V
    - Maximum 75V Boost Output
    - Multiple Dimming Modes
    - Two-Step Dimming via the H/L Pin
    - External PWM Dimming via the PDIM Pin
    - Integrated P-Channel Dimming MOSFET Driver
    - Available in AEC-Q100 Grade 1
- Supports Buck, Boost, and Buck-Boost Topologies
- **Low-Noise EMI/EMC:**
    - Frequency Spread Spectrum (FSS)
    - Configurable or Synchronizable Switching Frequency (f_{SW})
- **Robust Protections:**
    - Cycle-by-Cycle Current Limit
    - Output Over-Voltage Protection (OVP)
    - Open LED Protection
    - LED String Anode/Cathode to Battery/Ground Short Protection
    - One or More LEDs Short Protection
    - Over-Temperature Shutdown
    - Fault Flag Output
- **Additional Features:**
    - <5μA Shutdown Current
    - <1mA Quiescent Current
    - Configurable Current-Sense Reference via an External Setting Resistor
    - External Loop Compensation
    - Available in a TSSOP-28EP Package

APPLICATIONS

- **Automotive Exterior LED Lighting:**
    - Headlights
    - Daytime Running Lights (DRLs)
    - Fog Lights/Signal Lights
- Indoor and Outdoor LED Lighting
- Commercial and Industrial LED Lighting

TYPICAL APPLICATION

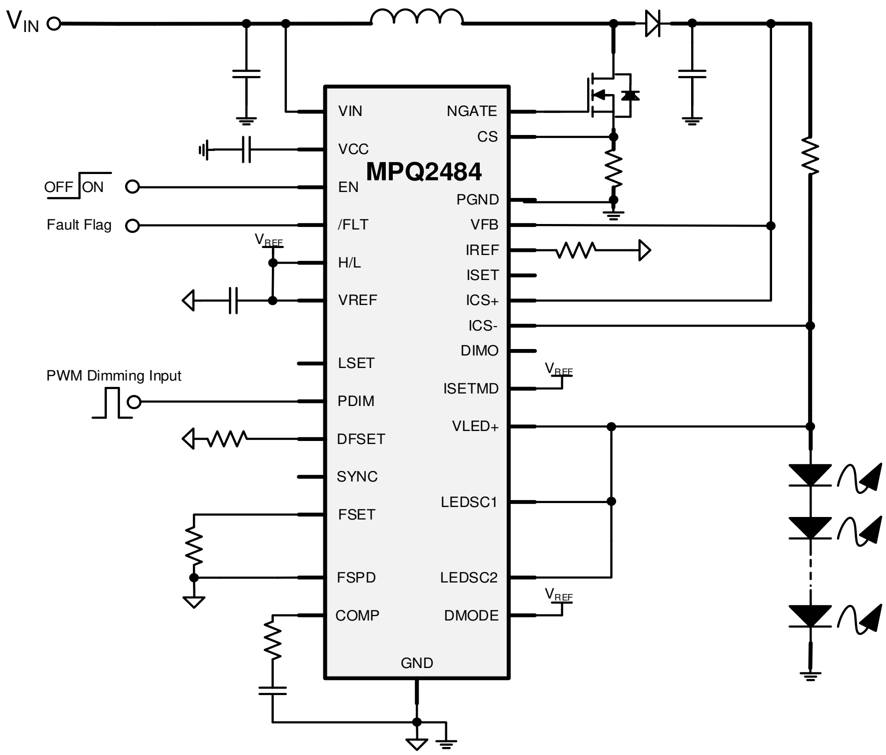


Figure 1: Boost Configuration

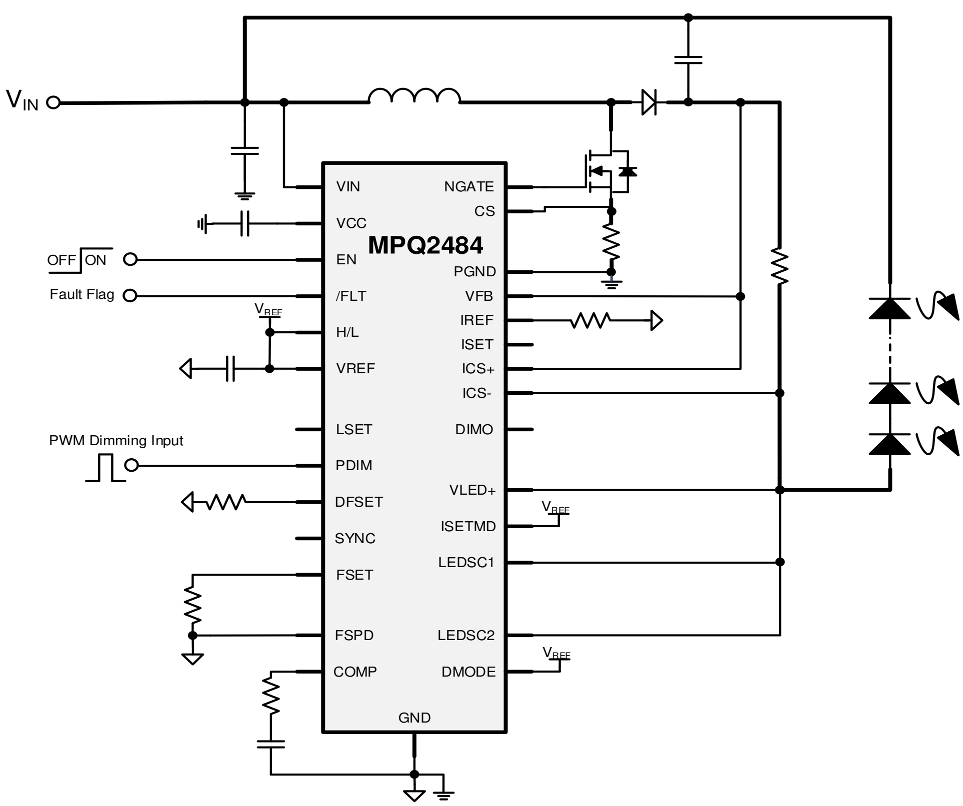


Figure 2: Buck-Boost Configuration

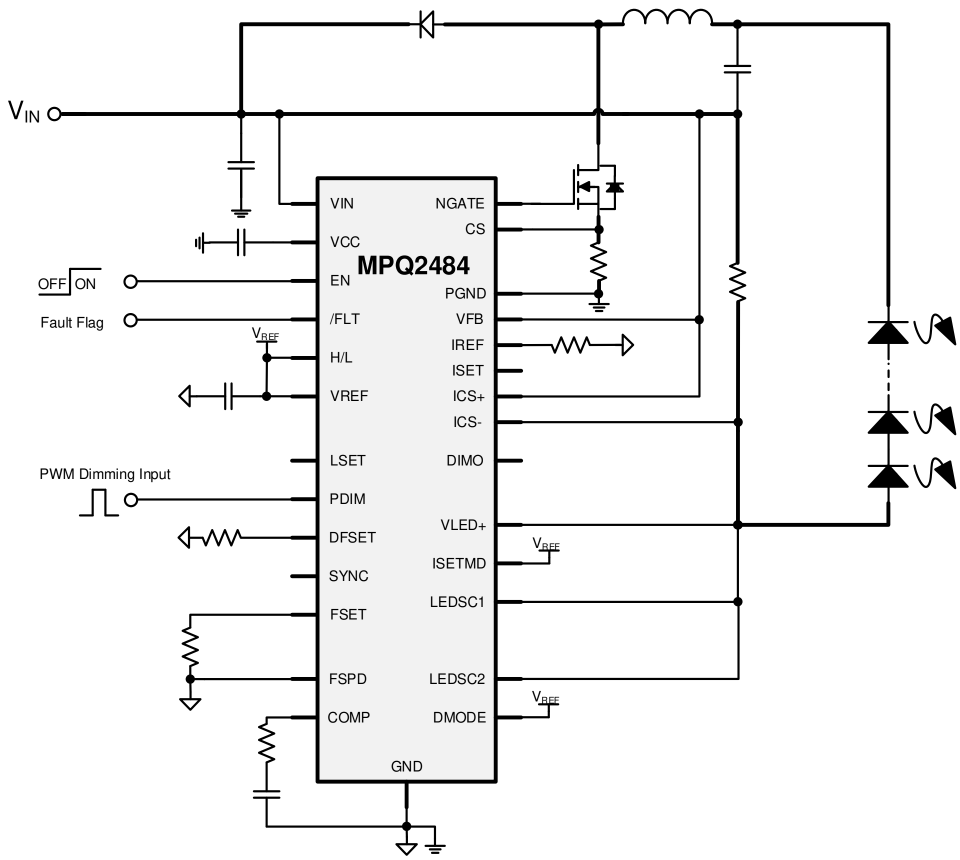


Figure 3: Buck Configuration

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2484GF-AEC1	TSSOP-28EP	*See Below*	Level 2a

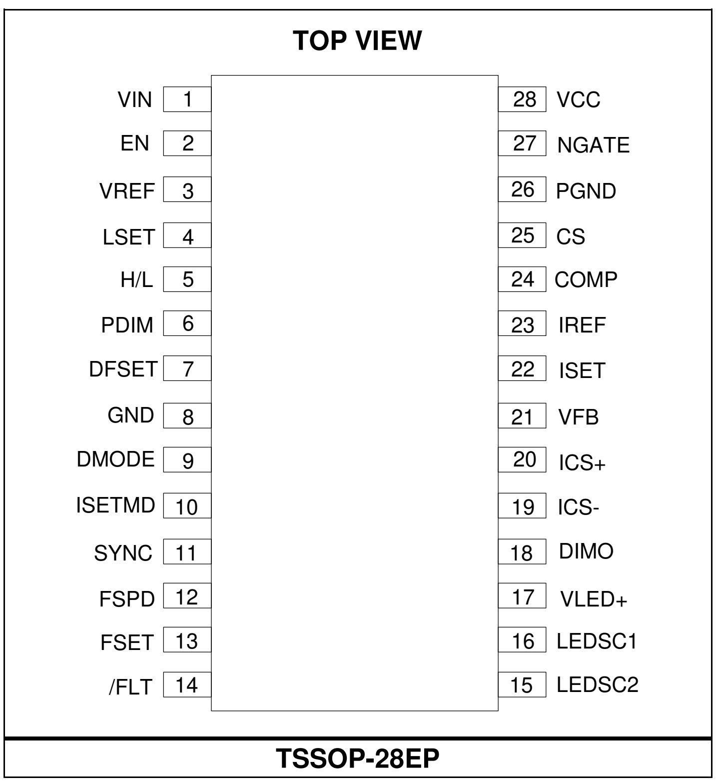
*For Tape & Reel, add suffix -Z (e.g. MPQ2484GF-AEC1-Z).
**Moisture Sensitivity Level Rating

TOP MARKING (MPQ2484GF-AEC1)

MPSYYWW
MP2484
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2484: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Power supply input.** Connect a bypass capacitor from VIN to PGND to reduce noise.
2	EN	**On/off control input and custom input UVLO setting.** The EN pin can be driven by an external logic signal to enable and disable the chip. Pull EN above 1.3V to enable the part; pull it below 0.4V to shut down the part. Set a configurable input voltage (V_{IN}) under-voltage lockout (UVLO) threshold by tying a resistor divider from the input to the EN pin. Do not float EN.
3	VREF	**2.37V reference output.** VREF is the reference for LED short detection. Bypass VREF to GND with an external 1nF to 10nF ceramic capacitor.
4	LSET	**Dimming duty setting for two-step dimming.** If the H/L pin is pulled down to ground, the LSET pin's voltage determines the two-step dimming duty cycle. A resistor divider is tied from VREF to LSET to set the two-step dimming threshold. If two-step dimming mode is not used, float the LSET pin.
5	H/L	**Two-step dimming control input.** When two-step dimming is selected and the H/L pin is logic high, the LED output current is set to full scale (no dimming). If the H/L pin is logic low, the LSET voltage sets the two-step dimming threshold. If two-step dimming mode is not used, connect the H/L pin to VREF. Do not float H/L.
6	PDIM	**PWM dimming pulse input.** If PWM dimming is selected, connect the H/L pin to VREF and apply a PWM signal to the PDIM pin for LED dimming. When PDIM is pulled down to logic low, switching stops and DIMO pulls high to turn off the dimming P-channel MOSFET. Connect a ceramic bypass capacitor from the PDIM pin to GND when two-step dimming is activated.
7	DFSET	**Two-step dimming frequency setting.** Connect an external capacitor from the DFSET pin to GND. The internal source/sink current source charges and discharges the capacitor repeatedly to generate a stable triangular wave. The LSET level is compared to the triangular wave to output a PWM dimming signal. If PWM dimming is used, tie the DFSET pin to ground using a 7.14kΩ to 8.46kΩ resistor. A 8.06kΩ resistor is recommended.
8	GND	**Signal ground.**
9	DMODE	**Dimming mode control input.** If the DMODE pin is pulled down to GND, place an additional P-channel MOSFET in series with the LED string to improve dimming performance. This additional MOSFET can also act as a protection MOSFET in buck-boost and boost mode. If this pin is logic high, the P-channel MOSFET driver is disabled. Do not float DMODE.
10	ISETMD	**Current-sense reference selection input.** If the ISETMD pin is logic high, the LED current-setting reference voltage (ICS+ - ICS-) is set between 0mV and 100mV when the ISET voltage (V_{ISET}) rises from 0.6V to 1.2V. This supports thermal derating when an NTC resistor is tied from ISET to GND. If the ISETMD pin is pulled down to GND, the LED current can be set at up to 200% of the nominal value when V_{ISET} rises from 0.6V to 1.8V. This feature can be used for analog dimming.
11	SYNC	**Synchronization input.** If an external clock pulse signal is connected to the SYNC pin, the frequency setting function on the FSET pin is disabled, and the chip synchronizes its switching with the external clock. Ensure that the SYNC high level exceeds 1.4V and that the low level is below 0.6V. Float SYNC if external synchronization is not used.
12	FSPD	**Frequency spread spectrum (FSS) output ramp.** Connect a capacitor from the FSPD pin to GND, and connect a resistor between the FSPD and FSET pins to dither the switching frequency (f_{SW}) for spread spectrum. Remove the resistor if FSS is disabled. For more details, see the Frequency Spread Spectrum section on page 44.
13	FSET	**Switching frequency setting.** Connect an external resistor from FSET to GND to set the internal switching clock frequency. R_{FSET} (kΩ) = 8333 / f_{SW} (kHz). Do not float FSET.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
14	/FLT	**Fault flag indicator output.** The /FLT pin is an active-low, open-drain output. Connect an external pull-up resistor to this pin. If a fault status is activated, /FLT is pulled down to GND. If the system recovers and no fault status is detected for 30µs, then the /FLT pin is released to an open-drain condition.
15	LEDSC2	**One or more LEDs short sense input 2.** The LEDSC2 pin senses the LED string's voltage drop via a resistor divider. Short LEDSC2 and LEDSC1 to LED+ if this protection is not used.
16	LEDSC1	**One or more LEDs short sense input 1.** The LEDSC1 pin senses a single LED's voltage drop via a resistor divider. Short LEDSC1 and LEDSC2 to LED+ if this protection is not used.
17	VLED+	**LED string anode input.** The VLED+ pin is used for fault detection with other pins. If an external dimming P-channel MOSFET is not connected, short VLED+ to ICS-.
18	DIMO	**Dimming P-channel MOSFET gate driver output.** If the dimming P-channel MOSFET is connected, the DIMO pin drives the external P-channel MOSFET as a dimming switch. Float DIMO if the external P-channel MOSFET is not connected.
19	ICS-	**High-side LED current-sense negative input.**
20	ICS+	**High-side LED current-sense positive input.** For full-scale LED current control, the voltage between ICS+ and ICS- is regulated to 100mV.
21	VFB	**LED string voltage feedback input.** Connect a resistor divider from ICS+ to the LED string cathode. The VFB pin is tied to the tap of the resistor divider to sense the LED string voltage for over-voltage protection (OVP).
22	ISET	**LED current setting.** Connect an external resistor from ISET to ground. V_{ISET} can set the reference voltage (V_{REF}) for the LED current regulator. When ISETMD is pulled down to GND and V_{ISET} rises up from 0.6V to 1.8V, V_{REF} rises from 0mV to 200mV. This feature can be used after setting a resistor on the LED light load, which allows the LED current to be adjusted. When ISETMD is pulled high and V_{ISET} rises from 0.6V to 1.2V, V_{REF} rises from 0mV to 100mV. If the ISET pin is left floating, the current reference is fixed at 100mV.
23	IREF	**Biased current setting for ISET.** The IREF pin sets the bias current (I_{ISET} = 100 x I_{IREF}) for the ISET resistor to improve accuracy. Tie a resistor from IREF to ground. Do not float IREF.
24	COMP	**Compensation connection.** The COMP pin is the internal error amplifier's (EA's) output. Connect a resistor and capacitor network to this pin for system stability.
25	CS	**N-channel MOSFET current-sense input.** Tie a current-sense resistor from the N-channel MOSFET source to PGND to sense the switching current and set the current limit. Add a resistor/capacitor network between CS and the current-sense resistor to configure the slope compensation.
26	PGND	**Power ground.** Ground return for the N-channel MOSFET's current sense.
27	NGATE	**Power N-channel MOSFET gate driver output.** Connect NGATE to the gate of the N-channel MOSFET.
28	VCC	**8.5V internal regulator output.** VCC supplies power to both control blocks and the N-channel MOSFET's gate driver. Bypass VCC to PGND with an external ceramic capacitor.

ABSOLUTE MAXIMUM RATINGS [1]

VIN to PGND .... -0.3V to +50V
VFB to PGND .... -0.3V to +80V
ICS+, ICS-, DIMO to PGND .... -0.3V to +80V
VFB to ICS+...................................... -6V to +6V
ICS- to ICS+ .... -6V to +0.3V
DIMO to ICS+ .... -12V to +0.3V
VLED+ to PGND.......................... -0.3V to +80V
VLED+ to ICS+ .... -90V to +0.3V
LEDSC1, LEDSC2 to PGND........ -0.3V to +80V
LEDSC1 to LEDSC2......................... -6V to +6V
VCC to PGND.............................. -0.3V to +12V
NGATE to PGND .... -0.3V to (V_{CC} + 0.3V)
CS to PGND .... -0.3V to +6V
PGND to GND .... -0.3V to +0.3V
All other pins to GND .... -0.3V to +6V
Continuous power dissipation……(T_A = 25°C) [2]
TSSOP-28EP 3.9W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature................ -65°C to +150°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM) .... Class 2 [3]
Charged device model (CDM) ....Class C2 [4]

Recommended Operating Conditions

Supply voltage (V_{IN}) .... 4.5V to 45V
Max boost voltage ICS+ to PGND................75V
Operating junction temp (T_J) ...-40°C to +150°C

Thermal Resistance [5]

	θ_{JA}	θ_{JC}	
TSSOP-28EP JESD51-7	32	6	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Operating range	V_{IN}		4.5		45	V
VIN under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.6	3.9	4.2	V
VIN UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			250	500	mV
Input Supply Current						
Shutdown current	I_{SD}	V_{EN} = 0V, ICS+ floating		1	5	μA
Quiescent current (normal)	I_Q	No switching		0.7	1	mA
VCC Regulator						
Regulator output voltage	V_{CC}	10V ≤ V_{IN} ≤ 15V, 0.1mA ≤ I_{CC} ≤ 50mA 15V ≤ V_{IN} ≤ 45V, 0.1mA ≤ I_{CC} ≤ 35mA	7.8	8.5	9.2	V
Dropout voltage	V_{CC_DR}	V_{IN} = 4.5V, I_{CC} = 50mA		520	1150	mV
Short-circuit current limit	I_{CC_MAX}	V_{CC} = 0V	55	100	150	mA
VCC UVLO threshold	V_{CC_UVLO}	V_{CC} falling	3.6	3.9	4.2	V
VCC UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			235	500	mV
Reference Regulator						
VREF output voltage	V_{REF}	4.5V ≤ V_{IN} ≤ 45V, 0μA ≤ I_{REF} ≤ 100μA	2.31	2.37	2.43	V
Short-circuit current limitation	I_{REF_MAX}	V_{REF} = 0V		220		μA
Oscillator						
Switching frequency	f_{SW}		100		2200	kHz
Oscillator frequency accuracy	f_{SW}	R_{FREQ} = 82.5kΩ	85	100	125	kHz
		R_{FREQ} = 17.8kΩ	423	470	517	kHz
		R_{FREQ} = 3.3kΩ	1980	2200	2420	kHz
Biased voltage at FSET	V_{FSET}		0.575	0.608	0.63	V
Maximum duty cycle	D_{MAX}	V_{CS} = 0V, V_{ICS+} - V_{ICS-} = 0.09V	92	95	98	%
Synchronization frequency range	f_{SYNC}	f_{SYNC} < 2.2MHz	110%		170%	f_{SW}
SYNC logic high threshold	V_{SYNC_H}	V_{SYNC} rising	1.4			V
SYNC logic low threshold	V_{SYNC_L}	V_{SYNC} falling			0.5	V
SYNC minimal logic high pulse width (6)	$t_{SYNC\_PW\_MIN}$		200			ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Frequency Spread Spectrum						
FSPD source current	I_{FSPD_SOURCE}	DIM on, V_{FSPD} = 0V	70	100	130	μA
FSPD sink current	I_{FSPD_SINK}	DIM on, V_{FSPD} = 2.5V	70	100	130	μA
FSPD high flip threshold	V_{FSPD_H}	DIM on, V_{FSPD} rising	1.1	1.2	1.3	V
FSPD low flip threshold	V_{FSPD_L}	DIM on, V_{FSPD} falling	0.52	0.6	0.68	V
Enable						
Logic enable threshold	$V_{EN\_LOGIC\_H}$	V_{EN} rising	1.3			V
Logic disable threshold	$V_{EN\_LOGIC\_L}$	V_{EN} falling			0.4	V
System enable threshold	$V_{EN\_SYS\_ON}$	V_{EN} rising	1.42	1.5	1.58	V
Pull-up hysteresis current	$I_{EN\_SYS\_HYS}$	After the converter works	200	630	1000	nA
Hysteresis voltage	$V_{EN\_SYS\_HYS}$		50	150	300	mV
NMOS Driver						
NGATE output voltage	V_{NGATE}	V_{CC} = 8.5V	8	8.5		V
		V_{CC} = V_{CC_UVLO} + 50mV	3.5			V
NGATE pull-up resistor	$R_{PULL-UP}$	V_{CC} = 8.5V, V_{NGATE} = 0V		1000	2000	mΩ
NGATE pull-up resistor	$R_{PULL-UP}$	V_{CC} = V_{NGATE} = 8.5V		1500	2500	mΩ
NGATE rising time (6)	t_{R_NG}	C_{NGATE} = 10nF		30		ns
NGATE falling time (6)	t_{F_NG}	C_{NGATE} = 10nF		30		ns
NMOS Current Sense Comparator						
Leading edge blanking time	t_{CS_LEB}			90		ns
Current-sense clamp voltage	V_{CS_CLAMP}	Cycle-by-cycle limit	360	400	440	mV
Slope compensation ramp peak current	I_{SLOP_PK}	Ramp peak current during each switching cycle	37	50	60	μA
Dimming PMOS Driver						
Biased voltage UVLO threshold	V_{ICS+_UVLO}	V_{ICS+} falling	7.9	8.5	9.1	V
Biased voltage UVLO hysteresis	V_{ICS+_HYS}		100	200	300	mV
DIMO lowest output voltage with respect to V_{ICS+}	V_{DIMO_MIN}	12V < V_{ICS+} < 75V	-12	-11	-10	V
		V_{ICS+} = V_{ICS+_UVLO} + 50mV			-6.5	V
DIMO peak source current	I_{DIMO_SOURCE}	V_{DIMO} - V_{ICS+} = -8.5V	25	50	80	mA
DIMO peak sink current	I_{DIMO_SINK}	V_{DIMO} = V_{ICS+}	30	50	65	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LED Current Regulation						
Feedback reference voltage	V_{ICS_FB}	100% scale, ±5%	93	100	107	mV
ICS+ bias current	I_{CS+}	DIM off, V_{ICS+} = 75V		170	250	µA
ICS- bias current	I_{CS-}		-200		+200	nA
Biased voltage at IREF	V_{IREF}		0.785	0.805	0.825	V
Current gain	I_{SET} / I_{REF}		95	100	105	%
ISET max current setting threshold	V_{ISET_MAX}	V_{ICS_FB} = 200mV	1.4	1.8	2.2	V
ISET min current setting threshold	V_{ISET_MIN}	V_{ICS_FB} = 10mV	0.5	0.63	0.73	V
VLED+ bias current	I_{VLED+}		40	75	100	µA
Compensation						
Error amplifier (EA) transconductance	G_{EA}		3.1	4.5	5.9	mA/V
COMP source current	I_{COMP_SOURCE}	V_{COMP} = 0V	200	570	1000	µA
COMP sink current	I_{COMP_SINK}	V_{COMP} = 4.5V	200	570	1000	µA
Two-Step Dimming						
H/L high level threshold	V_{H/L_H}	$V_{H/L}$ rising	1.4			V
H/L low level threshold	V_{H/L_L}	$V_{H/L}$ falling			0.6	V
DFSET source current	I_{DFSET_SOURCE}	Triangular wave, V_{DFSET} = 0V	70	100	130	µA
DFSET sink current	I_{DFSET_SINK}	Triangular wave, V_{DFSET} = 1.5V	70	100	130	µA
DFSET high flip threshold	V_{DFSET_H}	V_{DFSET} rising	1.122	1.2	1.278	V
DFSET low flip threshold	V_{DFSET_L}	V_{DFSET} falling	0.56	0.6	0.64	V
PWM Dimming (Tie an 8.06kΩ Resistor from DFSET to Ground, or Set V_{DFSET} = 1V)						
PDIM pull-up current	I_{PDIM}	$V_{H/L}$ = 2V, V_{PDIM} = 0V		3	5	µA
PDIM logic high threshold	V_{PDIM_H}	V_{PDIM} rising	V_{DFSET} + 100mV			V
PDIM logic low threshold	V_{PDIM_L}	V_{PDIM} falling			V_{DFSET} - 100mV	V
PDIM to DIMO turn-on delay	$t_{PWM\_DELAY\_ON}$	C_{DIMO-_ICS+} = 7nF		3		µs
PDIM to DIMO turn-off delay	$t_{PWM\_DELAY\_OFF}$	C_{DIMO-_ICS+} = 7nF		2		µs
Current-Sense Reference Selection						
ISETMD logic high threshold	V_{ISETMD_H}	V_{ISETMD} rising	1.4			V
ISETMD logic low threshold	V_{ISETMD_L}	V_{ISETMD} falling			0.6	V
ISETMD pull-up current	I_{ISETMD}	V_{ISETMD} = 0V		3	5	µA
Dimming Mode Selection						
DMODE logic high threshold	V_{DMODE_H}	V_{DMODE} rising	1.4			V
DMODE logic low threshold	V_{DMODE_L}	V_{DMODE} falling			0.6	V
DMODE pull-up current	I_{DMODE}	V_{DMODE} = 0V		3	5	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, typical values are at T_J = 25°C, unless otherwise noted.

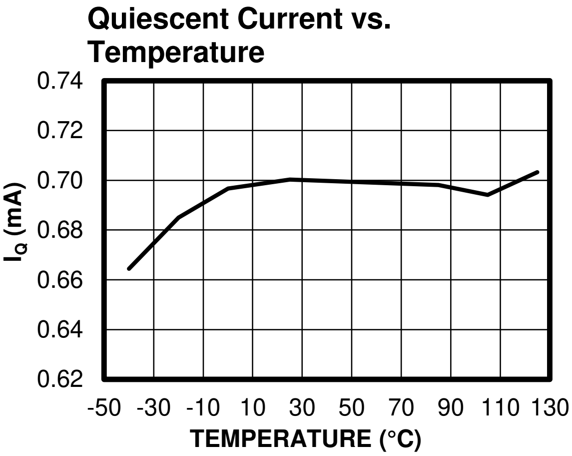
Parameters	Symbol	Condition	Min	Typ	Max	Units
Over-Voltage Protection (without Fault Flag Indication)						
OVP threshold with respect to V_{ICS+}	VFB_{OVP}	(V_{FB} - V_{ICS+}) falling	-1.24	-1.17	-1.1	V
OVP hysteresis	VFB_{OVP_HYS}		50	150	250	mV
VFB bias current	I_{VFB}		-65		+65	nA
Under-Current Protection (UCP) (for OLP and SCP, with Fault Flag Indication)						
UCP threshold with respect to V_{ICS+}	V_{UCP}	V_{CC_MODE} = 0V, (V_{ICS-} - V_{ICS+}) rising	-70	-50	-30	mV
Short-Circuit Protection (SCP) with Fault Flag Indication						
SCP threshold with respect to V_{ICS+}	V_{SCP}	(V_{ICS-} - V_{ICS+}) falling	-325	-300	-275	mV
VLED+ short threshold	V_{LED+_SCP}	V_{LED} + falling	1.3	1.5	1.7	V
		(V_{LED} + - V_{IN}) falling	1.1	1.5	2	V
		(V_{LED+} - V_{IN}) is almost equal to 0V	-0.45	0	+0.1	V
SCP fault activation delay time (counter increases only at dimming on)	t_{SCP_DELAY}	Only level I		4096		Clock cycles
		Level I and VLED+ short or level II		32		Clock cycles
Short One or More LEDs Protection (Activated and with Fault Flag Indication in V_{DMODE} = 2V)						
LED short threshold	V_{LED_SHORT}	Level I, |V_{LEDSC1} - V_{LEDSC2}| rising	20	80	150	mV
		Level II, |V_{LEDSC1} - V_{LEDSC2}| rising	70	180	270	mV
LED short fault activation delay time (counter increases only at dimming on)	$t_{LED\_SHORT\_DELAY}$	Level I		4096		Clock cycles
		Level II		32		Clock cycles
Thermal Shutdown						
Thermal shutdown threshold (6)	T_{SD}	T_J rising		170		°C
Thermal shutdown hysteresis (6)	T_{HYS}			20		°C
Fault Recovery Timer						
Hiccup delay time (counter increases when dimming is on)	t_{HICCUP}	After a fault status is activated, except OTP		8192		Clock cycles
Fault Flag (Open Drain)						
/FLT output low voltage	V_{FLT_L}	I_{FLT_SINK} = 1mA			200	mV
/FLT leakage current	I_{FLT_LKG}	V_{FLT} = 5V			1	µA

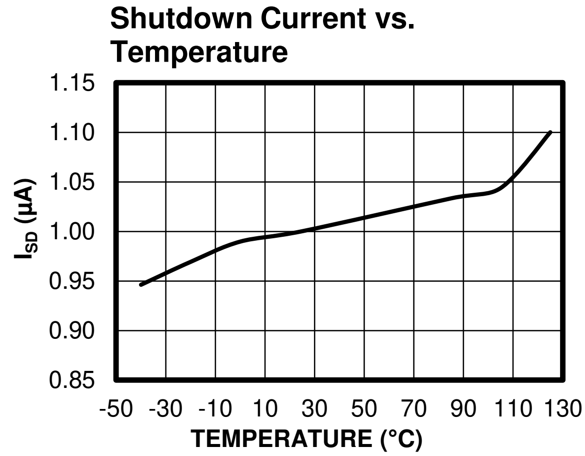
Note:

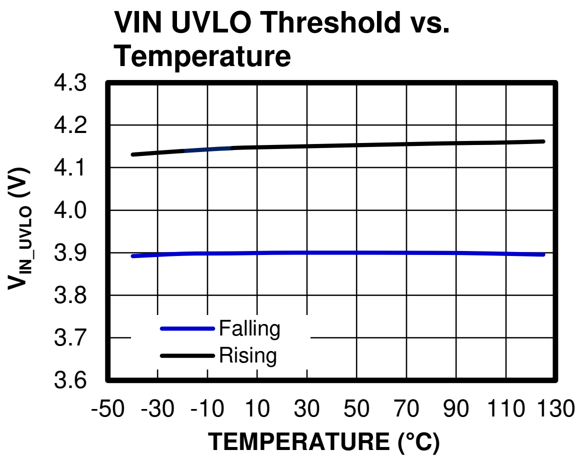
6) Not tested in production. Guaranteed by design and characterization.

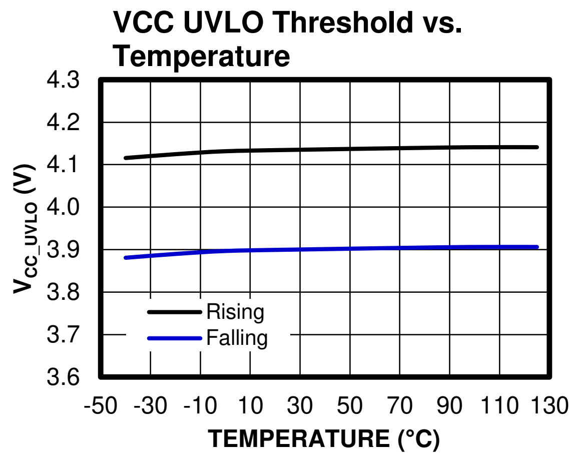
TYPICAL CHARACTERISTICS

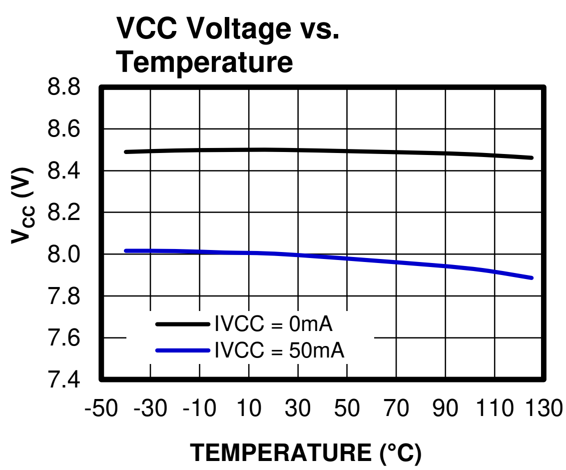
V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

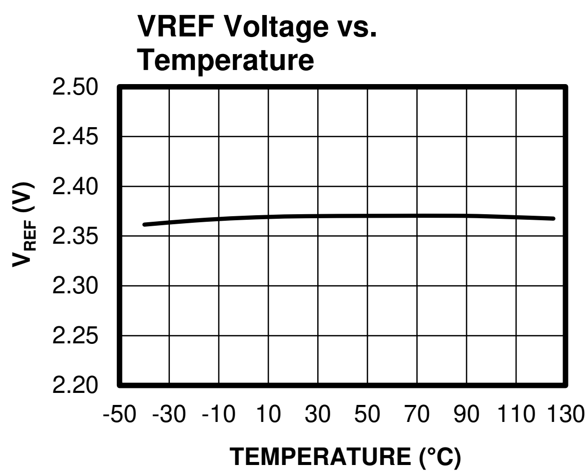








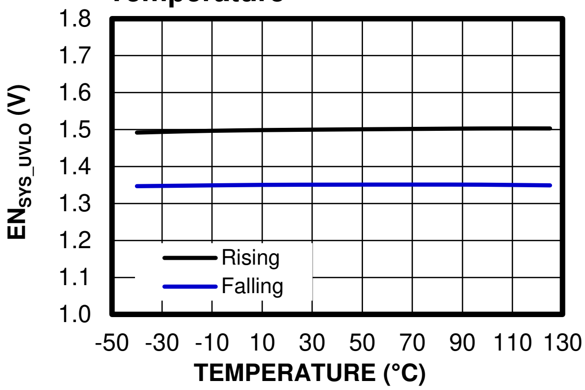




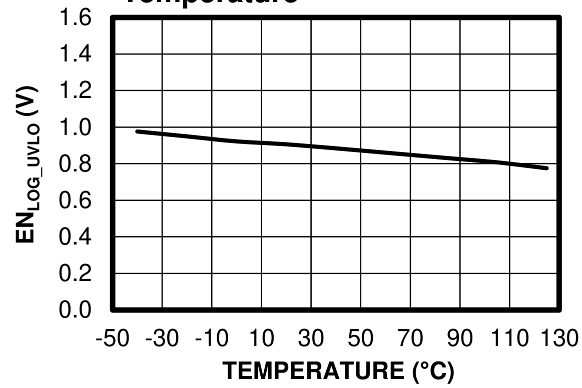
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

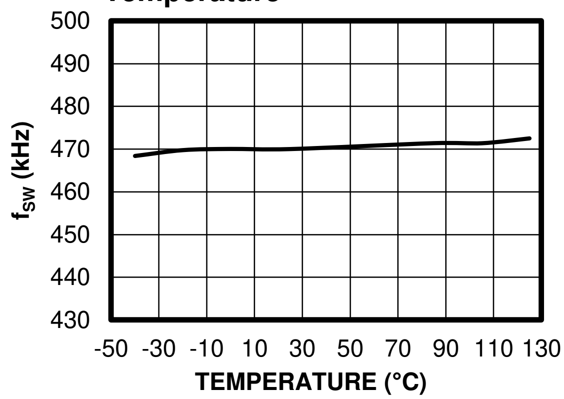
EN System UVLO vs. Temperature



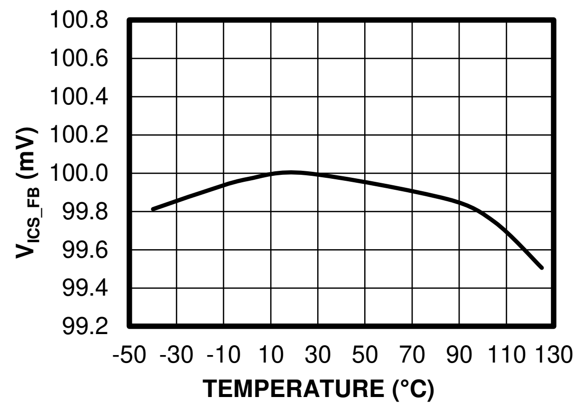
EN Logic UVLO Threshold vs. Temperature



Switching Frequency vs. Temperature

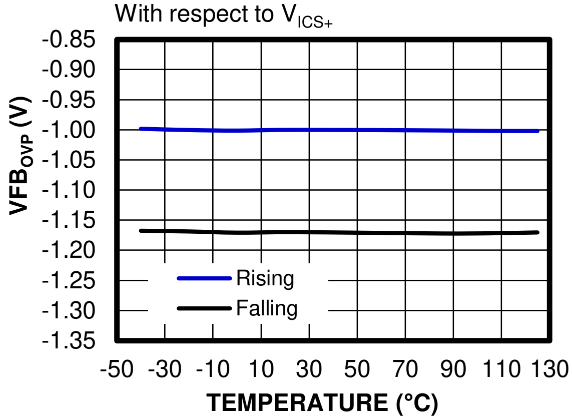


Feedback Reference Voltage vs. Temperature

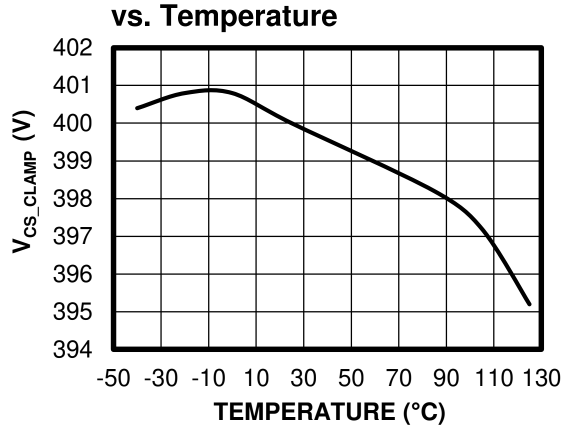


OVP Threshold vs. Temperature

With respect to V_{ICS+}



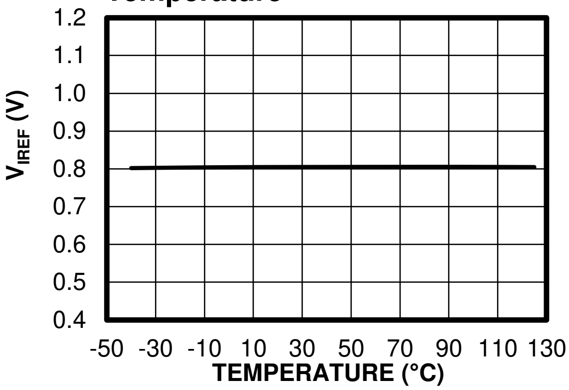
CS Cycle-by-Cycle Limit Voltage vs. Temperature



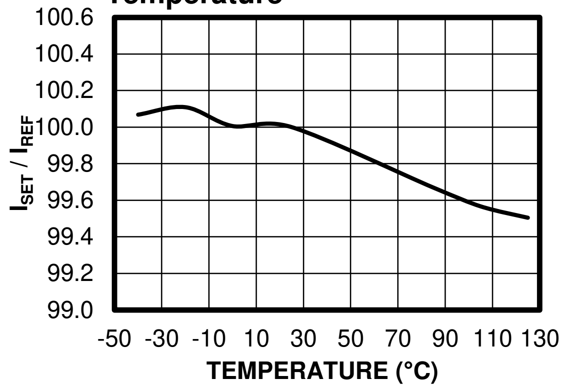
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

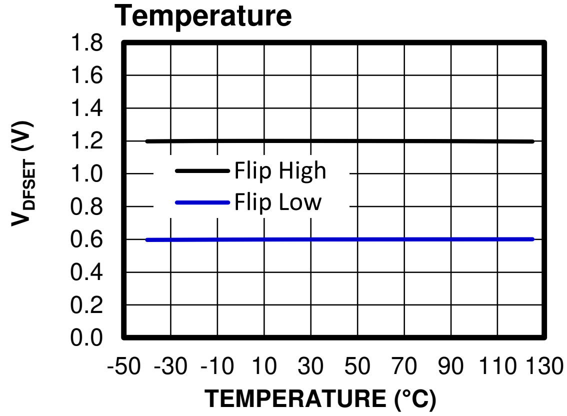
IREF Voltage vs. Temperature



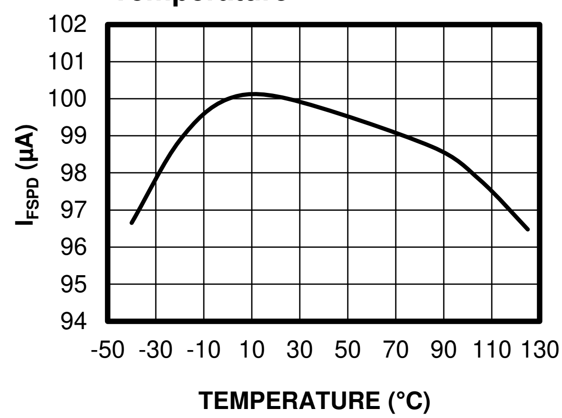
ISET to IREF Current Gain vs. Temperature



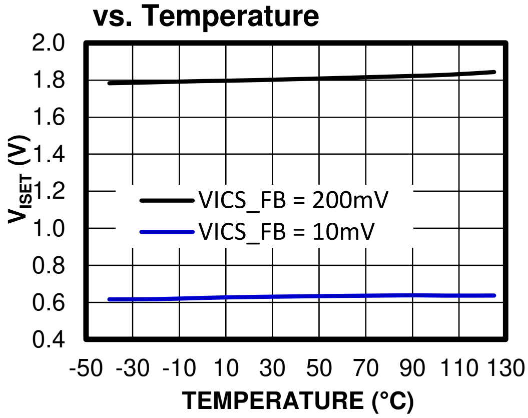
DFSET Flip Threshold vs. Temperature



FSPD Source/Sink Current vs. Temperature

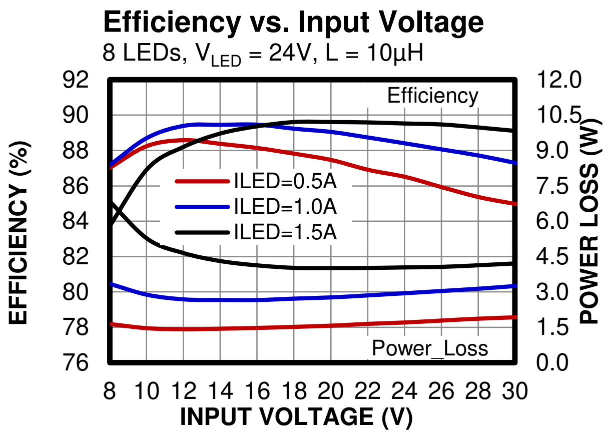


ISET Current-Setting Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Buck-boost mode, 8 LEDs (V_{LED} = 24V), V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

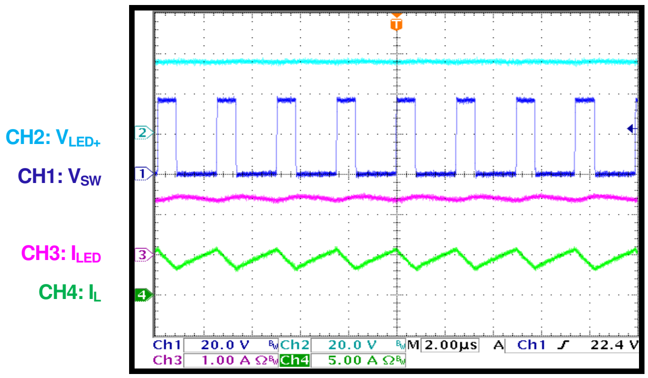


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

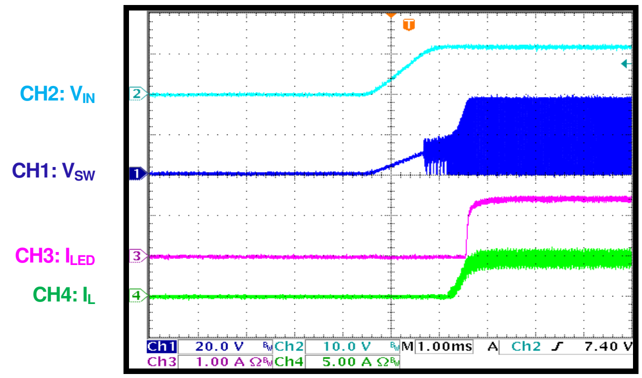
Steady State

I_{LED} = 1.5A



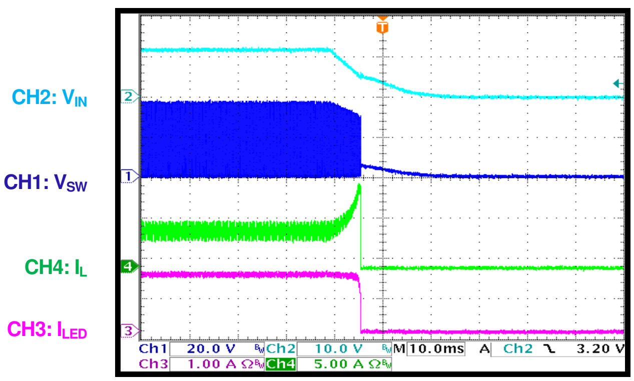
Start-Up through VIN

I_{LED} = 1.5A



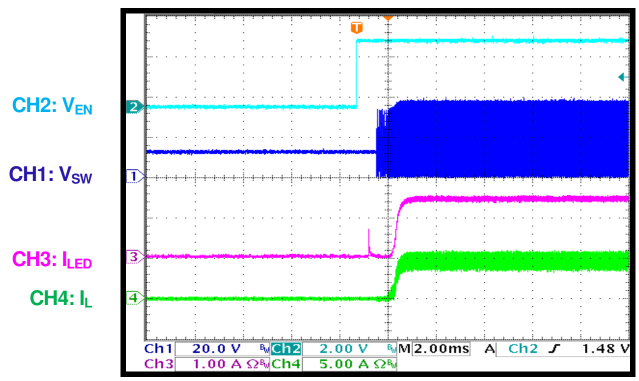
Shutdown through VIN

I_{LED} = 1.5A



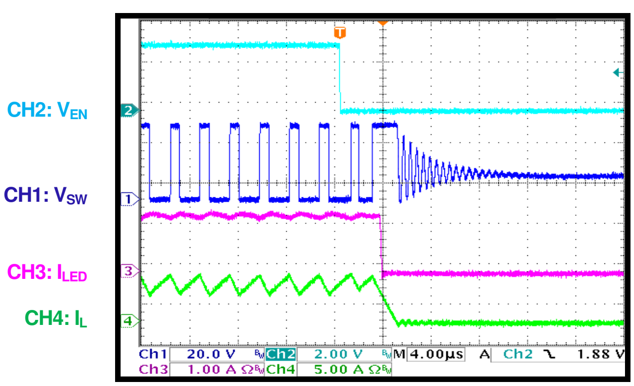
Start-Up through EN

I_{LED} = 1.5A



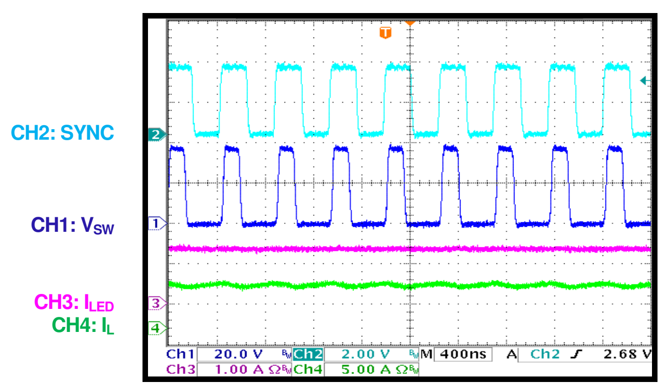
Shutdown through EN

I_{LED} = 1.5A



SYNC Function Steady State

SYNC frequency = 2.2MHz

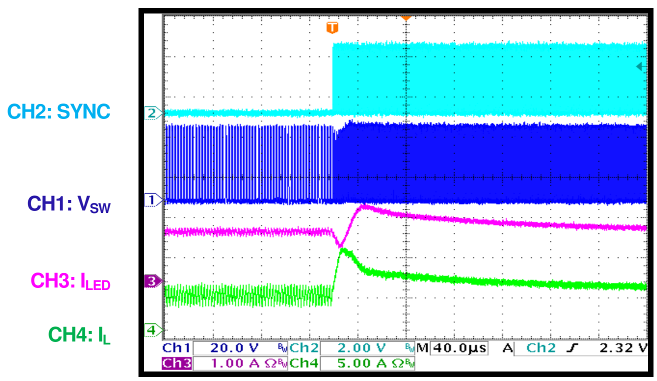


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

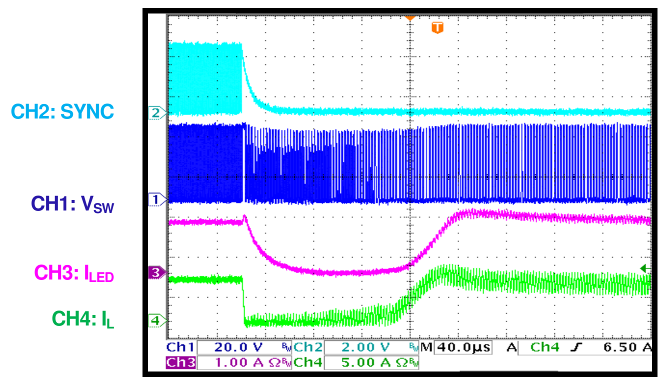
SYNC In

SYNC frequency = 2.2MHz



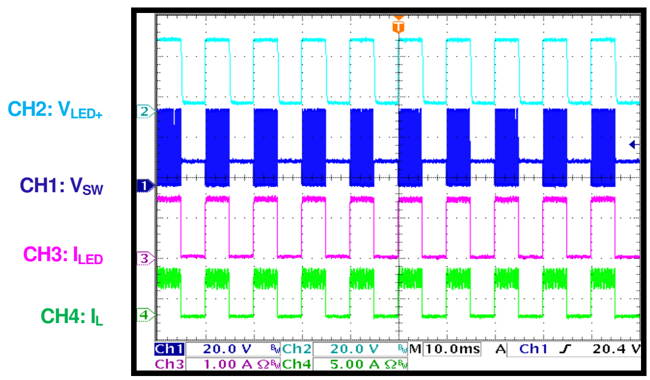
SYNC Out

SYNC frequency = 2.2MHz



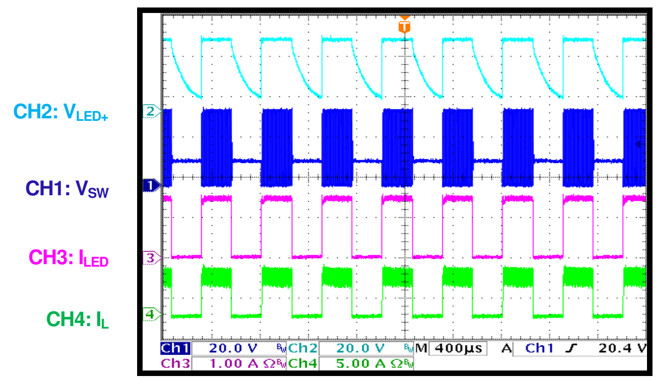
PWM Dimming Steady State

Dimming frequency = 100Hz



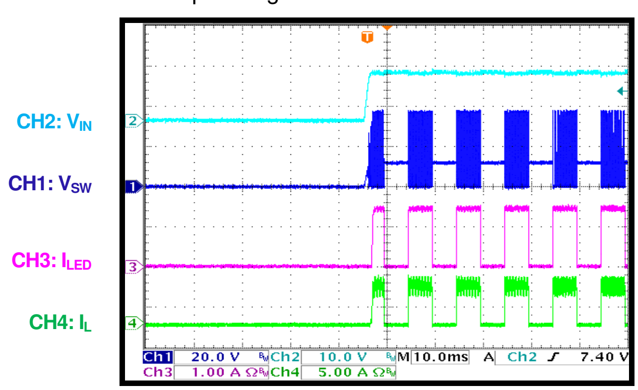
PWM Dimming Steady State

Dimming frequency = 2kHz



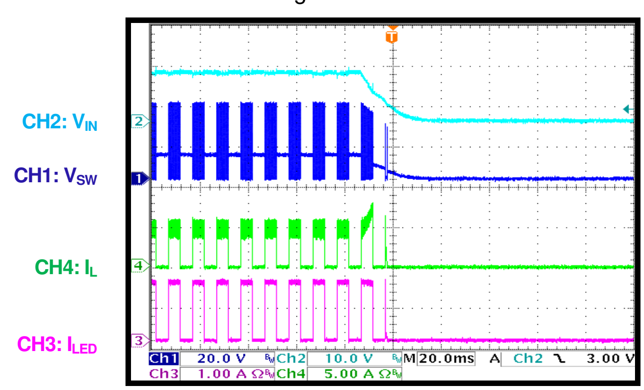
PWM Dimming

Start-up through VIN



PWM Dimming

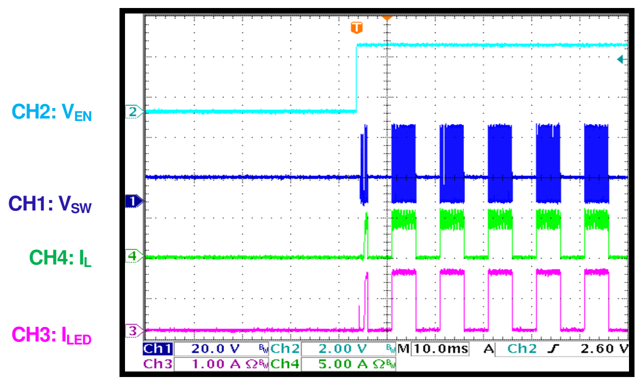
Shutdown through VIN



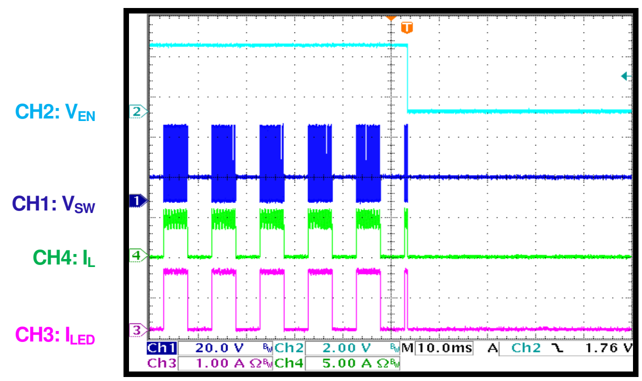
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

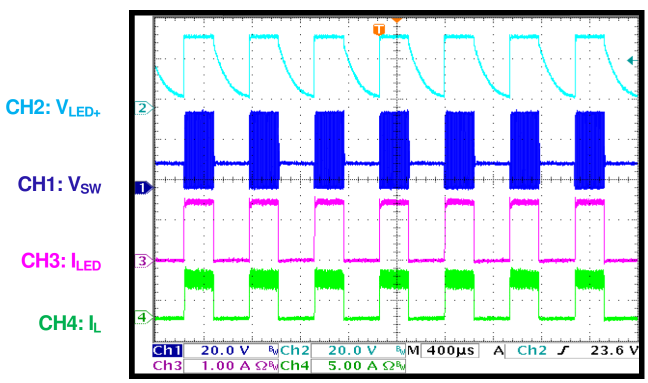
PWM Dimming
Start-up through EN



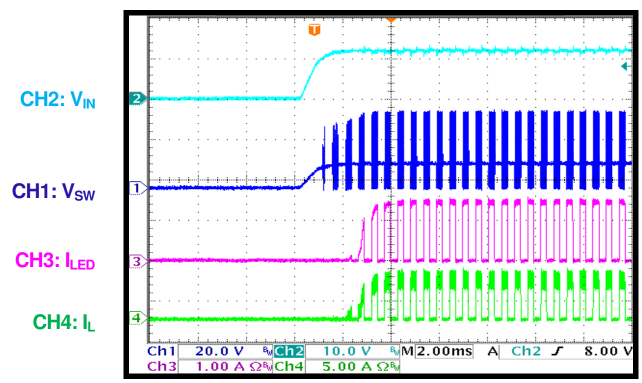
PWM Dimming
Shutdown through EN



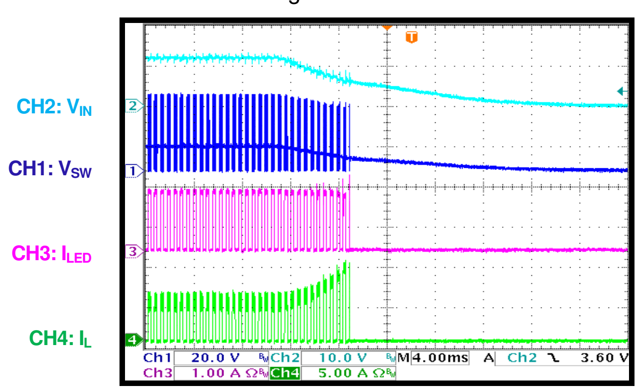
Two-Step Dimming Steady State
Dimming frequency = 1.8kHz



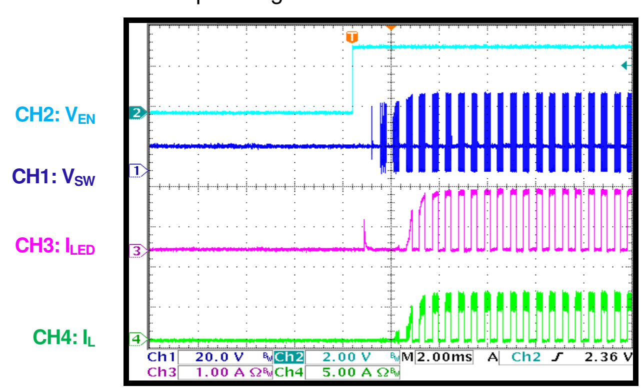
Two-Step Dimming
Start-up through VIN



Two-Step Dimming
Shutdown through VIN



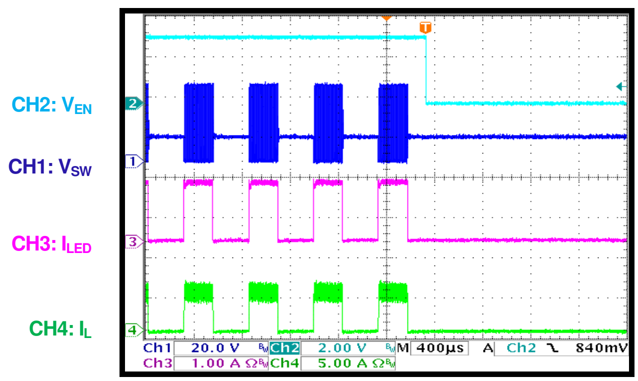
Two-Step Dimming
Start-up through EN



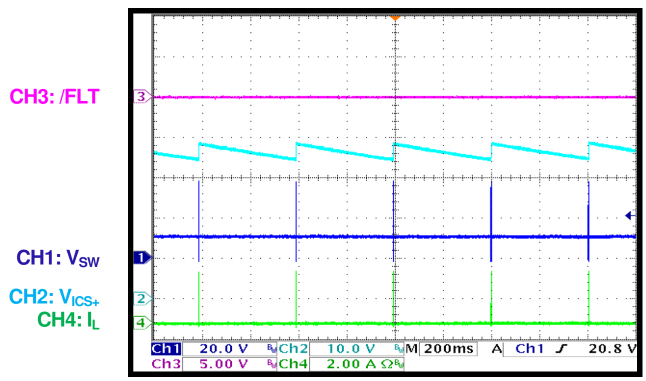
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

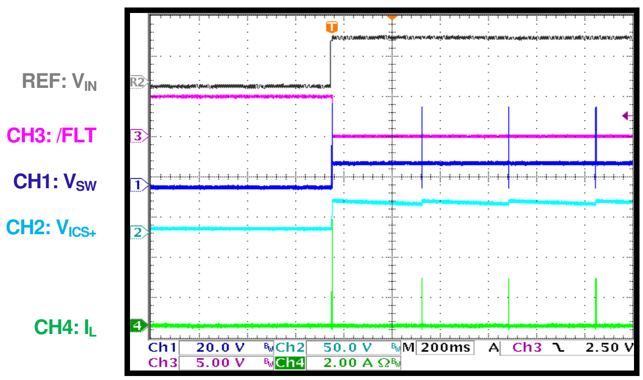
Two-Step Dimming
Shutdown through EN



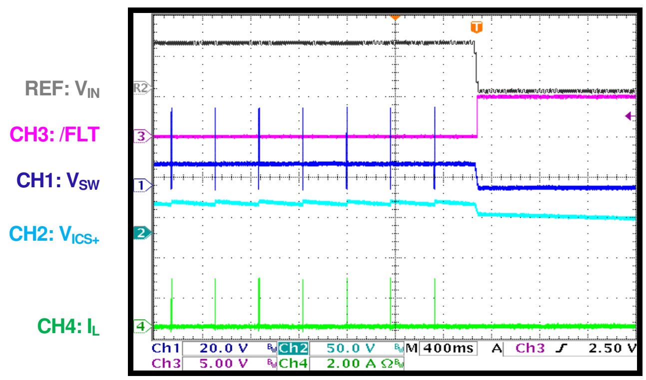
No Dimming
LED open fault, steady state



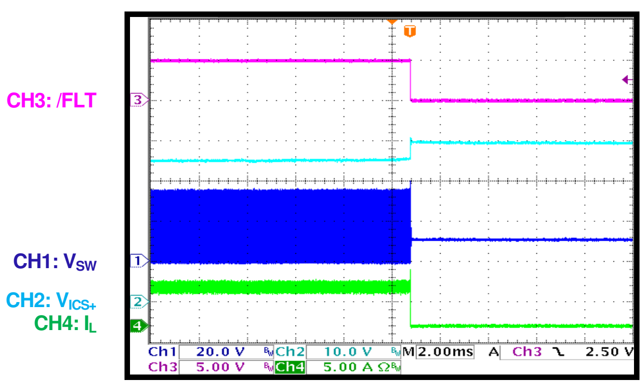
No Dimming
LED open fault, start-up



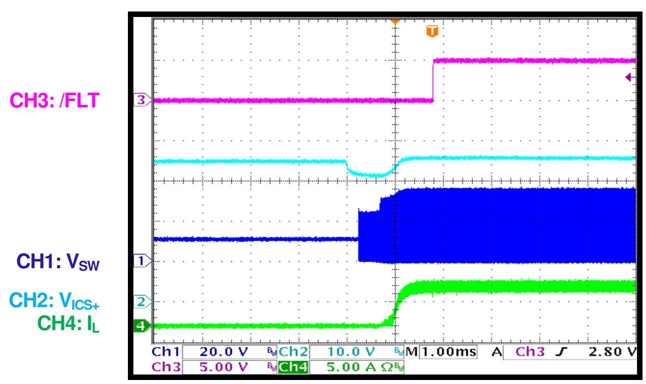
No Dimming
LED open fault, shutdown



No Dimming
LED open fault entry



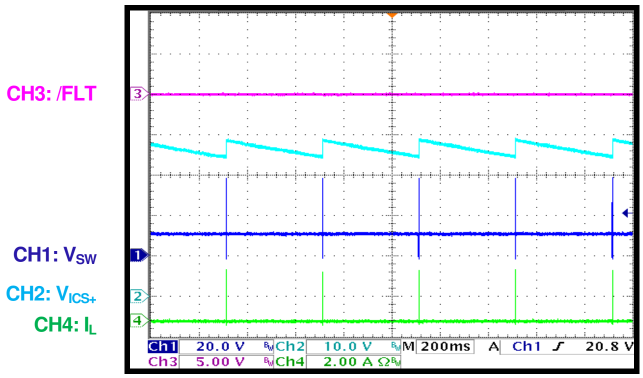
No Dimming
LED open fault recovery



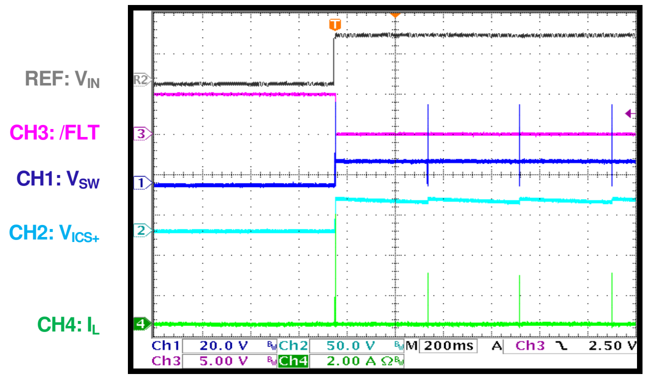
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10μH, T_A = 25°C, unless otherwise noted.

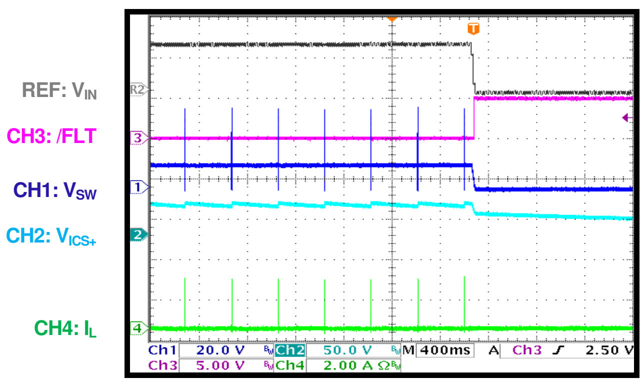
PWM Dimming
LED open fault, steady state



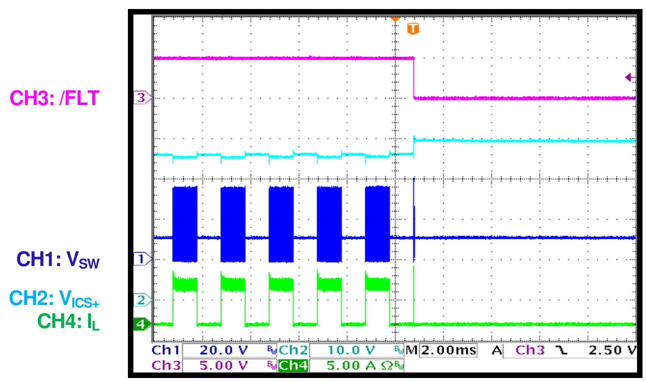
PWM Dimming
LED open fault, start-up



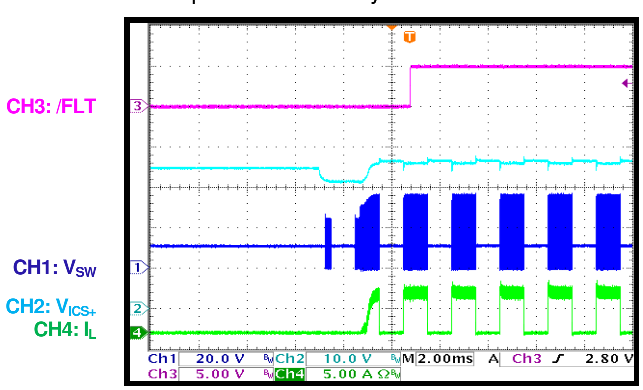
PWM Dimming
LED open fault, shutdown



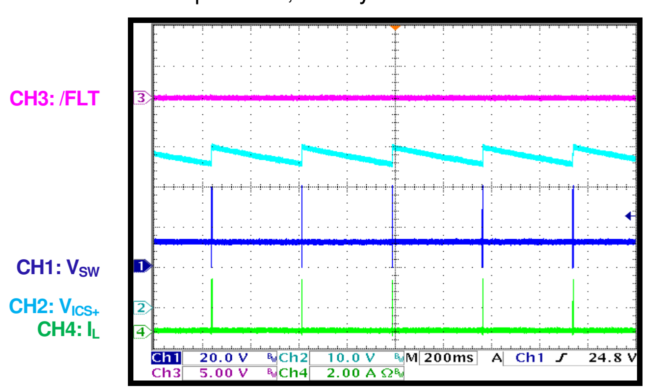
PWM Dimming
LED open fault entry



PWM Dimming
LED open fault recovery



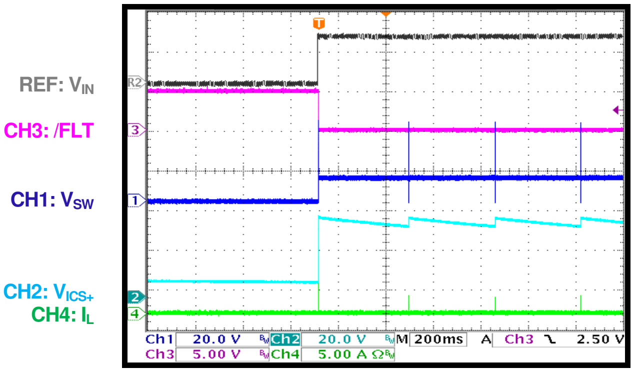
Two-Step Dimming
LED open fault, steady state



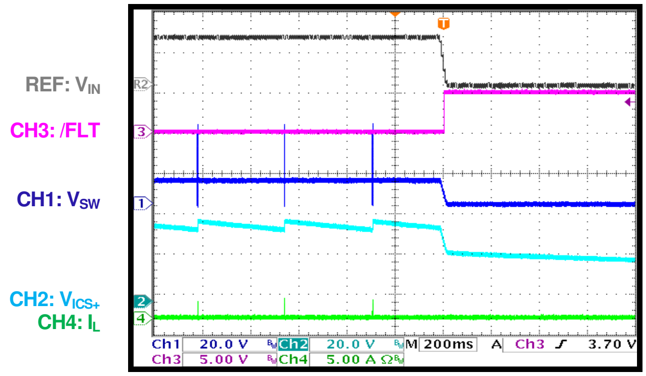
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs (V_{LED} = 24V), V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

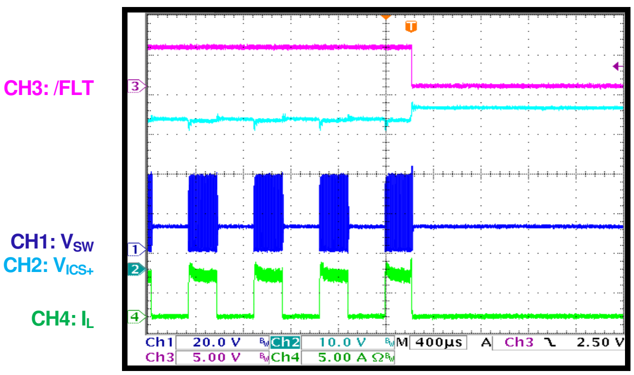
Two-Step Dimming
LED open fault, start-up



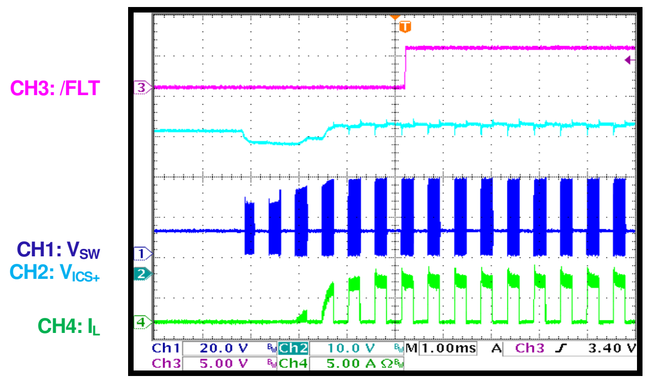
Two-Step Dimming
LED open fault, shutdown



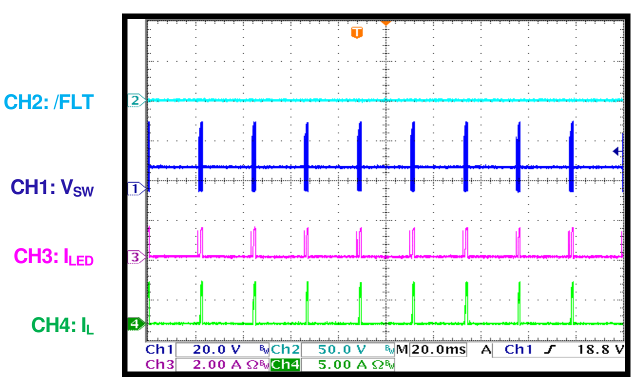
Two-Step Dimming
LED open fault entry



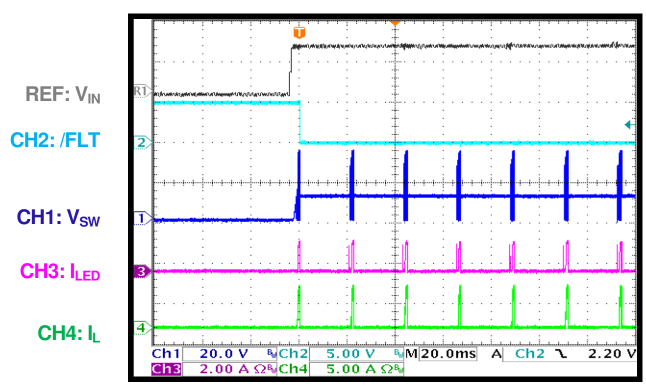
Two-Step Dimming
LED open fault recovery



No Dimming
One or more LED short faults, steady state



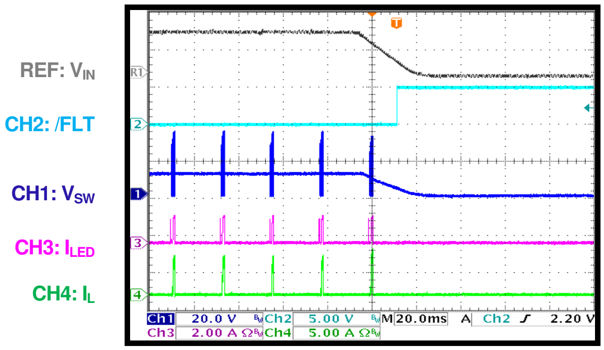
No Dimming
One or more LED short faults, start-up



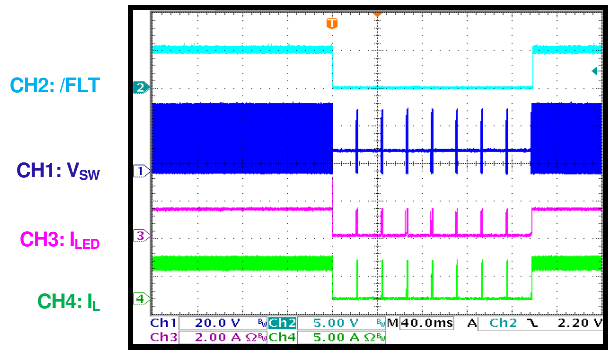
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

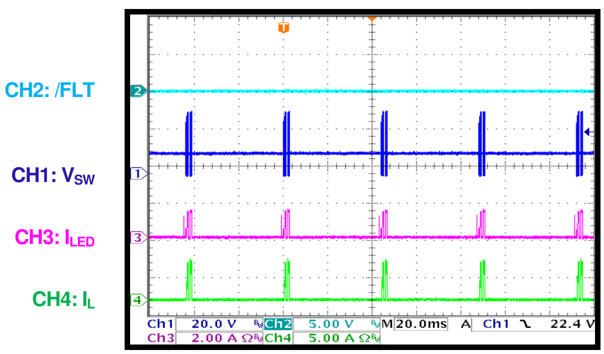
No Dimming
One or more LED short faults, shutdown



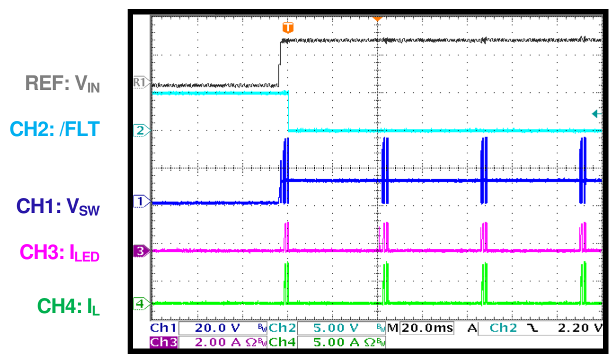
No Dimming
One or more LED short faults entry and recovery



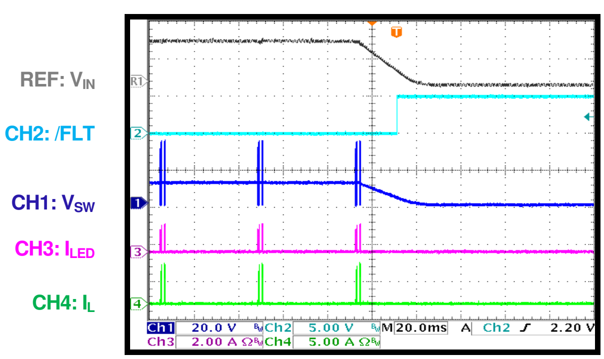
PWM Dimming
One or more LED short faults, steady state



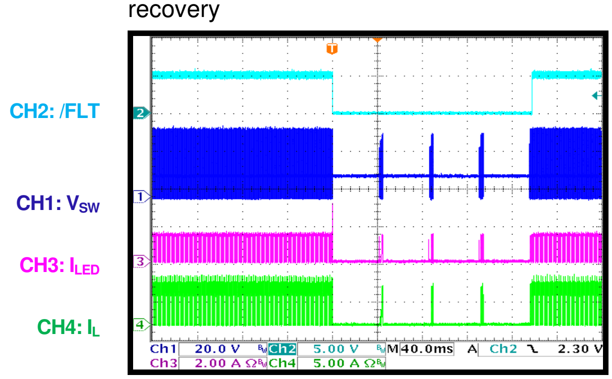
PWM Dimming
One or more LED short faults, start-up



PWM Dimming
One or more LED short faults, shutdown



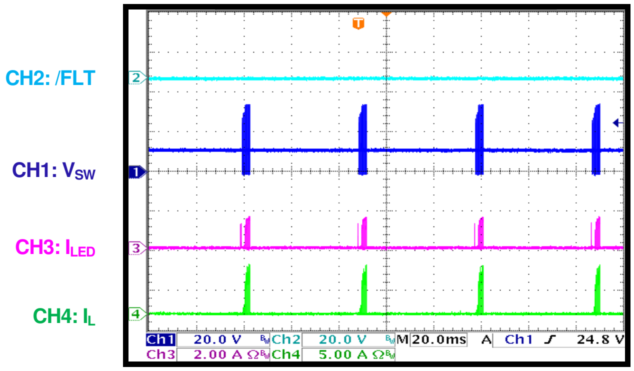
PWM Dimming
One or more LED short faults entry and recovery



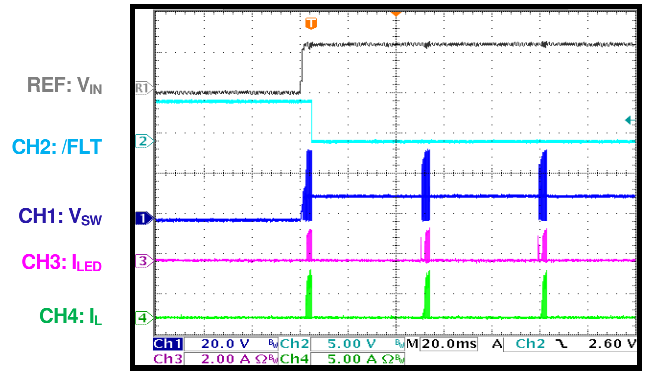
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

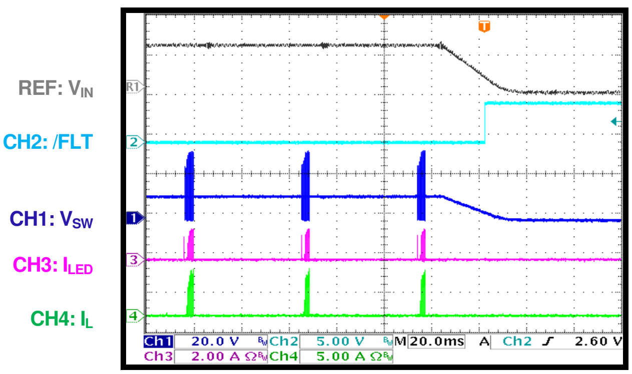
Two-Step Dimming
One or more LED short faults, steady state



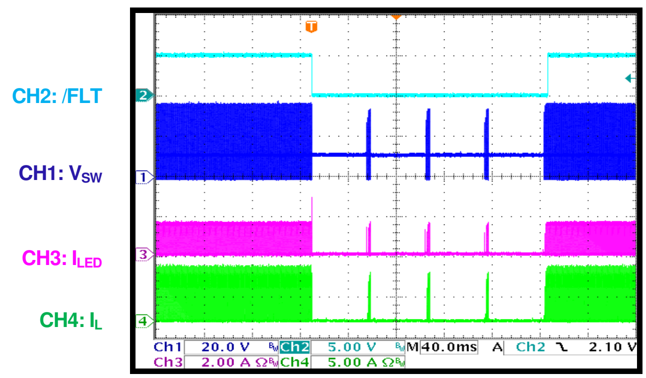
Two-Step Dimming
One or more LED short faults, start-up



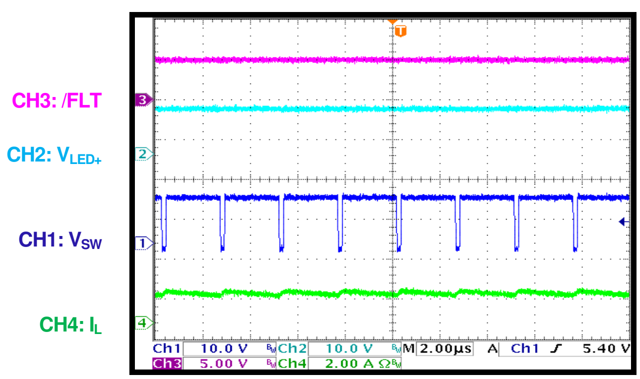
Two-Step Dimming
One or more LED short faults, shutdown



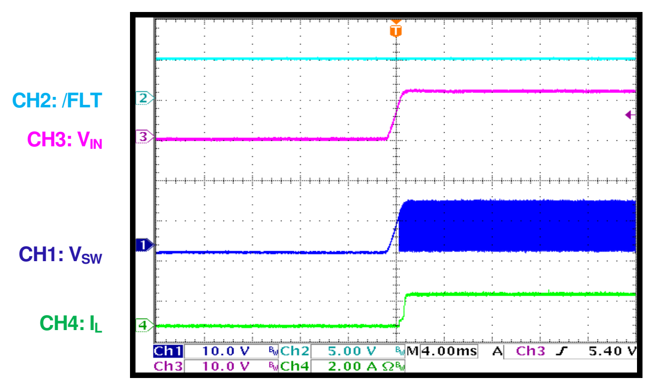
Two-Step Dimming
One or more LED short faults entry and recovery



No Dimming
LED+ to LED- short, steady state



No Dimming
LED+ to LED- short, start-up

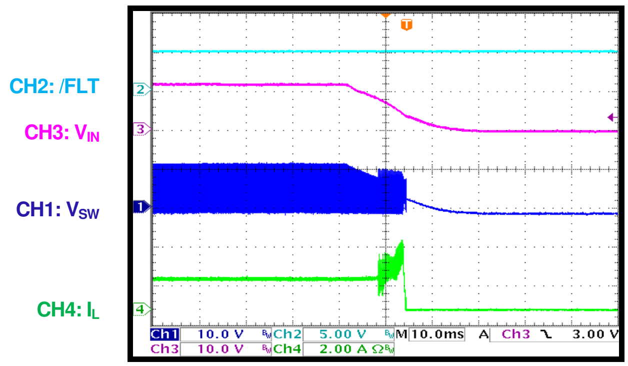


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

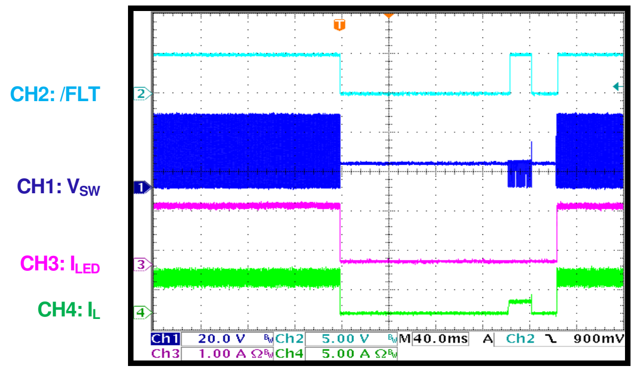
No Dimming

LED+ to LED- short, shutdown



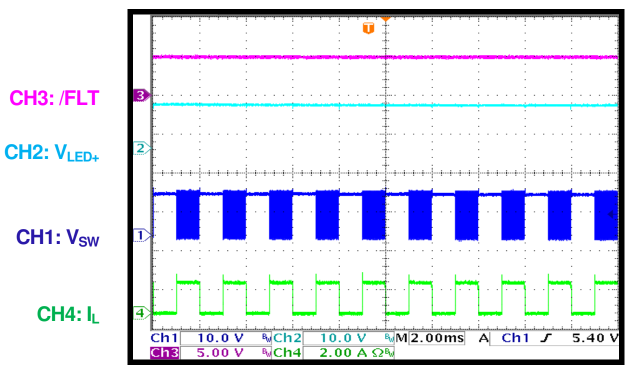
No Dimming

LED+ to LED- short entry and recovery



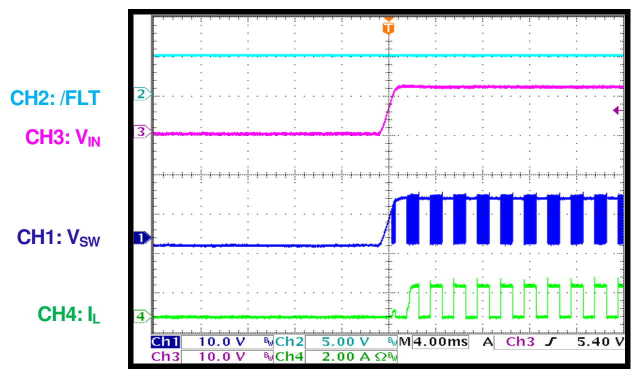
PWM Dimming

LED+ to LED- short, steady state



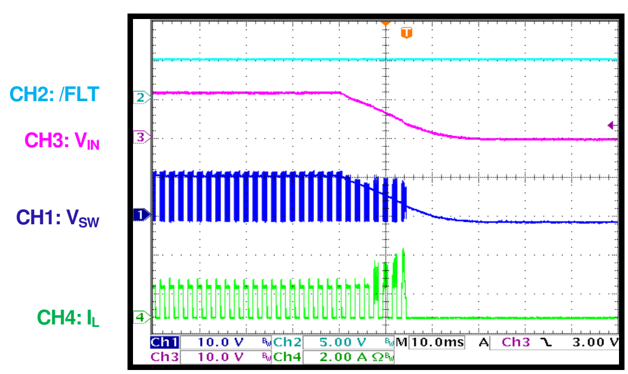
PWM Dimming

LED+ to LED- short, start-up



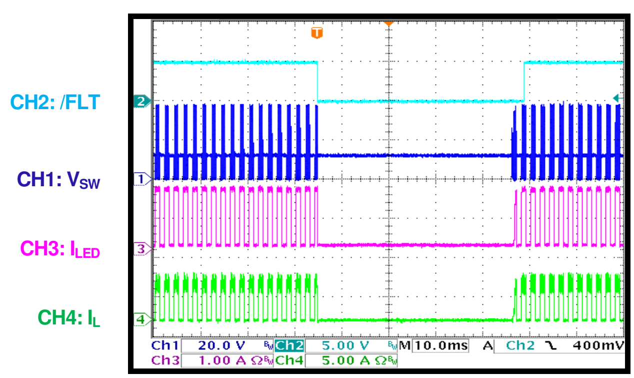
PWM Dimming

LED+ to LED- short, shutdown



PWM Dimming

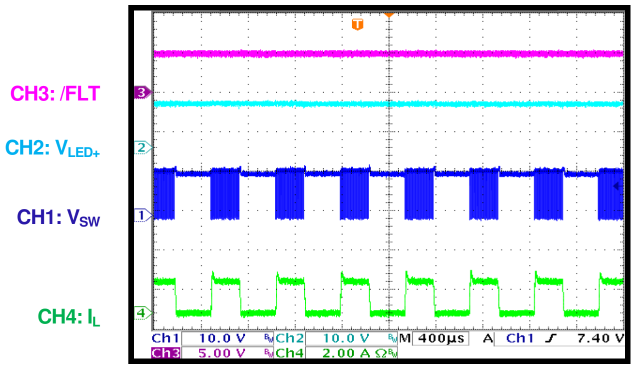
LED+ to LED- short entry and recovery



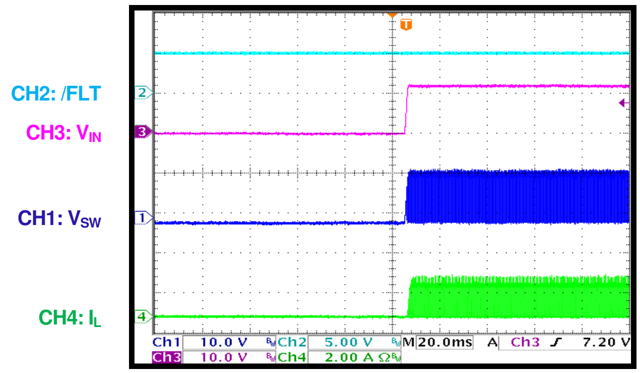
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

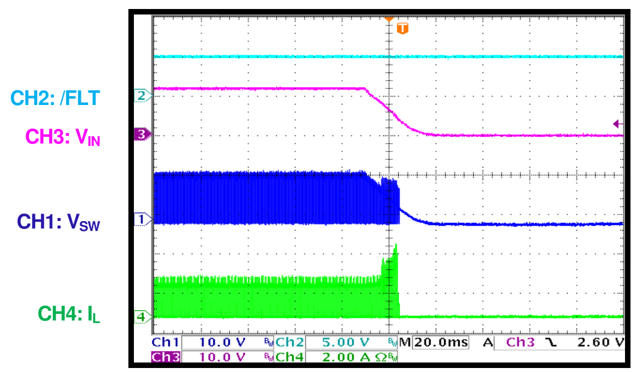
Two-Step Dimming
LED+ to LED- short, steady state



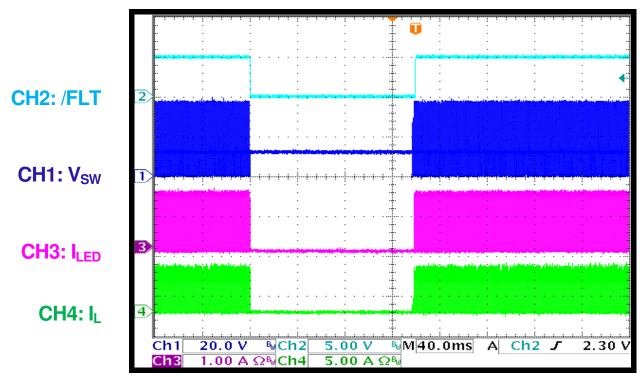
Two-Step Dimming
LED+ to LED- short, start-up



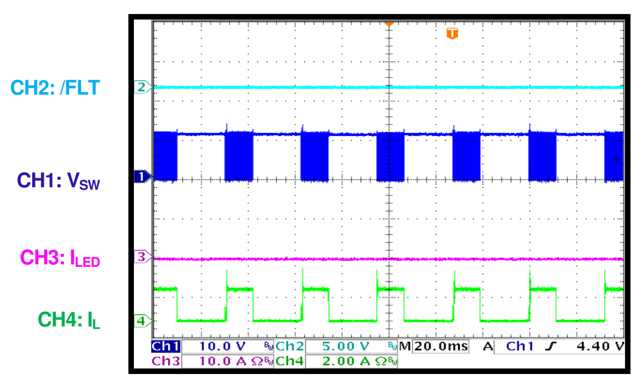
Two-Step Dimming
LED+ to LED- short, shutdown



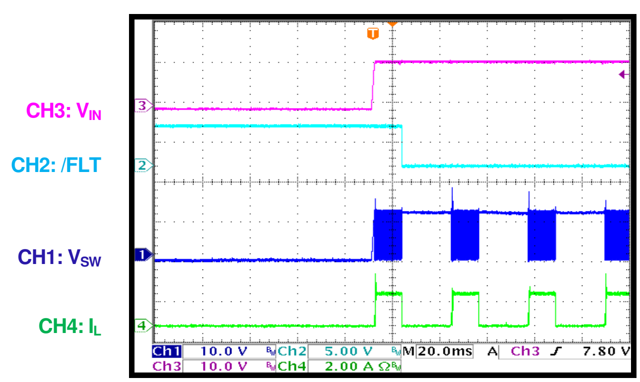
Two-Step Dimming
LED+ to LED- short entry and recovery



No Dimming
LED+ to PGND short, steady state



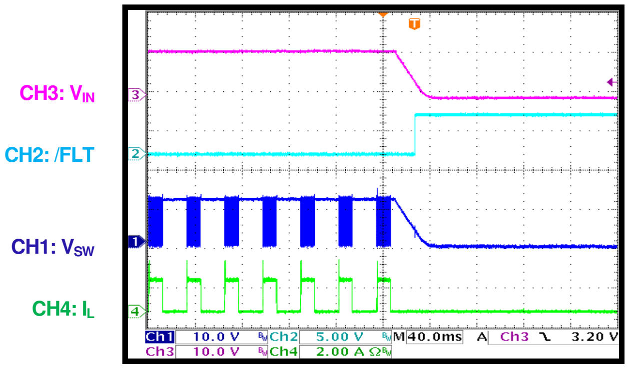
No Dimming
LED+ to PGND short, start-up



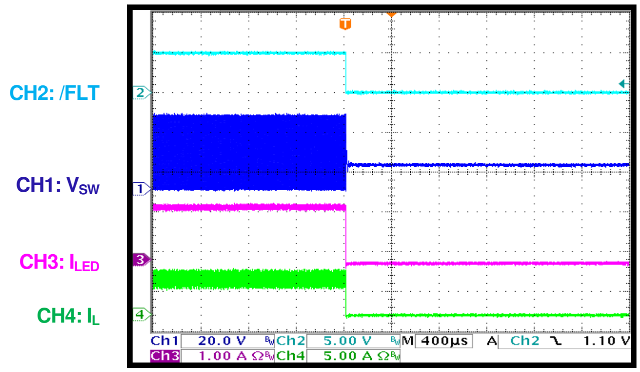
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

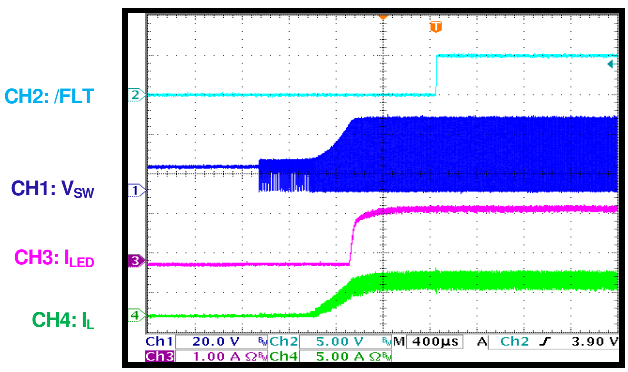
No Dimming
LED+ to PGND short, shutdown



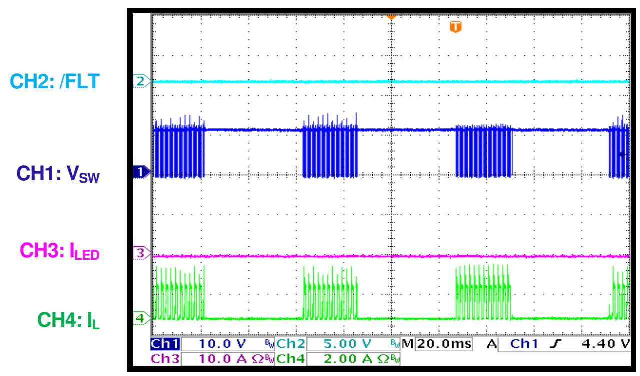
No Dimming
LED+ to PGND short entry



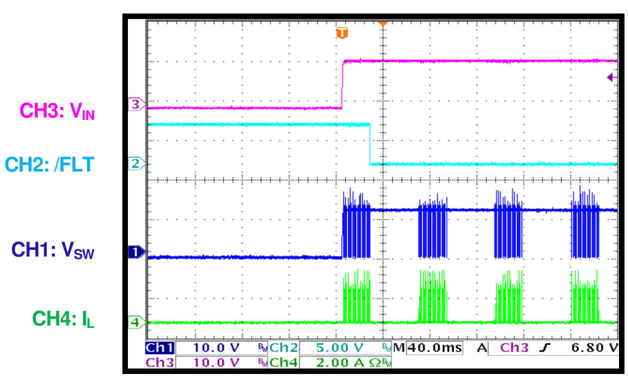
No Dimming
LED+ to PGND short recovery



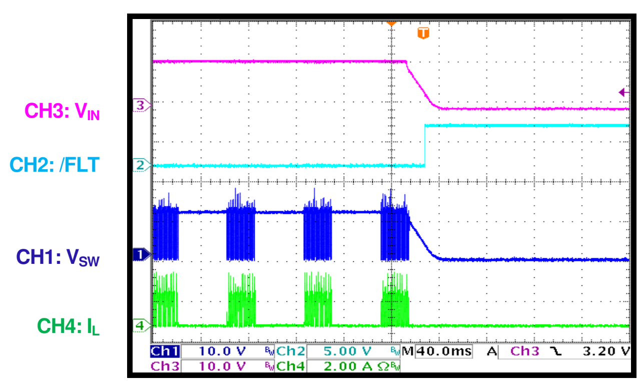
PWM Dimming
LED+ to PGND short, steady state



PWM Dimming
LED+ to PGND short, start-up



PWM Dimming
LED+ to PGND short, shutdown

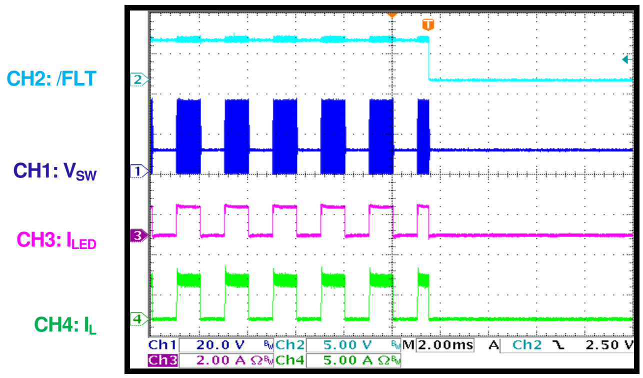


TYPICAL PERFORMANCE CHARACTERISTICS

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

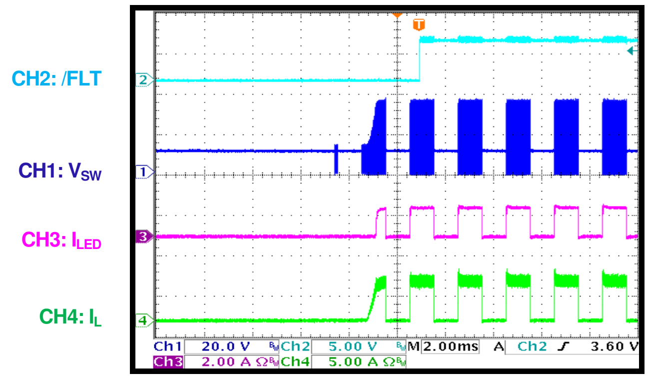
PWM Dimming

LED+ to PGND short entry



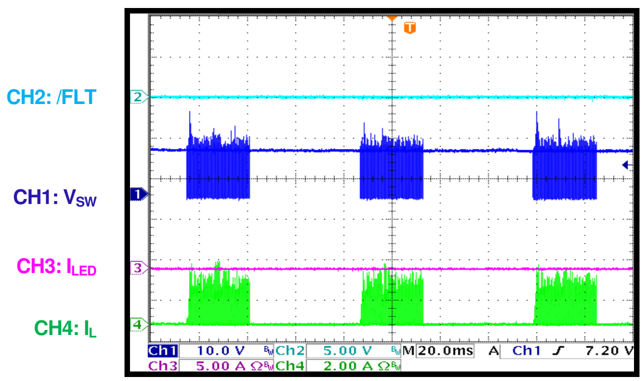
PWM Dimming

LED+ to PGND short recovery



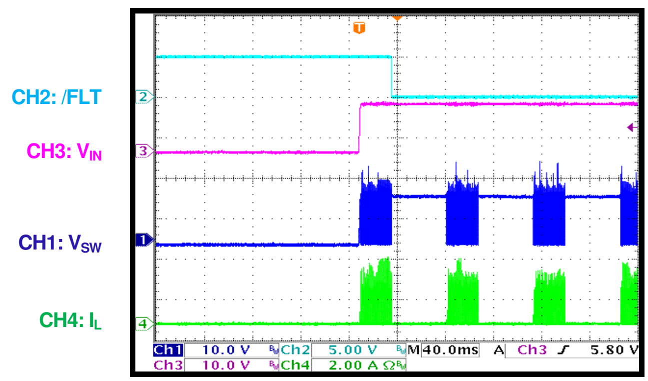
Two-Step Dimming

LED+ to PGND short, steady state



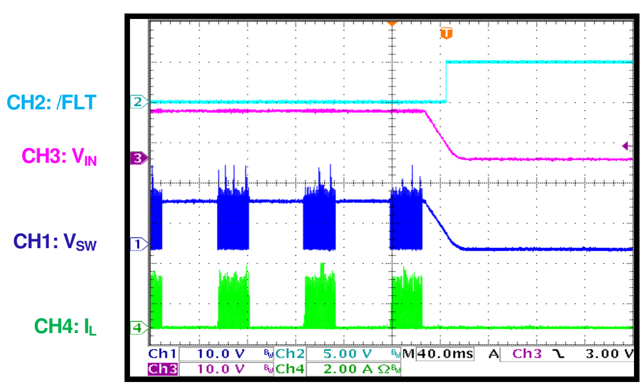
Two-Step Dimming

LED+ to PGND short, start-up



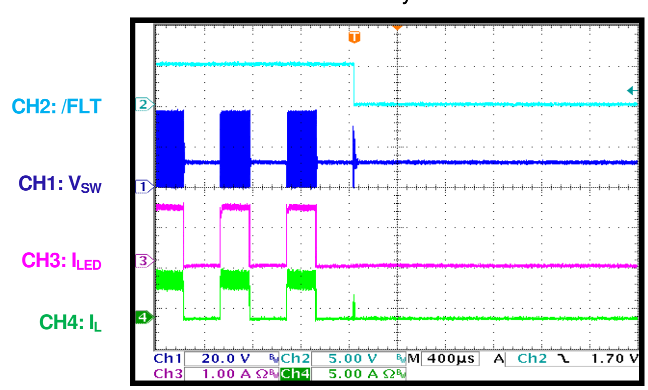
Two-Step Dimming

LED+ to PGND short, shutdown



Two-Step Dimming

LED+ to PGND short entry

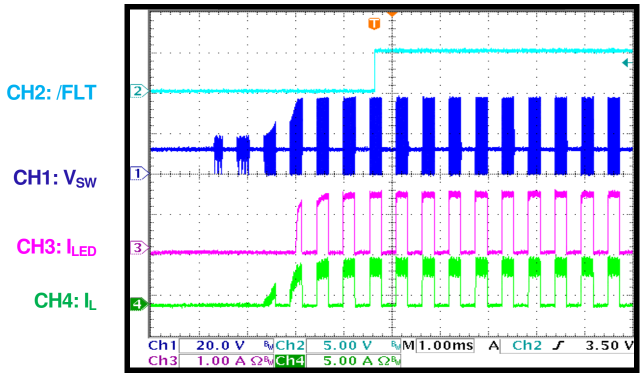


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Buck-boost mode, 8 LEDs, V_{LED} = 24V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

Two-Step Dimming

LED+ to PGND short recovery

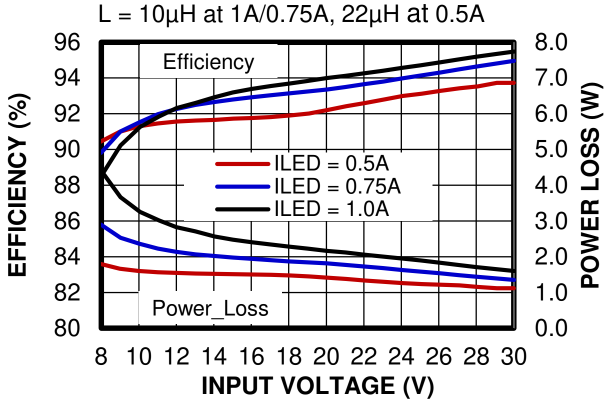


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Input Voltage

12 LEDs, V_{LED} = 36V,
L = 10µH at 1A/0.75A, 22µH at 0.5A

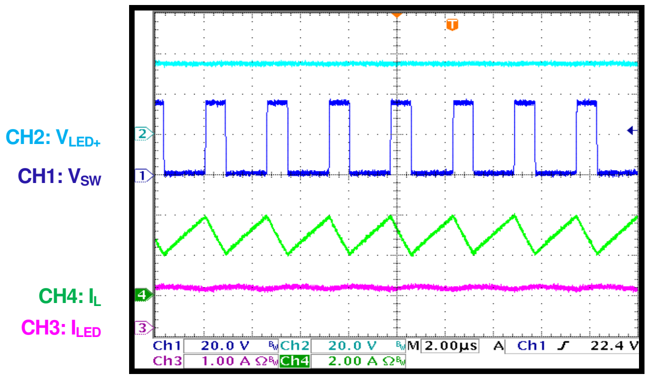


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

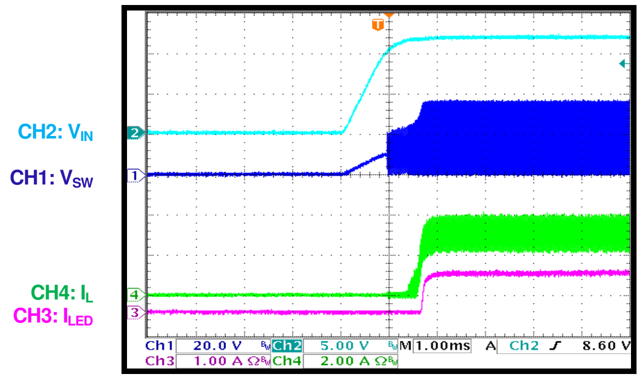
Steady State

I_{LED} = 1A



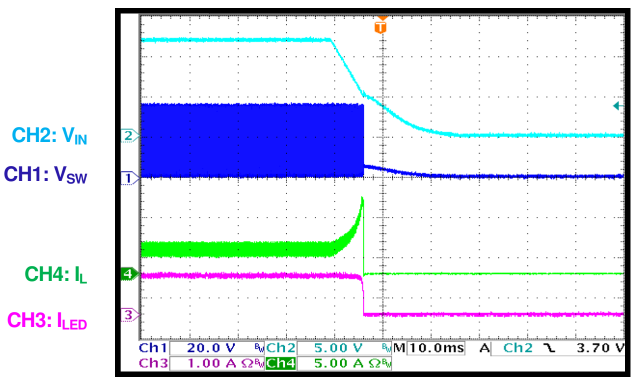
Start-Up through VIN

I_{LED} = 1A



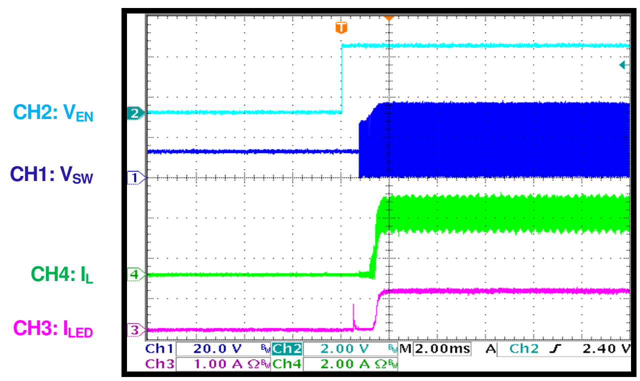
Shutdown through VIN

I_{LED} = 1A



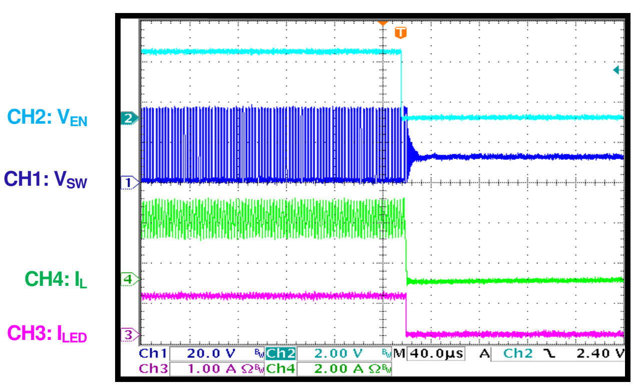
Start-Up through EN

I_{LED} = 1A



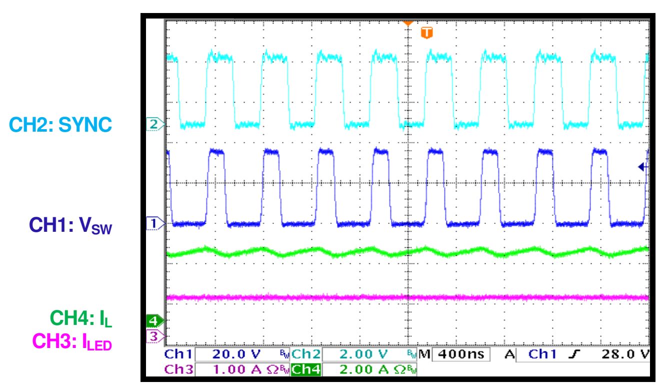
Shutdown through EN

I_{LED} = 1A



SYNC Function Steady State

SYNC frequency = 2.2MHz

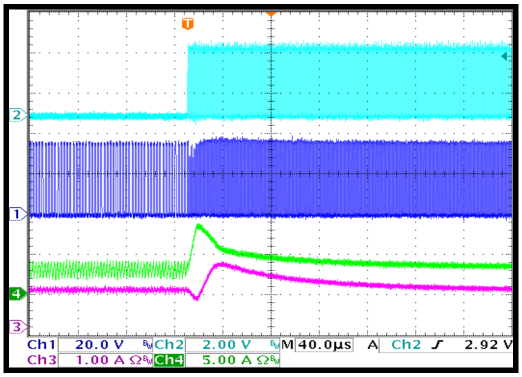


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

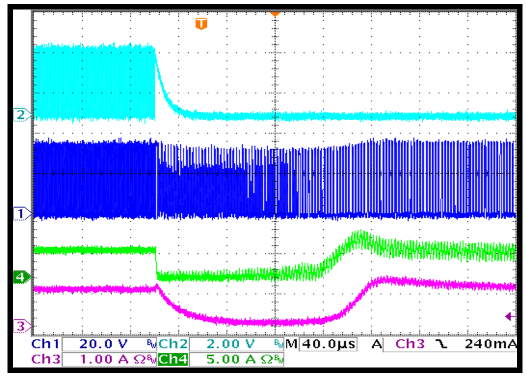
SYNC IN

SYNC frequency = 2.2MHz



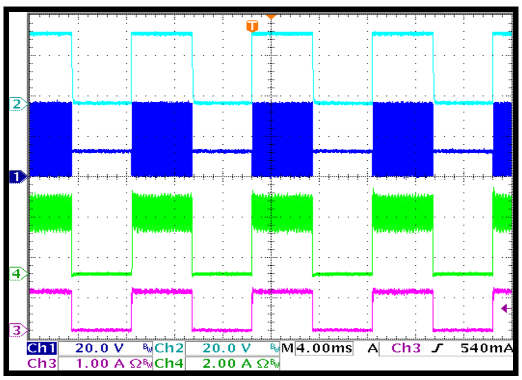
SYNC OUT

SYNC frequency = 2.2MHz



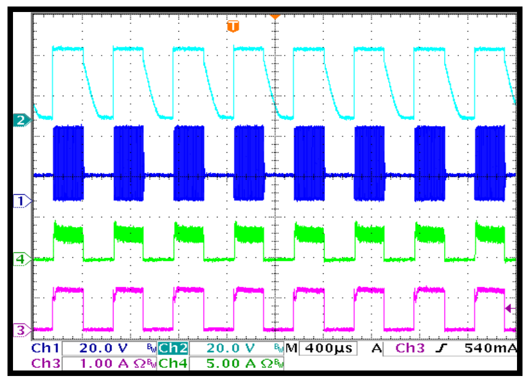
PWM Dimming Steady State

Dimming frequency = 100Hz



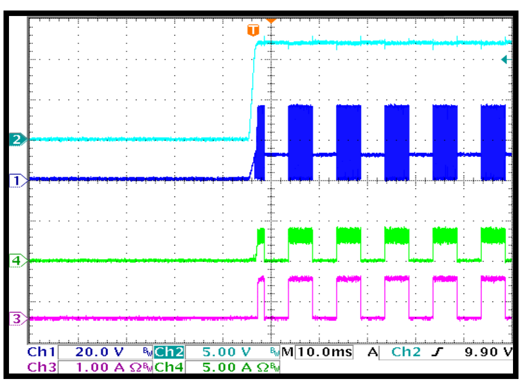
PWM Dimming Steady State

Dimming frequency = 2kHz



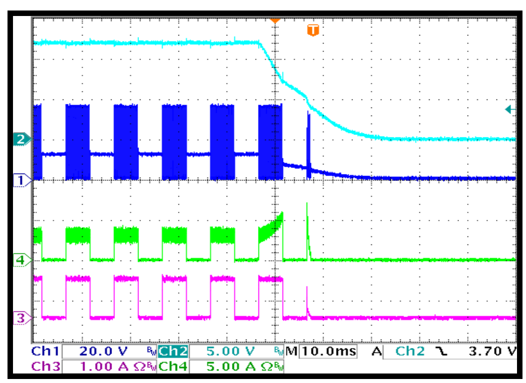
PWM Dimming

Start-up through VIN



PWM Dimming

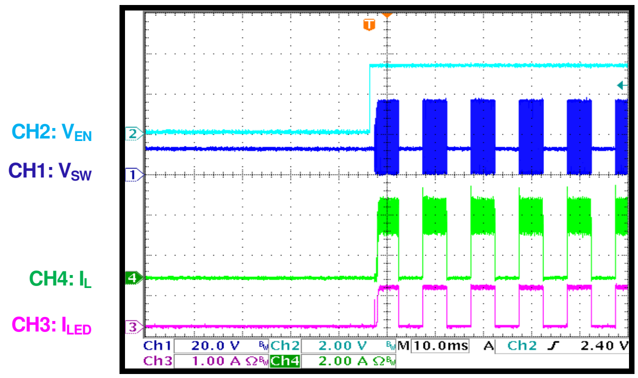
Shutdown through VIN



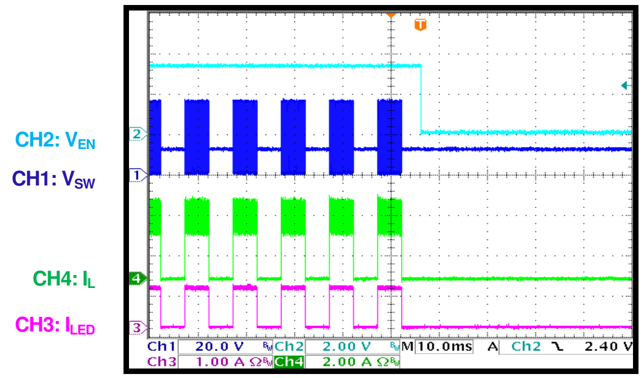
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

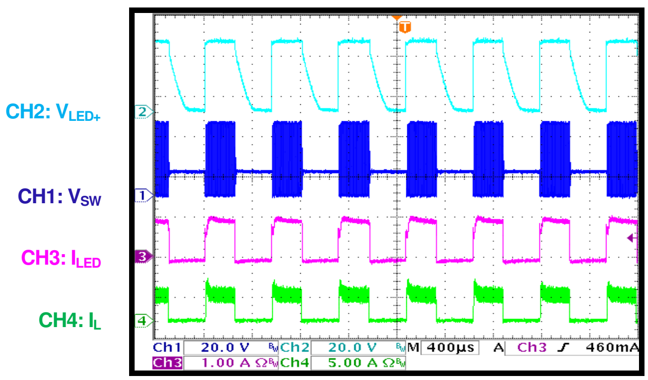
PWM Dimming
Start-up through EN



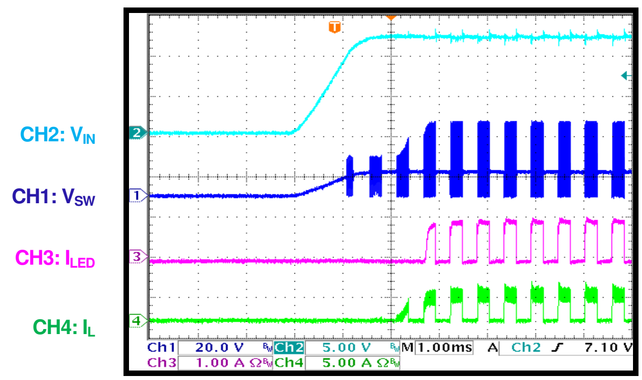
PWM Dimming
Shutdown through EN



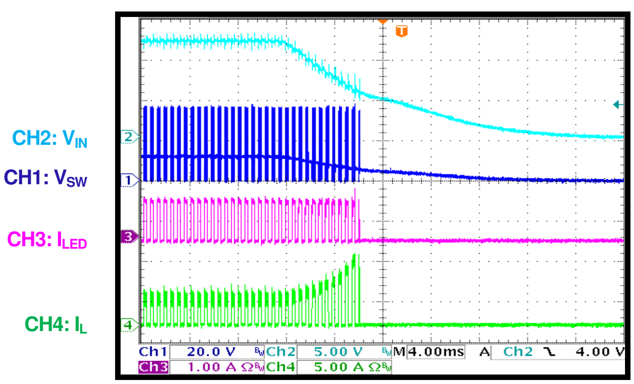
Two-Step Dimming Steady State
Dimming frequency = 1.8kHz



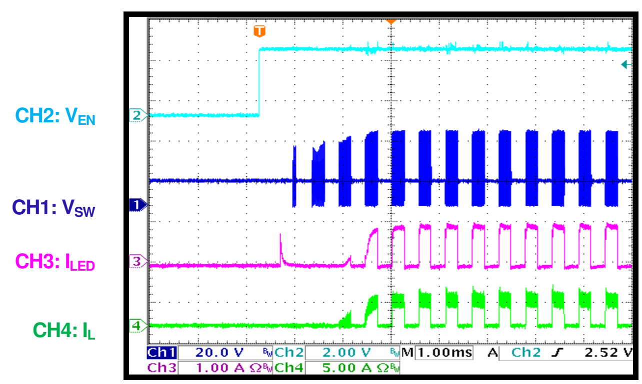
Two-Step Dimming
Start-up through VIN



Two-Step Dimming
Shutdown through VIN



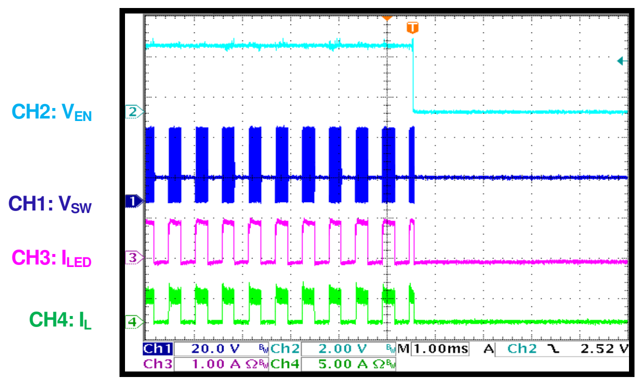
Two-Step Dimming
Start-up through EN



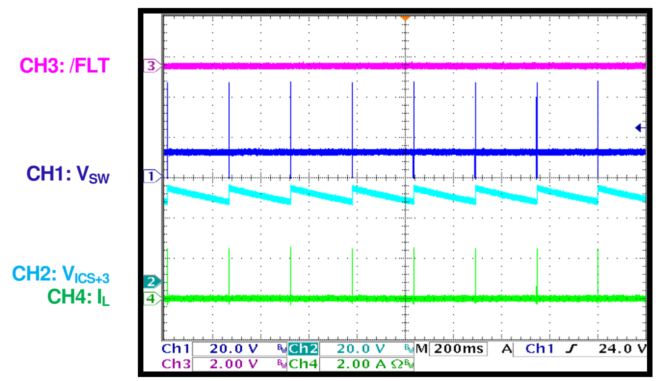
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

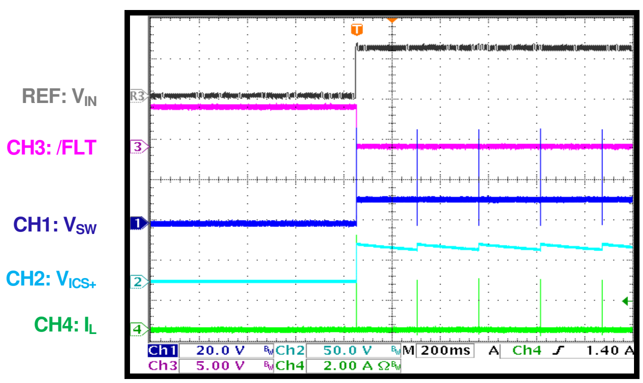
Two-Step Dimming
Shutdown through EN



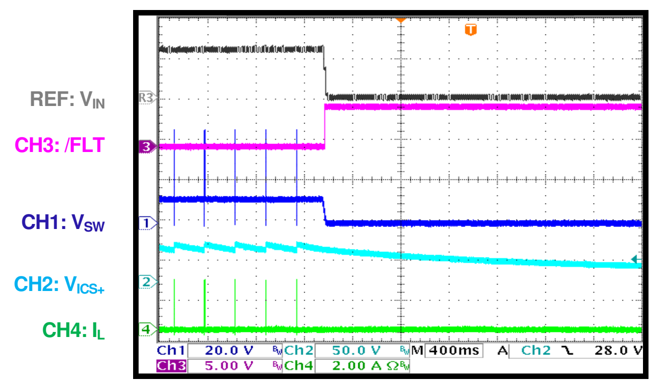
No Dimming
LED open, steady state



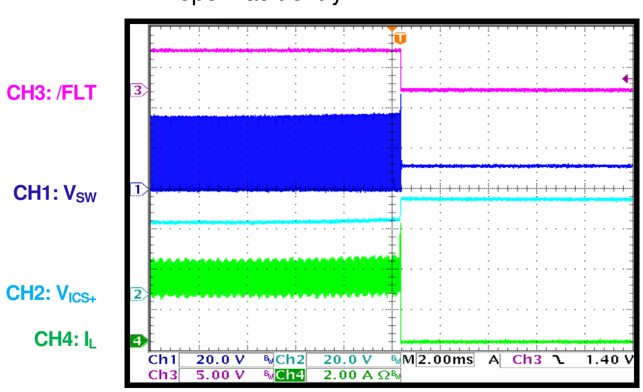
No Dimming
LED open fault, start-up



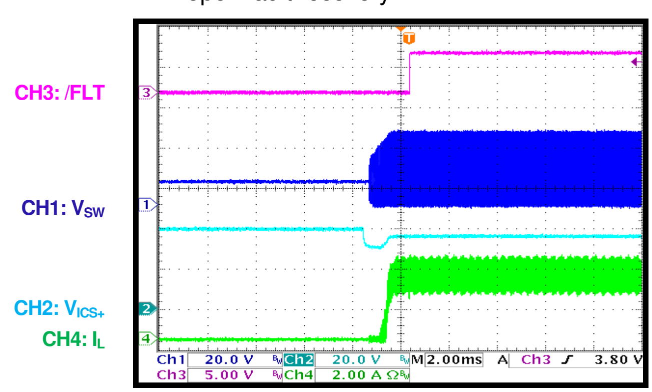
No Dimming
LED open fault, shutdown



No Dimming
LED open fault entry



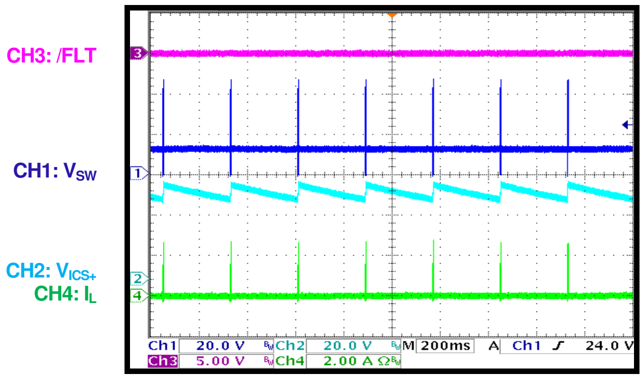
No Dimming
LED open fault recovery



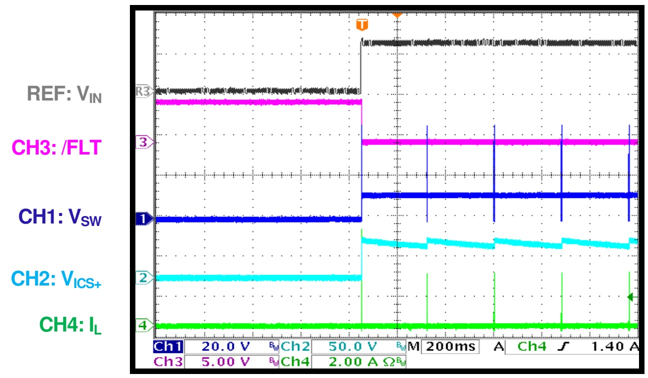
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

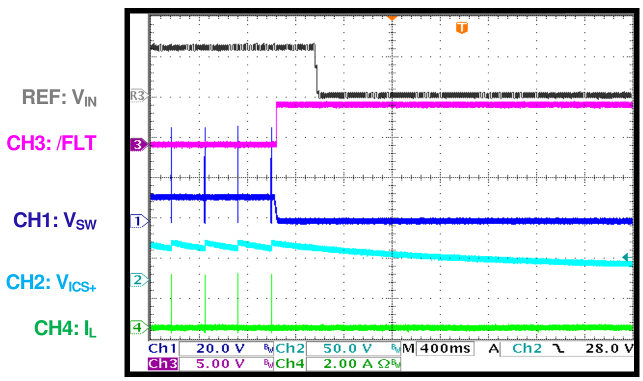
PWM Dimming
LED open fault, steady state



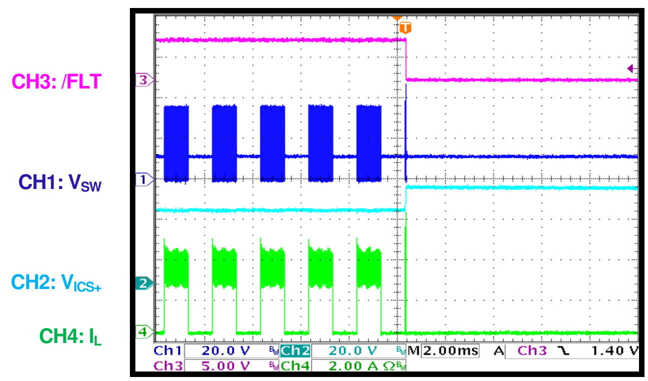
PWM Dimming
LED open fault, start-up



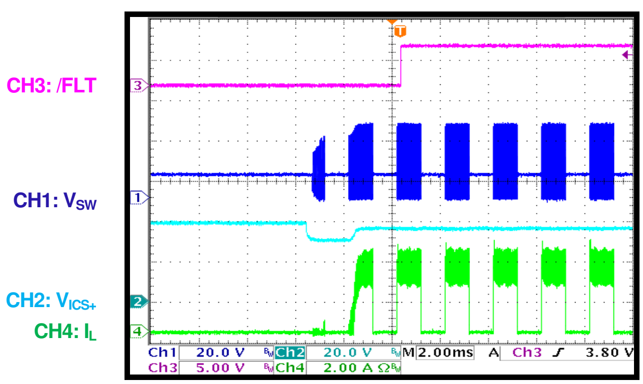
PWM Dimming
LED open fault, shutdown



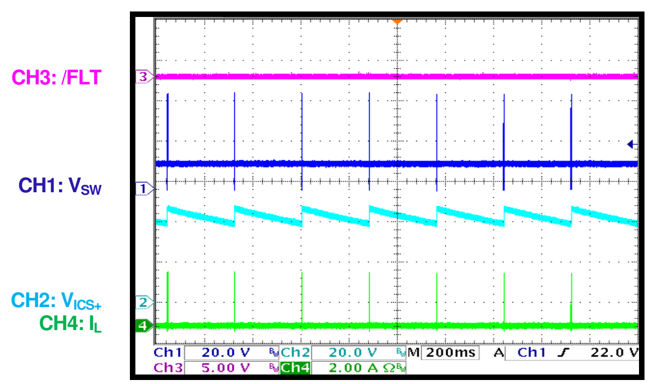
PWM Dimming
LED open fault entry



PWM Dimming
LED open fault recovery



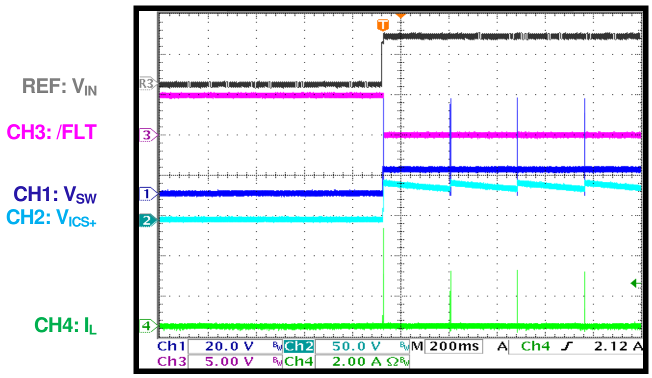
Two-Step Dimming
LED open fault, steady state



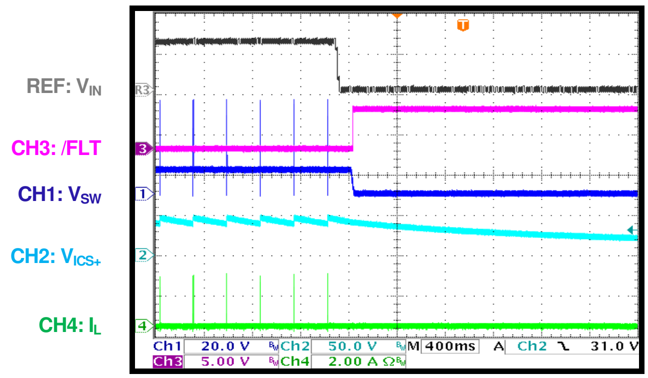
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10μH, T_A = 25°C, unless otherwise noted.

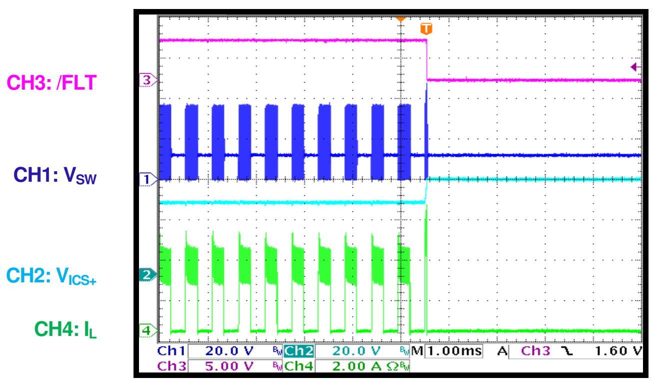
Two-Step Dimming
LED open fault, start-up



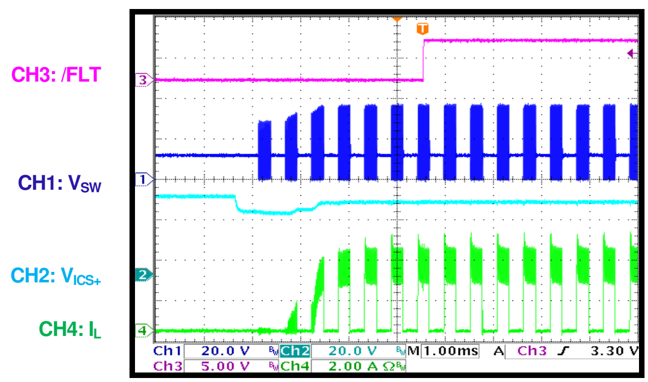
Two-Step Dimming
LED open fault, shutdown



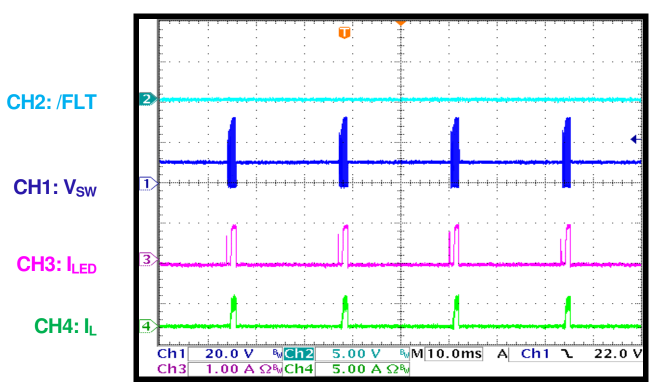
Two-Step Dimming
LED open fault entry



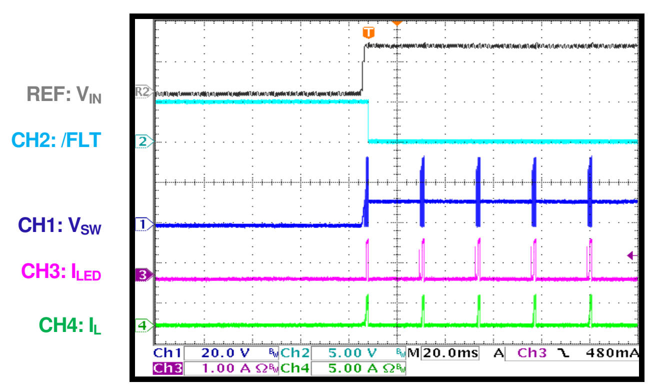
Two-Step Dimming
LED open fault recovery



No Dimming
One or more LED short fault, steady state



No Dimming
One or more LED short fault, start-up

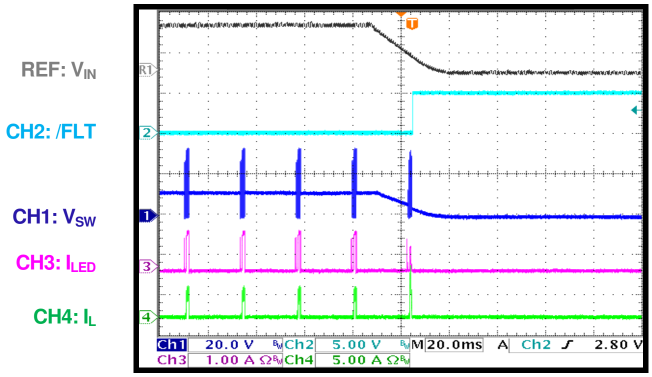


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

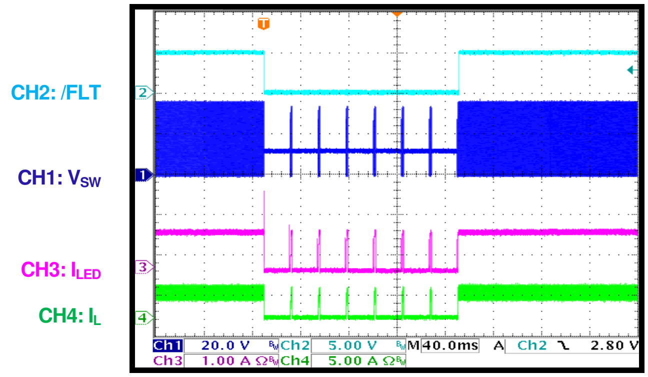
No Dimming

One or more LED short faults, shutdown



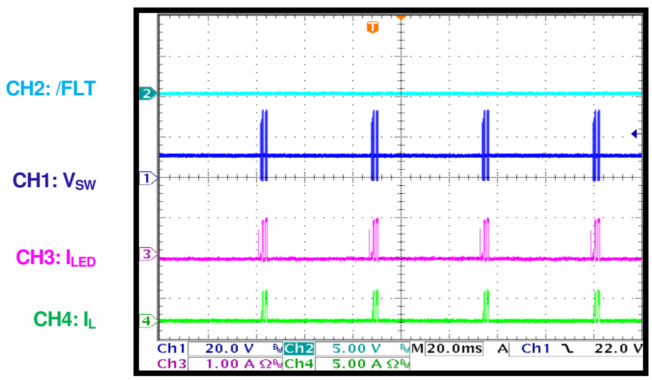
No Dimming

One or more LED short faults entry and recovery



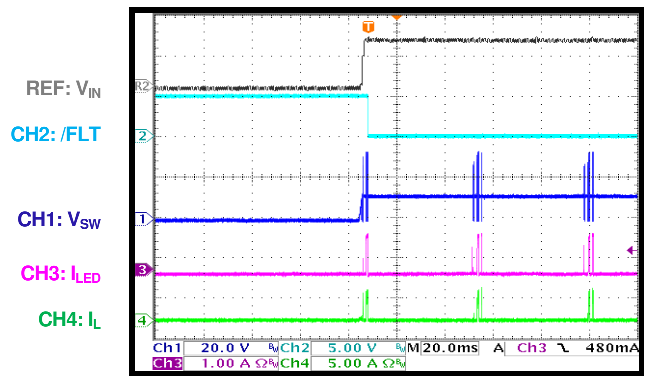
PWM Dimming

One or more LED short faults, steady state



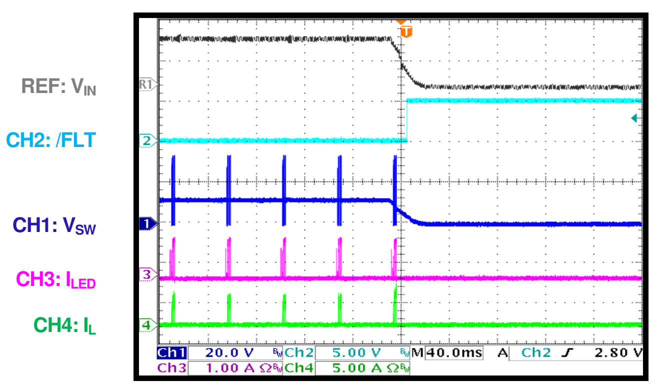
PWM Dimming

One or more LED short faults, start-up



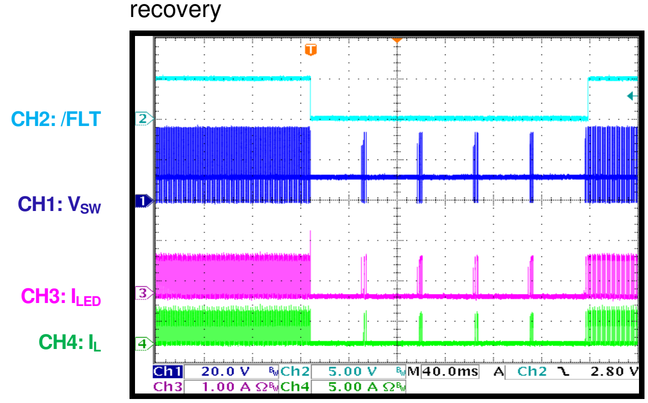
PWM Dimming

One or more LED short faults, shutdown



PWM Dimming

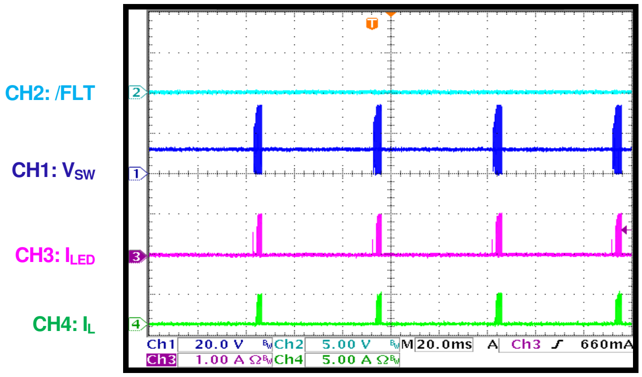
One or more LED short faults entry and recovery



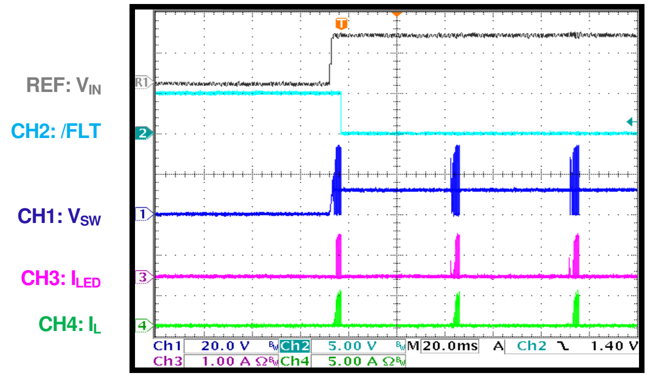
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

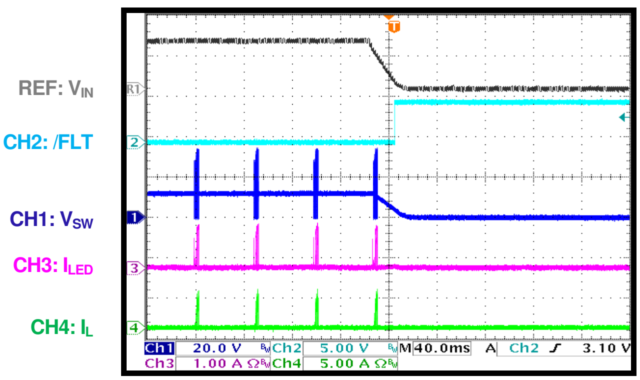
Two-Step Dimming
One or more LED short faults, steady state



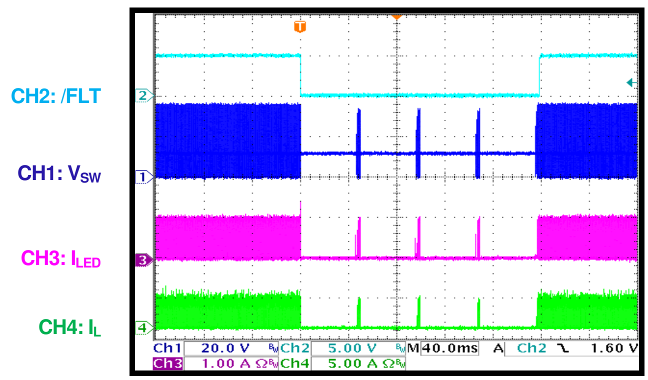
Two-Step Dimming
One or more LED short faults, start-up



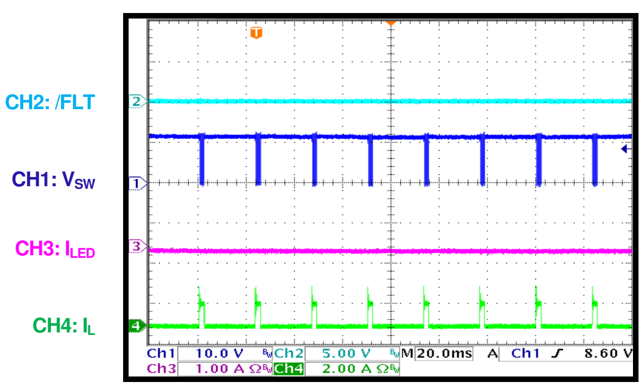
Two-Step Dimming
One or more LED short faults, shutdown



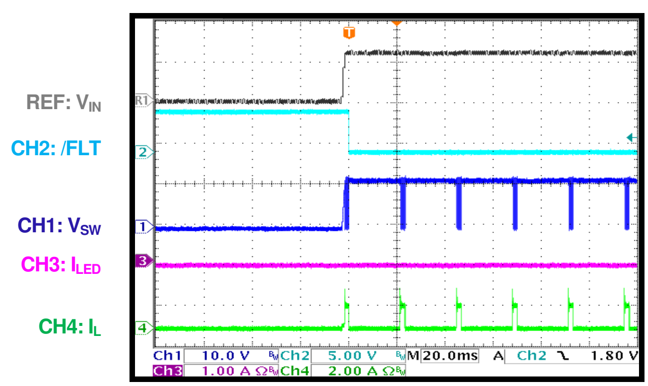
Two-Step Dimming
One or more LED short faults entry and recovery



No Dimming
LED+ short to LED-, steady state



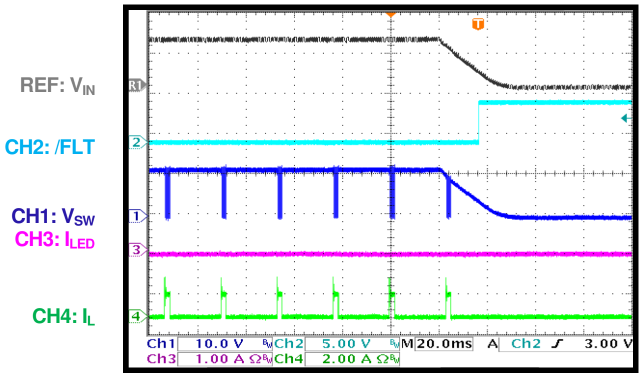
No Dimming
LED+ short to LED-, start-up



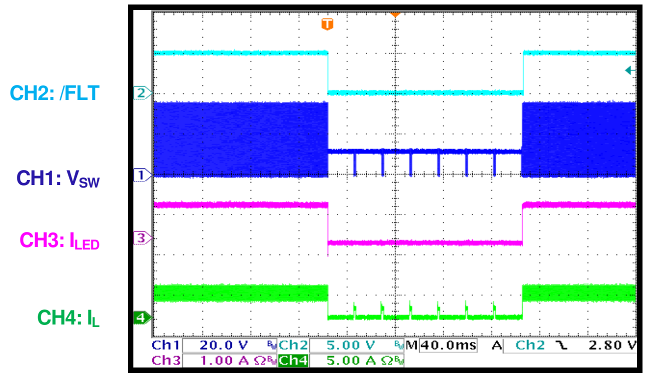
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

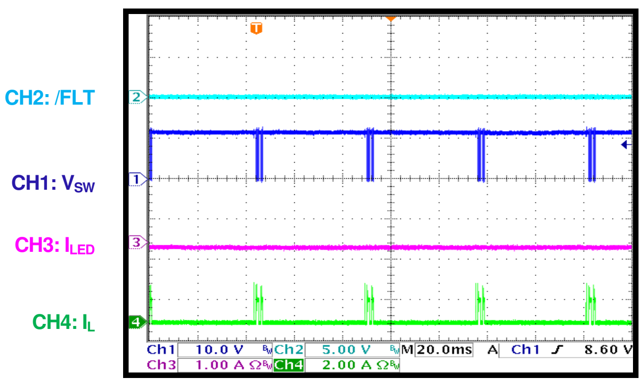
No Dimming
LED+ to LED- short, shutdown



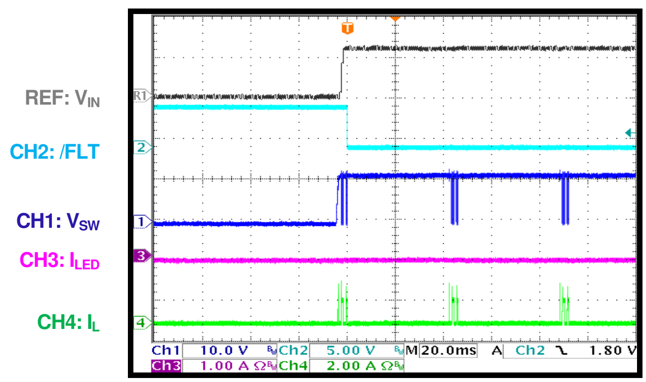
No Dimming
LED+ to LED- short entry and recovery



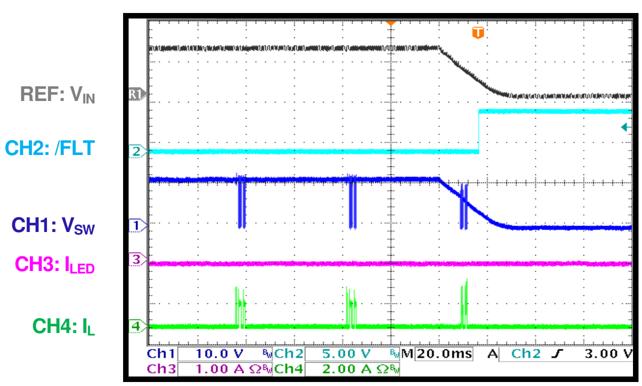
PWM Dimming
LED+ to LED- short, steady state



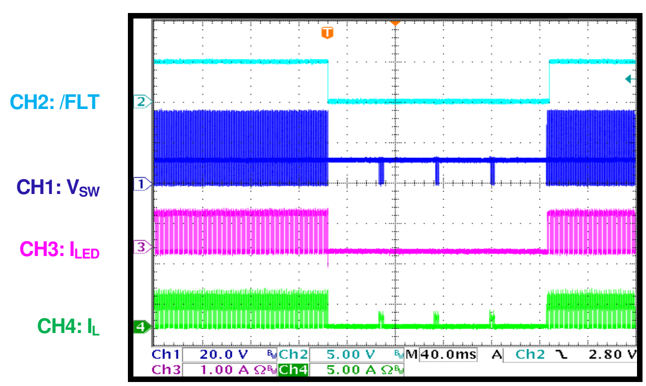
PWM Dimming
LED+ to LED- short, start-up



PWM Dimming
LED+ to LED- short, shutdown



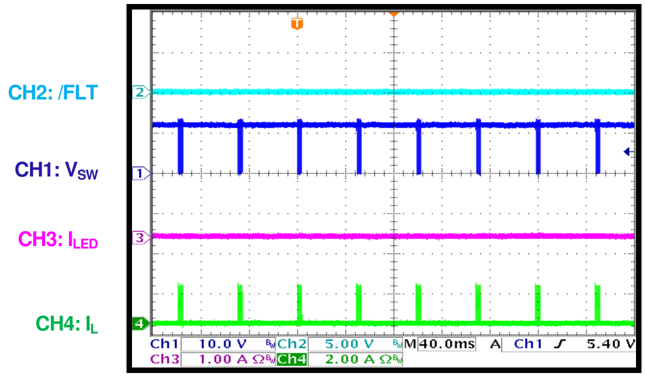
PWM Dimming
LED+ to LED- short entry and recovery



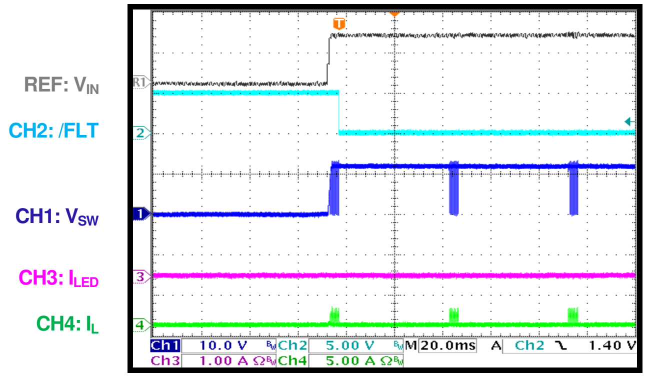
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Boost mode, 12 LEDs, V_{LED} = 36V, V_{IN} = 12V, f_{SW} = 410kHz, L = 10µH, T_A = 25°C, unless otherwise noted.

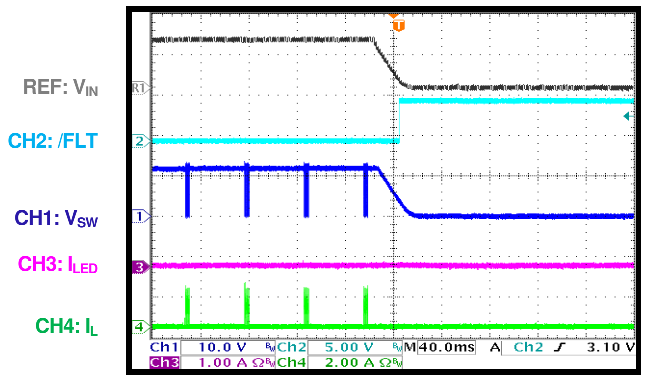
Two-Step Dimming
LED+ to LED- short, steady state



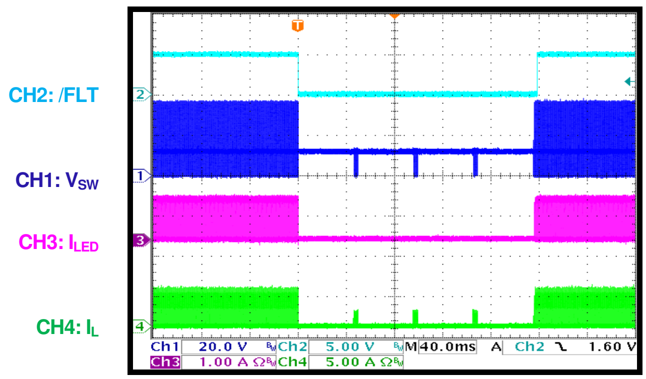
Two-Step Dimming
LED+ to LED- short, start-up



Two-Step Dimming
LED+ to LED- short, shutdown



Two-Step Dimming
LED+ to LED- short entry and recovery



FUNCTIONAL BLOCK DIAGRAM

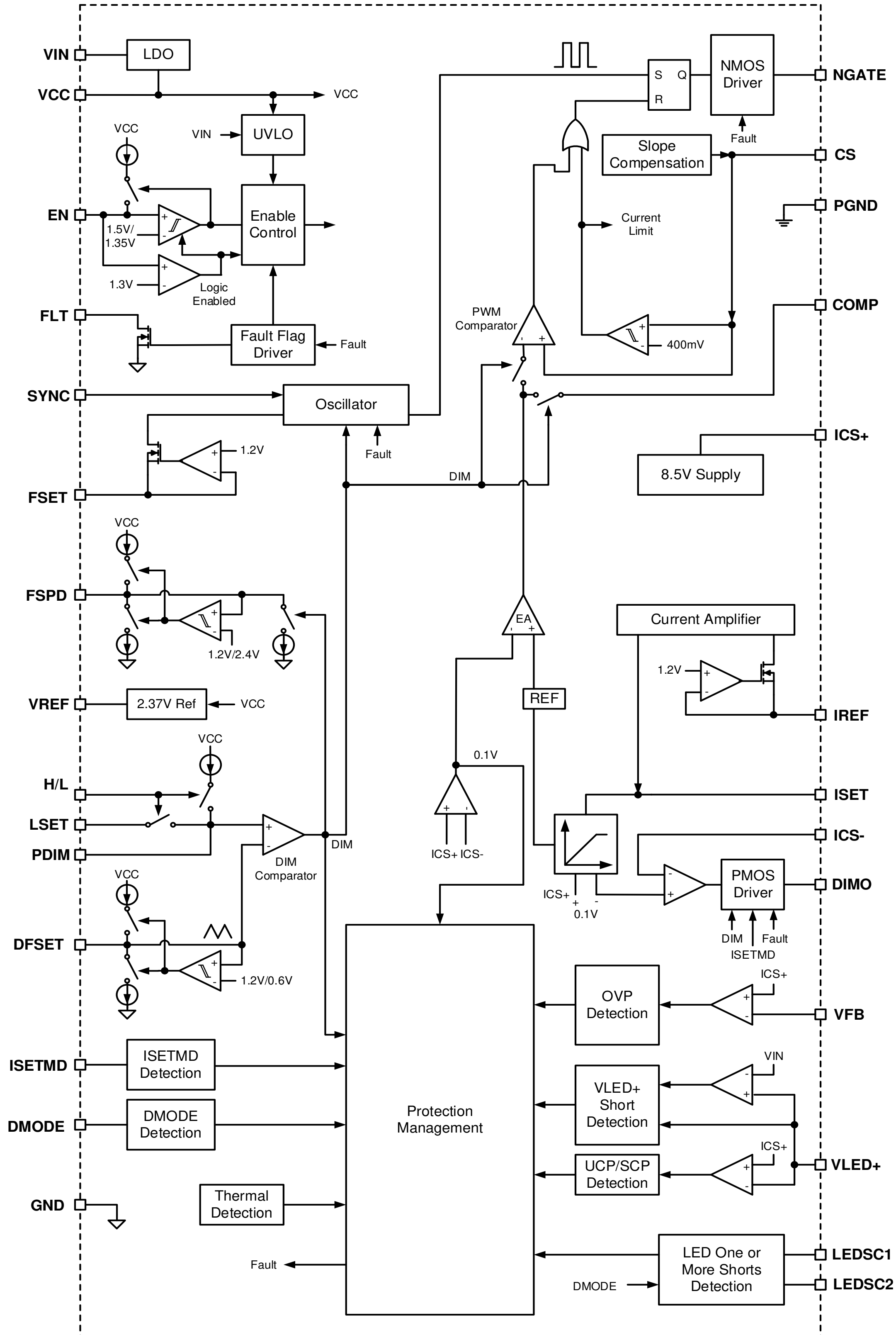


Figure 4: Functional Block Diagram

OPERATION

The MPQ2484 converter can support three single-channel LED driver configurations: boost mode, buck-boost mode, and low-side buck mode.

VCC Regulator

An internal low-dropout (LDO) regulator outputs a nominal 8.5V VCC supply from the VIN pin. This supplies power for both control blocks, as well as the N-channel MOSFET's gate driver. The VCC regulator features a 100mA current limit to prevent short circuits on the VCC rail. Place a 1µF to 10µF, low-ESR ceramic bypass capacitor from VCC to PGND.

The VCC supply cannot maintain an 8.5V output once V_{IN} drops below 8.5V. VCC can only be powered from VIN if V_{IN} is exceeds 8.5V, with the highest driver capacity possible. When V_{IN} is below 8.5V, choose a MOSFET with a lower V_{GS_TH}. VCC can also be powered by an external auxiliary supply that meets its voltage limit.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) prevents the device (and certain blocks) from operating at an insufficient supply voltage. There are three internal, fixed UVLO comparators that monitor V_{IN}, V_{CC}, and V_{ICS+}.

The MPQ2484 stops switching if either V_{IN} or V_{CC} falls below their respective UVLO threshold. Because the dimming P-channel MOSFET driver is powered from V_{ICS+}, this MOSFET shuts down if V_{ICS+} drops below its UVLO threshold.

If V_{IN} falls below 3.9V, all switching is disabled. Then the COMP voltage (V_{COMP}) is pulled down until V_{IN} exceeds 4.15V.

Similarly, if V_{CC} drops below 3.9V, switching is disabled and V_{COMP} is then pulled down until V_{CC} exceeds 4.135V.

Since V_{CC} is the internal LDO output from VIN, the actual V_{CC} is determined by V_{IN} and the dropout voltage of the VCC regulator. The dropout voltage depends on the load current drawn from VCC. For applications with a higher switching frequency (f_{SW}) or larger MOFFET driving capacity demand, there may be a rise in the VCC regulator's dropout voltage. If this occurs, V_{CC} may reach its UVLO threshold before V_{IN} when V_{IN} drops.

If the converter's output voltage (V_{ICS+}) drops below 8.5V, DIMO is pulled up to ICS+ to turn off the dimming P-channel MOSFET until V_{ICS+} exceeds 8.7V. If V_{ICS+} UVLO occurs, the device's performance is not affected.

In buck mode, VICS+ provides the input voltage, so ensure that V_{IN} exceeds V_{ICS+_UVLO} if the P-channel MOSFET is supposed to act as a dimming MOSFET. Note that the device can still operate in dimming mode without the dimming MOSFET. A dimming P-channel MOSFET is recommended for buck mode.

On/Off Control and Custom Input Under-Voltage Lockout (UVLO)

When EN is driven above its logic threshold, the VCC regulator is activated. Once V_{CC} exceeds its UVLO threshold, it starts to provide power to the internal control circuitry, and the integrated EN comparator begins operating.

If the EN voltage exceeds the comparator's upper threshold (typically 1.5V), the converter is enabled, and soft start (SS) begins. If EN falls below the comparator's lower threshold, then the converter stops switching; however, the VCC regulator and control circuitry continue working until the EN pin is pulled below its logic threshold (<0.4V). Then the chip enters shutdown mode while consuming a tiny input current.

In addition to providing standard on/off logic control, the integrated EN comparator allows the EN pin to set a custom input UVLO threshold by placing an external resistor divider from VIN to GND (see Figure 5).

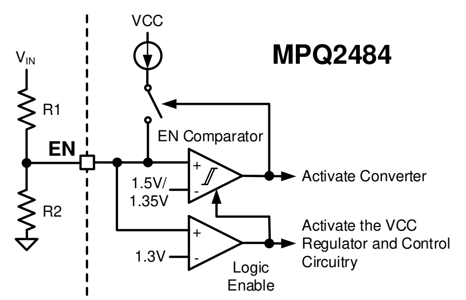


Figure 5: Custom Input UVLO Set by EN

The EN voltage is achieved via the resistor divider ratio from VIN. When the EN level reaches the UVLO rising threshold for the integrated EN comparator (about 1.5V), the converter starts switching. Meanwhile, an internal 0.63µA pull-up current source is enabled to source current out of the EN pin.

When V_{IN} drops to disable the converter, the EN voltage must drop below the EN comparator's UVLO threshold. This means V_{IN} must stay above the UVLO threshold to overcome the hysteresis from the 0.63µA pull-up current, as well as the inherent 150mV hysteresis of the EN comparator. As a result, the actual hysteresis can be set independently without changing the rising UVLO threshold.

Start-Up

If both VIN and EN exceed their UVLO rising thresholds, the internal LDO starts to charge the VCC capacitor. As V_{CC} rises to reach its V_{CC} UVLO threshold, the internal control circuitry and reference block operate. Once V_{IN}, V_{CC}, and EN are enabled, the MPQ2484 begins switching. Internal SS is implemented to prevent the converter's output voltage and current from overshooting during start-up. Once V_{ICS+} exceeds its UVLO threshold, the P-channel MOSFET is used as a dimming switch.

VREF Output

The MPQ2484 provides a 2.37V reference voltage (V_{REF}) on the VREF pin. Connect a 1nF to 10nF ceramic capacitor from VREF to GND. This reference can only source up to 80µA of current. V_{REF} can set the LSET level via a resistor divider for two-step dimming, or it can work as the pull-up source for the control pins to set a logic high input. V_{REF} is also the reference voltage for one or more internal LED shorts detection. If V_{REF} drops below its threshold, a short is triggered.

High-Side Current-Sense (CS) Reference Setting

The LED current is sensed by the high-side sensing resistor connected between ICS+ and ICS-. The ICS+ pin is tied to the output of the converter in boost or buck-boost mode, and connected to the input in buck mode. The ICS- pin, which is on the other side of the current-sense resistor, goes to the source of the P-channel MOSFET. If there is no external dimming MOSFET, then ICS- is directly connected to the LED string anode (VLED+). The chip regulates the voltage across the sensing resistor to 100mV if the ISET voltage exceeds 2.2V.

The MPQ2484 features a configurable LED current reference by monitoring the voltage on the setting resistor connected between ISET and ground. This resistor can be placed on LED light board to adjust the current. To reduce the noise created by a long connection wire, it is recommended to place a small capacitor close to the ISET pin.

The biased current can also be tuned by tying a resistor from IREF ($I_{REF} = V_{IREF} / R_{IREF}$) to ground. The current through the IREF resistor configures the biased current on ISET ($I_{SET} = 100 \times I_{REF}$). This means that changing the value of the setting resistor can adjust the LED current reference. For the relationship between V_{ISET} and the internal reference voltage, see the Mode and Current-Sense Reference Selection section on page 43.

Power Converter

Typically, the converter works in fixed-frequency, peak current control mode. At the beginning of each switching cycle, the N-channel MOSFET turns on at the rising edge of the clock. A resistor tied from the CS pin to GND senses the N-channel MOSFET's current signal.

To prevent subharmonic oscillations when the duty cycles exceeds 50%, a stabilizing ramp is added to the N-channel MOSFET current-sense signal to generate the inductor peak current information. When the inductor peak current reaches the value set by V_{COMP} (which is the output voltage of the error amplifier), the N-channel MOSFET turns off until the next switching clock begins. The current is also limited by the 400mV clamped voltage on the VCS pin. This sets the converter's maximum power.

Error Amplifier (EA)

The MPQ2484 converter incorporates a low-offset error amplifier (EA) to provide compensation for the control loop. The feedback signal and reference voltage provide two different modes to regulate the LED current. The feedback signal switches to the voltage on the high-side sensing resistor between ICS+ and ICS-. The reference voltage is about 100mV, but it can be adjusted by the ISET pin.

The internal EA outputs an amplified signal to the external compensation network. This signal is the difference between V_{REF} and the feedback voltage (V_{FB}), and it indicates V_{COMP}. V_{COMP} is connected to the PWM comparator to control the N-channel MOSFET's peak current, which is sensed by a sensing resistor connected between the source of N-channel MOSFET and ground. During the N-channel MOSFET's turn-on time, the CS pin outputs a current ramp. The current then flows through a resistor (R_{CS}) that is placed between the CS pin and the N-channel FET current-sense resistor. This current ramp configures slope compensation.

Once the CS level reaches V_{COMP}, the converter pulls down NGATE to turn off the N-channel MOSFET.

Note that the EA's transconductance is nonlinear. The EA's transconductance has a greater source ability than sink ability. Transconductance can help speed up LED regulation when PWM dimming is initiated.

Oscillator

The MPQ2484's f_{SW} can be configured between 100kHz and 2.2MHz by connecting a resistor (R_{FSET}) between the FSET pin and GND. R_{FSET} can be calculated with Equation (1):

$$R_{FSET}(k\Omega)=\frac{8333}{f_{SW}(kHz)} \quad (1)$$

For EMI-sensitive applications, the switching clock can be synchronized to an external clock signal that is applied to the SYNC pin. Once the external clock signal is added on the SYNC pin, the FSET setting no longer has any effect.

Ensure that the external clock signal frequency is at least 10% greater than the oscillator frequency set by FSET. If the external sync signal is lost, the internal oscillator controls the switching rate, and f_{SW} returns to the value set by FSET. This allows the switching clock to operate with intermittent synchronization signals.

Mode and Current-Sense Reference Selection

Table 1 lists different modes that can be selected using the DMODE and ISETMD pins.

Table 1: Mode Selection

	DMODE (High)	DMODE (Low)
ISETMD (High)	Normal operation mode: The LED current can be configured up to 100% of its nominal value.	Dimming switch mode: The LED current can be configured up to 100% of its nominal value.
ISETMD (Low)	Normal operation mode: The LED current can be configured up to 200% of its nominal value.	Dimming switch mode: The LED current can be configured up to 200% of its nominal value.

The DMODE pin selects whether the device operates in normal operation mode or dimming switch mode. If the logic is high, the dimming P-channel MOSFET is not used. If DMODE is pulled down to GND, the dimming P-channel MOSFET is used as a dimming switch. The P-channel MOSFET turns off during dimming, or if any fault is triggered.

The ISETMD pin sets the internal reference voltage. If ISETMD is pulled down to GND, the ISET voltage rises from 0.6V to 1.8V, and the reference voltage rises linearly from 0mV to 200mV, which can be used for analog dimming. When the ISET voltage exceeds 2.3V, the reference stays at about 100mV (see Figure 6 on page 44).

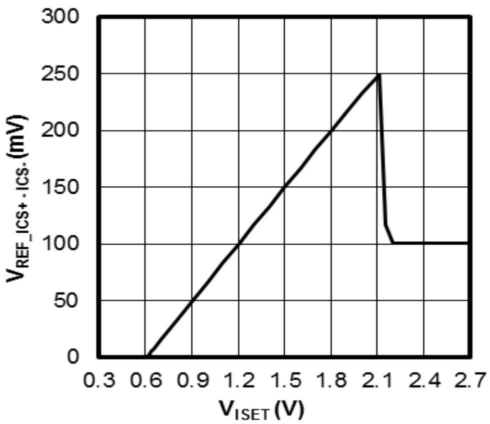


Figure 6: ISETMD is Low

When the ISETMD pin is logic high, and the voltage on ISET rises from 0.6V to 1.2V, the reference voltage rises linearly from 0mV to 100mV. When the ISET voltage exceeds 1.2V, the reference voltage stays at about 100mV (see Figure 7).

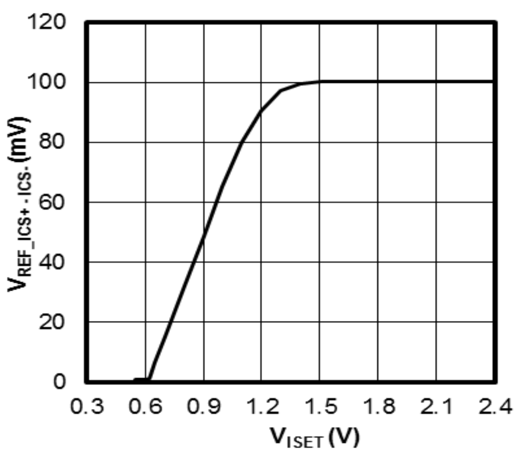


Figure 7: ISETMD is High

Frequency Spread Spectrum (FSS)

To optimize EMI performance, the MPQ2484 provides a frequency spread spectrum (FSS) function. Connect a capacitor from the FSPD pin to GND. The internal source and sink currents (both 100µA) charges or discharges the capacitor repeatedly to generate a stable triangular ramp waveform between 0.6V and 1.2V. This triangular ramp voltage works with the resistor connected between the FSPD and FSET pins to generate a current. The current flowing out from the FSET pin can dither f_{SW} for frequency spread spectrum. The spread spectrum frequency (f_{SS}) can be estimated with Equation (2):

$$f_{SS} = \frac{I_{FSPD}}{2 \times C_{FSPD} \times \Delta U} \quad (2)$$

Where I_{FSPD} is the FSPD source/sink current (100µA), C_{FSPD} is the capacitor between FSPD and GND, and ΔU = 0.6V (1.2V - 0.6V).

The spread spectrum scope (Δf_{SS}) can be calculated with Equation (3):

$$\Delta f_{SS} = f_{SW} \times \frac{R_{FSET}}{R_{FSPD}} \quad (3)$$

Where R_{FSPD} is the resistor between FSPD and FSET.

The f_{SW} scope is between (f_{SW} - Δf_{SS}) and f_{SW}. For example, if fsw = 400kHz, C_{FSPD} = 3.3nF, R_{FSET} = 21kΩ, and R_{FSPD} = 200kΩ, then f_{SS} is 20kHz and f_{SW} is dithered from 350kHz to 400kHz.

Figure 8 shows FSS operation.

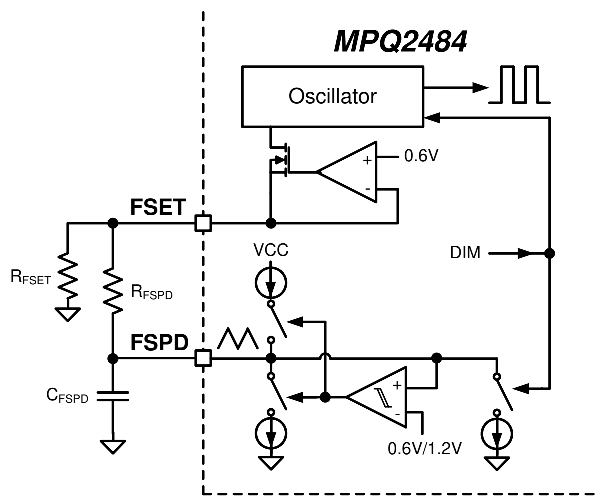


Figure 8: Frequency Spread Spectrum

Figure 9 shows FSS waveforms.

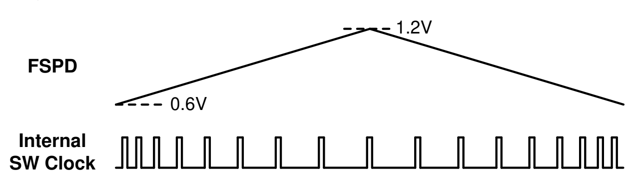


Figure 6: Frequency Spread Spectrum Waveforms

The modulation frequency should be lower than the oscillator frequency set by FSET by a minimum factor of 10.

If an external clock signal applied to the SYNC pin, the FSS mechanism is screened. Remove R_{FSPD} if FSS is disabled.

Two-Step Dimming

Connect a bypass capacitor from PDIM to GND for two-step dimming mode. The two-step dimming frequency can be configured by placing a capacitor between the DFSET pin and GND. The internal source and sink currents charge and discharge the capacitor repeatedly to generate a stable triangular ramp waveform between 0.6V and 1.2V. The two-step dimming frequency (f_{DIM}) can be estimated with Equation (4):

$$f_{DIM} = \frac{I_{DFSET}}{2 \times C_{DFSET} \times \Delta U} \quad (4)$$

Where I_{DFSET} is the source/sink current (100µA), C_{DFSET} is the capacitor between DFSET and GND, and ΔU = 0.6V (1.2V - 0.6V).

The two-step dimming duty (D_{DIM}) can be calculated with Equation (5):

$$D_{DIM} = \frac{V_{LSET} - 0.6}{1.2 - 0.6} \quad (5)$$

Where V_{LSET} is the LSET pin voltage. Figure 10 shows two-step dimming.

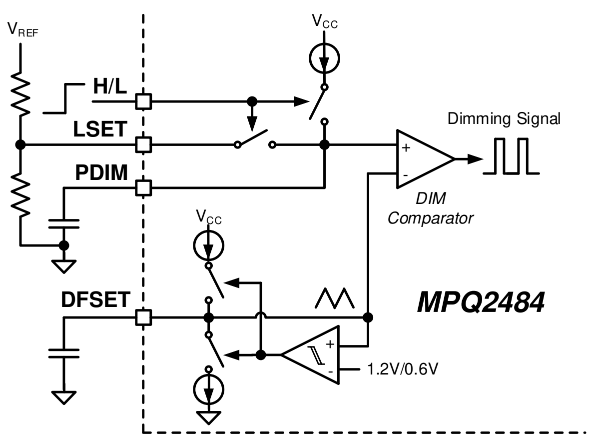


Figure 7: Two-Step Dimming

If the H/L pin is pulled up to a logic high input after two-step dimming is set, then the positive input of the DIM comparator is disconnected from the LSET pin. The internal pull-up current source charges the PDIM capacitor to 2V. The DIM comparator outputs a 100% duty cycle dimming signal, and the LED current is regulated at full scale.

If the H/L pin is set to logic low, the internal pull-up current turns off, and the positive input of the DIM comparator is connected to the LSET pin. The LSET level can be set between 0.6V and 1.2V via an external resistor divider connected from VREF to the LSET pin. When compared to the DFSET triangular ramp waveform, the LSET voltage determines the duty cycle of the final dimming signal (see Figure 11).

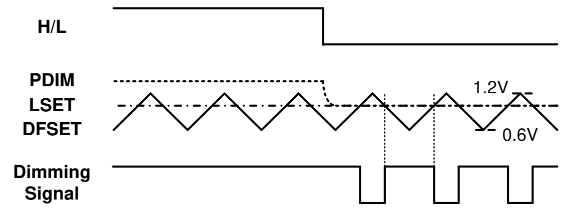


Figure 11: Dimming Signal Generation

The MPQ2484 can switch between full-scale LED brightness and lower levels via the H/L signal.

PWM Dimming

PWM dimming can be achieved by driving the PDIM pin with a pulsating voltage source. Tie the H/L pin to VREF, and connect a 8.06kΩ resistor from the DFSET pin to GND (V_{DFSET} is always 100µA x 8.06kΩ = 0.806V) to disable the dimming oscillator (see Figure 12).

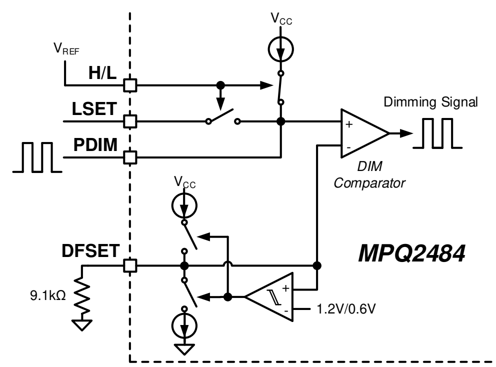


Figure 12: PWM Dimming

When the voltage on the PDIM pin exceeds 1.2V (meaning it exceeds V_{DFSET}), the DIM comparator outputs a dimming on signal. When the PDIM voltage drops below 0.4V (below V_{DFSET}), a dimming off signal is generated. Ensure that the minimum PWM dimming on time is longer than 60µs, or the part will stop switching.

Analog Dimming

Analog dimming can be achieved via the ISETMD and ISET pins, which set the internal reference voltage. When the ISETMD pin is pulled down to GND, provide a linear voltage between 0.6V and 1.8V for the ISET pin. The reference voltage rises linearly from 0mV to 200mV.

Dimming Performance

The DIM comparator outputs a dimming signal to control the pulse width that modulates the output LED current. When the dimming signal is logic high, the MPQ2484 is enabled and the dimming P-channel MOSFET turns on. When the dimming signal is logic-low, the device stops switching and the dimming P-channel MOSFET turns off.

When the dimming signal is low, the internal EA's output is disconnected from both the PWM comparator and the COMP pin. The COMP level can remain constant when dimming is off.

The dimming signal also affects the switching oscillator and FSS functions. If f_{SW} is set by the FSET pin, both the oscillator and FSS mechanisms are disabled when the dimming signal is off and the FSPD voltage is pulled down to 0.6V. When a dimming signal is received, the functions are reinitiated. This protocol can force the converter's switching clock to be synchronized by the dimming signal, which ensures each dimming cycle performs consistently (see Figure 13).

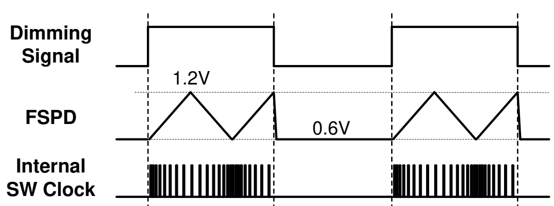


Figure 10: SW Clock Synchronization by the Dimming Signal

Over-Voltage Protection (OVP)

The MPQ2484 monitors the voltage across the LED strings. A resistor divider is connected from ICS+ to the cathode of the LED string, and the tap of the divider is tied to the VFB pin. When the differential voltage between ICS+ and VFB exceeds 1.17V, the converter stops switching, but the dimming P-channel MOSFET maintains its original status. If an open LED fault is triggered at the same time, then the P-channel MOSFET is disabled and the chip runs as it would during a fault condition. When the differential voltage drops below 1.02V, the over-voltage (OV) condition is removed, and the MPQ2484 restarts and resumes normal operation.

Over-Current Protection (OCP)

The cycle-by-cycle current limit restricts the N-channel MOSFET's maximum current via the current-sense resistor on the CS pin. V_{CS} is typically400mV.

Open LED Protection

If the LED string is disconnected from the system, the device cannot obtain the LED current information, and the converter automatically increases the output voltage until OVP is triggered.

If the dimming P-channel MOSFET is on when an OV condition is detected, the device checks the differential voltage between ICS+ and VLED+ to avoid start-up voltage overshoot. If the differential voltage is below 50mV, then an open LED fault occurs.

If the system operates without a dimming P-channel MOSFET when an OV condition occurs, the device checks the voltage on the LED current-sense resistor between ICS+ and ICS-. If the voltage is below 50mV, then an open LED fault occurs.

If an open LED fault occurs, the converter and dimming P-channel MOSFET turn off, V_{COMP} is pulled down to ground, and /FLT asserts. The fault recovery counter starts when the differential voltage between ICS+ and VFB drops below 1.02V. After 8192 consecutive clock cycles, the system restarts again with a soft start. During the recovery cycle, the /FLT signal stays latched. /FLT resets after 30µs without a fault.

LED String Anode/Cathode to Battery/Ground Short Protection

If an LED short fault is detected, then the converter and dimming P-channel MOSFET turn off, V_{COMP} is pulled down to ground, and /FLT asserts. After 8192 consecutive clock cycles, the system restarts again with a soft start. During the recovery cycle, the /FLT signal remains latched. /FLT resets once 30µs pass with no fault present.

One or More LED Short Protection

In certain cases, only one LED may short, but it is possible for several LEDs to short. The MPQ2484 features one or more LEDs short detection to guarantee that the light source stays sufficiently illuminated. There are two conditions that trigger one or more LED short protection:

- $|V_{LEDSC1} - V_{LEDSC2}| > 180mV$ for 32 consecutive clock cycles
- $|V_{LEDSC1} - V_{LEDSC2}| > 80mV$ for 4096 consecutive clock cycles

If the absolute value of the differential voltage between LEDSC1 and LEDSC2 exceeds either of these thresholds for the set time, the converter and dimming P-channel MOSFET turn off, V_{COMP} is pulled to ground, and /FLT asserts. After 8192 consecutive clock cycles, the system restarts again with a soft start. During the recovery cycle, the /FLT signal remains latched. /FLT resets once 30µs pass with no fault present.

LEDSC1 and LEDSC2 sense the voltage drop of one LED or the whole LED string. V_{LEDSC1} can be estimated with Equation (6):

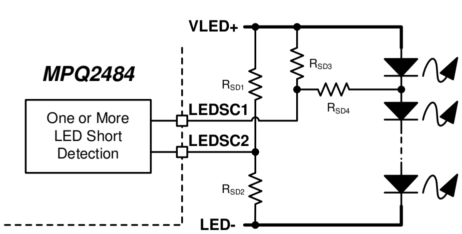
$$V_{LEDSC1} = V_{LED+} - \frac{1}{K} V_{LED} \times \frac{R_{SD3}}{R_{SD3} + R_{SD4}} \quad (6)$$

Where the K is the LED number of the LED string, and V_{LED} is the whole LED string voltage drop.

V_{LEDSC2} can be calculated with Equation (7):

$$V_{LEDSC2} = V_{LED+} - V_{LED} \times \frac{R_{SD1}}{R_{SD1} + R_{SD2}} \quad (7)$$

It is recommended to set R3:R4 = 1:1. It is required to set R1:R2 = 1:(2K - 1).



R_{SD1}:R_{SD2} = 1:(2K - 1)
R_{SD3}:R_{SD4} = 1:1
(K is the LED number of the LED strings)

Figure 11: One or More LED Short Protection

For applications with 8 LEDs (such as in Figure 15 and Figure 16 on page 52), set R_{SD2} = 100kΩ, R_{SD1} = 6.65kΩ, and R_{SD3} = R_{SD4} = 6.65kΩ.

For applications with 12 LEDs (such as in Figure 17 and Figure 18 on page 53), set R_{SD2} = 100kΩ, R_{SD1} = 4.32kΩ, and R_{SD3} = R_{SD4} = 4.32kΩ.

Thermal Protection

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures and possibly being damaged. If the silicon die temperature exceeds 170°C, over-temperature protection (OTP) shuts down the chip and /FLT asserts. When the temperature returns to below the lower threshold (about 150°C), the chip restarts and resumes normal operation. During the recovery cycle, the /FLT signal remains latched. /FLT resets once 30µs pass with no fault present.

The ISET pin can be used as an NTC pin by connecting an NTC resistor between ICS+ and ISET. When the voltage on the NTC resistor rises from 0.6V to 1.8V, the reference voltage rises from its minimum value to 200mV. Then the LED current is dimmed according to the value of the NTC resistor.

Fault Flag (/FLT)

The /FLT pin is an active-low, open-drain output that should be connected to a voltage source through an external pull-up resistor for fault indication. For normal operation, the /FLT pin is pulled high to indicate that there is no fault. The /FLT pin is pulled high before soft start begins. If there is a fault, /FLT is pulled down to ground.

If the fault is removed after soft start ends during a recovery cycle, the /FLT pin resets once the converter operates normally (without a fault) for 30µs consecutively.

Table 2: UVLO, OCP, and OVP (No /FLT Assertion)

Protection	Trigger Condition	Release Condition	Action
V_{IN} UVLO	V_{IN} < 3.9V	V_{IN} > 4.15V	Disables the chip
V_{CC} UVLO	V_{CC} < 3.9V	V_{CC} > 4.135V	Disables the chip
V_{ICS+} UVLO	V_{ICS+} < 8.5V	V_{ICS+} > 8.7V	Disables the dimming MOSFET
Custom input UVLO	V_{EN} < 1.35V	V_{EN} > 1.5V	Disables the converter
OVP	V_{ICS+} - V_{FB} > 1.17V	0V < V_{ICS+} - V_{FB} < 1.02V	Disables the converter
N-channel MOSFET current limit	V_{CS} > 400mV	Next SW clock comes	Disables the converter in this switching cycle

Table 3: OLP, SCP, and OTP (with Dimming P-Channel MOSFET)

Protection	Activate			Release
	Boost	Buck-Boost	Buck	
Open LED	OVP status and V_{ICS+} - VLED+ < 0.1V			Must satisfy all of the release conditions in Table 2
LED+ to PGND short	V_{ICS+} - V_{ICS-} > 0.3V for 1µs			
LED- to PGND short	Normal connection	Short input	If V_{IN} is high (> 1.17 x V_{OUT}), OVP occurs, then SCP is triggered If V_{IN} is < (1.17 x V_{OUT}), SCP is triggered	
LED+ to battery short	V_{ICS+} - V_{ICS-} > 0.3V for 1µs		If the N-channel MOSFET reaches its current limit and V_{ICS+} - VLED+ < 0.1V for 1µs	
LED- to battery short	Short input	Normal connection		
Short one or more LEDs	$\lvert V_{LEDSC1} - V_{LEDSC2} \rvert$ > 180mV for 32 consecutive clock cycles $\lvert V_{LEDSC1} - V_{LEDSC2} \rvert$ > 80mV for 4096 consecutive clock cycles			
OTP	T_J > 170°C			T_J < 150°C

Table 4: OLP, SCP, and OTP (without Dimming P-Channel MOSFET)

Protection	Activate			Release
	Boost	Buck-Boost	Buck	
Open LED	OVP status and V_{ICS+} - V_{ICS-} < 50mV			Must satisfy all of the release conditions in Table 2
LED+ to PGND short	N/A	N/A	N/A	
LED- to PGND short	N/A	N/A	N/A	
LED+ to battery short	V_{ICS+} - V_{ICS-} > 0.3V for 1µs		If the N-channel MOSFET reaches its current limit and V_{ICS+} - VLED+ < 50mV for 1µs	
LED- to battery short	N/A	N/A		
Short one or more LEDs	$\lvert V_{LEDSC1} - V_{LEDSC2} \rvert$ > 180mV for 32 consecutive clock cycles $\lvert V_{LEDSC1} - V_{LEDSC2} \rvert$ > 80mV for 4096 consecutive clock cycles			
OTP	T_J > 170°C			T_J < 150°C

APPLICATION INFORMATION

Setting the LED Current

The external resistor between ICS+ and ICS- sets the output LED current. When $V_{ISET} > 2.2V$, the reference voltage on ICS+ and ICS- is always 100mV. V_{ISET} can be adjust by changing the values of R_{IREF} and R_{ISET}. V_{ISET} can be estimated with Equation (8):

$$V_{ISET} = 100 \times \frac{0.805 \times R_{ISET}}{R_{IREF}} \quad (8)$$

Where R_{IREF} is the resistor connect to the IREF pin, and R_{ISET} is the resistor connected to the ISET pin.

When the reference voltages on ICS+ and ICS- are 100mV, it is recommended for $R_{IREF} = R_{ISET} = 80.6k\Omega$. R_{SENSE} is the resistor between ICS+ and ICS-. R_{SENSE} can be calculated with Equation (9):

$$R_{SENSE} = \frac{0.1V}{I_{LED}} \quad (9)$$

Consider the power consumption when selecting the packages of the LED current-sense resistor. For example, if the required LED current is 1A, the resistor should have a 1206 package.

The reference voltages on ICS+ and ICS- can be adjusted via ISETMD and V_{ISET}. See the Mode and Current-Sense Reference Selection section on page 43 for more details.

Selecting the Inductor

For most applications, use a 4.7µH to 100µH inductor with a DC current rating greater than the maximum inductor current. Consider the inductor's DC resistance when estimating the inductor's output current and power consumption.

For buck converter designs, estimate the required inductance (L) with Equation (10):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (10)$$

Where f_{SW} is the switching frequency, and ΔI_L is the inductor current ripple.

Choose the inductor ripple current to be 30% of the maximum load current. The maximum inductor peak current (I_{L_PEAK}) can be calculated with Equation (11):

$$I_{L\_PEAK} = I_{L\_AVG} + \frac{\Delta I_L}{2} \quad (11)$$

Where I_{L_AVG} is the average current through the inductor.

I_{L_AVG} is equal to the output load current (LED current) for buck applications. For buck-boost converter designs, estimate the required inductance (L) with Equation (12):

$$L = \frac{V_{OUT} \times V_{IN}}{(V_{OUT} + V_{IN}) \times \Delta I_L \times f_{SW}} \quad (12)$$

Where ΔI_L is the inductor peak-to-peak current ripple.

Select ΔI_L to be about 25% of the inductor average current (I_{L_AVG}). I_{L_AVG} can be calculated with Equation (13):

$$I_{L\_AVG} = I_{LED} \times (1 + \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

I_{L_PEAK} can be calculated with Equation (14):

$$I_{L\_PEAK} = I_{L\_AVG} + \frac{\Delta I_L}{2} \quad (14)$$

For boost converter designs, calculate the required inductance (L) with Equation (15):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times \Delta I_L \times f_{SW}} \quad (15)$$

Select ΔI_L to be around 30% of the inductor average current (I_{L_AVG}). I_{L_AVG} can be estimated with Equation (16):

$$I_{L\_AVG} = I_{LED} \times \frac{V_{OUT}}{V_{IN}} \quad (16)$$

I_{L_PEAK} can be calculated with Equation (17):

$$I_{L\_PEAK} = I_{L\_AVG} + \frac{\Delta I_L}{2} \quad (17)$$

Under light-load conditions below 200mA, use a larger-value inductor to improve efficiency.

Selecting the Input Capacitor

The input current in buck mode and buck-boost mode is discontinuous, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 10µF to 44µF capacitor. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, it is recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the smaller capacitor as close as possible to VIN and GND (INGND = PGND in buck mode. In buck-boost mode, connect the capacitor to VIN, INGND, and PGND).

Because C_{IN} absorbs the input switching current in buck mode, the MPQ2484 requires an adequate ripple current rating. The RMS current in the input capacitor (I_{CIN}) can be estimated with Equation (18):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (18)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (19):

$$I_{CIN} = \frac{I_{LED}}{2} \quad (19)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (20):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

If ΔI_L ≥ the I_{LED} in buck-boost mode, then the input voltage ripple (ΔV_{IN}) can be calculated with Equation (21):

$$\Delta V_{IN} = \frac{I_{LED} \times V_{OUT}}{(V_{IN} + V_{OUT}) \times f_{SW} \times C_{IN}} \quad (21)$$

If ΔI_L ≥ the I_{LED} in boost mode, then the input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (22):

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_{IN}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (22)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For the best results, use low-ESR capacitors to maintain a low output voltage ripple.

In buck mode, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (23):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{sw} \times C_{OUT}}) \quad (23)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (24):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (24)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, ΔV_{OUT} can be calculated with Equation (25):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (25)$$

If ΔI_L ≥ I_{LED} for buck-boost applications, ΔV_{OUT} can be estimated with Equation (26):

$$\Delta V_{OUT} = I_{LED} \times (R_{ESR} + \frac{V_{OUT}}{f_{sw} \times C_{OUT} \times (V_{IN} + V_{OUT})}) \quad (26)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, ΔV_{OUT} can be calculated with Equation (27):

$$\Delta V_{OUT} = I_{LED} \times R_{ESR} \quad (27)$$

If $I_{BANDVALLEY}$ ≥ the I_{LED} in boost applications, the output capacitor can be estimated using Equation (28):

$$\Delta V_{OUT} = I_{LED} \times (R_{ESR} + \frac{V_{OUT} - V_{IN}}{f_{sw} \times C_{OUT} \times V_{OUT}}) \quad (28)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, ΔV_{OUT} can be calculated with Equation (29):

$$\Delta V_{OUT} = I_{LED} \times R_{ESR} \quad (29)$$

Selecting the N-Channel MOSFET

The MOSFET gate driver is sourced from VCC. The maximum gate charge is limited by the 50mA V_{CC} sourcing current limit. A leadless package is recommended for designs with a high f_{SW}. The MOSFET gate capacitance should be small enough that the gate voltage is fully discharged during the off time.

During start-up (especially when the V_{IN} range is below the V_{CC} regulation target), V_{CC} must be sufficient to fully turn on the MOSFET. If the MOSFET's drive voltage is below its gate plateau voltage during start-up, the boost converter may not start up normally, and the converter may not operate at the maximum duty cycle in a high power dissipation state. To avoid this, select an N-channel MOSFET with a lower threshold and set the V_{IN} on threshold above 5V.

Selecting the Diode

It is recommended to use a Schottky diode for D1 due to its low forward voltage drop and small reverse recovery charge. A low reverse leakage current is critical when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage, as well as any switching node ringing. The diode must also be able to handle the average output current.

Selecting the Dimming P-Channel MOSFET

The P-channel MOSFET is typically used for dimming to improve dimming performance. In boost mode and buck-boost mode, the P-channel MOSFET can also provide protection for LED+ to battery shorts, as well as LED+ to PGND shorts.

When dimming is off, the voltage on the P-channel MOSFET is equal to the LED voltage. Select the P-channel MOSFET V_{DS} to exceed the LED voltage, and ensure that the continuous drain current exceeds the LED current with a lower $R_{DS(ON)}$.

Over-Current Protection (OCP) Setting

Place a resistor in series with the N-channel MOSFET to sense the inductor current and set the current limit.

To ensure that there is a sufficient LED current, the current-limit threshold must be set via the current-sense resistor (R_{CS}) on the CS pin. $I_{L\_PEAK\_LIMIT}$ can be estimated with Equation (30):

$$I_{L\_PEAK\_LIMIT}(A) = \frac{400(mV)}{R_{CS}(m\Omega)} \quad (30)$$

The $I_{L\_PEAK\_LIMIT}$ value is typically set to 120% to 130% of I_{L_PEAK}.

For the applications shown in Figure 15, Figure 16, Figure 17, and Figure 18 on pages 52 and 53, It is recommended follow the guidelines below:

- Place three current-sense resistors (70mΩ, 70mΩ, and 70mΩ) with 2512 packages in parallel with one another to limit $I_{L\_PEAK\_LIMIT}$ to 17A.
- Use R9 to provide slope compensation.
- Use C4 to filter out the switching noise on the CS pin.

Over-Voltage Protection (OVP) Setting

The resistor divider network (R10 and R11) connected to ICS+, VFB, and the cathode of the LED string monitors the output voltage (see Figure 15 on page 52).

The resistor divider network can determine whether there is an open fault on an LED string. If the voltage between ICS+ and VFB exceeds 1.17V, then the converter stops switching and does not recover until the voltage drops below 1.02V.

Set the over-voltage protection (OVP) threshold to be 10% to 30% greater than the maximum output voltage (LED string voltage). The OVP threshold (V_{OVP}) can be calculated with Equation (31):

$$V_{OVP} = \frac{R10 + R11}{R10} \times 1.17 \quad (31)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to improve thermal performance. For the best results, follow the guidelines below:

1. Use large copper areas to minimize conduction loss and thermal stress, and ensure that all heat-dissipating components have adequate cooling.
2. Isolate the power components and high-current paths from the sensitive analog circuitry, such as CS.
3. Keep the high-current paths short, especially at the ground terminals. This is recommended for stable, jitter-free operation.
4. Keep the switching loops short.
5. Connect the anode of D1 close to the drain of the MOSFET (M1).
6. Connect the cathode of D1 close to the output capacitor (C_{OUT}).
7. Connect C_{OUT} and the current-sense resistors (R1A, R1B, and R1C) directly to PGND.
8. Route high-speed switching nodes away from the sensitive analog areas.
9. Use an internal PCB layer for the GND plane. This layers acts as an EMI shield to keep radiated noise away from the device.

TYPICAL APPLICATION CIRCUITS

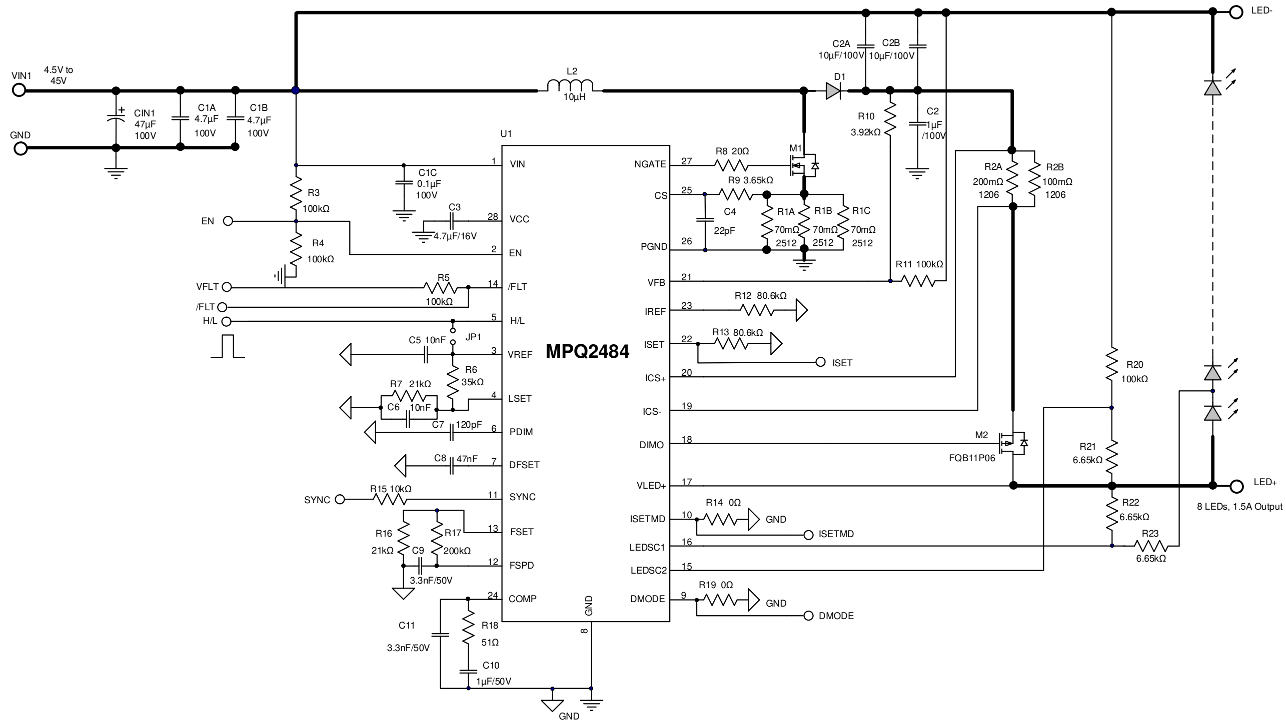


Figure 15: Typical Application Circuit for Buck-Boost Topology (Two-Step Dimming)

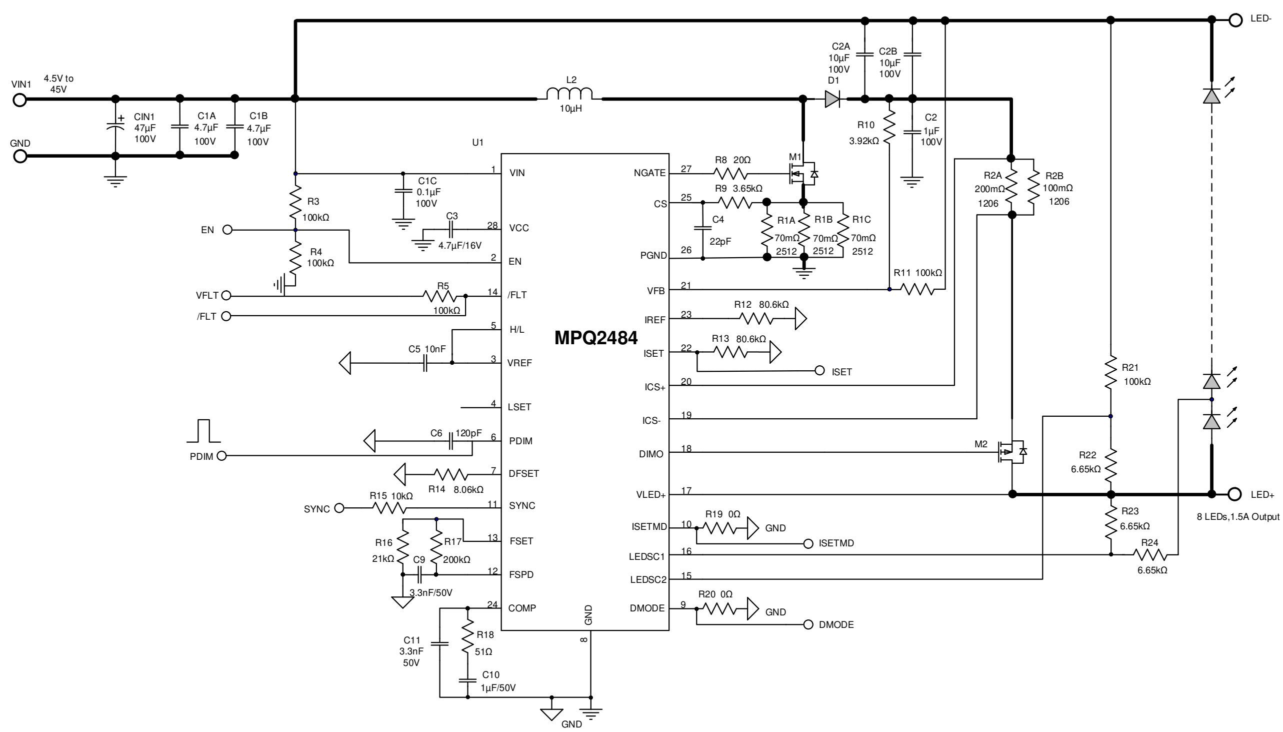


Figure 16: Typical Application Circuit for Buck-Boost Topology (PWM Dimming)

TYPICAL APPLICATION CIRCUITS *(continued)*

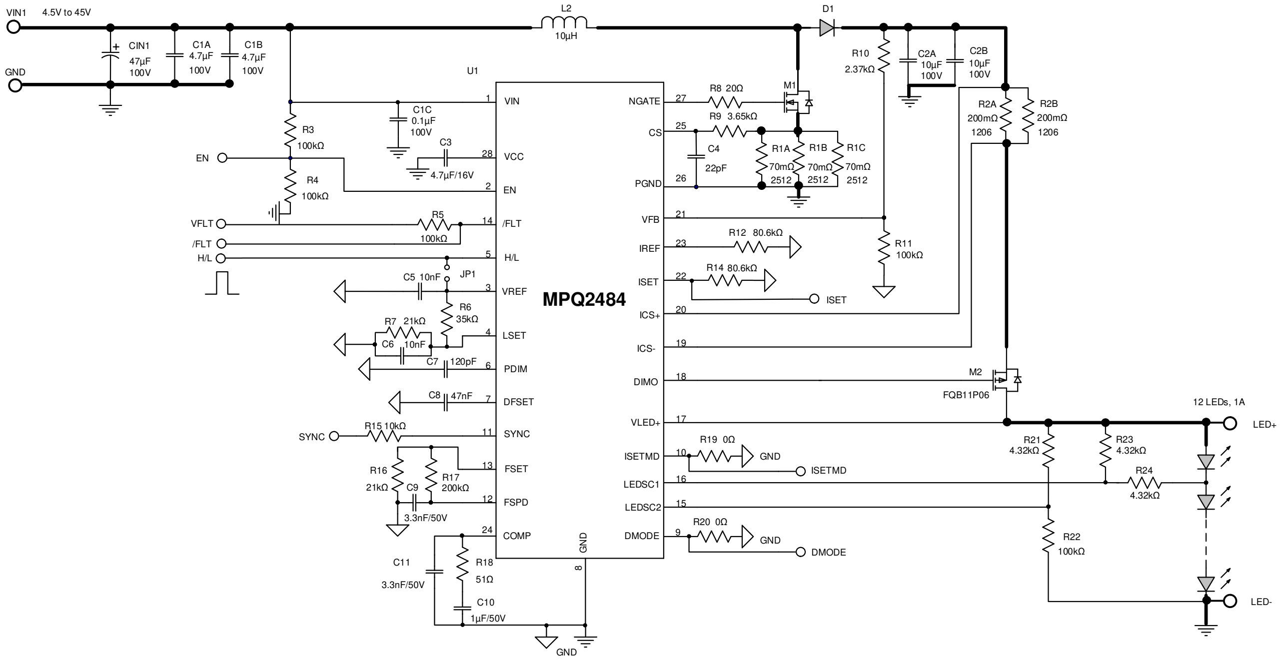


Figure 17: Typical Application Circuit for Boost Topology (Two-Step Dimming)

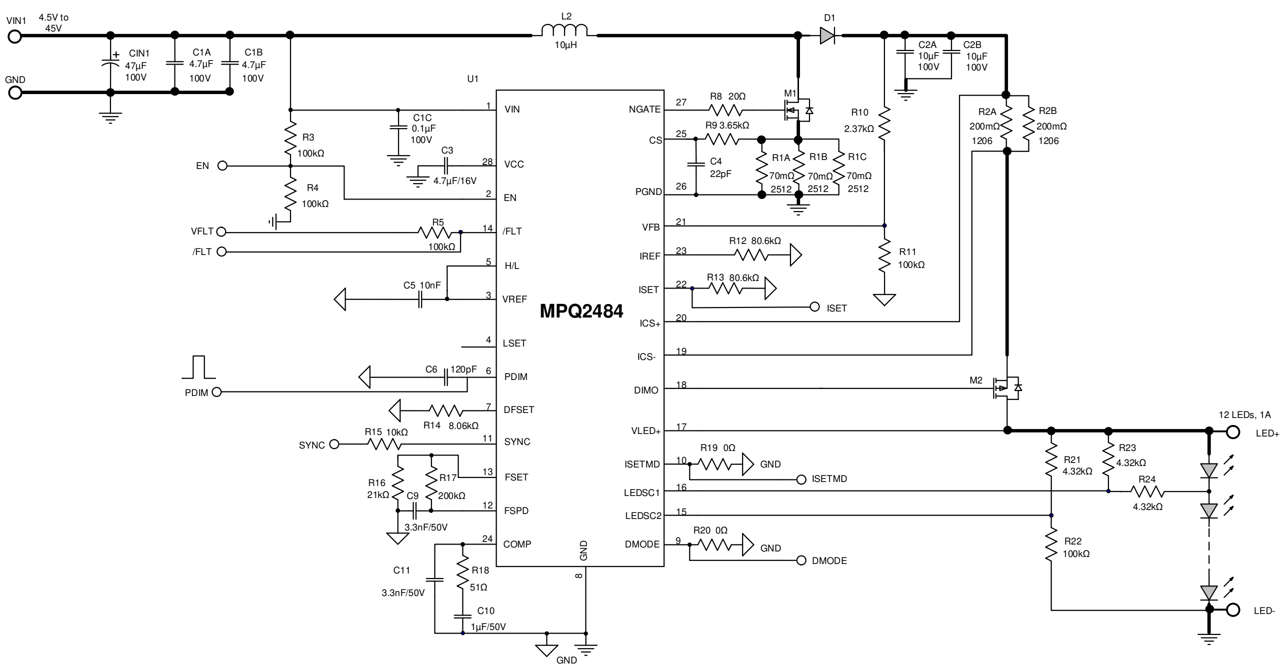
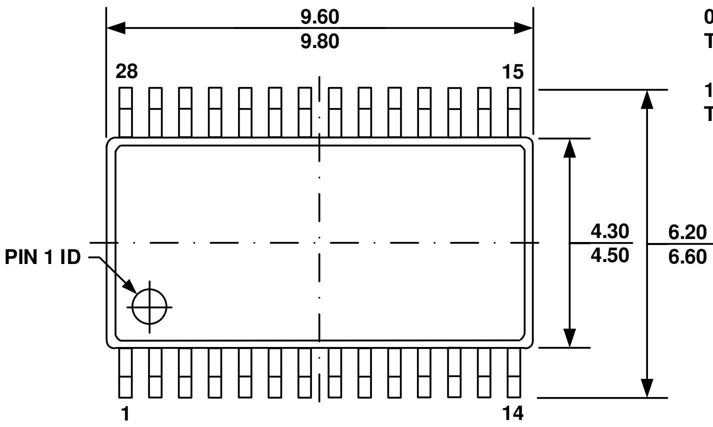


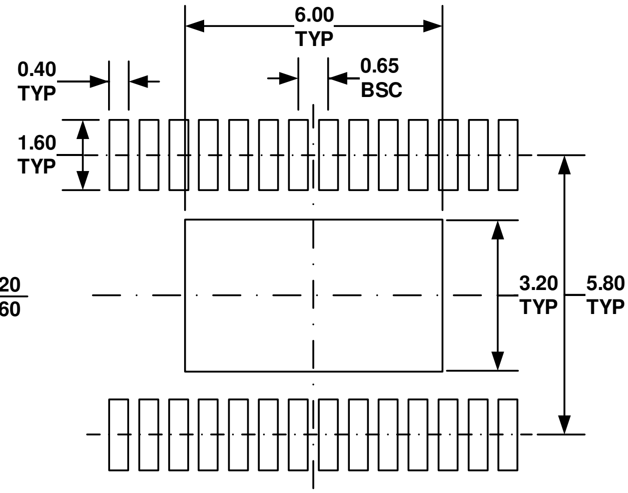
Figure 18: Typical Application Circuit for Boost Topology (PWM Dimming)

PACKAGE INFORMATION

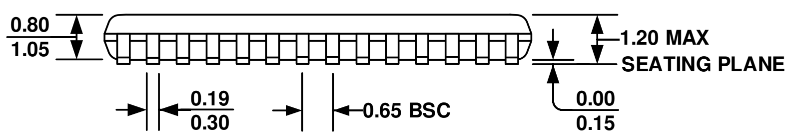
TSSOP-28EP



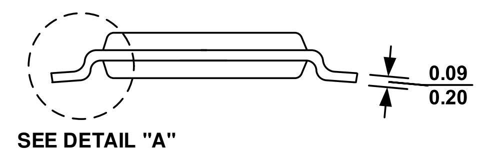
TOP VIEW



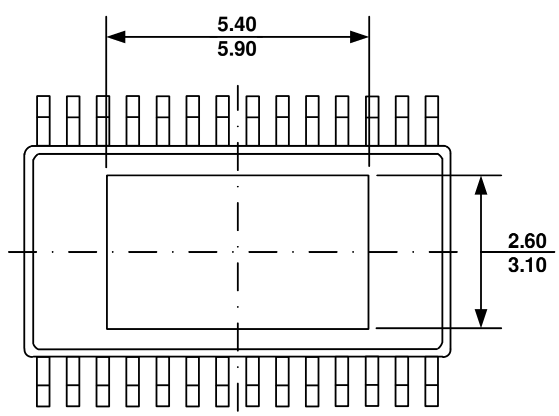
RECOMMENDED LAND PATTERN



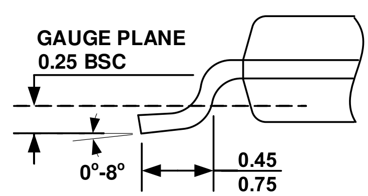
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

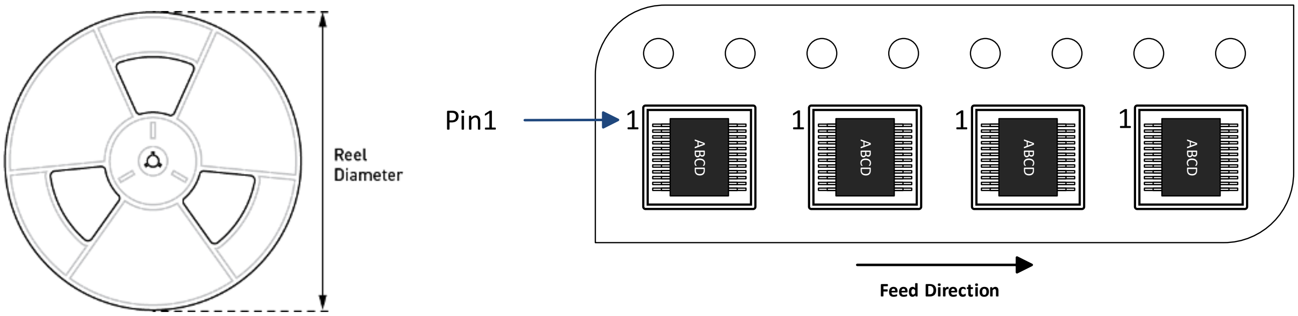


DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2484GF-AEC1-Z	TSSOP-28EP	2500	N/A	13in	16mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/08/2021	Initial Release	-