19-5786; Rev 0; 3/11

16-Channel, Linear, High-Voltage Analog Switches

General Description

The MAX4968/MAX4968A are 16-channel, high-linearity, high-voltage, bidirectional SPST analog switches with 18Ω (typ) on-resistance. The devices are ideal for use in applications requiring high-voltage switching controlled by a low-voltage control signal, such as ultrasound imaging and printers. The MAX4968A provides integrated 40kΩ (typ) bleed resistors on each switch terminal to discharge capacitive loads. Using HVCMOS technology, these switches combine high-voltage bilateral MOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

The MAX4968 is pin-to-pin compatible with the MAX14802 and Supertex HV2601. The MAX4968A is pin-to-pin compatible with the MAX14803 and Supertex HV2701. The only difference is the V_{PP} positive supply voltage level. The MAX4968/MAX4968A require a low +10V (typ) voltage (V_{PP}), whereas the MAX14802/MAX14803 and HV2601/HV2701 require a high +100V supply voltage.

In a typical ultrasound application, these devices do not require a dedicated high-voltage supply that implies a significant simplification of system requirement. The negative voltage supply can be shared with the transmitter, and the positive voltage supply is typically +10V.

The devices are available in the 48-pin LQFP package and are specified over the -40°C to +85°C extended temperature range.

Applications

Medical Ultrasound Imaging

Nondestructive Testing (NDT)/Industrial Ultrasound Imaging

Printers

Features

- **Latch Free**
  SOI HVCMOS Process Technology for High Performance and Robustness
- **No Dedicated High-Voltage Supplies Required**
- **R_{ON} Flatness Guaranteed in Entire Input Range**
- **Low-Power Dissipation**
- **Low-Charge Injection and Voltage Spike**
- **25MHz Serial Interface (+2.5V to +5V)**
- **2nd Harmonic Distortion < -45dB at 2MHz ± 90V Pulse**
- **Low Parasitic Capacitance Guarantees High Bandwidth**
- **DC to 30MHz Small-Signal Analog Bandwidth (C_{LOAD} = 200pF)**
- **500kHz to 20MHz High-Signal Analog Bandwidth (C_{LOAD} = 200pF)**
- **Extended Input Range Up to 210V_{P-P}**
- **-80dB (typ) Off-Isolation at 5MHz (50Ω)**
- **Shunt (Bleed) Resistors on Outputs (MAX4968A Only)**
- **Daisy-Chainable Serial Interface**

Ordering Information/Selector Guide

PART	TEMP RANGE	SWITCH CHANNELS	BLEED RESISTOR	PIN-PACKAGE
MAX4968ECM+*	-40°C to +85°C	16	No	48 LQFP
MAX4968AECM+	-40°C to +85°C	16	Yes	48 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—Contact factory for availability.*

16-Channel, Linear, High-Voltage Analog Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{DD} Logic Supply Voltage Range .....-0.3V to +6V
V_{PP} - V_{NN} Supply Voltage..... +172V
V_{PP} Supply Voltage Range .....-0.3V to +12V
V_{NN} Negative Supply Voltage.....-160V
Logic Input Voltage Range (CLK, DIN, CLR) .....-0.3V to +6V
Logic Input Voltage Range
($\overline{LE}$) .....-0.3V to a minimum of (V_{PP} + 0.3V) or 6V
Logic Output Voltage Range (DOUT)..... -0.3V to (V_{DD} + 0.3V)
Analog Signal Range (SW_) .....(V_{NN} - 0.3V) to (V_{NN} + 220V)
Continuous Power Dissipation (T_A = +70°C)
LQFP (derate 22.7mW/°C above +70°C) 1818mW
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

LQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....44°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....10°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.37V to +5.5V, V_{PP} = +10V ±5%, V_{NN} = 0 to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +3.3V, V_{NN} = -100V, V_{PP} = +10V at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{DD} Logic Supply Voltage	V_{DD}		+2.37		+5.5	V
V_{NN} Supply Voltage	V_{NN}		-160		0	V
V_{PP} Supply Voltage	V_{PP}		+9.5	+10	+10.5	V
V_{DD} Static Current	I_{DDS}				4	µA
V_{DD} Dynamic Current	I_{DD}	V_{DD} = +5V, f_{CLK} = 5MHz, f_{DIN} = 2.5MHz			200	µA
V_{NN} Static Current	I_{NNS}	All switches remain on or off, SW_ = GND		10	20	µA
V_{NN} Supply Dynamic Current (All Channels Switching Simultaneously)	I_{NN}	V_{PP} = +10V, V_{NN} = -100V, $f_{TURN\_ON/OFF}$ = 50kHz, SW_ = GND		3.3	5	mA
V_{PP} Supply Static Current	I_{PPS}	All switches remain on or off, SW_ = GND		12	25	µA
V_{PP} Supply Dynamic Current (All Channels Switching Simultaneously)	I_{PP}	V_{PP} = +10V, V_{NN} = -100V, $f_{TURN\_ON/OFF}$ = 50kHz, SW_ = GND		4	6	mA
SWITCH CHARACTERISTICS						
Analog Dynamic Signal Range	$V_{SW\_}$	AC operation only, f > 500kHz	V_{NN}		V_{NN} + 210	V
Small-Signal On-Resistance	R_{ONS}	V_{PP} = +10V, V_{NN} = -100V, $V_{SW\_}$ = 0V, $I_{SW\_}$ = 5mA		18	34	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.37V to +5.5V, V_{PP} = +10V ±5%, V_{NN} = 0 to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +3.3V, V_{NN} = -100V, V_{PP} = +10V at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal On-Resistance Matching	ΔR_{ONS}	V_{PP} = +10V, V_{NN} = -100V, $I_{SW\_}$ = 5mA		3		%
Small-Signal On-Resistance Flatness	R_{ONF}	AC measured, $f_{SW\_}$ = 0.5MHz, $V_{SW\_}$ = 80V_{P-P}, R_{LOAD} = 50Ω, V_{PP} = +10V, V_{NN} = -100V		2		%
Switch Output Bleed Resistor	R_{INT}	MAX4968A only	30	40	50	kΩ
Switch-Off Leakage	$I_{SW\_(OFF)}$	$V_{SW\_}$ = 0V, switch off (MAX4968 only)		0	1	µA
Switch-Off DC Offset		No load (MAX4968A only)	-15	0	+15	mV
Switch-On DC Offset		No load (MAX4968A only)	-15	0	+15	mV
Switch Output Isolation Diode Current		300ns pulse width, 2% duty cycle		3.0		A
SWITCH DYNAMIC CHARACTERISITICS						
Turn-On Time	t_{ON}	V_{SW_A} = +1V, R_L = 100Ω, V_{NN} = -100V, from enable to V_{SW_B} = +0.9V		2	5	µs
Turn-Off Time	t_{OFF}	V_{SW_A} = +1V, R_L = 100Ω, V_{NN} = -100V, from disable to V_{SW_B} = +0.9V		2	3.5	µs
Maximum $V_{SW\_}$ Slew Rate	dV/dt	C_L = 100pF	20			V/ns
Off-Isolation	V_{ISO}	f = 5MHz, R_L = 1kΩ, C_L = 10pF, V_{NN} = -1V		-40		dB
		f = 5MHz, R_L = 1kΩ, C_L = 10pF, V_{NN} = -100V		-48		
		f = 5MHz, R_L = 50Ω		-76		
Crosstalk	V_{CT}	f = 5MHz, R_L = 50Ω		-76		dB
SW_ Off-Capacitance	$C_{SW\_(OFF)}$	f = 1MHz, small signal close to zero		9		pF
SW_ On-Capacitance	$C_{SW\_(ON)}$	f = 1MHz, small signal close to zero		13		pF
Output Voltage Spike	V_{SPK}	R_L = 50Ω		±70		mV
Large-Signal Analog Bandwidth (-3dB)	f_{BW_L}	C_{LOAD} = 200pF, 60V amplitude sinusoidal burst, 1% duty cycle		30		MHz
Small-Signal Analog Bandwidth (-3dB)	f_{BW_S}	C_{LOAD} = 200pF, 100mV amplitude sinusoidal		50		MHz
Charge Injection	Q	V_{PP} = +10V, V_{NN} = -100V, Figure 1		150		pC
LOGIC LEVELS						
Logic-Input Low Voltage	V_{IL}				0.75	V
Logic-Input High Voltage	V_{IH}		V_{DD} - 0.75			V
Logic-Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Logic-Output High Voltage	V_{OH}	I_{SOURCE} = 1mA	V_{DD} - 0.4			V
Logic-Input Capacitance	C_{IN}			5		pF
Logic-Input Leakage	I_{IN}		-1		+1	µA

16-Channel, Linear, High-Voltage Analog Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.37V to +5.5V, V_{PP} = +10V ±5%, V_{NN} = 0 to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +3.3V, V_{NN} = -100V, V_{PP} = +10V at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 2)						
CLK Frequency	f_{CLK}				25	MHz
DIN to CLK Setup Time	t_{DS}		8			ns
DIN to CLK Hold Time	t_{DH}		3			ns
CLK to $\overline{LE}$ Setup Time	t_{CS}		8			ns
$\overline{LE}$ Low Pulse Width	t_{WL}		12			ns
CLR High Pulse Width	t_{WC}		12			ns
CLK Rise and Fall Times	t_R, t_F				50	ns
CLK to DOUT Delay	t_{DO}	V_{DD} = +5V ±10%, C_{DOUT} = 15pF			28	ns
		V_{DD} = +2.5V ±5%, C_{DOUT} = 15pF			45	

Note 2: All devices are 100% tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design.

Test Circuits/Timing Diagrams

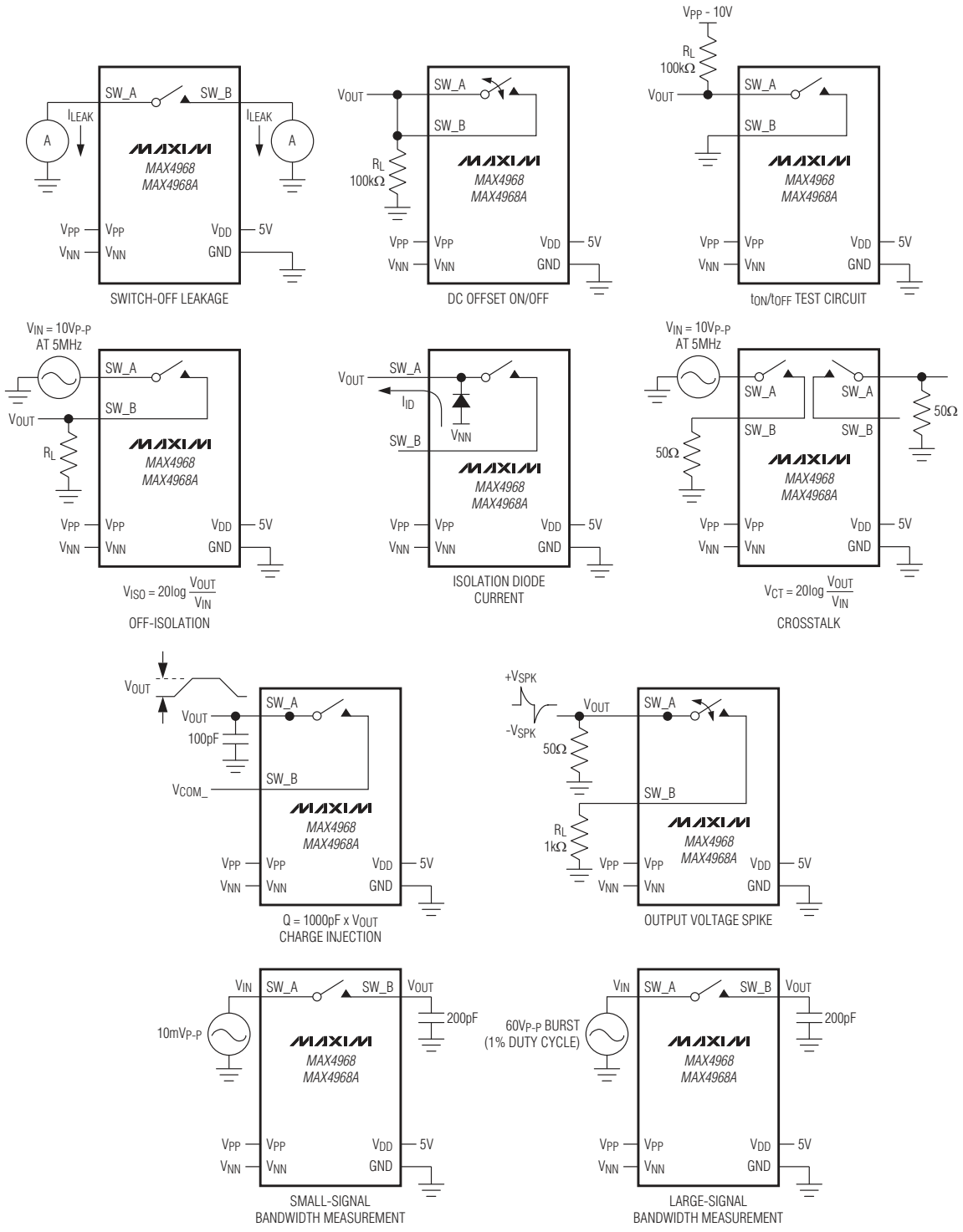


Figure 1. Test Circuits

16-Channel, Linear, High-Voltage Analog Switches

Test Circuits/Timing Diagrams (continued)

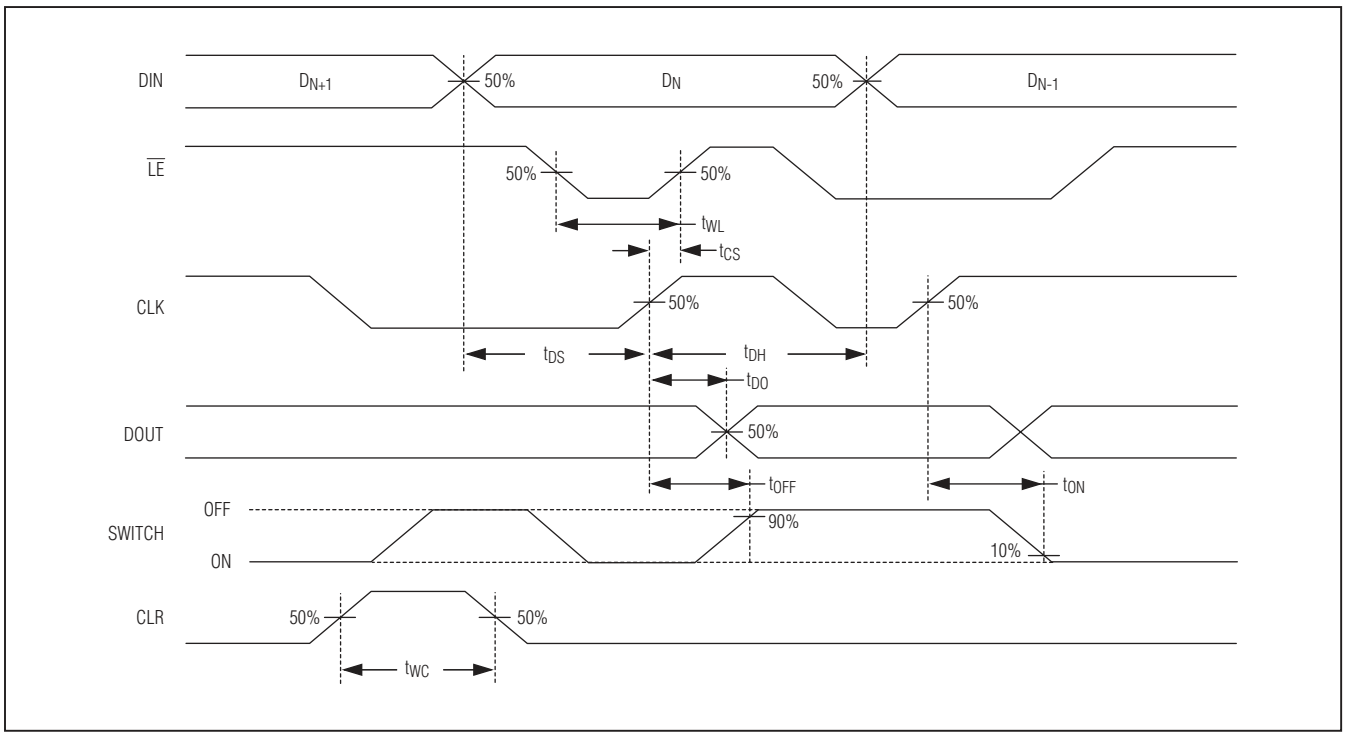


Figure 2. Serial Interface Timing

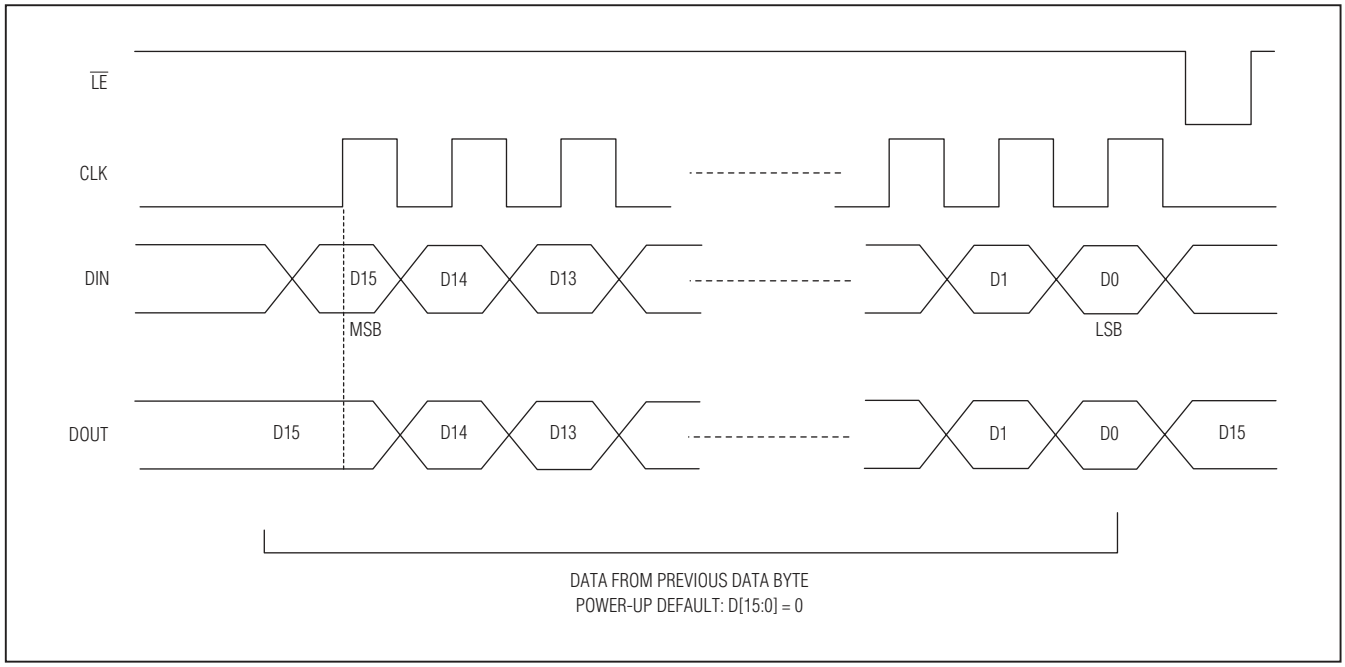
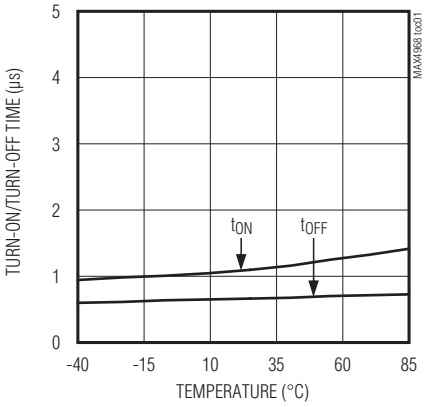


Figure 3. Latch-Enable Interface Timing

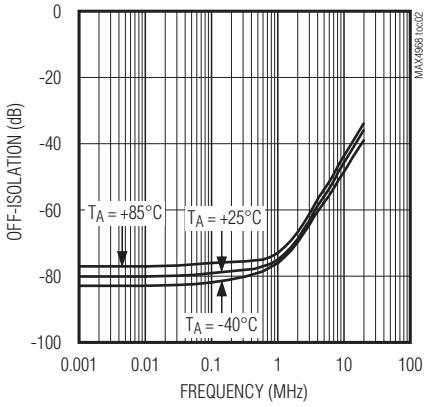
Typical Operating Characteristics

(V_{DD} = +3V, V_{PP} = +10V, V_{NN} = -100V, R_L = 100Ω, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

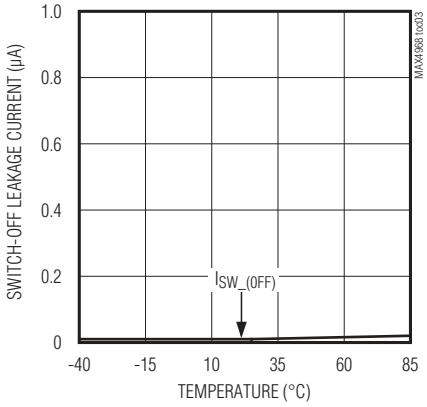
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



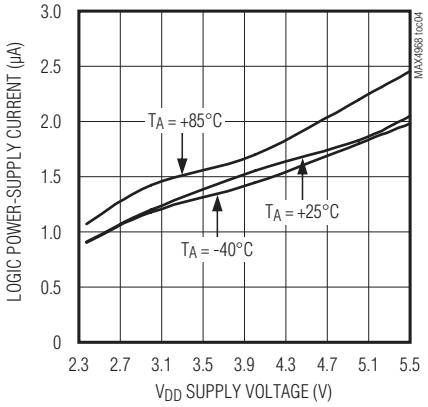
OFF-ISOLATION vs. FREQUENCY



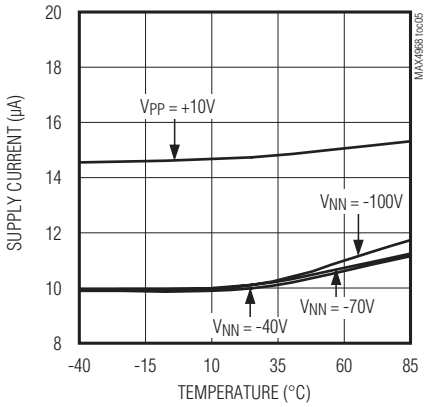
SWITCH-OFF LEAKAGE CURRENT vs. TEMPERATURE



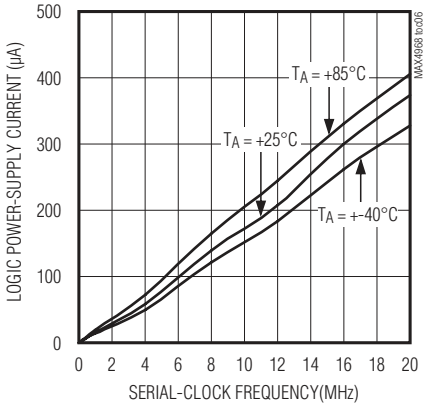
LOGIC POWER-SUPPLY CURRENT vs. SUPPLY VOLTAGE



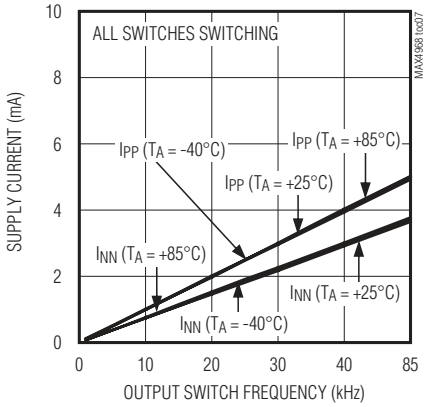
POSITIVE AND NEGATIVE POWER-SUPPLY CURRENT vs. TEMPERATURE



LOGIC POWER-SUPPLY CURRENT vs. SERIAL-CLOCK FREQUENCY

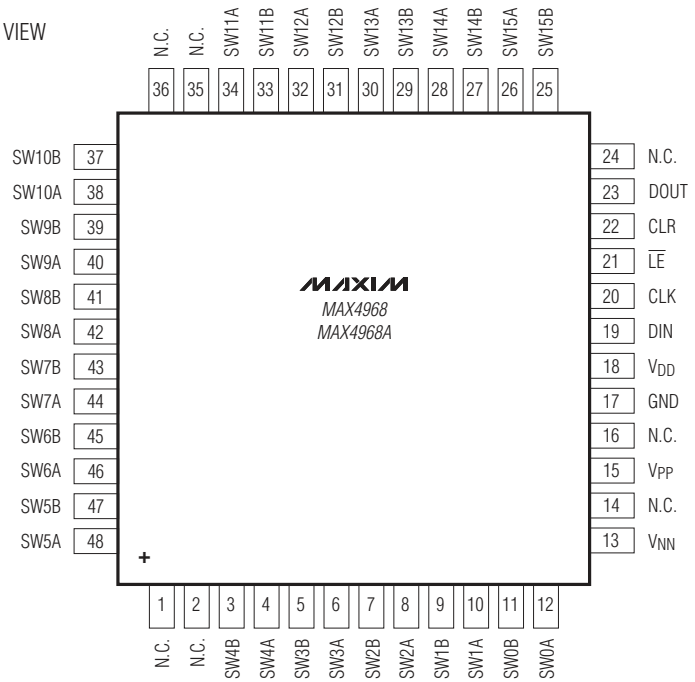


HIGH-VOLTAGE SUPPLY CURRENT vs. OUTPUT SWITCH FREQUENCY



16-Channel, Linear, High-Voltage Analog Switches

Pin Configuration



LQFP
(7mm × 7mm)

Pin Description

PIN	NAME	FUNCTION
1, 2, 14, 16, 24, 35, 36	N.C.	No Connection. Not connected internally.
3	SW4B	Analog Switch 4—Terminal
4	SW4A	Analog Switch 4—Terminal
5	SW3B	Analog Switch 3—Terminal
6	SW3A	Analog Switch 3—Terminal
7	SW2B	Analog Switch 2—Terminal
8	SW2A	Analog Switch 2—Terminal
9	SW1B	Analog Switch 1 —Terminal
10	SW1A	Analog Switch 1—Terminal
11	SW0B	Analog Switch 0—Terminal
12	SW0A	Analog Switch 0—Terminal
13	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.

PIN	NAME	FUNCTION
15	V_{PP}	Positive Voltage Supply. Bypass V_{PP} to GND with a 0.1µF or greater ceramic capacitor.
17	GND	Ground
18	V_{DD}	Logic Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
19	DIN	Serial-Data Input
20	CLK	Serial-Clock Input
21	$\overline{LE}$	Active-Low Latch-Enable Input
22	CLR	Latch-Clear Input
23	DOUT	Serial-Data Output
25	SW15B	Analog Switch 15—Terminal
26	SW15A	Analog Switch 15—Terminal
27	SW14B	Analog Switch 14—Terminal

Pin Description (continued)

PIN	NAME	FUNCTION
28	SW14A	Analog Switch 14—Terminal
29	SW13B	Analog Switch 13—Terminal
30	SW13A	Analog Switch 13—Terminal
31	SW12B	Analog Switch 12—Terminal
32	SW12A	Analog Switch 12—Terminal
33	SW11B	Analog Switch 11—Terminal
34	SW11A	Analog Switch 11—Terminal
37	SW10B	Analog Switch 10—Terminal
38	SW10A	Analog Switch 10—Terminal
39	SW9B	Analog Switch 9—Terminal
40	SW9A	Analog Switch 9—Terminal
41	SW8B	Analog Switch 8—Terminal
42	SW8A	Analog Switch 8—Terminal
43	SW7B	Analog Switch 7—Terminal
44	SW7A	Analog Switch 7—Terminal
45	SW6B	Analog Switch 6—Terminal
46	SW6A	Analog Switch 6—Terminal
47	SW5B	Analog Switch 5—Terminal
48	SW5A	Analog Switch 5—Terminal

Detailed Description

The MAX4968/MAX4968A are 16-channel, high-linearity, high-voltage, bidirectional SPST analog switches with 18Ω (typ) on-resistance. The devices are ideal for use in applications requiring high-voltage switching controlled by a low-voltage control signal, such as ultrasound imaging and printers. The MAX4968A provides integrated 40kΩ (typ) bleed resistors on each switch terminal to discharge capacitive loads. Using HVCMOS technology, these switches combine high-voltage, bilateral MOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

The MAX4968 is pin-to-pin compatible with the MAX14802 and Supertex HV2601. The MAX4968A is pin-to-pin compatible with the MAX14803 and Supertex HV2701. The only difference is the V_{PP} positive supply voltage level. The MAX4968/MAX4968A require a low +10V (typ) voltage (V_{PP}), whereas the MAX14802/MAX14803 and HV2601/HV2701 require a high +100V supply voltage.

In typical ultrasound applications, these devices do not require dedicated high-voltage supply, which implies a significant simplification of system requirement. The negative voltage supply can be shared with the transmitter and the positive voltage supply is typically +10V.

Analog Switch

The devices can transmit analog signals up to $210V_{P-P}$, with an analog signal range from V_{NN} to V_{NN} + 210V. Before starting the high-voltage burst transmission (V_{P-P} > +20V), the input voltage is required to be close to GND to allow a proper settling of the pass FET. The high-voltage burst frequency must be greater than 500kHz.

Extremely long high-voltage bursts (V_{P-P} > +10V) with duty cycle greater than 20% could result in signal degradation, especially for unipolar transmission. In general, this applies for burst transmission with a nonzero DC content.

Low-voltage signal (V_{P-P} < 10V) continuous-wave bipolar transmission is supported for frequencies greater than 500kHz. For very small signals, such as the small echoes in typical ultrasound imaging systems (V_{P-P} < 10V), the devices are not limited to a low-frequency bandwidth and can transmit DC signals.

Voltage Supplies

The devices operate with a high-voltage supply V_{NN} from -160V to 0, V_{PP} supply of +10V (typ), and a logic supply V_{DD} (+2.37V to +5.5V).

16-Channel, Linear, High-Voltage Analog Switches

Bleed Resistors (MAX4968A)

The MAX4968A features integrated 40kΩ (typ) bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog switch terminal is connected to GND with a bleed resistor.

Serial Interface

The MAX4968/MAX4968A are controlled by a serial interface with a 16-bit serial shift register and transparent latch. Each of the 16 data bits controls a single analog switch (see Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by 16 clock cycles (see Figures 2 and 3).

Latch Enable ($\overline{LE}$)

Drive $\overline{LE}$ logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 3). Drive $\overline{LE}$ logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive $\overline{LE}$ logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse $\overline{LE}$ logic-low to load the contents of the shift register into the latch.

Latch Clear (CLR)

The MAX4968/MAX4968A feature a latch-clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches. CLR does not affect the contents of the data shift register. Pulse $\overline{LE}$ logic-low to reload the contents of the shift register into the latch.

Power-On Reset

The MAX4968/MAX4968A feature a power-on-reset circuit to ensure all switches are open at power-on. The internal 16-bit serial shift register and latch are set to zero on power-up.

Table 1. Serial Interface Programming (Notes 1–6)

DATA BITS								CONTROL BITS		FUNCTION							
D0 (LSB)	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	Off	Off	Off	Off	Off	Off	Off	Off

Table 1. Serial Interface Programming (Notes 1–6) (continued)

DATA BITS								CONTROL BITS		FUNCTION							
D8	D9	D10	D11	D12	D13	D14	D15 (MSB)	$\overline{LE}$	CLR	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	Off	Off	Off	Off	Off	Off	Off	Off

Note 1: The 16 switches operate independently.
Note 2: Serial data is clocked in on the rising edge of CLK.
Note 3: The switches go to a state retaining their present condition on the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift register data flows through the latch.
Note 4: DOUT is high when switch 15 is on.
Note 5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
Note 6: The CLR input overrides all other inputs.

Applications Information

In typical ultrasound applications, the MAX4968/MAX4968A do not require dedicated high-voltage supplies; the negative voltage supply can be shared with the transmitter and the positive voltage supply is typically +10V. See Figures 5, 6, and 7 for medical ultrasound applications.

Logic Levels

The MAX4968/MAX4968A digital interface inputs CLK, DIN, $\overline{LE}$, and CLR operate on the V_{DD} logic supply voltage.

Daisy-Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple MAX4968/MAX4968A devices by daisy-chaining (Figure 4). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, $\overline{LE}$, and CLR inputs of all devices, and drive $\overline{LE}$ logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Additional shift registers can be included anywhere in series with the MAX4968/MAX4968A daisy-chain.

Supply Sequencing and Bypassing

The MAX4968/MAX4968A do not require special sequencing of the V_{DD}, V_{PP}, and V_{NN} supply voltages. Bypass V_{DD}, V_{PP}, and V_{NN} to GND with a 0.1µF ceramic capacitor as close as possible to the device.

Note: Keep $\overline{LE}$ low during power-up.

16-Channel, Linear, High-Voltage Analog Switches

Application Diagrams

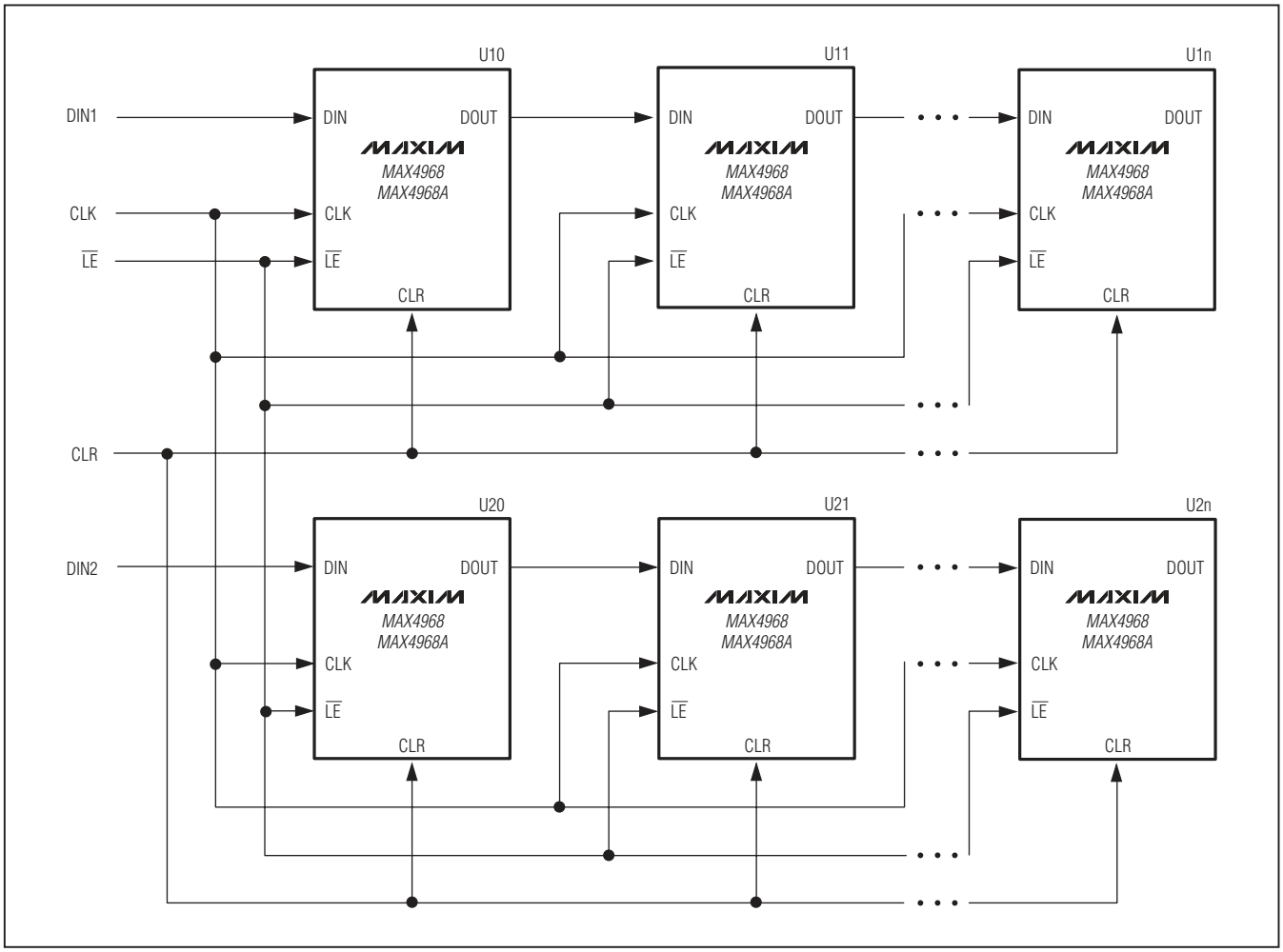


Figure 4. Interfacing Multiple Devices by Daisy-Chaining

Application Diagrams (continued)

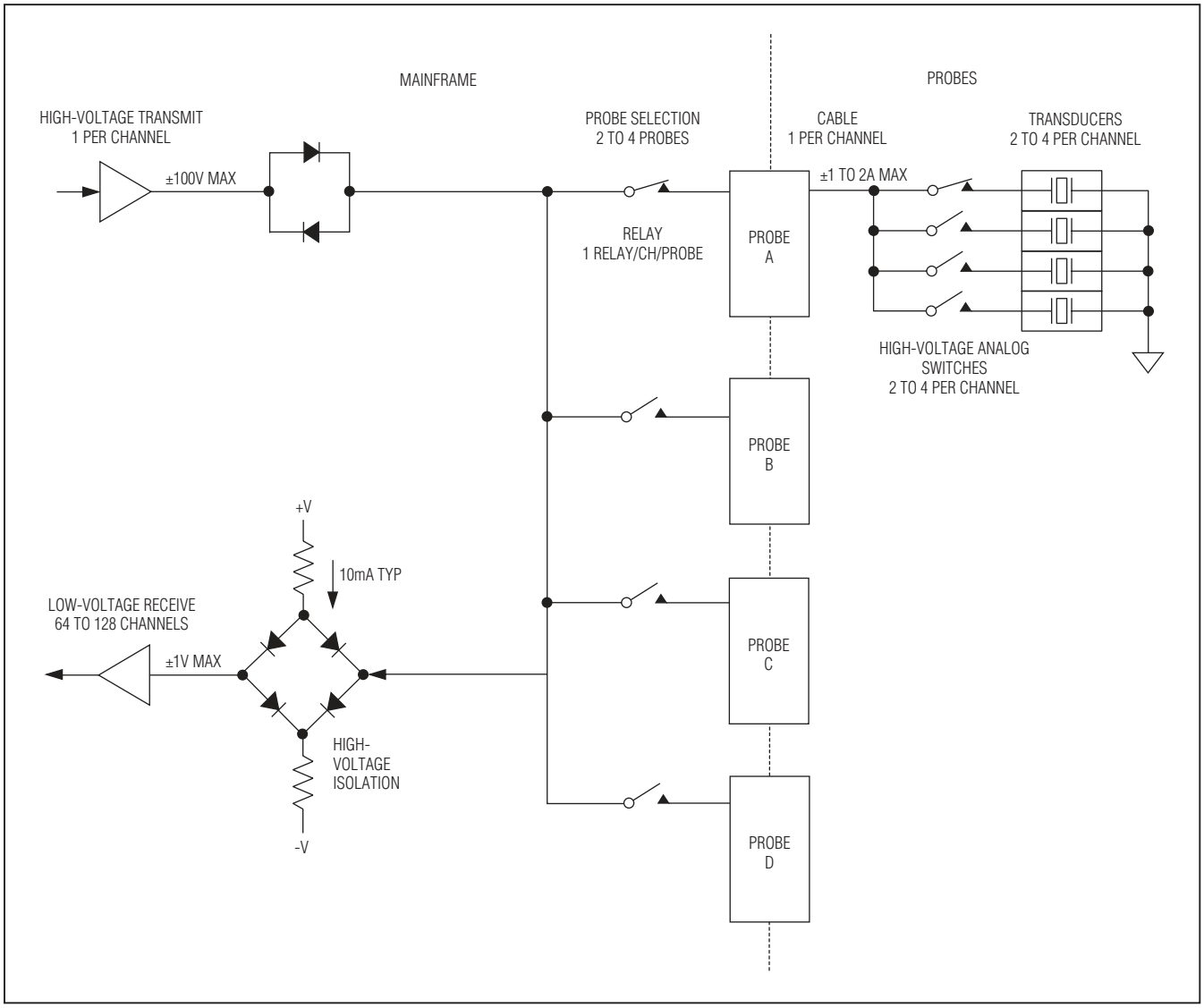


Figure 5. Medical Ultrasound Application—High-Voltage Analog Switches in Probe

16-Channel, Linear, High-Voltage Analog Switches

Application Diagrams (continued)

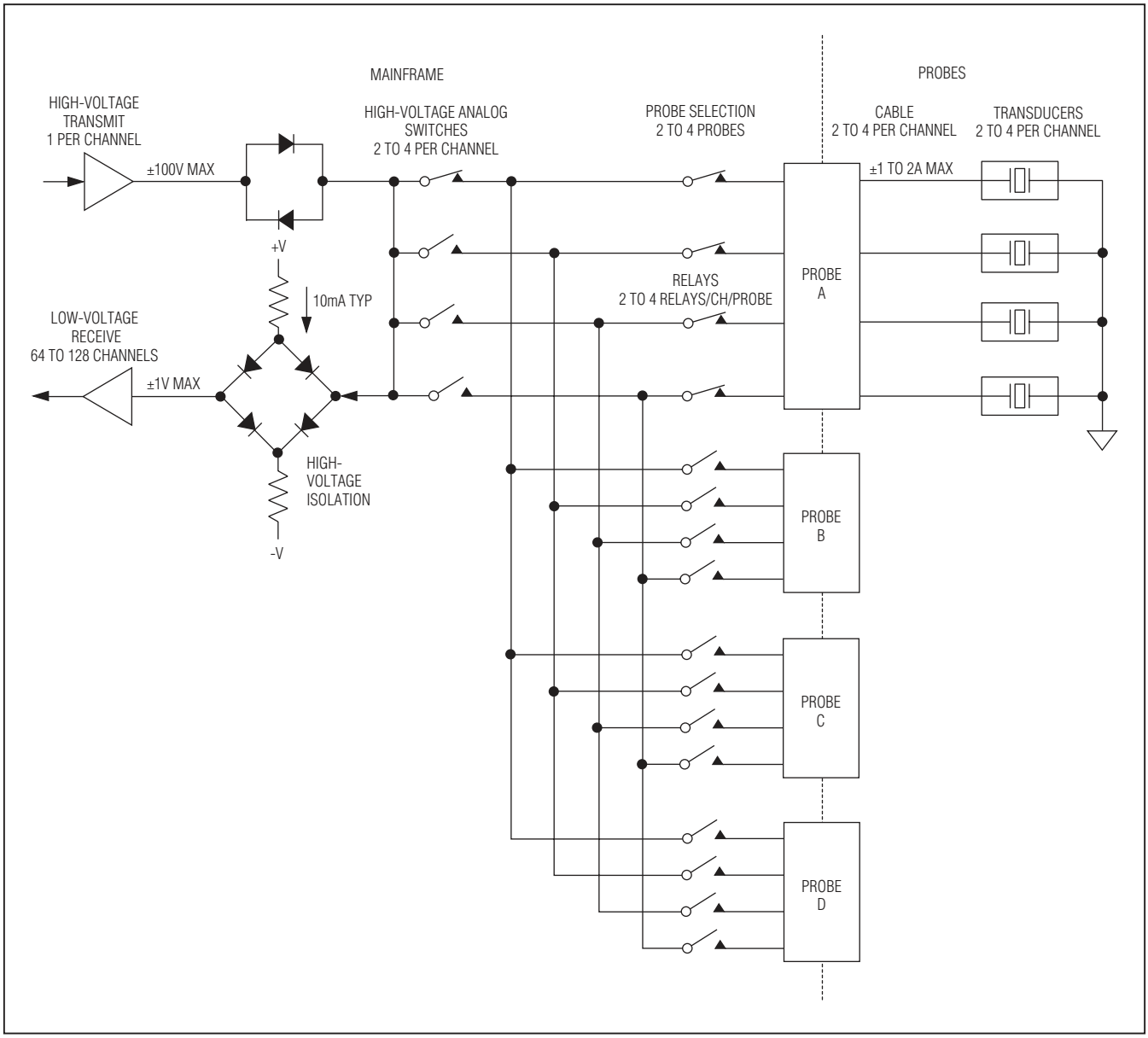


Figure 6. Medical Ultrasound Application—High-Voltage Analog Switches in Mainframe

Application Diagrams (continued)

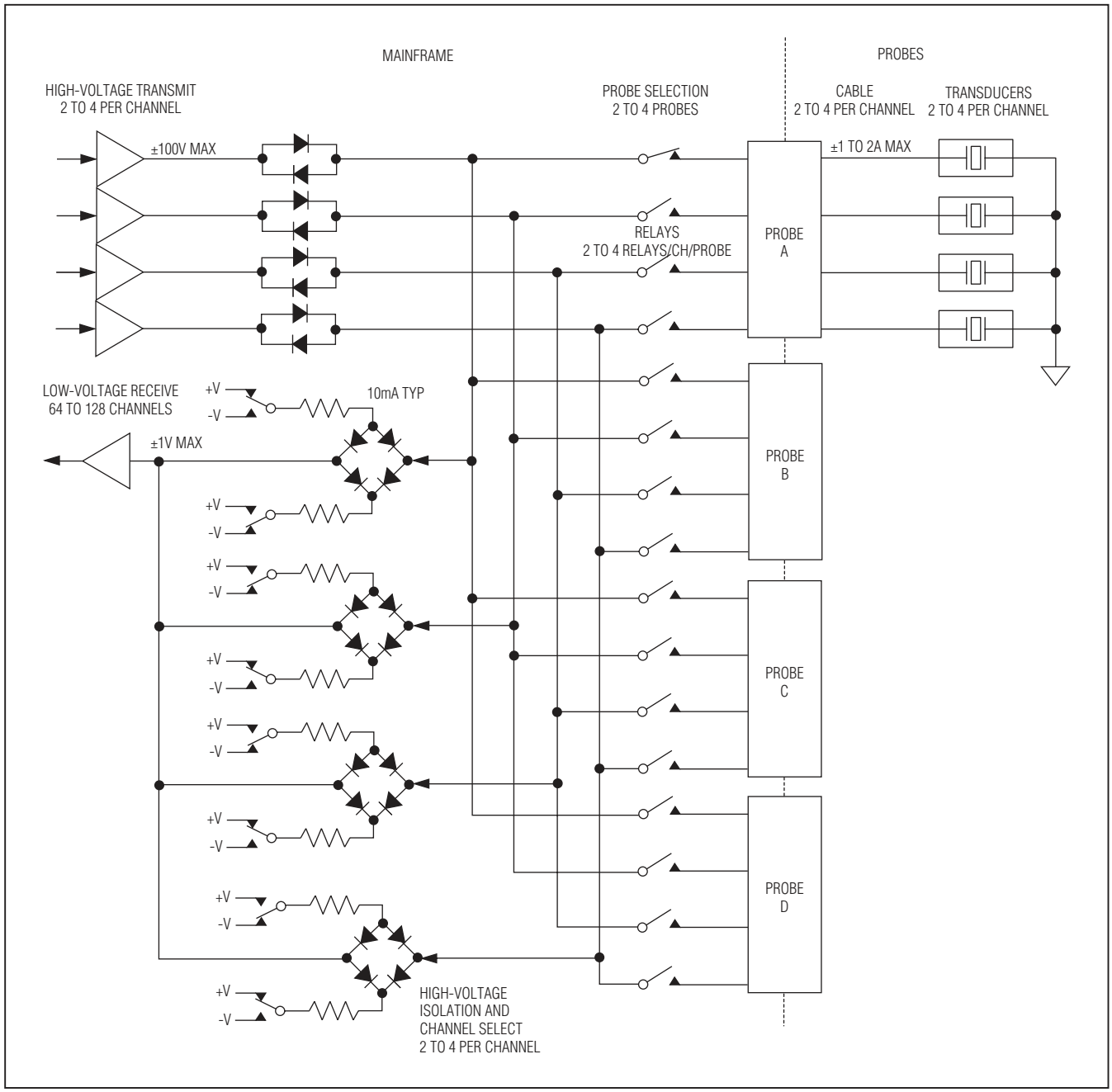
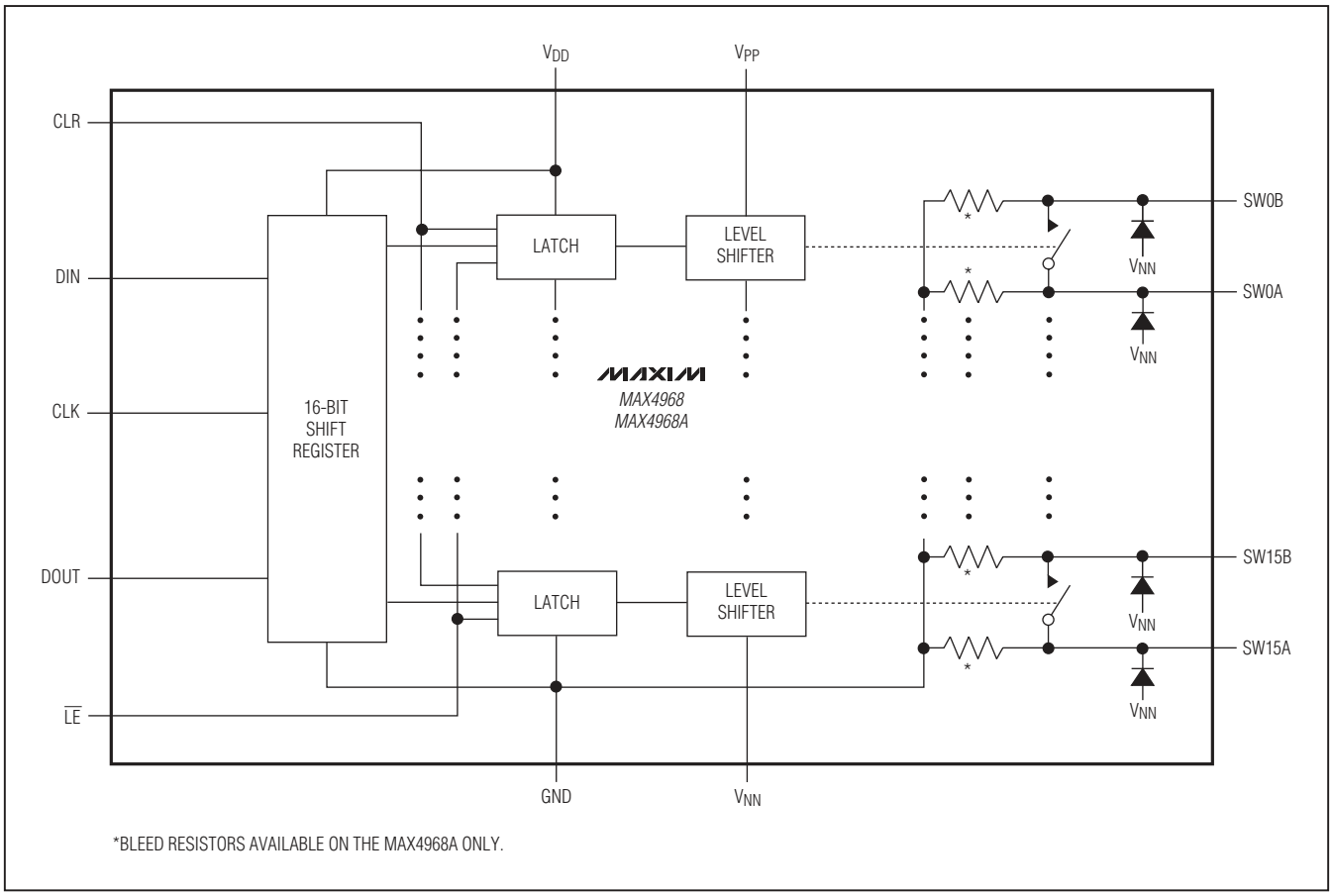


Figure 7. Medical Ultrasound Application—Multiple Transmit and Isolation per Receiver Channel

16-Channel, Linear, High-Voltage Analog Switches

Functional Diagram



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 LQFP	C48+6	21-0054	90-0093

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—