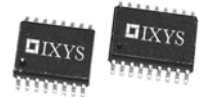


# IX6R11

## 600 Volt, 6 Ampere High & Low-side Driver for N-Channel MOSFETs and IGBTs



### Features

- Floating High Side Driver with boot-strap Power supply along with a Low Side Driver.
- Fully operational to 600V
- $\pm 50\text{V/ns}$   $dV/dt$  immunity
- Gate drive power supply range: 10 - 35V
- Undervoltage lockout for both output drivers
- Separate Logic power supply range: 3.3V to  $V_{CL}$
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected over entire operating range
- High peak output current: 6A
- Low output impedance
- Low power supply current
- Immune to negative voltage transients

### Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

### General Description

The IX6R11 Bridge Driver for N-channel MOSFETs and IGBTs with a high side and low side output, whose input signals reference the low side. The High Side driver can control a MOSFET or IGBT connected to a positive bus voltage up to 600V. The logic input stages are compatible with TTL or CMOS, have built-in hysteresis and are fully immune to latch up over the entire operating range. The IX6R11 can withstand  $dV/dt$  on the output side up to  $\pm 50\text{V/ns}$ .

### Ordering Information

The IX6R11 is available in the 14-Pin DIP, the 16-Pin SOIC, and the heat-sinkable 18-Pin SOIC Cooltab™ packages.

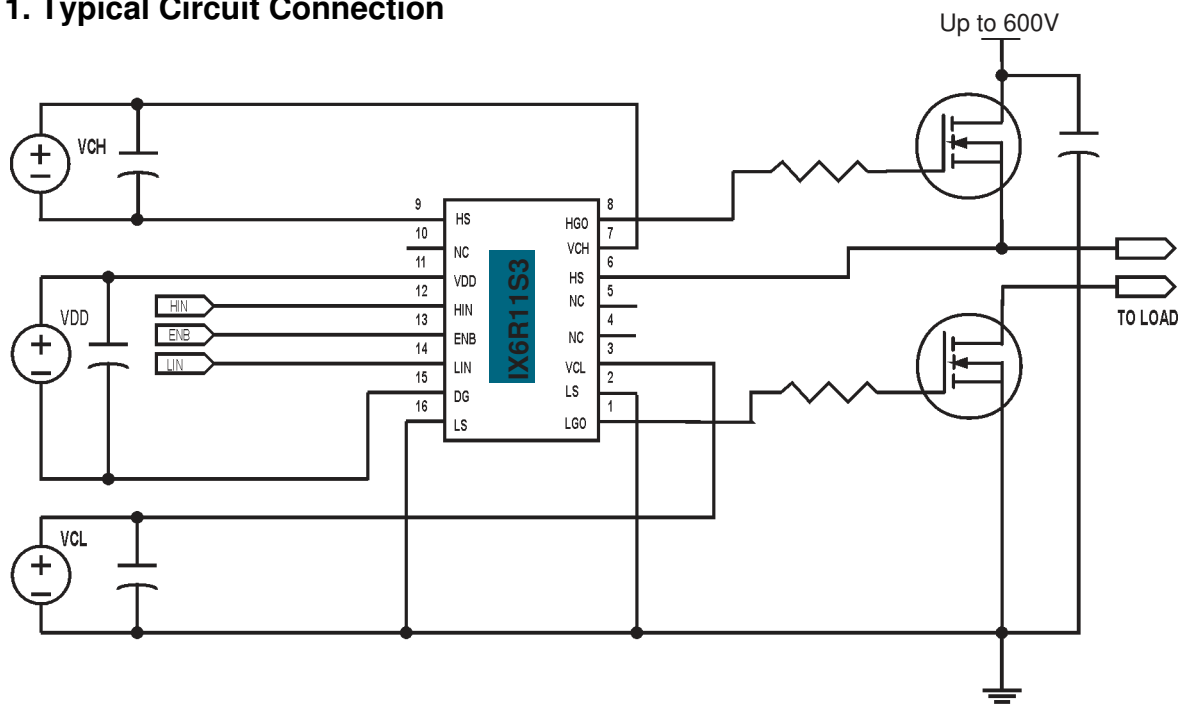
Part Number	Package Type
IX6R11P7	14-Pin DIP
IX6R11S3	16-Pin SOIC
IX6R11S6	18-Pin SOIC

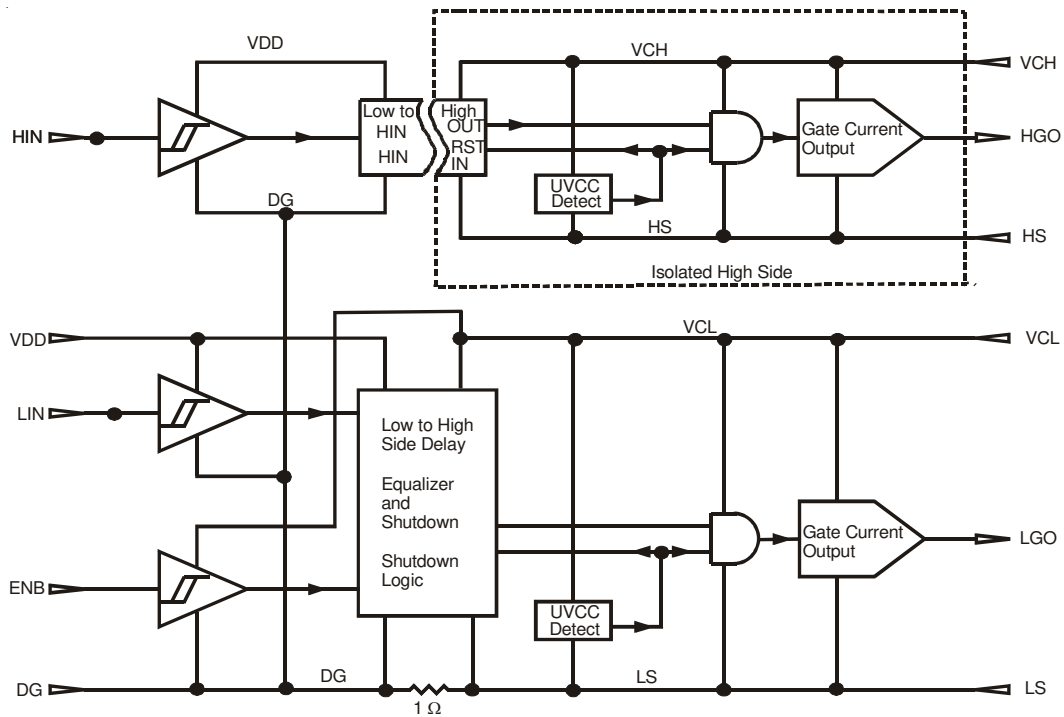
**Warning: The IX6R11 is ESD Sensitive**

Precaution: when performing the High-Voltage tests, adequate safety precautions should be taken!

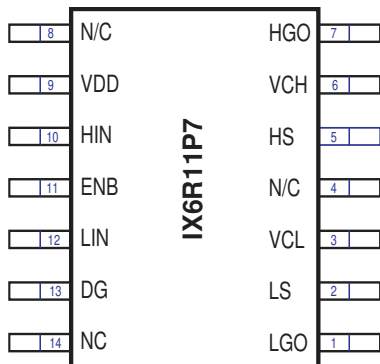
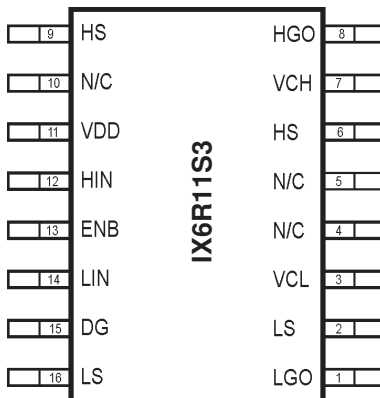
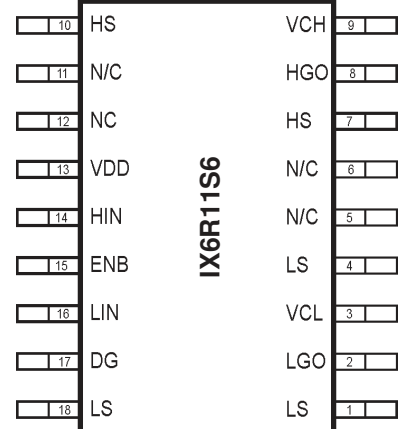
\*Operational voltage rating of 600V determined in a typical half-bridge circuit configuration (refer to Figure 10 and Figure 11).  
Operational voltage in other circuit configurations may vary.

**Figure 1. Typical Circuit Connection**



**Figure 2 - IX6R11 Functional Block Diagram**

**Pin Description and Configuration**

SYMBOL	FUNCTION	DESCRIPTION
VDD	Logic Supply	Positive power supply for chip CMOS functions
HIN	HS Input	High side input signal, TTL or CMOS compatible; HGO in phase
LIN	LS Input	Low side input signal, TTL or CMOS compatible; LGO in phase
ENB	Enable	Chip enable, active low. When driven high, both outputs go low
DG	Ground	Logic reference ground
VCH	Supply Voltage	High side power supply, referenced to HS
HGO	Output	High side driver output
HS	Return	High side voltage return pin
VCL	Supply Voltage	Low side power supply, referenced to LS
LGO	Output	Low side driver output
LS	Ground	Low side voltage return pin

**14-PIN DIP**

**16-PIN SOIC**

**18-PIN SOIC w/Cooltab™**


**Absolute Maximum Ratings**

Symbol	Definition	Min	Max	Units
$V_{CH}$	High side floating supply voltage	-0.3	+35	V
$V_{HS}$	High side floating supply offset Voltage	-200	+600	V
$V_{HGO}$	High side floating output voltage	$V_{HS}-0.3$	$V_{CH}+0.3$	V
$V_{CL}$	Low side fixed supply voltage	-0.3	35	V
$V_{LGO}$	Low side output voltage	-0.3	$V_{CL}+0.3$	V
$V_{DD}$	Logic supply voltage	-0.3	$V_{CL}+0.3$	V
$V_{DG}$	Logic supply offset voltage	$V_{LS}-3.8$	$V_{LS}+3.8$	V
$V_{IN}$	Logic input voltage(HIN & LIN)	$V_{LS}-0.3$	$V_{CL}+0.3$	V
$dV_S/dt$	Allowable offset supply voltage transient		50	V/ns
$P_D$	Package power dissipation@ $T_A \leq 25C$		1.25	W
$P_D$	Package power dissipation@ $T_C \leq 25C$		2.5	W
$R_{THJA}$	Thermal resistance, junction-to-ambient		100	K/W

**Recommended Operating Conditions**

Symbol	Definition	Min	Max	Units
$V_{CH}$	High side floating supply absolute voltage	$V_{HS}+10$	$V_{HS}+20$	V
$V_{HS}$	High side floating supply offset voltage	-20	+600	V
$V_{HGO}$	High side floating output voltage	$V_{HS}$	$V_{CH}+20$	V
$V_{CL}$	Low side fixed supply voltage	10	20	V
$V_{LGO}$	Low side output voltage	0	$V_{CC}$	V
$V_{DD}$	Logic supply voltage	$V_{DG}+3$	$V_{DG}+V_{CL}$	V
$V_{DG}$	Logic supply offset voltage	$V_{LS}-0.5$	$V_{LS}+0.5$	V
$V_{IN}$	Logic input voltage(HIN, LIN, ENbar)	$V_{DG}$	$V_{DD}$	V
$T_A$	Ambient Temperature	-40	125	°C

**Dynamic Electrical Characteristics\***

$V_{CL} = V_{CH} = V_{DD} = +15V$ ,  $C_{load} = 5nF$ , and  $V_{DG} = V_{LS}$  unless otherwise specified. The dynamic electrical characteristics are measured using Figure 7.

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
$t_{on}$	Turn-on propagation delay	$V_{HS} = 0V$		120	160	ns
$t_{off}$	Turn-off propagation delay	$V_{HS} = 600V$		94	125	ns
$t_{enb}$	Device not enable delay			110	140	ns
$t_r$	Turn-on rise time			25	35	ns
$t_f$	Turn-off fall time			17	25	ns
$t_{dm}$	Delay matching, HS & LS turn-on/off			25	50	ns

**Static Electrical Characteristics**

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
$V_{INH}$	Logic "1" input voltage, HIN, LIN, ENB	$V_{DD} = V_{CL} = 15V$	9.5			V
$V_{INL}$	Logic "0" input voltage, HIN, LIN, ENB	$V_{DD} = V_{CL} = 15V$	0		6	V
$V_{HLGO} / V_{HHGO}$	High level output voltage, $V_{CH} - V_{HGO}$ or $V_{CL} - V_{LGO}$	$I_O = 0A$			0.1	V
$V_{LLGO} / V_{LHGO}$	Low level output voltage, $V_{HGO}$ or $V_{LGO}$	$I_O = 0A$			0.1	V
$I_{HL}$	HS to LS bias current.	$V_{HS} = V_{CH} = 600V$		170		$\mu A$
$I_{QHS}$	Quiescent $V_{CH}$ supply current	$V_{IN} = 0V$ or $V_{DD} = 15V$		1	3	mA
$I_{QLS}$	Quiescent $V_{CL}$ supply current	$V_{IN} = 0V$ or $V_{DD} = 15V$		1	3	mA
$I_{QDD}$	Quiescent $V_{DD}$ supply current	$V_{IN} = 0V$ or $V_{DD} = 15V$		15	30	$\mu A$
$I_{IN+}$	Logic "1" input bias current	$V_{IN} = V_{DD}$		20	40	$\mu A$
$I_{IN-}$	Logic "0" input voltage	$V_{IN} = 0V$			1	$\mu A$
$V_{CHUV+}$	$V_{CH}$ supply undervoltage positive going threshold.		7.5	8.6	9.7	V
$V_{CHUV-}$	$V_{CH}$ supply undervoltage negative going threshold.		7	8.2	9.4	V
$V_{CLUV+}$	$V_{CL}$ supply undervoltage positive going threshold		7.4	8.5	9.6	V
$V_{CLUV-}$	$V_{CL}$ supply undervoltage negative going threshold.		7	8.2	9.4	V
$I_{GO+}$	HS or LS Output high short circuit current; $V_{GO} = 15V$ , $V_{IN} = 15V$ , $PW < 10\mu s$		4	6		A
$I_{GO-}$	HS or LS Output low short circuit current; $V_{GO} = 0V$ , $V_{IN} = 0V$ , $PW < 10\mu s$			-7	-5	A

\* These characteristics are guaranteed by design only. Tested on a sample basis.

IXYS reserves the right to change limits, test conditions, and dimensions.

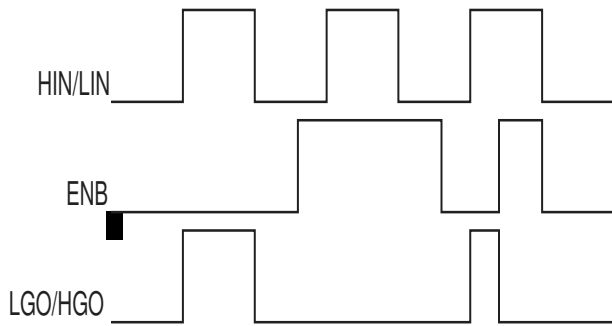


Figure 3. INPUT/OUPUT Timing Diagram

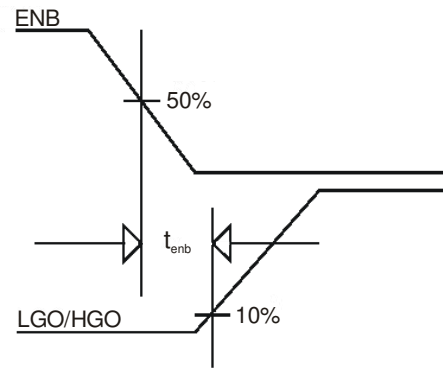


Figure 4. ENABLE Waveform Definitions

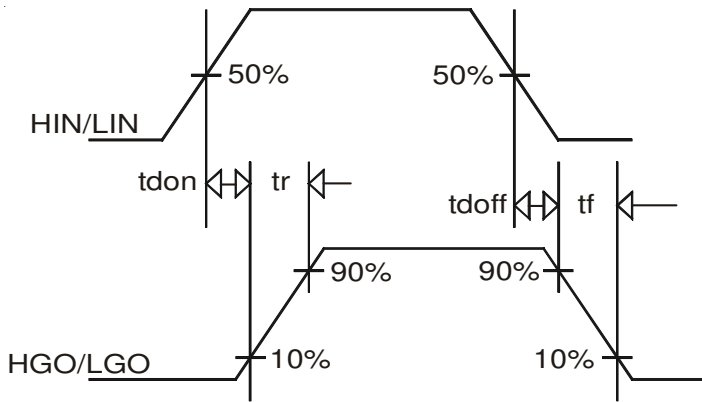


Figure 5. Definitions of Switching Time Waveforms

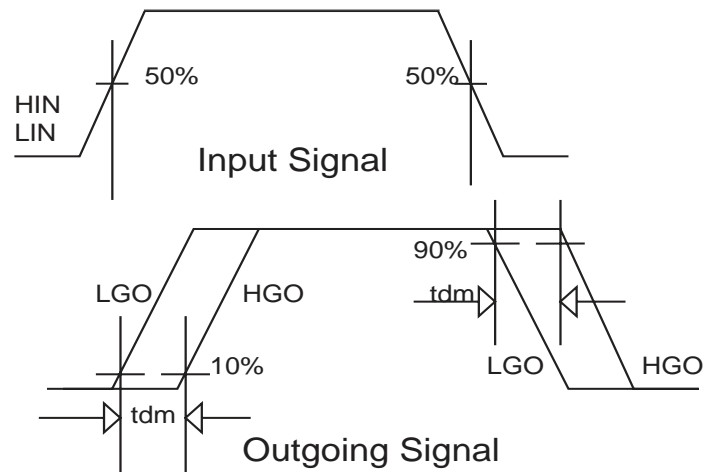


Figure 6. Definitions of Delay Matching Waveforms

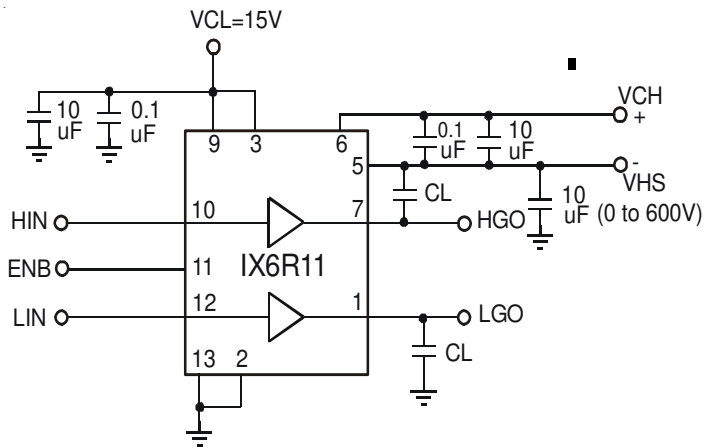


Figure 7. Switching Time Test Circuit

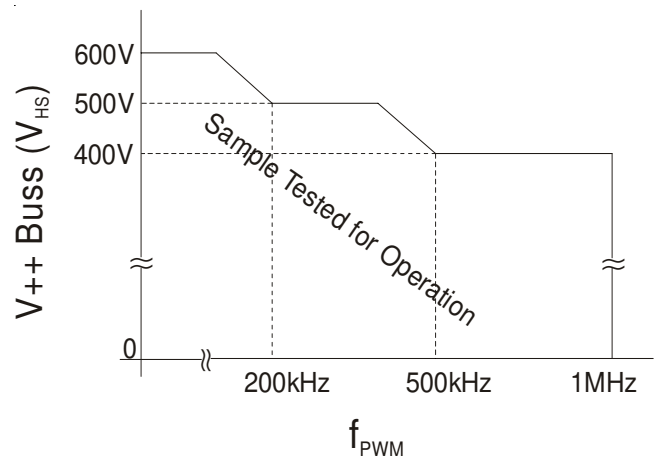


Figure 8. Device operating range: Buss voltage vs. Frequency Tested in typical circuit configuration (refer to Figure 10 & 11)

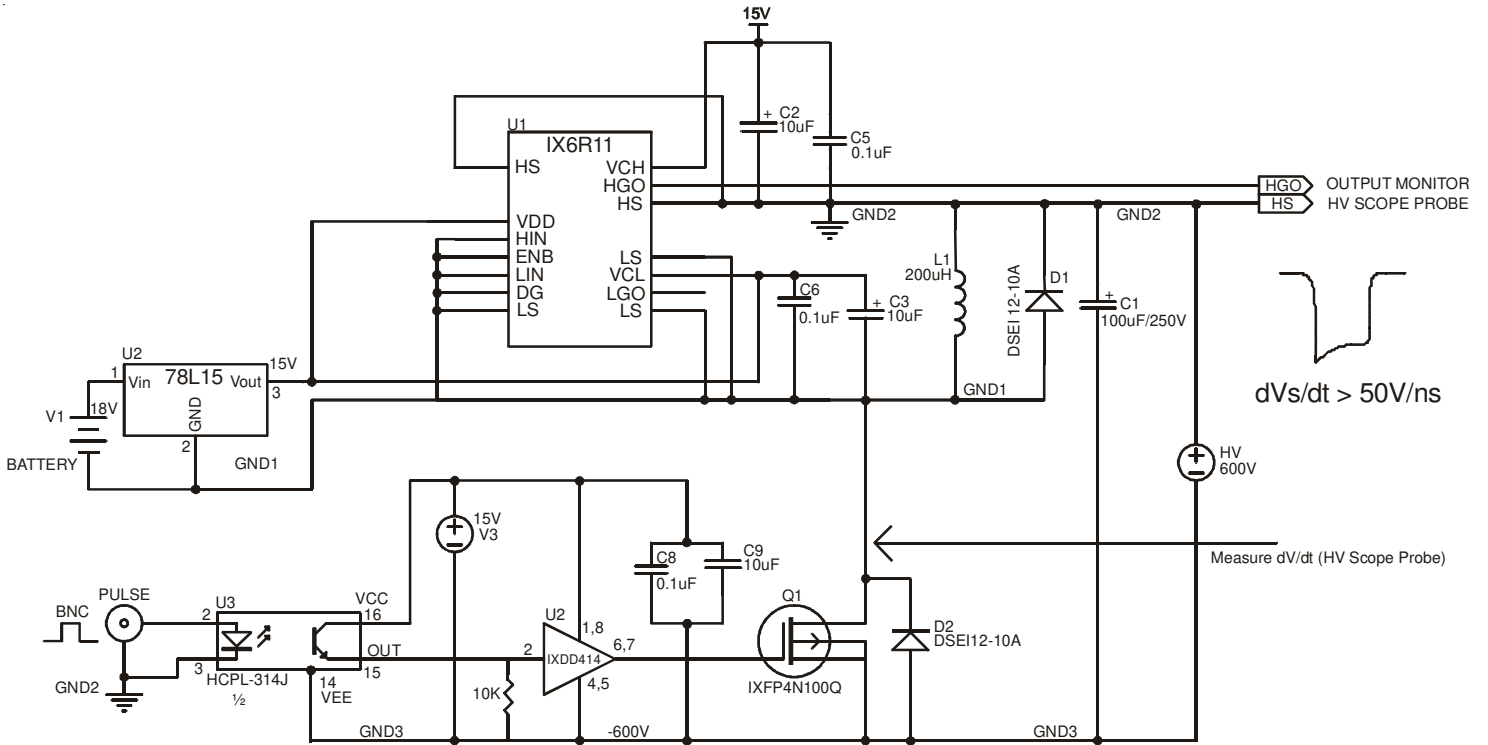


Figure 9. Test circuit for allowable offset supply voltage transient.

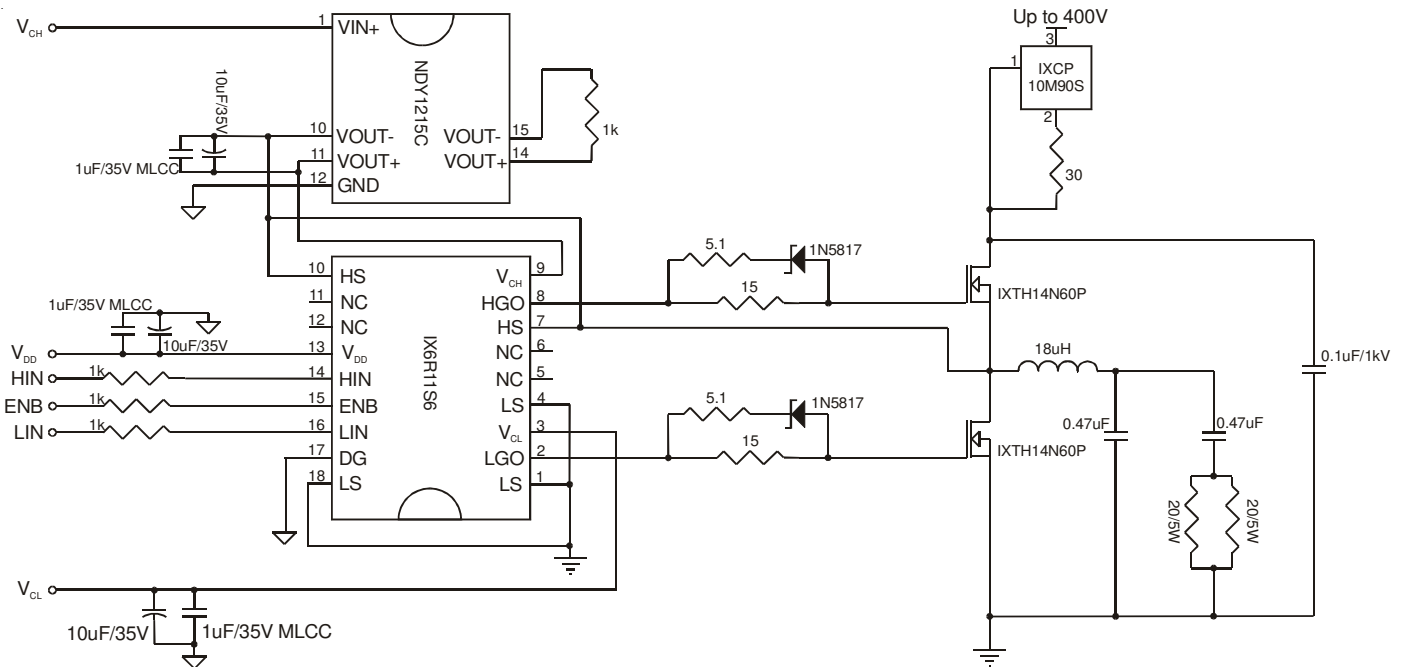


Figure 10. Test circuit for high frequency, 750kHz, operation.

$$V_{DD}, V_{CH}, V_{CL} = 15V$$

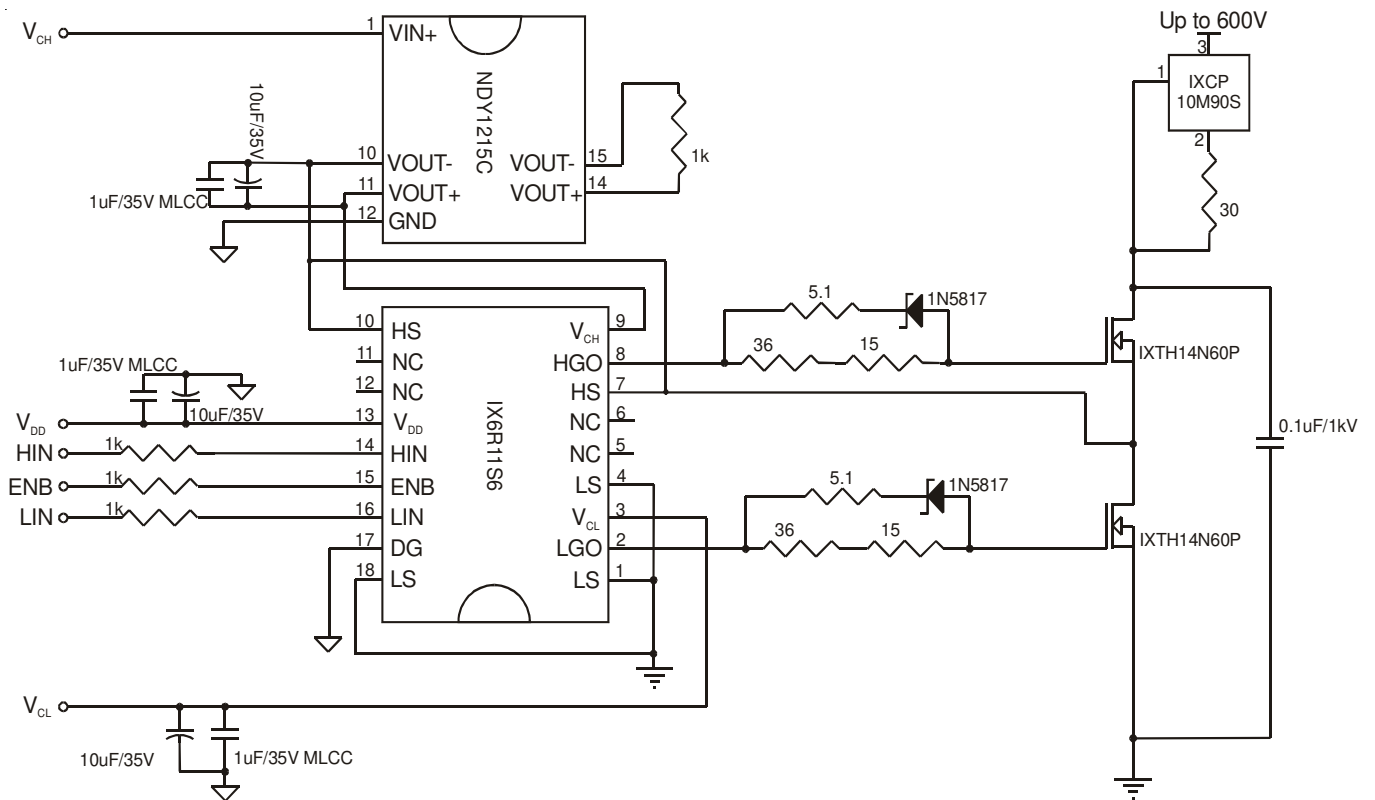


Figure 11. Test circuit for low frequency, 75kHz, operation.

$$V_{DD}, V_{CH}, V_{CL} = 15V$$

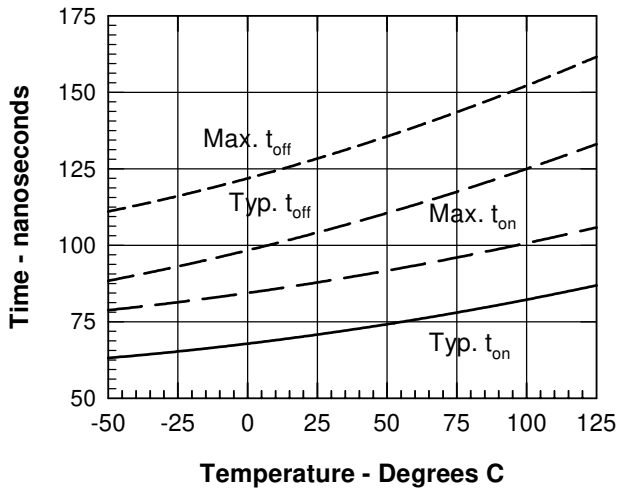


Fig. 12a. Low side turn-on and turn-off delay times vs. temperature.

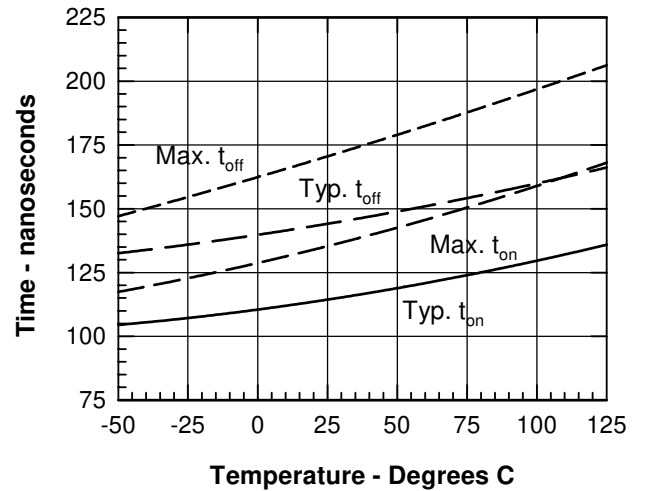


Fig. 12b. High side turn-on and turn-off times vs. temperature.

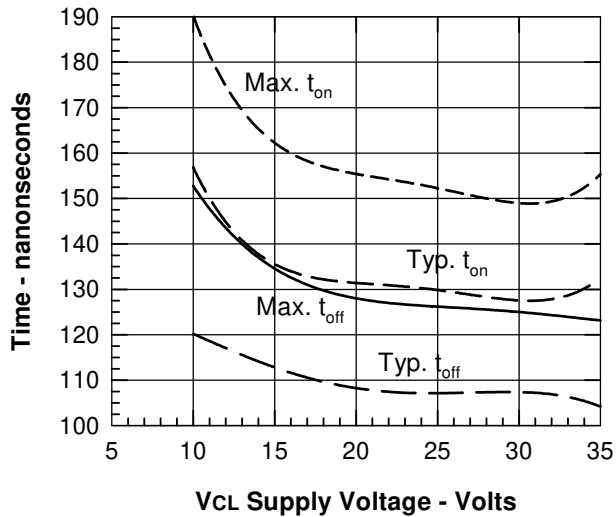


Fig. 13a. Low side turn-on and turn-off delay times vs.  $V_{CL}$ .

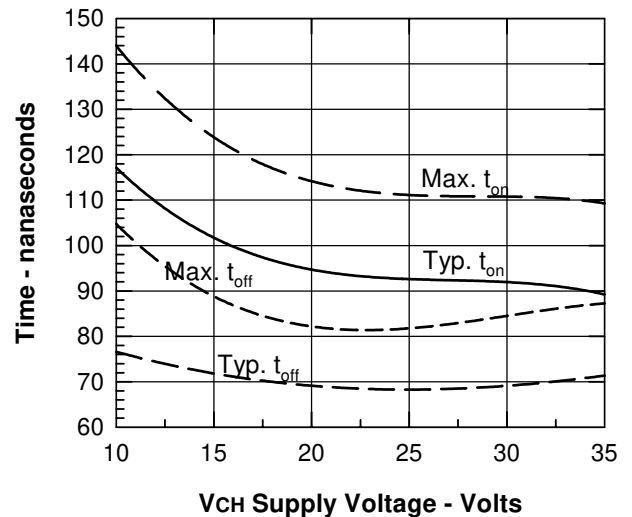


Fig. 13b. High side turn-on and turn-off delay times vs.  $V_{CH}$ .

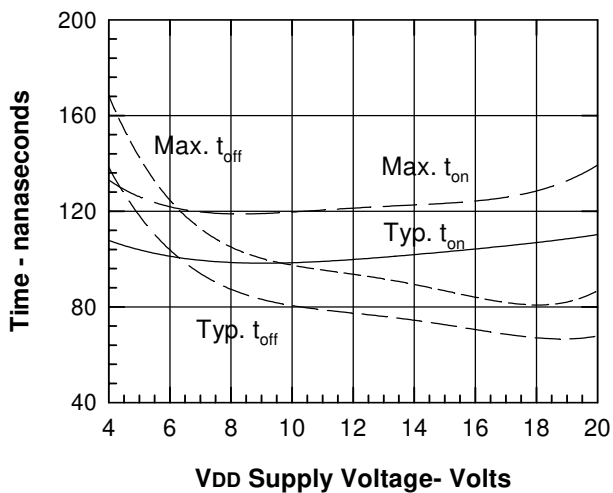


Fig. 14a. Low side turn-on and turn-off delay times vs.  $V_{DD}$  supply voltage.

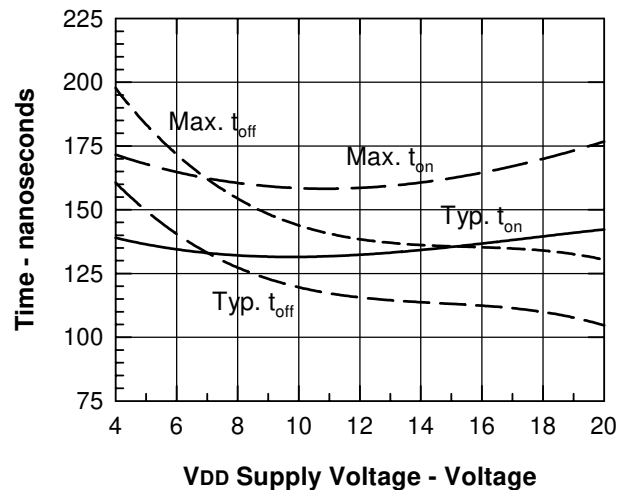


Fig. 14b. High side turn-on and turn-off delay times vs.  $V_{DD}$ .



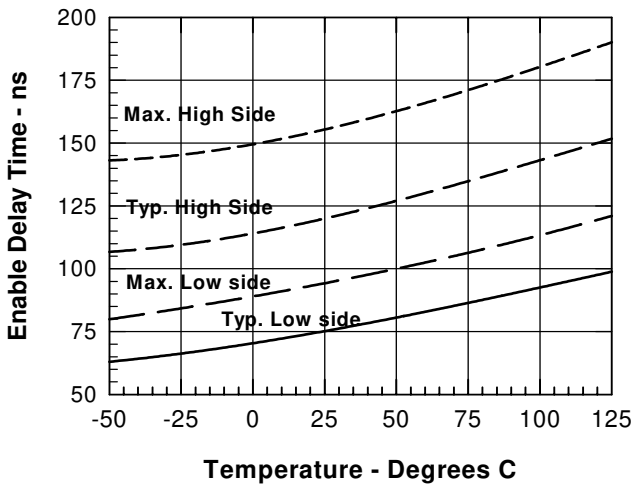


Fig. 15a. High and Low side ENABLE (Shutdown) times vs. temperature.

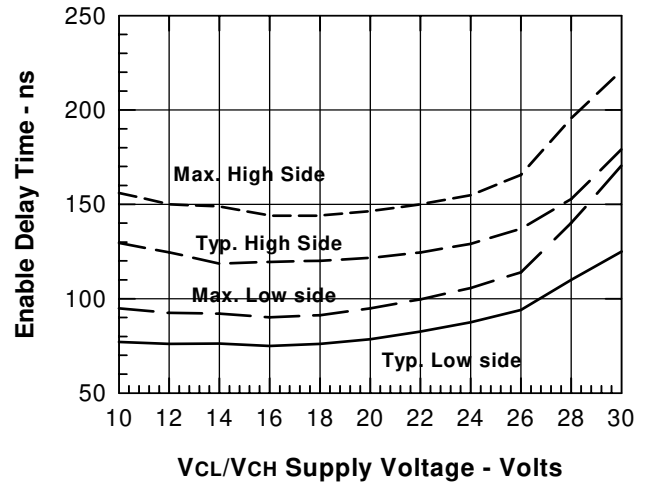


Fig. 15b. High and Low side ENABLE (Shutdown) times vs. supply voltage.

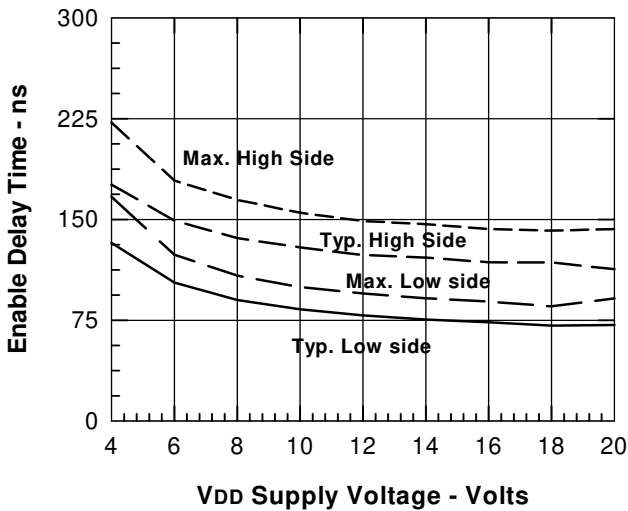


Fig. 15c. High and Low side ENABLE (Shutdown) times vs. supply voltage.

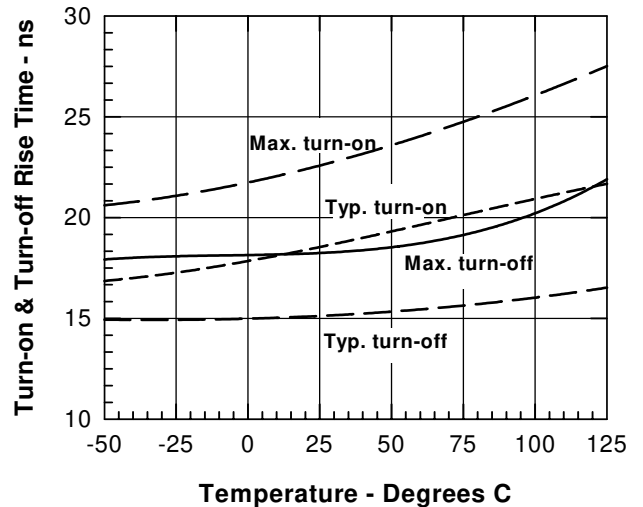


Fig. 16a. Turn-on and turn-off rise times vs. temperature.

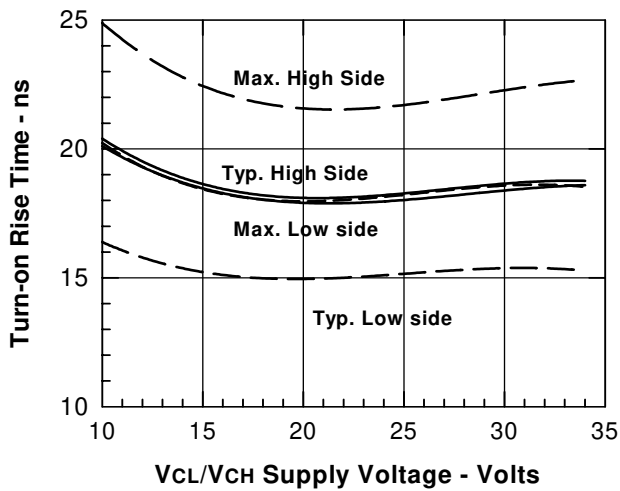


Fig. 16b. Turn-on rise times vs. bias supply voltages.

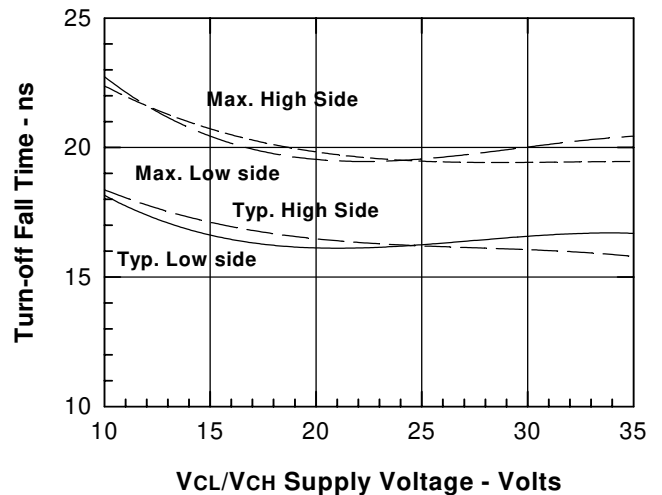


Fig. 16c. Turn-off delay times vs. bias supply voltages.

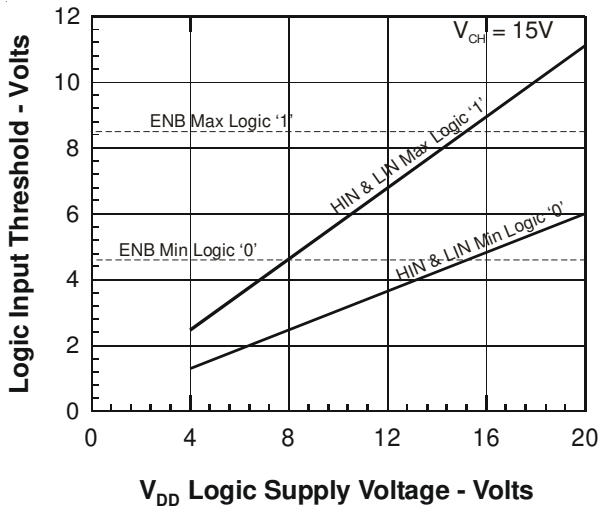


Fig. 17. Logic input threshold voltage vs bias supply voltage.

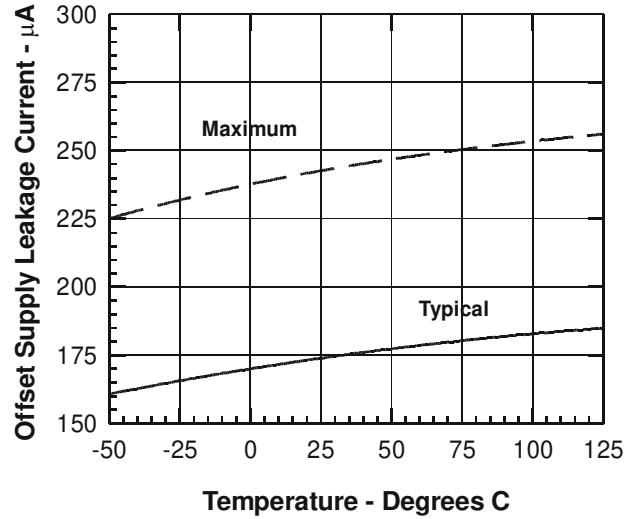


Fig. 18. Offset supply leakage current vs. temperature.

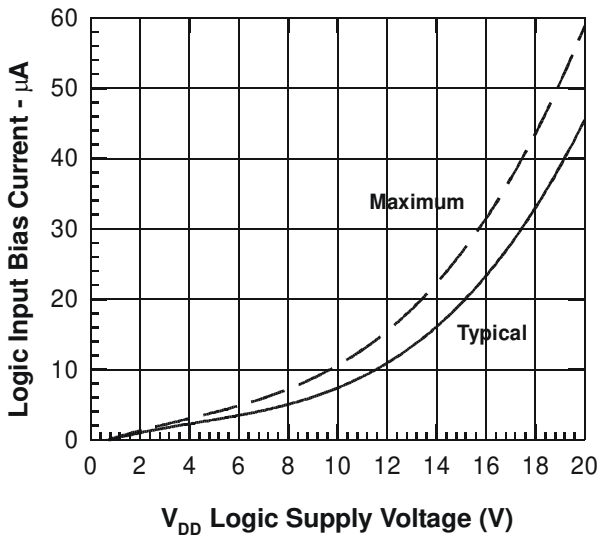


Fig. 19. Logic input current vs. bias voltage.

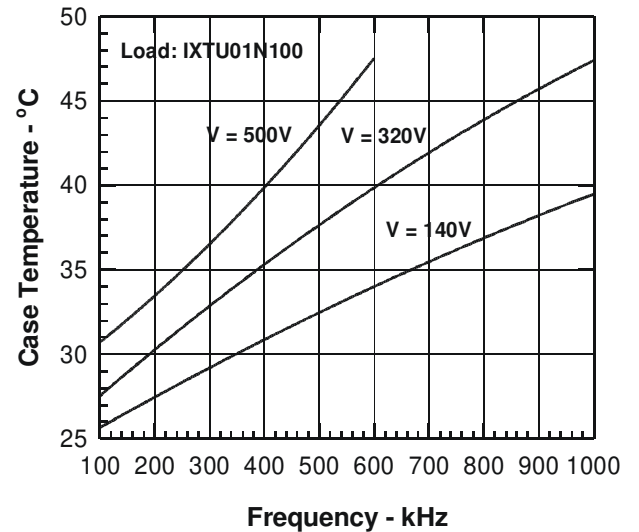


Fig. 20. IX6R11S3 Case temperature rise vs. operating frequency

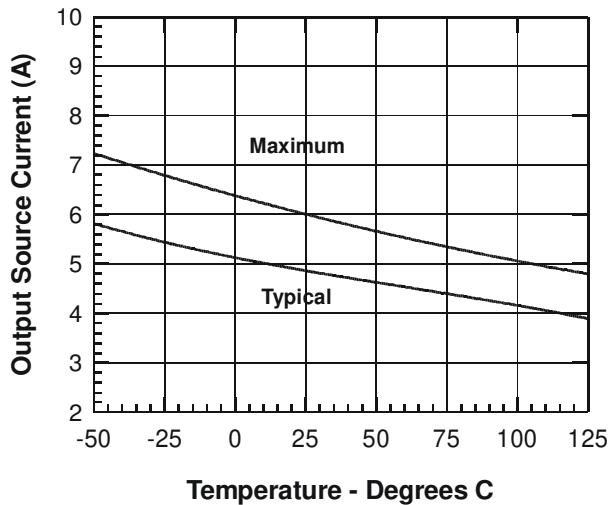


Fig. 21a. Output source current vs. temperature

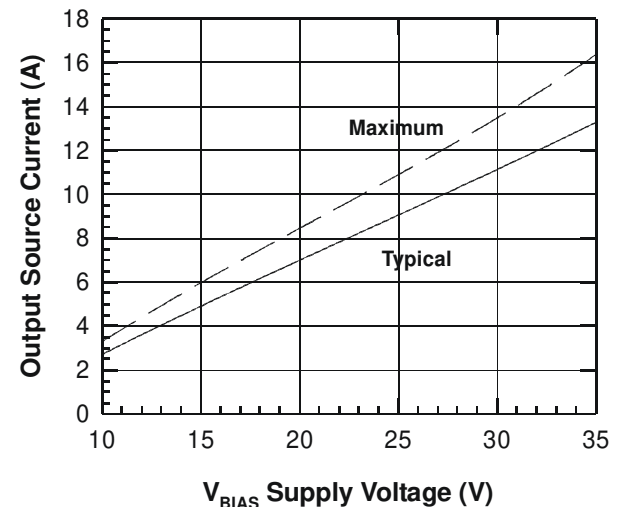


Fig. 21b. Output source current vs supply voltage

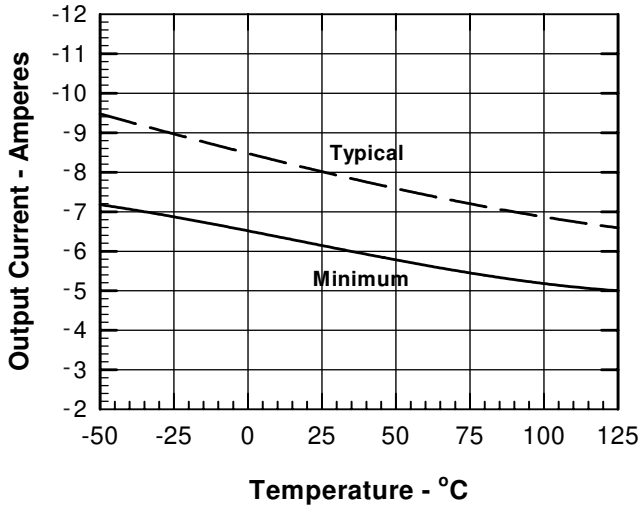


Fig. 22a. Output sink current vs. temperature

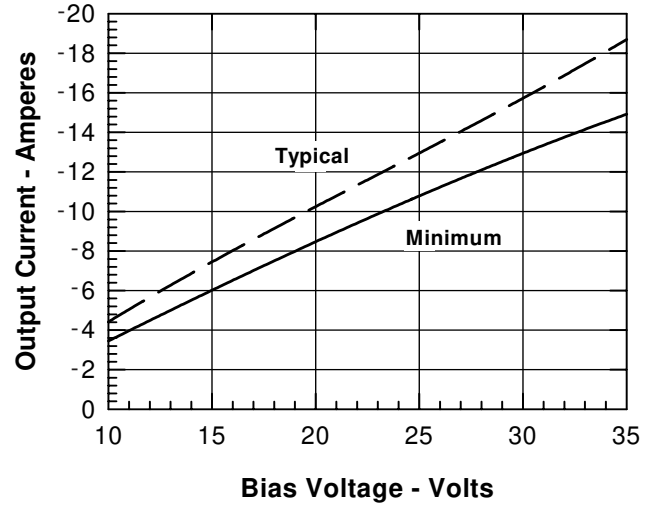


Fig. 22b. Output sink current vs. bias voltage

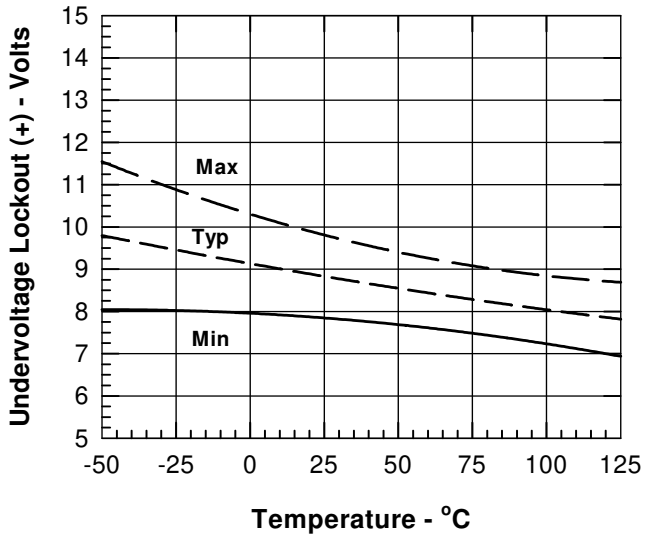


Fig. 23a. V<sub>CH</sub> Undervoltage positive trip vs. temperature.

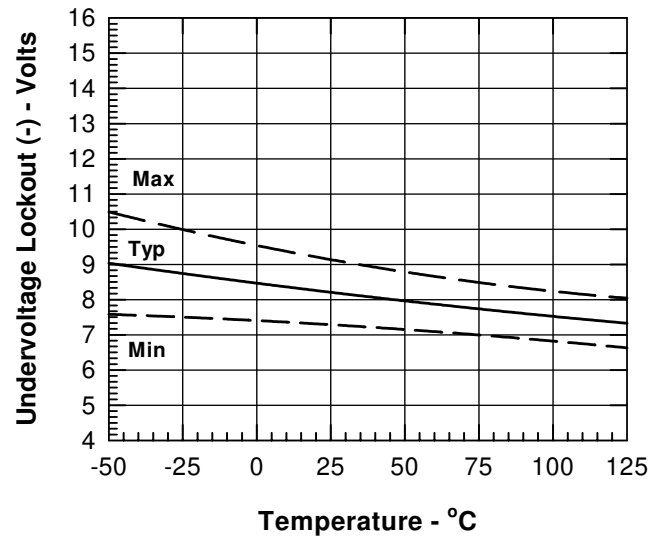


Fig. 23b. V<sub>CH</sub> Undervoltage negative trip vs. temperature.

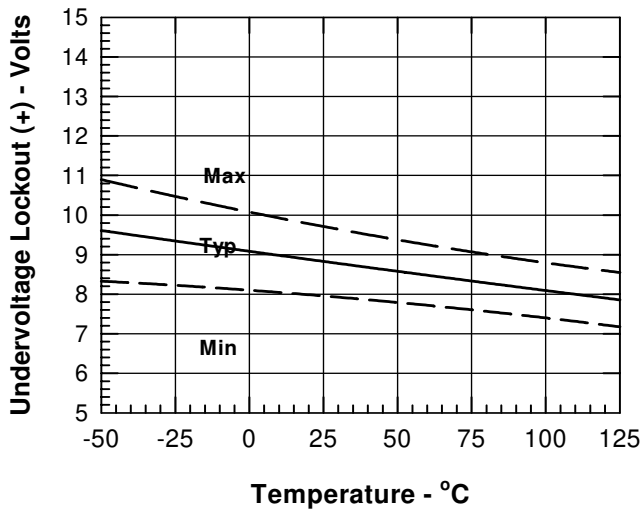


Fig. 24a. V<sub>CL</sub> Undervoltage positive trip vs. temperature.

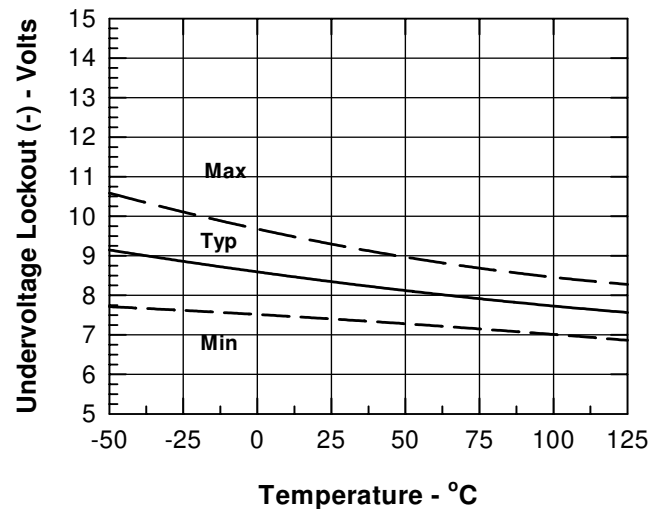


Fig. 24b. V<sub>CL</sub> Undervoltage negative trip vs. temperature.

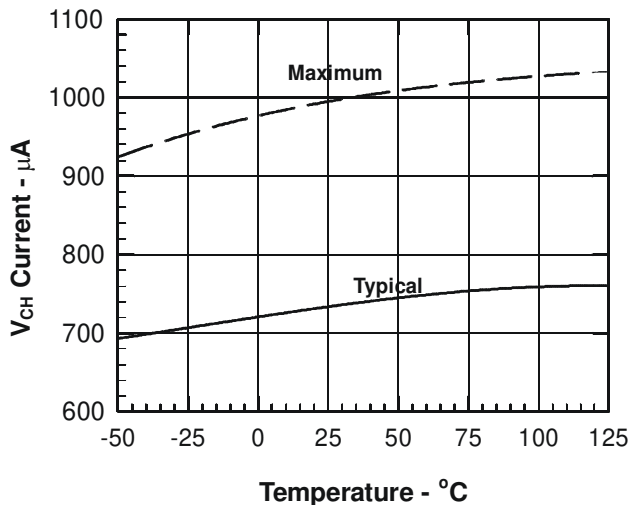


Fig. 25a. Quiescent current vs. temperature for the high side power supply.

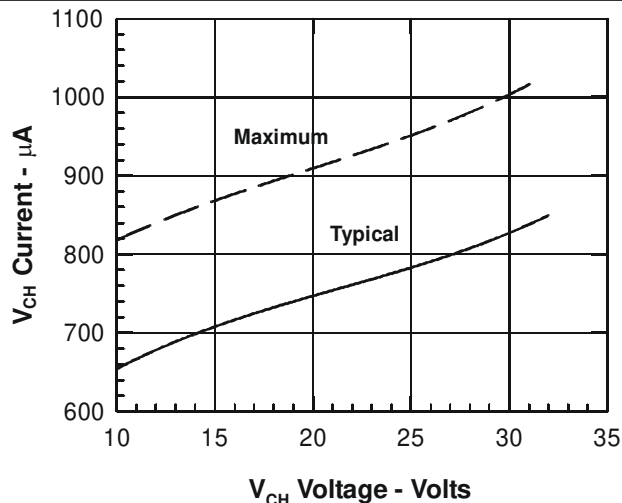


Fig. 25b. Quiescent current vs. voltage for the high side power supply.

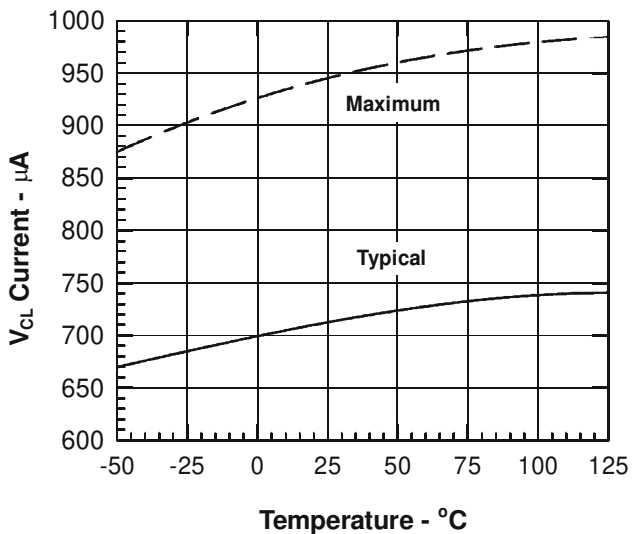


Fig. 26. Quiescent current vs. temperature for the low side power supply

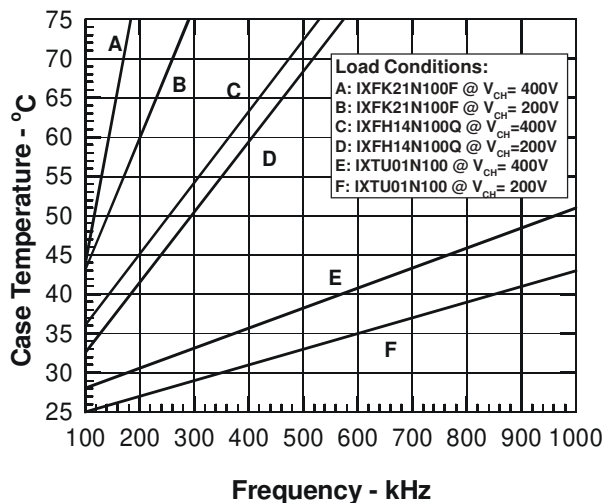


Fig. 27a. Case temperature rise vs. switching frequency for IX6R11S3

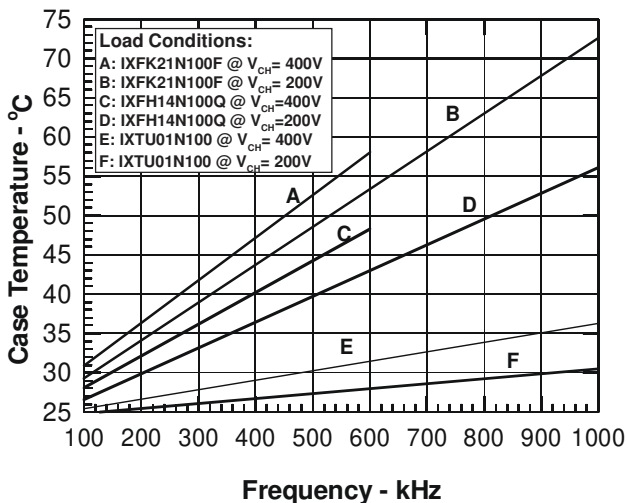


Fig. 27b. Case temperature rise vs. switching frequency for IX6R11S6

