

UCC28742 High-Efficiency Flyback Controller with Optocoupler Feedback

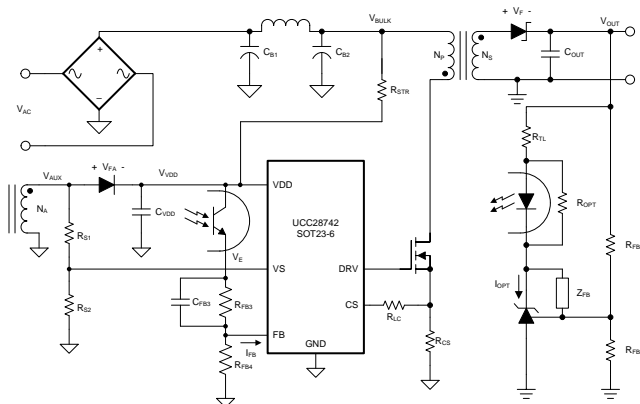
1 Features

- Opto-Coupled Feedback Enables up to 1% Regulation
- Accurate Current Limit with Overload Timeout Protection and Delayed Hiccup Response
- Resonant-Ring Valley-Switching Operation for Highest Overall Efficiency
- 80-kHz Maximum Switching Frequency
- Frequency Dithering to Ease EMI Compliance
- Clamped Gate-Drive Output for MOSFET
- Ultra-Low Start-Up Current and Large VDD Hysteresis
 - High Value Start-Up Resistor
 - Low Bias Capacitance
- Fault Protections
 - Input Low Line
 - Output Over-Voltage
 - Over-Current
 - Short-Circuit
- SOT23-6 Package
- Create a Custom Design Using the UCC28742 with the [WEBENCH® Power Designer](#)

2 Applications

- Industrial and Medical AC-to-DC Power Supplies
- Smart Electricity Meters
- Bias Supply for UPS, Server PSU, etc.
- Power Supply for Cable Modem, Television, Set-Top Box, and Wireless Routers
- AC-to-DC Power Supply for Appliances

Simplified Schematic



3 Description

The UCC28742 off-line flyback controller is a highly integrated, 6-pin secondary-side regulated PWM controller for efficient AC-to-DC power supplies. It is an isolated-flyback power-supply controller that provides Constant-Voltage (CV) using an optical coupler to improve transient response to large-load steps. This device processes information from opto-coupled feedback and an auxiliary flyback winding for high-performance control of output voltage and current.

The UCC28742 employs advanced control algorithms to achieve high operating efficiency and performance. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley-switching reduces switching losses. Modulation of switching frequency and primary current-peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

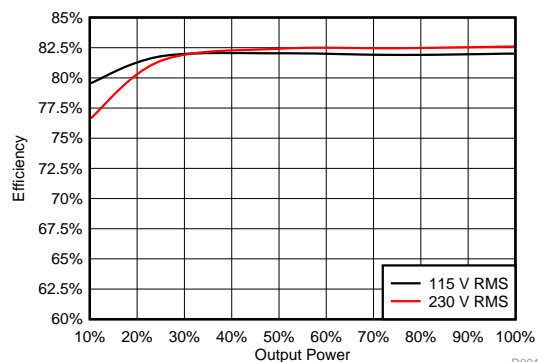
The controller has a maximum switching frequency of 80 kHz and always maintains control of the peak-primary current in the transformer. A minimum switching frequency of 200 Hz facilitates the achievement of low no-load input power.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28742	SOT23-6	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Efficiency of a 10-W, 5-V AC-to-DC Converter



D001



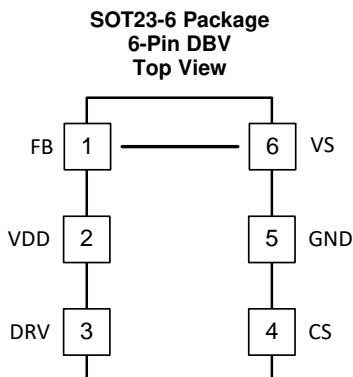
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4 Revision History

DATE	REVISION	NOTES
May 2018	A	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	4	I	The current-sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage monitors and controls the peak primary current. A series resistor is added to this pin to compensate for peak switch current levels as the AC-mains input varies.
DRV	3	O	DRV is an output pin used to drive the gate of an external high voltage MOSFET switching transistor.
FB	1	I	The feedback (FB) input receives a current signal from the optocoupler output transistor. An internal current mirror divides the feedback current applies it to an internal pullup resistor to generate a control voltage, VCL. The voltage at this resistor directly drives the control law function, which determines the switching frequency and the peak amplitude of the switching current.
GND	5	G	The ground (GND) pin is both the reference pin for the controller, and the low-side return for the drive output. Special care must be taken to return all AC-decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal-return paths.
VDD	2	P	VDD is the bias supply input pin to the device. A carefully placed bypass capacitor to GND is required on this pin. Typical bypass capacitor values are from 0.047 μ F to 10 μ F depending on a design.
VS	6	I	Voltage sense (VS) is an input used to provide demagnetization timing feedback to the controller to limit frequency, to control constant-current operation, and to provide output-overvoltage detection. VS is also used for AC-mains input-voltage detection for peak primary-current compensation. This pin connects to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider programs the AC-mains run and stop thresholds, and factors into line compensation at the CS pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{VDD}	Bias supply voltage		38	V
VS	Voltage range	-0.75	7	V
FB	Voltage range	-0.5	7	V
CS	Voltage range	-0.5	5	V
V _{DRV}	Gate-drive voltage at DRV	-0.5	Self-limiting	V
I _{DRV}	DRV continuous sink current		50	mA
I _{DRV}	DRV continuous source current		15	mA
I _{DRV}	DRV peak sourcing current, V _{DRV} = 10 V to 0 V		Self-limiting	mA
I _{DRV}	DRV peak sink current, V _{DRV} = 0 V to 10 V		Self-limiting	mA
I _{FB}	FB, peak current		1.0	mA
I _{VS}	VS, peak, 1% duty-cycle, when detecting line voltage		1.2	mA
T _J	Operating junction temperature range	-55	150	°C
T _{STG}	Storage temperature	-65	150	°C
T _{LEAD}	Lead temperature 0.6 mm from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
V _(ESD)	Electrostatic discharge	Charged-device model (CDM) ESD stress voltage ⁽²⁾	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VDD	Bias supply operating voltage	9	35	V
C _{DD}	VDD bypass capacitor	0.047	no limit	μF
I _{FB}	Feedback current, continuous		50	μA
I _{VS}	VS pin sourcing current when detecting line voltage		1.0	mA
T _J	Operating junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC		UCC28742	
		DBV	UNIT
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽¹⁾	150	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽²⁾	55	°C/W
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	60	°C/W
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	55	°C/W

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

6.5 Electrical Characteristics

Over operating free-air temperature range, $V_{VDD} = 25\text{ V}$, $V_{FB} = 0\text{ V}$, $V_{VS} = 4\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $T_J = T_A$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	$I_{DRV} = 0$, run state	1.30	1.80	2.40	mA
I_{WAIT}	Supply current, wait	$I_{DRV} = 0$, $V_{VDD} = 20\text{ V}$, wait state	50	80	115	μA
I_{START}	Supply current, start	$I_{DRV} = 0$, $V_{VDD} = 17\text{ V}$, start state		1.50	2.75	μA
I_{FAULT}	Supply current, fault	$I_{DRV} = 0$, fault state	1.30	1.80	2.40	mA
UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	17.5	21.6	24.5	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	7.25	7.80	8.30	V
VS INPUT						
V_{VSNC}	Negative clamp level	$I_{VS} = -300\ \mu\text{A}$	-304	-225	-164	mV
I_{VSB}	Input bias current	$V_{VS} = 4\text{ V}$	-0.25	0	0.25	μA
FB INPUT						
I_{FBMAX}	Full-range input current	$f_{SW} = f_{SW(min)}$	16	23	30	μA
V_{FBMAX}	Input voltage at full-range	$I_{FB} = 26\ \mu\text{A}$	0.70	0.90	1.10	V
R_{FB}	FB-input resistance	$\Delta I_{FB} = 6\text{ to }26\ \mu\text{A}$	10	14	18	k Ω
CS INPUT						
$V_{CST(max)}$	Max CS threshold voltage ⁽¹⁾	$I_{FB} = 0\ \mu\text{A}$	710	770	830	mV
$V_{CST(min)}$	Min CS threshold voltage ⁽¹⁾	$I_{FB} = 35\ \mu\text{A}$	164	190	216	mV
K_{AM}	AM control ratio	$V_{CST(max)} / V_{CST(min)}$	3.55	4.00	4.50	V/V
V_{CCR}	Constant-current regulating level		338	363	390	mV
K_{LC}	Line compensating current ratio, $I_{VSLs} /$ (current out of CS pin)	$I_{VSLs} = -300\ \mu\text{A}$	23	25	29	A/A
T_{CSLEB}	Leading-edge blanking time	DRV output duration, $V_{CS} = 1\text{ V}$	195	270	350	ns

- (1) These threshold voltages represent average levels. This device automatically varies the current sense threshold to improve EMI performance.

Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{VDD} = 25\text{ V}$, $V_{FB} = 0\text{ V}$, $V_{VS} = 4\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $T_J = T_A$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRV						
I_{DRS}	DRV source current	$V_{DRV} = 5\text{ V}$, $V_{VDD} = 9\text{ V}$	24	30	36	mA
R_{DRVLS}	DRV low-side drive resistance	$I_{DRV} = 10\text{ mA}$		6.5	12	Ω
V_{DRCL}	DRV clamp voltage	$V_{VDD} = 35\text{ V}$	8.8	10.6	13	V
R_{DRVSS}	DRV pull-down in start state		135	175	250	k Ω
TIMING						
$f_{SW(max)}$	Maximum switching frequency ⁽²⁾	$I_{FB} = 0\text{ }\mu\text{A}$	80	105	130	kHz
$f_{SW(min)}$	Minimum switching frequency	$I_{FB} = 35\text{ }\mu\text{A}$	140	200	255	Hz
t_{ZTO}	Zero-crossing timeout delay		1.45	2.45	3.30	μs
t_{OVL_TIME}	Delay time before shutdown	$Demag_Duty = V_{CCR} / V_{CST(max)}$	85	120	160	ms
PROTECTION						
V_{OVP}	Over-voltage threshold ⁽³⁾	At VS input, $T_J = 25^{\circ}\text{C}$	4.45	4.65	4.85	V
V_{OCP}	Over-current threshold ⁽³⁾	At CS input	1.41	1.50	1.59	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin – increasing	170	210	250	μA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin – decreasing	60	75	90	μA
K_{VSL}	VS pin, line-sense current ratio, $I_{VSL(run)} / I_{VSL(stop)}$		2.50	2.80	3.05	A/A
$T_{J(stop)}$	Thermal shut-down temperature ⁽⁴⁾	Internal junction temperature		165		$^{\circ}\text{C}$

(2) These frequency limits represent average levels. This device automatically varies the switching frequency to improve EMI performance.

(3) The OVP threshold at VS decrease with increasing temperature by 1 mV/ $^{\circ}\text{C}$. This compensation over temperature is included to reduce the variances in power supply over-voltage detection with respect to the external output rectifier.

(4) Ensured by design. Not tested in production.

6.6 Typical Characteristics

V_{DD} = 25 V, unless otherwise noted.

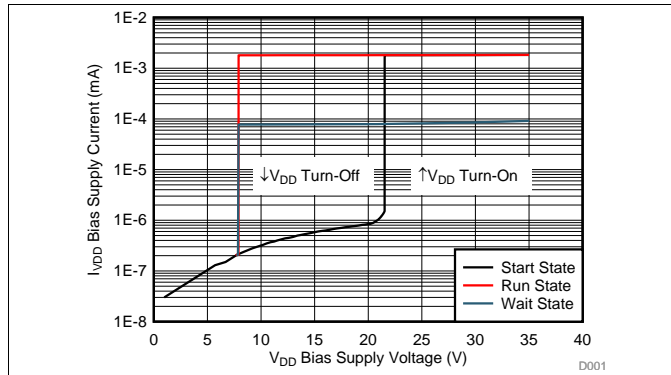


Figure 1. Bias Supply Current vs. Bias Supply Voltage

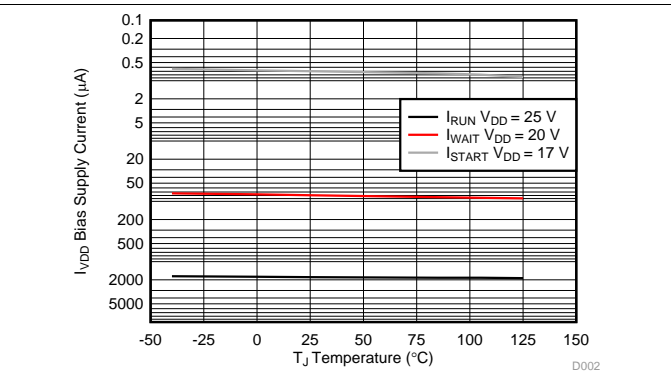


Figure 2. Bias Supply Current vs. Temperature

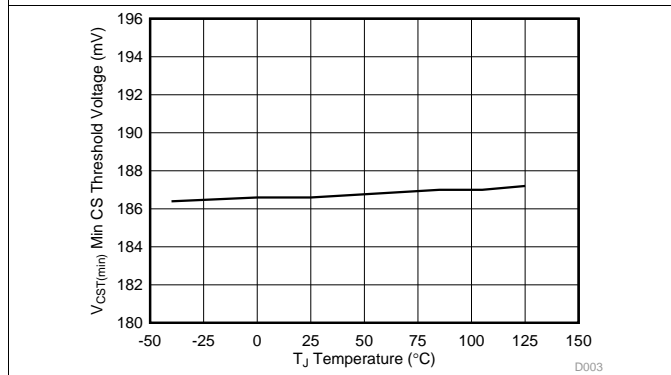


Figure 3. Minimum CS Threshold vs. Temperature

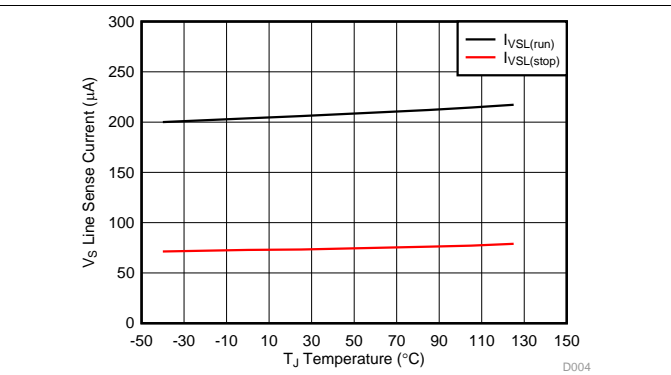


Figure 4. VS Line-Sense Current vs. Temperature

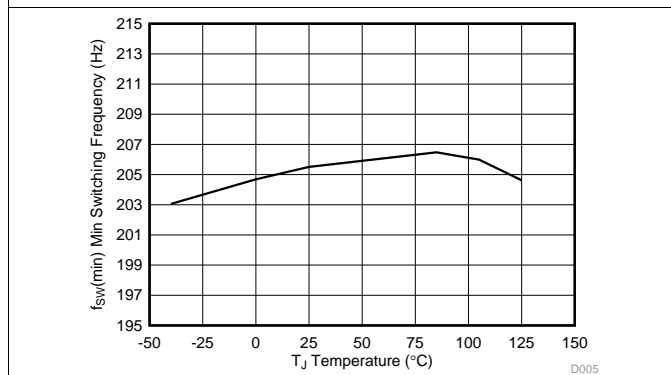


Figure 5. Minimum Switching Frequency vs. Temperature

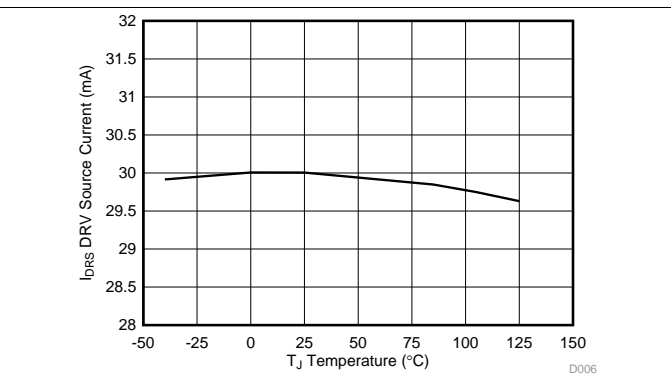


Figure 6. DRV Source Current vs. Temperature

Typical Characteristics (continued)

VDD = 25 V, unless otherwise noted.

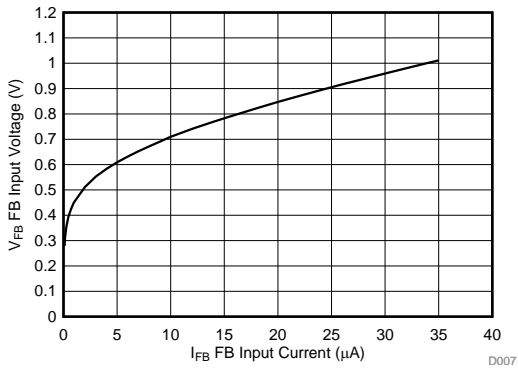


Figure 7. FB Input Voltage vs. FB Input Current

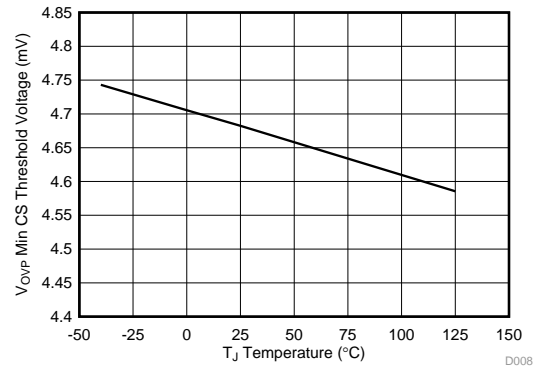


Figure 8. VS Overvoltage Threshold vs. Temperature

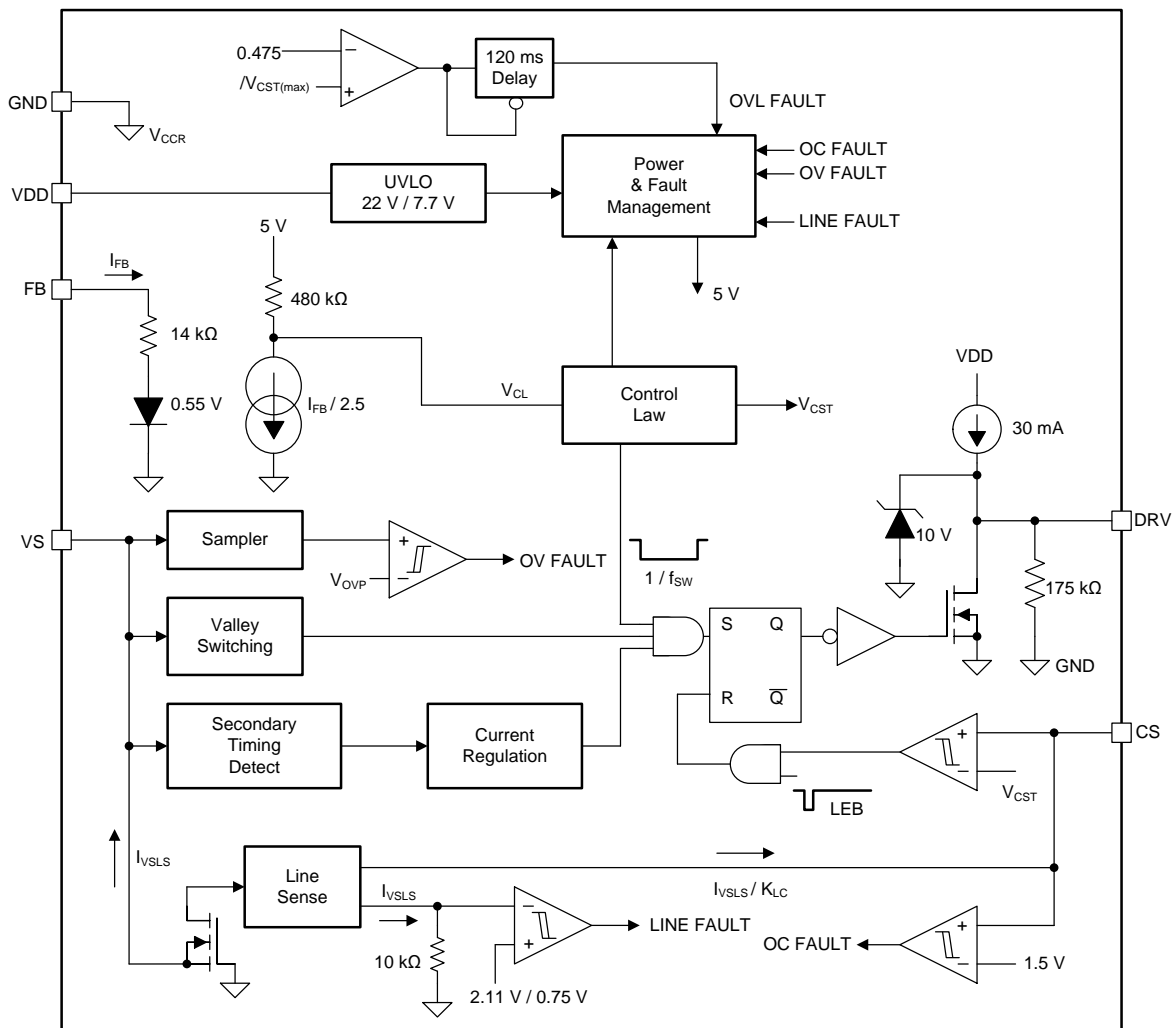
7 Detailed Description

7.1 Overview

The UCC28742 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses and allow for the use of low cost output rectifiers. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to achieve low standby power dissipation.

During low-power operating conditions, the power-management features of the controller reduce the device-operating current at switching frequencies below 25 kHz. At and above this frequency, the UCC28742 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count solution is realized using a straight-forward design process.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detailed Pin Description

7.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin is typically powered from a rectified auxiliary transformer winding, the same winding that is used to capture the output voltage level. A bypass capacitor, with minimum value 0.047 μF , on the VDD pin is used for initially biasing the device to start-up along with a resistive or active source of start-up charging current. UVLO start / stop levels of 21.6 V / 7.8 V accommodate lower values of VDD capacitance that in turns keeps the start-up current low, which for resistive start-up has an impact on both stand-by power and power-on delay. A high, 35-V, maximum operating level on VDD alleviates concerns with leakage energy charging of VDD and gives added flexibility to when varying power supply output voltage must be supported.

7.3.1.2 GND (Ground)

This is an external return pin, and provides the reference point for both external signal and the gate drive of the device. The VDD bypass capacitor should be placed close to this pin. Critical component GND connections from the VS, FB and CS pins should have dedicated and short paths to this pin.

Feature Description (continued)

7.3.1.3 VS (Voltage-Sense)

The VS pin connects to a resistor-divider from the auxiliary winding to ground. The auxiliary voltage waveform is sampled at the end of the transformer secondary-current demagnetization time. The waveform on the VS pin determines (1) the timing information to achieve valley-switching, (2) the timing to control the duty-cycle of the transformer secondary current, and (3) the output voltage over-voltage. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.

Besides, the VS pin also has these two functions: (4) senses the bulk capacitor input voltage to provide for ac-input run and stop thresholds, and (5) to compensate the current-sense threshold across the AC-input range. This information is sensed by monitoring the current pulled out of the VS pin during the MOSFET on-time. During this time the voltage on the VS pin is clamped to about 250 mV below GND. As a result, the current out of the pin is determined by the upper VS divider resistor, the auxiliary to primary turns-ratio and the bulk input voltage level. For the AC-input run/stop function, the run threshold on VS is $I_{VSL(run)}$ (typical 210 μ A) and the stop threshold is $I_{VSL(stop)}$ (typical 75 μ A). The values for the auxiliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \approx \frac{V_{BULK(run)}}{N_{PA} \times I_{VSL(run)}}$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC rms voltage to enable turn-on of the flyback converter (run),
- $V_{BULK(run)}$ is the DC bulk voltage to enable turn-on of the flyback converter (run),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the primary MOSFET on-time. (see the [Electrical Characteristics](#) table). (1)

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} + V_F) - V_{OVP}}$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output,
- V_F is the output rectifier forward voltage drop at near-zero current,
- N_{AS} is the transformer auxiliary to secondary turns ratio,
- R_{S1} is the VS divider upper-resistor resistance,
- V_{OVP} is the overvoltage detection threshold at the VS input (see the [Electrical Characteristics](#) table). (2)

Notice that VS pin absolute maximum current I_{VS} in its negative clamping is 1.2 mA. After determined R_{S1} it is required to check if VS pin current stays ≤ 1.2 mA. The check is to determine the input voltage ratio in this design and make $V_{IN(max)} / V_{IN(run)} \leq I_{VS} / I_{VSL(run)} = 1.2 \text{ mA} / 0.25 \text{ mA} = 4.8$, i.e., $V_{IN(max)} / V_{IN(run)} \leq 4.8$. If the design cannot meet this criterion, external circuit is needed to add in to make sure VS pin current ≤ 1.2 mA, for example, to use a zener type of device to clamp the transformer aux-winding negative voltage to achieve $V_{IN(max)} / V_{IN(run)} \leq 4.8$.

7.3.1.4 DRV (Gate Drive)

The DRV pin is connected to the MOSFET gate pin, usually through a series resistor. The DRV provides a gate drive signal which is clamped to 10-V internally. During turn-on the driver applies a typical 30-mA current source out of the DRV pin. When the DRV voltage rises to above 9 V the output current is reduced to about 100 μ A. This current brings the DRV voltage to the 10-V clamp level, or to VDD, whichever is less. The 30-mA current provides adequate turn-on speed while automatically limiting noise generated at turn-on by the MOSFET drain dv/dt and by the leading edge turn-on current spike. The gate drive turn-off current is internally limited to about 400 mA when DRV is above about 4 V. At lower DRV voltages the current will reduce, eventually being limited by the low-side on resistance, $R_{DS(on)}$. The drain turn-on and turn-off dv/dt can be further impacted by adding external resistor in series with DRV pin. The drain current resonances can be damped with a small series gate resistor, generally less than a 1 Ω .

Feature Description (continued)

7.3.1.5 CS (Current Sense)

The current sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The controller varies the internal current sense threshold between 190 mV and 770 mV, setting a corresponding control range for the peak-primary winding current to a 4-to-1 range. The series resistor R_{LC} provides an input voltage feed-forward function. The voltage drop across this resistor reduces primary-side peak current as the line voltage increases, compensating for the increased di/dt and delays in the MOSFET turn-off. There is an internal leading-edge blanking time of 270 ns to eliminate sensitivity to the MOSFET turn-on leading edge current spike. If additional blanking time is needed, a small bypass capacitor, up to 30 pF, can be placed on between CS pin and GND pin. The value of R_{CS} is determined by the target output current in constant current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer core and copper losses, bias power, and primary leakage inductance losses.

Example: With a transformer core and copper losses of 3%, leakage inductance caused power losses 2%, and bias power to output power ratio of 0.5%. The transformer power transfer efficiency is estimated as $\eta_{XFMR} = 100\% - 3\% - 2\% - 0.5\% = 94.5\%$

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}}$$

where

- V_{CCR} is a current regulation constant (see the [Electrical Characteristics](#) table),
- N_{PS} is the transformer primary-to-secondary turns ratio (a typical turns-ratio of 12 to 15 is recommended for 5-V output as an example),
- I_{OCC} is the target output current in constant-current limit (refer to [Constant Current Limit and Delayed Shutdown](#) for more detail),
- η_{XFMR} is the transformer efficiency. (3)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times (t_D + t_{GATE_OFF}) \times N_{PA}}{L_P}$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the current-sense delay (typical 50 ns) plus MOSFET turn-off delay,
- t_{GATE_OFF} is the primary-side main MOSFET turn-off time,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see the [Electrical Characteristics](#) table). (4)

7.3.1.6 FB (Feedback)

The FB pin connects to the emitter of an analog optocoupler output transistor which usually has the collector connected to VDD. The current supplied to FB by the optocoupler is reduced internally by a factor of 2.5 and the resulting current is applied to an internal 480-k Ω resistor to generate the control law voltage (V_{CL}). This V_{CL} directly determines the converter switching frequency and peak primary current required for regulation per the control-law for any given line and load condition.

Typical circuit connection between FB and optocoupler along with typical values of resistors and capacitors should be made as shown in [Figure 9](#). The resistors and capacitors in the connections help to stabilize operation during control mode transition.

Feature Description (continued)

7.3.2 Secondary-Side Optically Coupled Constant-Voltage (CV) Regulation

Figure 9 shows a simplified flyback convertor with the main output-regulation blocks of the device shown, along with typical implementation of secondary-side-derived regulation. The power-train operation is the same as any DCM-flyback circuit. A feedback current is optically coupled to the controller from a shunt-regulator sensing the output voltage.

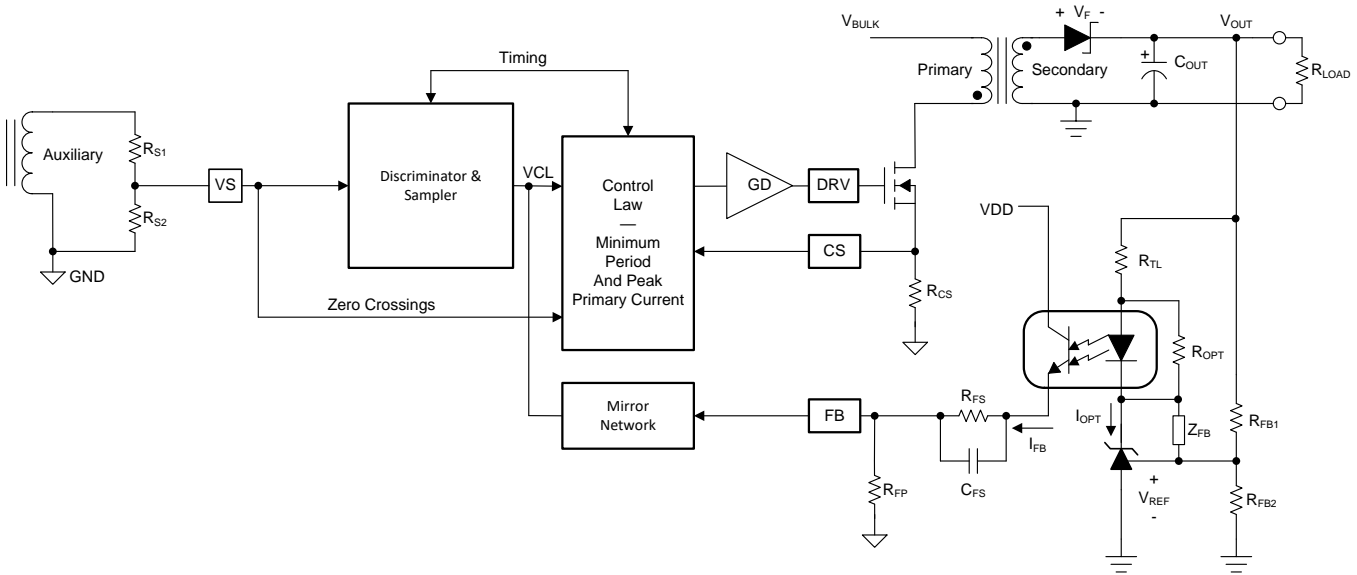


Figure 9. Simplified Flyback Converter (with the Main Voltage Regulation Blocks)

In this configuration, a secondary-side shunt-regulator, such as the TL431 (or ATL431), generates a current through the input photo-diode of an optocoupler. The photo-transistor delivers a proportional current that is dependent on the current-transfer ratio (CTR) of the optocoupler to the FB input of the UCC28742 controller. This FB current then converts into the V_{CL} by the input-mirror network, detailed in the device block diagram (see [Functional Block Diagram](#)). Output-voltage variations convert to FB-current variations. The FB-current variations modify the V_{CL} which dictates the appropriate I_{PP} and f_{SW} necessary to maintain CV regulation. At the same time, the VS input senses the auxiliary winding voltage during the transfer of transformer energy to the secondary output to monitor for an output overvoltage condition. When f_{SW} reaches the converter target maximum frequency (i.e., corresponding de-mag time duty reaches 0.475), Constant Current Limit is triggered and further increases in V_{CL} cannot increase f_{SW} anymore. (see [Figure 10, Control Law](#) and [Constant Current Limit and Delayed Shutdown](#))

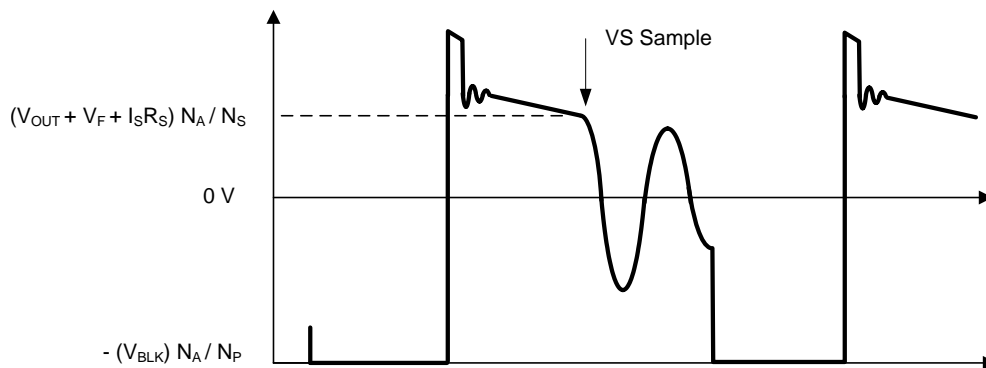


Figure 10. Auxiliary Winding Voltage

Feature Description (continued)

The UCC28742 samples the VS input voltage at the end of demagnetization time for output overvoltage detection and to determine the total demagnetization time for output current control in Constant Current Limit operation.

In order to maintain best performance of these functions the reset time and ringing of the auxiliary winding voltage should meet certain guidelines. Referring to [Figure 11](#), the width of the leakage spike at the VS input should be less than t_{DM_BLANK} . Minimum t_{DM_BLANK} is 3 μs at maximum peak primary current levels and proportionally less at lower peak primary current levels (the lowest 0.75 μs should be observed at high line and no load condition). In addition, any ringing following the spike should be reduced to < 160 mVpp (scaled to the VS pin) 200 ns before the end of the demagnetization time.

As mentioned in [Device Functional Modes](#), when $I_{PP} < I_{PP(max)}$, the device operation enters a “Wait” state during each switching cycle of its non-switching portion as shown in [Figure 11](#). In the *Wait* state, the device bias current changes to I_{WAIT} (typical 80 μA) from I_{RUN} (typical 1.8 mA), reducing its bias power to help boost efficiency at light load and to reduce no-load input power.

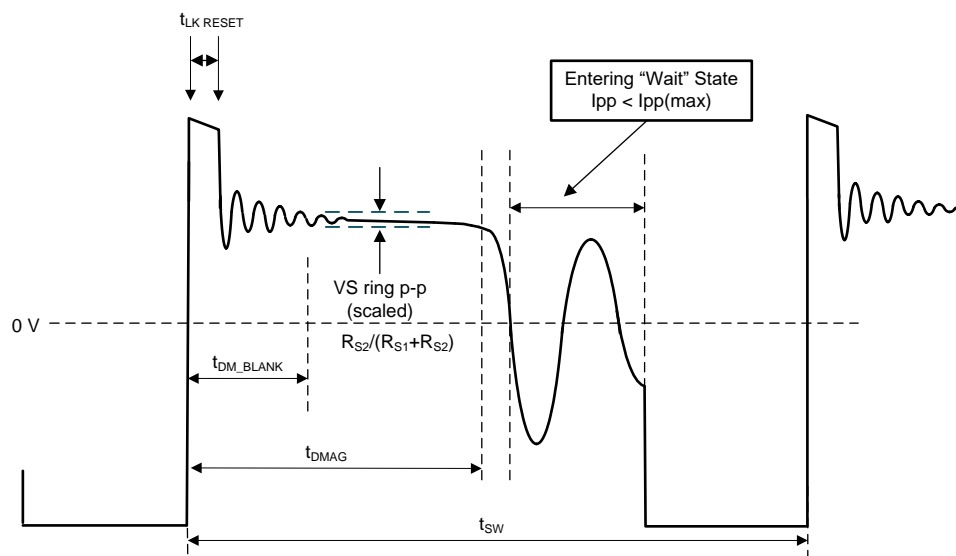


Figure 11. Auxiliary Waveform Details

Feature Description (continued)

7.3.3 Control Law

During voltage regulation (CV mode), the controller operates in frequency modulation mode and peak current amplitude modulation mode as illustrated in Figure 12 below. In CV mode operation, the control consists of four regions, namely, region FM 1, 2, AM and FM 3. The device internal V_{CL} sets a particular region of operation. Refer to Figure 12 for V_{CL} .

The device internally limits its operating frequency between $f_{SW(min)}$ and $f_{SW(max)}$, typically between 200 Hz and 105 kHz. The choice of transformer primary inductance and primary-peak current sets the maximum operating frequency of the converter, which must be equal to or lower than $f_{SW(max)}$. Conversely, the choice of maximum target operating frequency and primary-peak current determines the transformer primary-inductance value. The actual minimum switching frequency for any particular converter depends on several factors, including minimum loading level, leakage inductance losses, switch-node capacitance losses, other switching and conduction losses, and bias-supply requirements. In any case, the minimum steady-state frequency of the converter must always exceed $f_{SW(min)}$ or the output voltage may rise to the over-voltage protection level (OVP) and the controller responds as described in Fault Protection.

To achieve a regulated output voltage in the CV mode operation, energy balance has to be maintained. As the UCC28742 has a minimum switching frequency typical 200 Hz, together with the energy per switching cycle determined by converter parameters, such as the transformer primary inductance L_p and the selected R_{CS} resistor, the converter has a minimum input power. A proper pre-load needs to be selected to ensure that this minimum energy is balanced during the no-load condition. The selection of the line compensation resistor value (R_{LC}) connected to the CS pin can impact the energy per switching cycle based on low-line and high-line conditions. Typical Application section provides a design example to show how to implement these considerations.

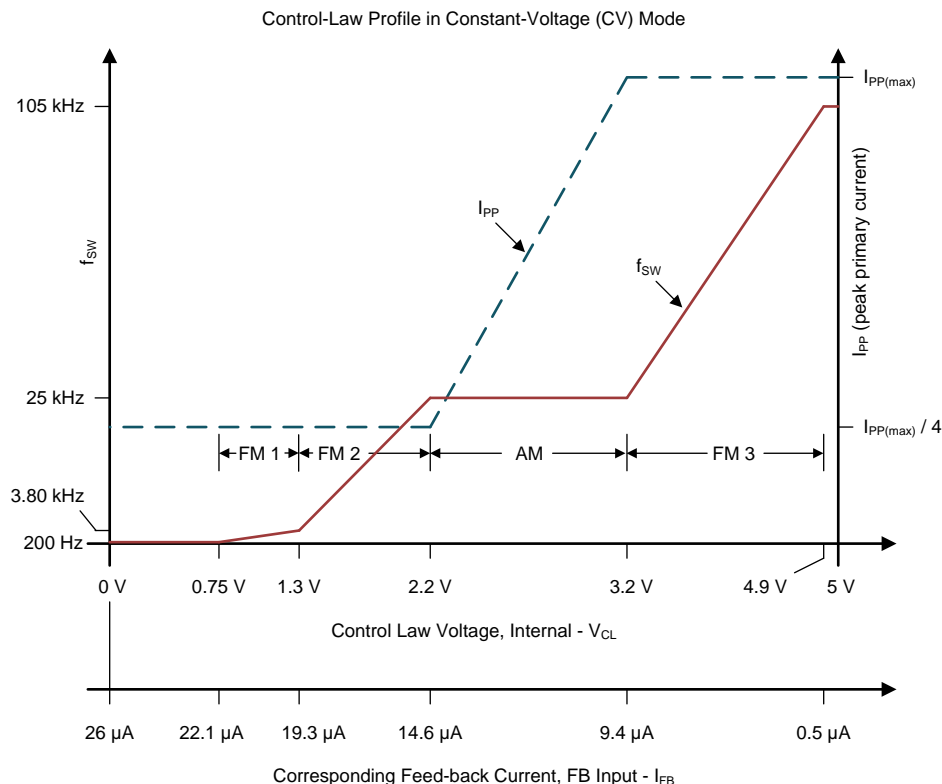


Figure 12. Frequency and Amplitude Modulation Modes (during CV mode)

Feature Description (continued)

The steady-state control-law voltage, V_{CL} , ranges between 0.75 V to 4.90 V. Heavy load operation is usually in Region FM 3 where frequency modulation to output regulation is used and primary-peak current is controlled at its maximum. The AM region is usually for medium-load range typically from 10% load and above. In this region switching frequency is fixed at nominal 25 kHz along with primary-peak current varying from 25% to 100% of its maximum. The low operating frequency ranges are for lighter loads to achieve stable regulation at low frequencies. In regions FM 1 and 2, peak-primary current is always maintained at $I_{PP(max)}/4$. Transitions between levels are automatically accomplished by the controller depending on the internal control-law voltage, V_{CL} and its corresponding FB pin current I_{FB} . An internal frequency-dithering mechanism is enabled in Region FM 3 to reduce conducted EMI, and is disabled otherwise. The *Wait* state is enabled in regions FM 1, 2, and AM, refer to [Figure 11](#).

7.3.4 Constant Current Limit and Delayed Shutdown

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary constant current limit, CCL, thus to achieve load over-current protection. The control law dictates that as power is increased in CV regulation and approaching CCL the primary-peak current is at $I_{PP(max)}$. Referring to [Figure 13](#) below, the primary peak current (I_{PP}), turns-ratio (N_S/N_P), secondary demagnetization time (t_{DMAG}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by [Equation 5](#). By regulating the secondary rectifier conduction duty cycle, the output current limit is achieved for given I_{PP} and transformer turns-ratio. When the load increases, the secondary-side rectifier conduction duty cycle keep increasing. Once this duty cycle reaches preset value of 0.475, the converter switching frequency stops increasing and starts adjusting to reduce and maintain 0.475 secondary-side duty cycle. Therefore, the output constant current limit is achieved. Because the current is kept constant, the increasing load results in lower output voltage.

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DMAG}}{t_{SW}} \tag{5}$$

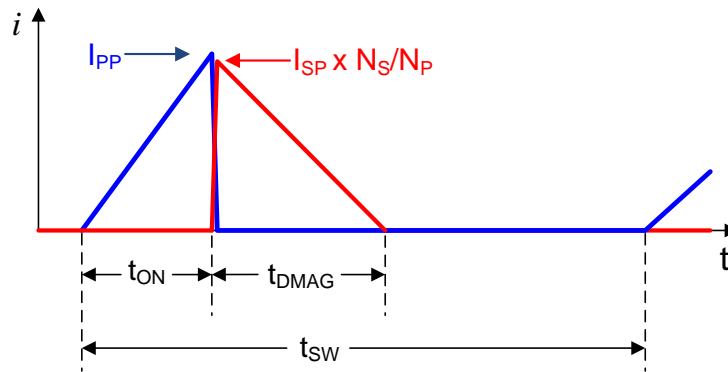


Figure 13. Transformer Currents

As shown in [Figure 14](#) below, CV mode operation is from $I_O = 0$ to $< I_{OCC}$; at $I_O = I_{OCC}$, the operation enters constant current limit mode and V_O starts to drop as the load resistance becomes further lower while I_O is maintained at I_{OCC} for a time interval specified by t_{OVL_TIME} typically 120 ms then DRV stops to achieve converter output delayed shutdown. During the 120-ms timing interval, if load I_O reduces to $< I_{OCC}$, the timer will be reset and no shutdown will occur. The V-I curve corresponding to the operation is shown in [Figure 14](#), and the delayed shutdown timing diagram is shown in [Figure 15](#). Note (1) The timer t_{OVL_TIME} is triggered whenever I_O reaches I_{OCC} and reset when I_O drops to $< I_{OCC}$ before 120ms-time-out. (2) during 120-ms time interval, when load resistance becomes so low during constant current interval that causes the device VDD to reach its $V_{VDD(off)}$ and then the shutdown will be through VDD undervoltage lockout instead of through Constant Current Limit and Delayed Shutdown. In such a case, the shutdown can happen before 120ms timer out.

Feature Description (continued)

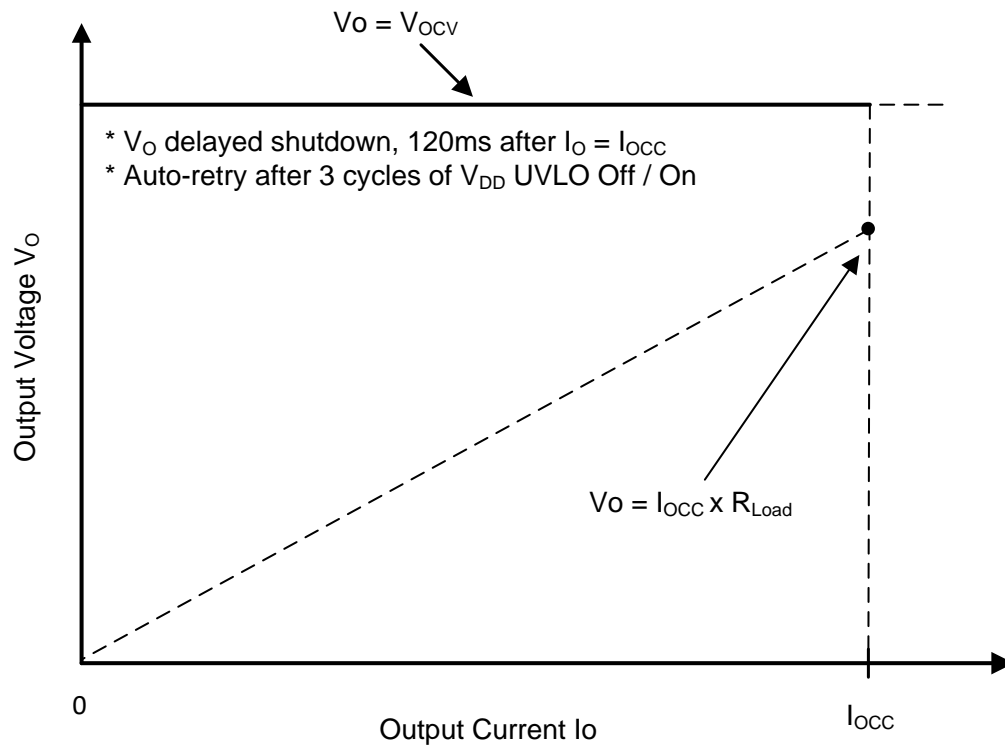


Figure 14. Typical Target Output V-I Characteristics

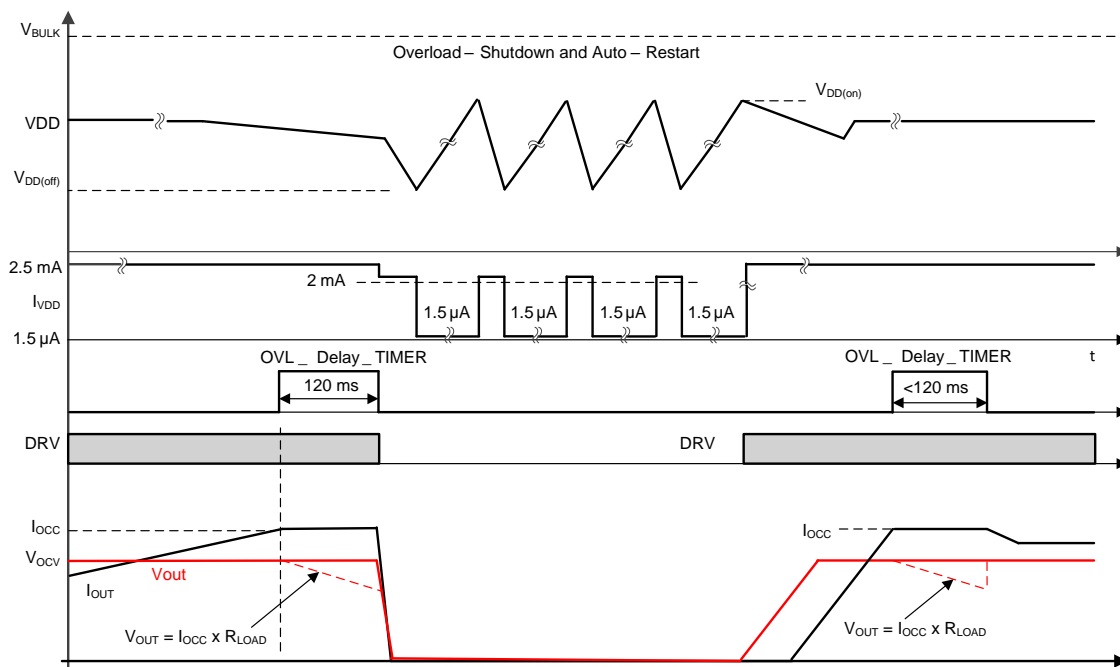


Figure 15. Output Delayed Shutdown Timing

Feature Description (continued)

7.3.5 Valley-Switching and Valley-Skipping

The UCC28742 utilizes valley switching to reduce switching losses in the MOSFET, reduce induced-EMI, and minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing diminished.

Referring to [Figure 16](#) below, the UCC28742 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

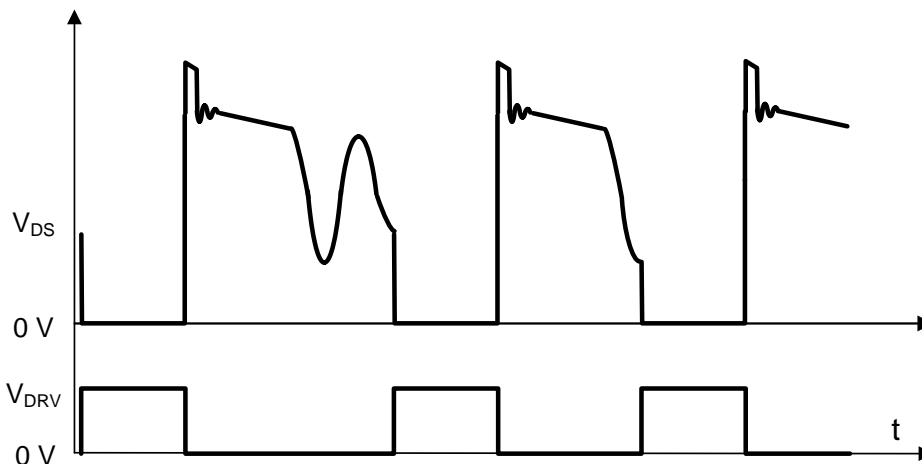


Figure 16. Valley-Skipping Mode

The UCC28742 forces a controlled minimum switching period corresponding to the power supply operating frequency. In each switching cycle, after the minimum period is expired, the UCC28742 looks for the next resonant valley on the auxiliary winding. The controller initiates a new power cycle at this valley point which corresponds to a reduced voltage level on the power MOSFET. If at the point in time when the minimum period expires ringing on the transformer winding has decayed such that no further resonant valleys can be detected a new power cycle is initiated following a fixed time, t_{ZTO} . This also applies when primary inductance L_P is designed with a high value that causes de-mag end ringing cycle longer than t_{ZTO} . When either happens, the valley switching is lost but the converter output voltage will still be in regulation.

Feature Description (continued)

7.3.7 Fault Protection

There is comprehensive fault protection incorporated into the UCC28742. Protection functions include:

- Output Over-Voltage
- Input Under-Voltage
- Primary Over-Current Fault
- CS Pin Open Fault
- CS Pin Short-to-GND Fault
- VS Pin Fault
- Device Internal Over-Temperature
- Constant Current Limit and Delayed Output Shutdown - Output Over-Current Protection

Output Over-Voltage: The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 4.65 V (V_{OVP}), for three consecutive switching cycles an OV fault is asserted. Once asserted the device stops switching, initiating a UVLO reset and re-start fault cycle. During the fault, the VDD bias current remains at the run current level, discharging the VDD pin to the UVLO turn-off threshold, $V_{VDD(off)}$. After that, the device returns to the start state, VDD now charging to $V_{VDD(on)}$ where switching is initiated. The UVLO sequence repeats as long as the fault condition persists.

Input Under-Voltage: The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through R_{S1} , out of the VS pin, is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. From the start state, the sensed VS current, I_{VSL} , must exceed the run current threshold, $I_{VSL(run)}$ (typical 211 μ A), within the first three cycles after switching starts as VDD reaches $V_{VDD(on)}$. If it does not, then switching stops and the UVLO reset and re-start fault cycle is initiated. Once running, I_{VSL} must drop below the stop level, $I_{VSL(stop)}$ (typically 75 μ A), for three consecutive cycles to initiate the fault response.

Primary Over-Current: The UCC28742 always operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 190 mV to 770 mV. If the voltage on CS exceeds the 1.5-V over-current level, any time after the internal leading edge blanking time and before the end of the transformer demagnetization, for three consecutive cycles, the device shuts down and the UVLO reset and re-start fault cycle begins.

CS Pin Open: The CS pin has a 2- μ A minimum pull-up that brings the CS pin above the 1.5-V OC fault level if the CS pin is open. This causes the primary over-current fault after three cycles.

CS Pin Short to GND: On the first, and only the first, cycle at start-up during power on, the device checks to verify that the $V_{CST(min)}$ threshold is reached at the CS pin within 5 μ s of DRV going high. If the CS voltage fails to reach this level then the device terminates the current cycle and immediately enters the UVLO reset and re-start fault sequence.

VS Pin: Protection is included in the event of component failures on the VS pin. If the high-side VS divider resistor opens the controller stops switching. VDD collapses to its $V_{VDD(off)}$ threshold, a start-up attempt follows with a single DRV on-time when VDD reaches $V_{VDD(on)}$. The UVLO cycle will repeat. If the low-side VS divider resistor is open then an output over-voltage fault occurs.

Device Internal OTP: The internal over-temperature protection threshold is 165 °C. If the junction temperature of the device reaches this threshold the device initiates the UVLO reset and re-start fault cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Constant Current Limit and Delayed Output Shutdown - Output Over-Current Protection: The load over-current protection is made precisely using constant current limit and delayed output shutdown as described in section [Constant Current Limit and Delayed Shutdown](#)

7.4 Device Functional Modes

The UCC28742 operates in different modes according to input voltage, VDD voltage, and output load conditions:

- At start-up, when VDD is less than the turn-on threshold, $V_{VDD(on)}$, the device is simply waiting for VDD to reach this threshold while the VDD capacitor is getting charged.
- When VDD exceeds $V_{VDD(on)}$, the device starts switching to deliver power to the converter output. The initial 3 switching cycles control the primary-peak current to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. When confirmed with input voltage above predetermined level and no fault conditions, start up process proceeds and normal power conversion follows. The converter will remain in discontinuous current mode operation during charging of the output capacitor(s), maintaining a constant output current, I_{OCC} , until the output voltage reaches its regulation point. The maximum time duration when I_O stays on I_{OCC} can only last 120 ms, and when 120-ms timer out, the device will initiate shutdown. Therefore, a design needs to make sure the maximum time when output current reaches and stays on I_{OCC} does not exceed 120 ms during start. For more details refer to [Constant Current Limit and Delayed Shutdown](#)
- When operating with $I_{PP} = I_{PP(max)}$, the UCC28742 operates continuously in the *run* state. In this state, the VDD bias current is always at I_{RUN} plus the average gate-drive current.
- When operating with $I_{PP} < I_{PP(max)}$, the UCC28742 operates in the *wait* state between switching cycles and in the *run* state during a switching cycle. In the *wait* state, the VDD bias current is reduced to I_{WAIT} after demagnetizing time of each switching cycle to improve efficiency at light loads. This helps reduce no-load to medium-load power losses, particularly for achieving higher efficiency at 10%, 25% load conditions, and possible at < 50% load conditions, depending on a design.
- The device operation will stop if any events occur as listed below:
 - If VDD drops below the $V_{VDD(off)}$ threshold, the device stops switching, its bias current consumption is lowered to I_{START} until VDD rises above the $V_{VDD(on)}$ threshold. The device then resumes operation through start-up.
 - If a fault condition is detected, the device stops switching and its bias current consumption becomes I_{FAULT} . This current level discharges VDD to $V_{VDD(off)}$ where the bias current changes from I_{FAULT} to I_{START} until VDD rises above the $V_{VDD(on)}$ threshold.
- If a fault condition persists, the operation sequence described above in repeats until the fault condition or the input voltage is removed. Refer to [Fault Protection](#) for fault conditions and post-fault operation.

Typical Application (continued)

8.2.1 Design Requirements

The following table illustrates a typical subset of high-level design requirements for a particular converter of which many of the parameter values are used in the various design equations in this section. Other necessary design parameters, $V_{BULK(min)}$ for example, may not be listed in such a table. These values may be selected based on design experience or other considerations, and may be iterated to obtain optimal results.

Table 1. UCC28742 Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	AC-line input voltage		85	115/230	265	V_{RMS}
f_{LINE}	Line frequency		47	50/60	63	Hz
P_{STBY}	No-load input power	$V_{IN} = \text{typ}, I_O = 0A$		65		mW
OUTPUT CHARACTERISTICS						
V_O	DC output voltage	$V_{IN} = \text{typ}, I_O = 0 \text{ to } I_{OR}$		5		V
V_{RIPPLE}	Output voltage ripple	$V_{IN} = \text{typ}, I_O = I_{OR}$		50		mV
I_{OR}	Output rated current	$V_{IN} = \text{min to max}$		2.0		A
I_{OVL}	Overload current Limit	$V_{IN} = \text{typ}$		2.05		A
OVL delay	Overload shutdown delay	$V_{IN} = \text{typ}, I_O = I_{OCC}$		120		ms
η_{AVG}	Average efficiency	$V_{IN} = \text{typ}$, average of 25%, 50%, 75%, and 100% Load		82		%
SYSTEMS CHARACTERISTICS						
f_{sw}	Switching frequency		0.2		65	kHz

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant output voltage (V_{OCV}) flyback converter using the UCC28742 controller. Please refer to the [Figure 18](#) for circuit details and section for variable definitions used in the applications equations below.

8.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the UCC28742 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage. At this time the auxiliary winding can sustain the voltage to the UCC28742. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved to maintain VDD above its $V_{DD(on)}$. The gate-drive current depends on particular MOSFET to be used. If with an estimated average 1.0 mA of gate-drive current, C_{DD} is determined by [Equation 6](#), and at I_{OCC} , $V_{OCC} = V_{OCV}$.

$$C_{DD} = \frac{(I_{RUN} + 1.0\text{mA}) \times \frac{C_{OUT} \times V_{OCV}}{I_{OCC}}}{(V_{DD(on),min} - V_{DD(off),max})} \quad (6)$$

8.2.2.3 VDD Start-Up Resistance, R_{STR}

Once the VDD capacitance is known, the start-up resistance from V_{BULK} to achieve the power-on delay time (t_{STR}) target can be determined.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{t_{STR}}} \quad (7)$$

8.2.2.4 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum N_p to N_s turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input rms voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV} , load current over load $I_{OVL} = I_{OCC}$, and the full-load efficiency target. An initial estimate of efficiency can be assumed for full-load efficiency, for example 89% for a converter of rated power 48 W and output voltage 24 V.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \quad (8)$$

Equation 9 provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{P_{IN} \times \left(0.5 + \frac{1}{\pi} \times \arcsin \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right)}{\left(2V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \quad (9)$$

8.2.2.5 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is $\frac{1}{2}$ of the DCM resonant period, or 1 μ s assuming 500-kHz resonant frequency. D_{MAX} can be determined using Equation 10.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX} \right) - D_{MAGCC} \quad (10)$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle when load current reaches a specified limit operation. It is set internally by the UCC28742 at 0.475. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV} and the secondary rectifier V_F .

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F)} \quad (11)$$

N_{PS} is determined also with other design factors such as voltage and current ratings of primary MOSFET, secondary rectifier diode, as well as secondary MOSFET if synchronous rectifier is used. Once an optimum turns-ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28742 controller constant current limit is achieved by maintaining $D_{MAGCC} = 0.475$ at the maximum primary current setting. The transformer turns ratio and current limit determine the current sense resistor for a target constant current limit.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. A bias power can be initially estimated at 0.1% to 0.5% rated power depending on power rating. An overall transformer efficiency of 94.5% is a good estimation of assuming 2% leakage inductance, 3% core and winding loss, and 0.5% bias power.

R_{CS} is used to program the primary-peak current with Equation 12:

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (12)$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output and transformer efficiency are included in [Equation 14](#).

Initially the transformer primary current should be determined. Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (13)$$

$$L_P = \frac{2 \times (V_{OCV} + V_F) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (14)$$

The primary inductance L_P in [Equation 14](#) also needs to consider primary MOSFET minimum turn on time as described in [Transformer Parameter Verification](#).

The auxiliary winding to secondary winding transformer turns-ratio (N_{AS}) is determined by the lowest target operating output voltage V_{OVL} at current limit and above the $V_{DD(off)}$ of the UCC28742. The output voltage reaches V_{OVL} when output current reaches its limit I_{OCC} ; V_{OVL} is determined by I_{OCC} and the expected minimum load resistance R_{LOAD} at I_{OCC} , *i.e.*, $V_{OVL} = I_{OCC} \times R_{LOAD}$. Note that V_{OVL} can only be maintained within typical 120ms, and after that time, the output voltage will enter the cycle of shutdown and auto-start retry, as described in [Constant Current Limit and Delayed Shutdown](#), and shown in [Figure 14](#) and [Figure 15](#). There is additional energy supplied to VDD from the transformer leakage inductance energy which may allow a slightly lower turns-ratio to be used in a design. The N_{AS} is then determined by the below equation.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (15)$$

8.2.2.6 Transformer Parameter Verification

The transformer turns-ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage so these should be reviewed. The UCC28742 controller requires a minimum on time of the MOSFET (t_{ON}) and minimum D_{MAG} time ($t_{DMAG(min)}$) of the secondary rectifier in the high line, under minimum-load condition. The selection of f_{MAX} , L_P and R_{CS} affects the minimum t_{ON} and t_{DMAG} .

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} \quad (16)$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2} \right) + \left(V_{OCV} + V_F \right) \times N_{PS} + V_{LK} \quad (17)$$

The following equations are used to determine for the minimum t_{ON} target of 0.35 μ s and minimum de-mag time, $t_{DMAG(min)}$, target of 1.7 μ s. Notice that the minimum t_{ON} target of 0.35 μ s is determined by CS pin **Leading-edge blanking time**, T_{CSLEB} in [Electrical Characteristics](#). The target is to design L_P and make $t_{ON(min)} \geq T_{CSLEB}$. But in very worst normal operation condition, during the $t_{ON(min)}$, the CS pin OCP should not be triggered, *i.e.*, the CS pin should not reach near 1.41 V defined by V_{OCP} in [Electrical Characteristics](#).

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (18)$$

$$t_{DMAG(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)} \quad (19)$$

8.2.2.7 VS Resistor Divider and Line Compensation

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer auxiliary to primary turns-ratio and the desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (20)$$

$I_{VSL(run)}$ is VS pin run current with a typical value 210 μ A for a design. The low-side VS pin resistor is selected based on desired output over voltage V_{OV} .

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} + V_F) - V_{OVP}} \quad (21)$$

The UCC28742 can maintain tight output current limit over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected gate drive and MOSFET turn-off delay. Assume a 50-ns internal delay in the UCC28742.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times (t_D + t_{GATE_OFF}) \times N_{PA}}{L_P} \quad (22)$$

8.2.2.8 Standby Power Estimate

Assuming no-load standby power is a required design parameter, determine the estimated no-load power based on target converter maximum switching frequency and output power rating. The following equation estimates the stand-by power of the converter.

$$P_{SB_CONV} \cong \frac{P_{OUT} \times f_{MIN}}{\eta \times K_{AM}^2 \times f_{MAX}} \quad (23)$$

The output preload resistor can be estimated by V_{OCV} and the difference between the converter stand-by power and the no-load bias power P_{NL_BIAS} (that can be set as zero initially and adjust it later, particularly through the bench test), then the preload resistor value is estimated in [Equation 24](#) :

$$R_{PL} = \frac{V_{OCV}^2}{P_{SB_CONV} - P_{NL_BIAS}} \quad (24)$$

A physical resistor component R_{PL} may not be needed as other components on the secondary-side such as TL431 can already provide enough preload.

The capacitor bulk voltage for the loss estimation is based on the highest voltage for the standby power measurement, typically as $325 V_{DC}$ (or AC input of 230 Vrms). Power loss of R_{STR} is estimated in [Equation 25](#):

$$P_{RSTR} = \frac{(V_{BULK} - V_{DD})^2}{R_{STR}} \quad (25)$$

The total standby power, including the converter standby power loss, the start-up resistance power, and the snubber power loss, is estimated in [Equation 26](#):

$$P_{SB} = P_{SB_CONV} + P_{RSTR} + P_{SNBR} \quad (26)$$

8.2.2.9 Output Capacitance

The output capacitance value is typically determined by the transient response requirement. [Equation 27](#) assumes that the switching frequency can be at the UCC28742 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN} \left(\frac{1}{f_{SW(min)}} + 50\mu s \right)}{\Delta V_O} \quad (27)$$

Another consideration of the output capacitor(s) is the ripple voltage requirement. The output capacitors and their total ESR are the main factors to determine the output voltage ripple. [Equation 28](#) provides a formula to determine required ESR value R_{ESR} , and [Equation 28](#) provides a formula to determine required capacitance. The total output ripple is the sum of these two parts with scale factors and 10mV to consider other noise as shown in [Equation 30](#),

$$R_{ESR} = \frac{1}{I_{PP(max)} \times N_{PS}} \times V_{RIPPLE_R} \quad (28)$$

$$C_{OUT} = \frac{LP \times I_{PP(max)}^2}{4 \times (V_{OCV})} \times \frac{1}{V_{RIPPLE_C}} \quad (29)$$

$$V_{RIPPLE} = 0.81 \times V_{RIPPLE_R} + 1.15 \times V_{RIPPLE_C} + 10mV \quad (30)$$

Example: if require $V_{RIPPLE} = 70$ mV, assume $0.81 \times V_{RIPPLE_R} = 1.15 \times V_{RIPPLE_C} = 30$ mV, then $R_{ESR} = 4.05$ mΩ, and $C_{OUT} = 643$ μF, with assumption of $L_P = 700$ μH, $I_{PP(max)} = 0.713$ A, $N_{PS} = 13$, $V_{OCV} = 5.3$ V.

8.2.2.10 Feedback Loop Design Consideration

Refer to [Figure 18](#), the UCC28742 converter feedback network is composed of TL431, optocoupler and several resistors and capacitors. R_{FB1} and R_{FB2} set up the converter output regulation point. A series-resistor R_{FB3} is necessary to limit the current into FB and to avoid excess draining of C_{VDD} during this type of transient situation, although connecting the emitter directly to the FB input of the UCC28742 is possible. However, an unload-step response may unavoidably drive the optocoupler into saturation which will overload the FB input with full VDD applied. The value of R_{FB3} is to limit the excess I_{FB} to an acceptable level when the optocoupler is saturated. The R_{FB3} value is chosen to allow the current into the FB pin to reach the 30 μ A, the maximum I_{FB} control level. This will be met if the voltage at I_{FB} can reach 1V at no load conditions. To improve transient response R_{FB3} can be bypassed with C_{FB3} .

R_{FB4} can be used to set a nominal operating current of the optocoupler to improve the current transfer ratio and bandwidth of the optocoupler. For low standby power this operating current level should be kept small since it must be supplied from VDD operating voltage. The value of R_{FB4} is determined empirically due to the variable nature of the specific optocoupler chosen for the design. The ratio of R_{FB4} to R_{FB3} is typically in a range of 1/10 to 1/4 with typical value of R_{FB4} in 4 k Ω to 25 k Ω , and R_{FB3} in 25 k Ω to 200 k Ω . A good starting point is to select R_{FB4} around 4 k Ω and R_{FB3} around 30 k Ω for a design.

The shunt-regulator compensation network, Z_{FB} , is determined using well-established design techniques for control-loop stability. Typically, a Type-II compensation network is used. An effective approach is to set Z_{FB} to be a capacitor, $Z_{FB} = C_{FB}$ to form an integrator, and adding a bypass capacitor R_{FB3} will extend the frequency response of the optocoupler CTR.

Referring again to [Figure 18](#), the shunt-regulator (typically a TL431) current is at about 1 mA even when almost no optocoupler diode current flows. Since even a near-zero diode current establishes a forward voltage, R_{OPT} is selected to provide regulator bias current such as for TL431. The optocoupler input diode must be characterized by the designer to obtain the actual forward voltage versus forward current at the low currents expected. At the full-load condition of the converter, I_{FB} is around 0.5 μ A, I_{CE} may be around (0.4 V / R_{FB4}), and CTR at this level is about 10%, so the diode current typically falls in the range of 25 μ A to 100 μ A. Typical opto-diode forward voltage at this level is about 0.97 V which is applied across R_{OPT} . If R_{OPT} is set equal to 1 k Ω , this provides 970 μ A plus the diode current for I_{OPT} .

As output load decreases, the voltage across the shunt-regulator also decreases to increase the current through the optocoupler diode. This increases the diode forward voltage across R_{OPT} . CTR at no-load (when I_{CE} is higher) is generally a few percent higher than CTR at full-load (when I_{CE} is lower). At steady-state no-load condition, the shunt-regulator current is maximized and can be estimated by and [Equation 31](#). I_{OPTNL} , plus the sum of the leakage currents of all the components on the output of the converter, constitute the total current required for use in to estimate secondary-side standby loss.

$$I_{OPTNL} = \frac{I_{CENL}}{CTR_{NL}} + \frac{V_{OPTNL}}{R_{OPT}} \quad (31)$$

The shunt-regulator voltage can decrease to a minimum, saturated level of about 2 V. To prevent excessive diode current, a series resistor, R_{TL} , is added to limit I_{OPT} to the maximum value necessary for regulation. [Equation 32](#) provides an estimated initial value for R_{TL} , which may be adjusted for optimal limiting later during the prototype evaluation process.

$$R_{TL} = \frac{V_{OUTNL} - V_{OPTNL} - 2 \text{ V}}{I_{OPTNL}} \quad (32)$$

8.2.3 Application Curves

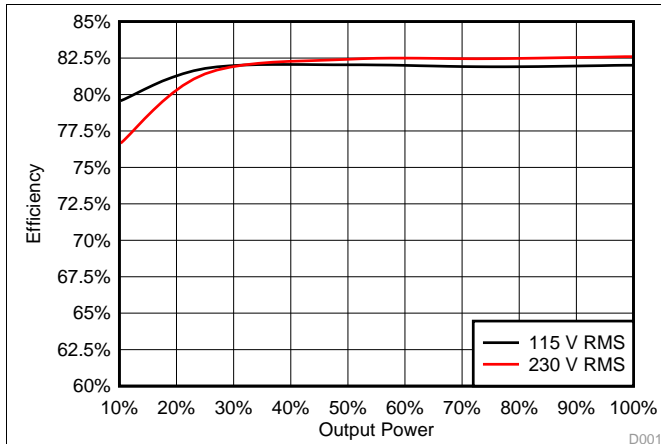


Figure 19. Efficiency

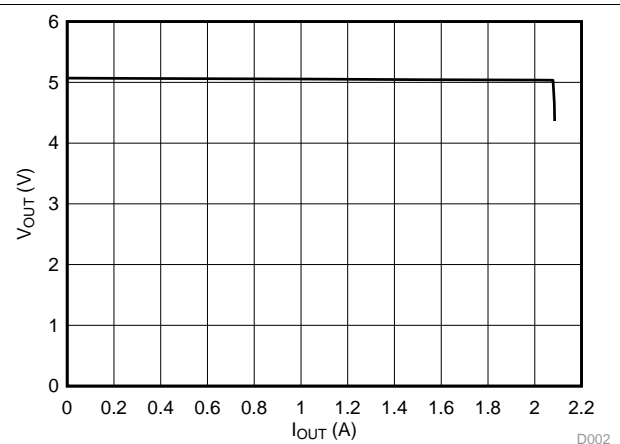


Figure 20. Output V-I Curves

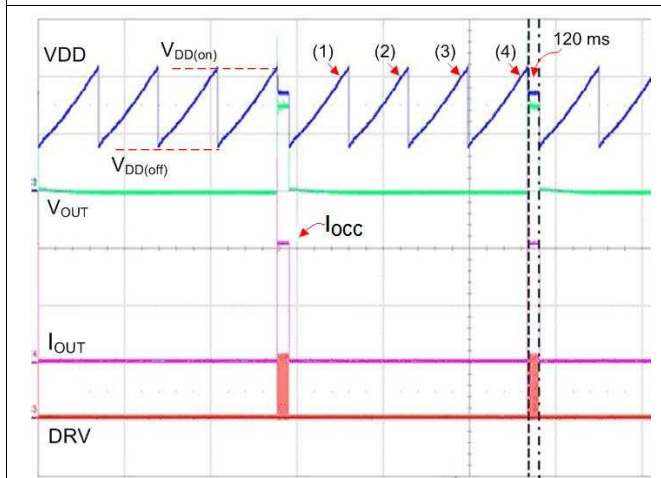


Figure 21. Constant Current Limit and Delayed Shutdown

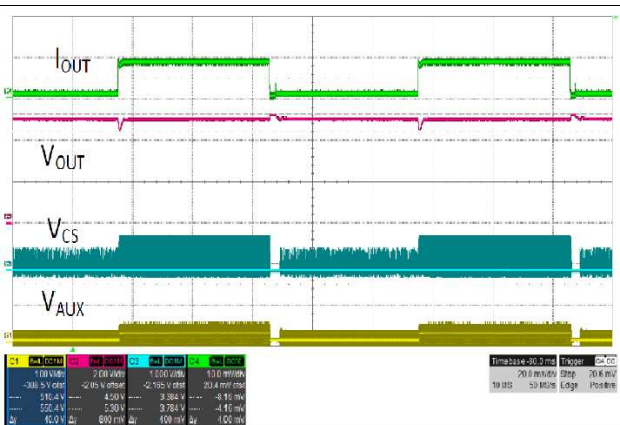


Figure 22. Response to Load Step Changes

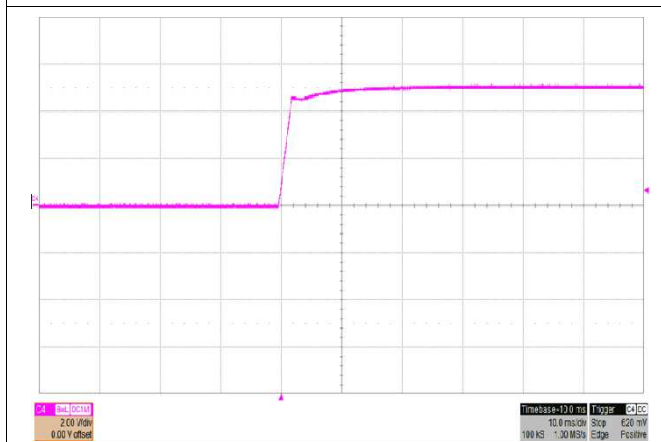


Figure 23. Typical V_{OUT} Start Up

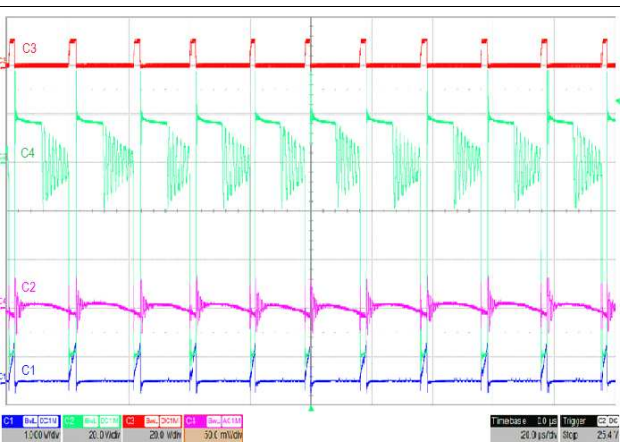


Figure 24. Switching Waveforms (C3 = DRV, C4 = V_{DS}, C2 = V_O Ripple, C1 = I_{PP})

8.3 Do's and Don'ts

- During no-load operation, do allow sufficient margin for variations in VDD level to avoid the UVLO shutdown threshold. Also, at no-load, keep the average switching frequency greater than $1.5 \times f_{SW(min)}$ typical to avoid a rise in output voltage. R_{LC} needs to be adjusted based on no-load operation accounting for both low-line and high-line operation..
- Do clean flux residue and contaminants from the PCB after assembly. Uncontrolled leakage current from VS to GND causes the output voltage to increase, while leakage current from VDD to VS can cause output voltage to increase.
- If ceramic capacitors are used for VDD, do use quality parts with X7R or X5R dielectric rated 50 V or higher to minimize reduction of capacitance due to DC-bias voltage and temperature variation.
- Do not use leaky components if low stand-by input power consumption is a design requirement.
- Do not probe the VS node with an ordinary oscilloscope probe; the probe capacitance can alter the signal and disrupt regulation.
- Do observe VS indirectly by probing the auxiliary winding voltage at R_{S1} and scaling the waveform by the VS divider ratio.
- Do follow [Equation 27](#) to [Equation 30](#) for C_{OUT} .

9 Power Supply Recommendations

The UCC28742 is intended for AC-to-DC adapters and chargers with universal input voltage range of 85 V_{RMS} to 265 V_{RMS} , 47 Hz to 63 Hz, using flyback topology. It can also be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

10 Layout

10.1 Layout Guidelines

In general, try to keep all high current loop areas as small as possible. Keep all traces with high current and high frequency away from other traces in the design. If necessary, high frequency/high current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low-voltage nets.

In order to increase the reliability and feasibility of the project it is recommended to adhere to the following guidelines for PCB layout. Figure 25 shows a typical 10-W, 5-V/2-A converter design schematics.

- Minimize stray capacitance on the VS node. Place the voltage sense resistors (R_{S1} and R_{S2}) close to the VS pin.
- Arrange the components to minimize the loop areas of the switching currents as much as possible. These areas include such loops as the transformer primary winding current loop (a), the MOSFET gate-drive loop (b), the primary snubber loop (c), the auxiliary winding loop (d) and the secondary output current loop (e). In practice, trade-offs may have to be made. Loops with higher current should be minimized with higher priority. As a rule of thumb, the priority goes from high to low as (a) – (e) – (c) – (d) – (b).
- The R_{LC} resistor location is critical. To avoid any dv/dt induced noise (for example MOSFET drain dv/dt) coupled onto this resistor, it is better to place R_{LC} closer to the controller and avoid nearby the MOSFET.
- Using Kelvin connection for long distance connection such as for connection between optocoupler and FB pin.
- To improve thermal performance increase the copper area connected to GND pins.

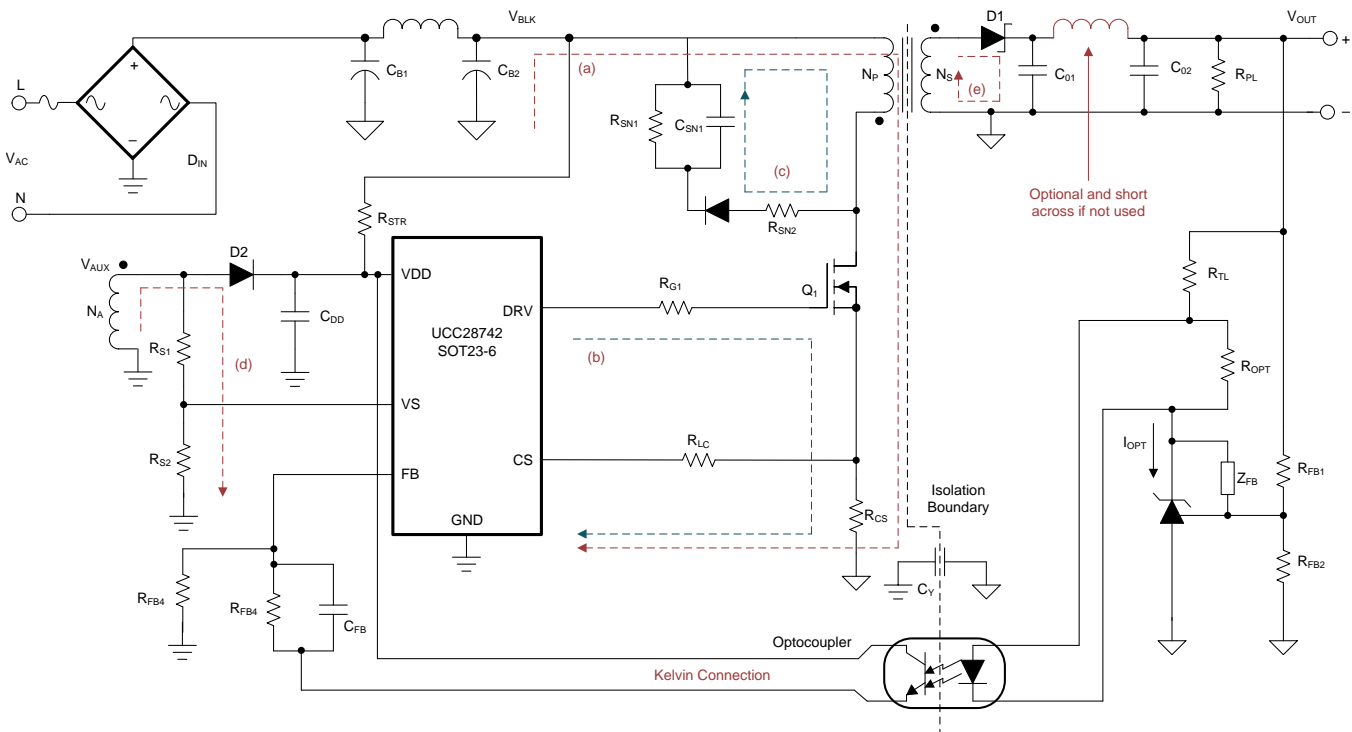


Figure 25. 10-W, 5-V/2-A Converter Schematics

10.2 Layout Example

Figure 26 demonstrates a layout of 10-W, 5-V/2-A converter with trade-offs to minimize the loops while effectively placing components and tracks for low noise operation on a single-layer printed circuit board. In addition to the consideration of minimal loops, one another layout guideline is always to use the device GND as reference point. This applies to both power and signal to return to the device GND pin (pin 5).

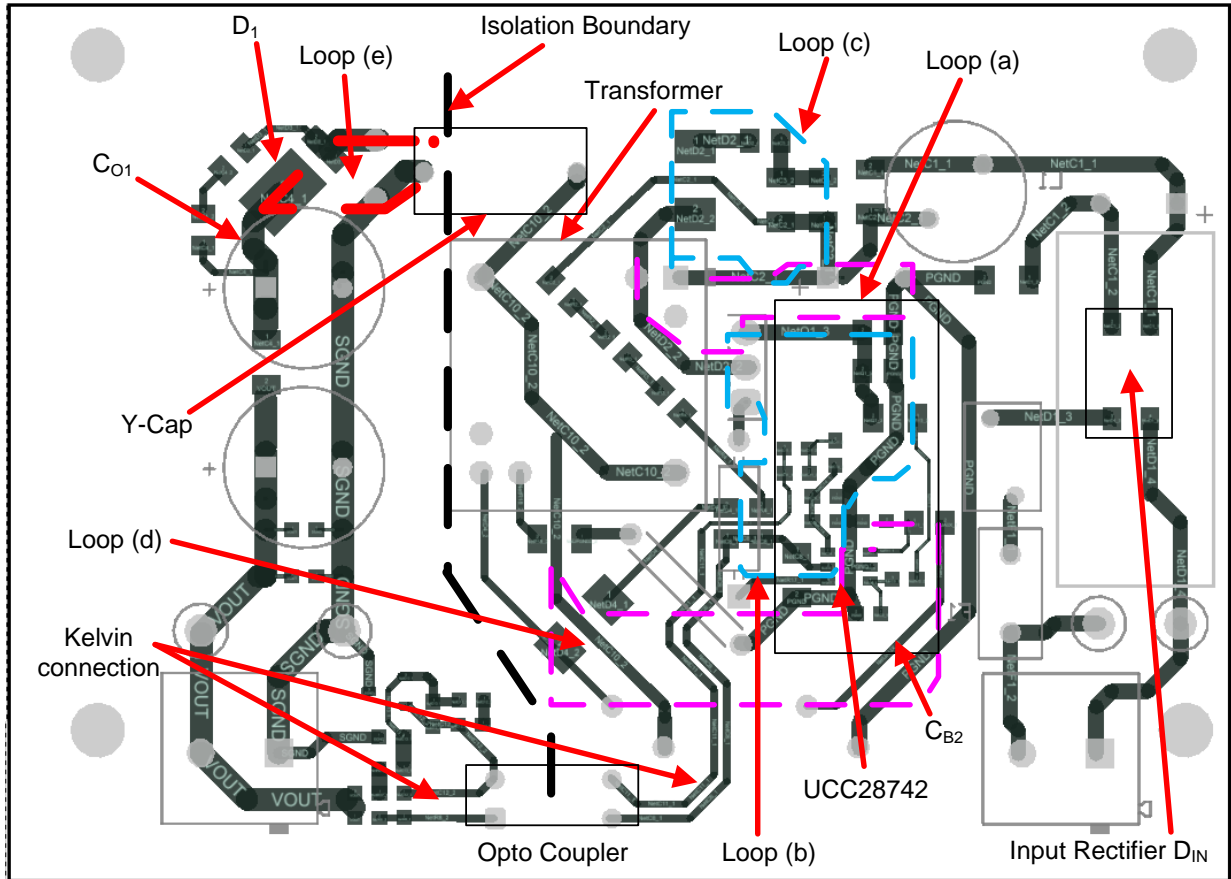


Figure 26. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the UCC28742 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.1.2 Device Nomenclature

11.1.2.1 Capacitance Terms in Farads

C_{BULK}	total input capacitance of C_{B1} and C_{B2} .
C_{DD}	minimum required capacitance on the VDD pin.
C_{OUT}	minimum output capacitance required.

11.1.2.2 Duty Cycle Terms

D_{MAGCC}	secondary diode conduction duty cycle in CC, 0.475.
D_{MAX}	maximum MOSFET on-time duty cycle.

11.1.2.3 Frequency Terms in Hertz

f_{LINE}	minimum line frequency.
f_{MAX}	target full-load maximum switching frequency of the converter.
f_{MIN}	minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device.
$f_{SW(lim)}$	switching frequency in transient after a load step-down change
$f_{SW(min)}$	minimum switching frequency (see the Electrical Characteristics table)
$f_{SW(max)}$	maximum switching frequency (see the Electrical Characteristics table)
$f_{SW(standby)}$	switching frequency before load change at light load condition

11.1.2.4 Current Terms in Amperes

I_{OCC}	converter output constant-current target.
I_{OR}	converter rated output current.
$I_{PP(max)}$	maximum transformer primary current.
I_{START}	start-up bias supply current (see the Electrical Characteristics table).
I_{TRAN}	required positive load-step current.

Device Support (continued)

$I_{VSL(run)}$ VS pin run current (see the [Electrical Characteristics](#) table).

I_{WAIT} VDD bias current during the Wait-state . (see the [Electrical Characteristics](#) table).

11.1.2.5 Current and Voltage Scaling Terms

K_{AM} maximum-to-minimum peak primary current ratio (see the [Electrical Characteristics](#) table).

K_{Co} stability factor of 100, used in calculations for C_{OUT} .

K_{LC} current-scaling constant (see the [Electrical Characteristics](#) table).

Device Support (continued)
11.1.2.6 Transformer Terms

L_P	transformer primary inductance.
L_S	transformer secondary inductance.
N_{AS}	transformer auxiliary-to-secondary turns ratio.
N_{PA}	transformer primary-to-auxiliary turns ratio.
N_{PS}	transformer primary-to-secondary turns ratio.
N_A	number of turns of transformer auxiliary winding.
N_P	number of turns of transformer primary winding.
N_S	number of turns of transformer secondary winding.

11.1.2.7 Power Terms in Watts

P_{IN}	converter maximum input power.
P_{OUT}	full-load output power of the converter.
P_{RSTR}	VDD start-up resistor power dissipation.
P_{SB}	total stand-by power.
P_{SB_CONV}	P_{SB} minus start-up resistor and snubber losses.

11.1.2.8 Resistance Terms in Ω

R_{CS}	primary current programming resistance
R_{ESR}	total ESR of the output capacitor(s).
R_{PL}	preload resistance on the output of the converter.
R_{S1}	high-side VS pin resistance.
R_{S2}	low-side VS pin resistance.
R_{STR}	Start-up resistor connected between bulk voltage and VDD

11.1.2.9 Timing Terms in Seconds

t_D	current-sense delay.
$t_{DMAG(min)}$	minimum secondary rectifier conduction time.
t_{GATE_OFF}	primary-side main MOSFET turn-off time.
$t_{ON(min)}$	minimum MOSFET on time.
t_R	period of the resonant ringing after t_{DMAG} .
t_{STR}	power-on delay time due to charge-up time needed for VDD capacitance C_{DD} .
t_{ZTO}	t_{ZTO} : zero-crossing timeout delay without zero-crossing detected on VS (see the Electrical Characteristics table).

Device Support (continued)

11.1.2.10 Voltage Terms in Volts

V_{BLK} or V_{BULK} bulk capacitor voltage.

$V_{BULK(max)}$ highest bulk capacitor voltage for stand-by power measurement.

$V_{BULK(min)}$ minimum voltage on C_{B1} and C_{B2} at full power.

$V_{BULK(run)}$ converter start-up (run) bulk voltage.

V_{CBC} cable compensation voltage at the output of board-end at full load.

V_{CCR} constant-current regulating voltage (see the [Electrical Characteristics](#) table).

V_{CCUV} VS threshold for constant-current output voltage shutdown (see the [Electrical Characteristics](#) table).

$V_{CST(max)}$ CS pin maximum current-sense threshold (see the [Electrical Characteristics](#) table).

$V_{CST(min)}$ CS pin minimum current-sense threshold (see the [Electrical Characteristics](#) table).

$V_{DD(off)}$ or $V_{VDD(off)}$ UVLO turn-off voltage (see the [Electrical Characteristics](#) table).

$V_{VDD(on)}$ or $V_{DD(on)}$ UVLO turn-on voltage (see the [Electrical Characteristics](#) table).

V_F secondary rectifier forward voltage drop at near-zero current.

V_{FA} auxiliary rectifier forward voltage drop.

V_{LK} estimated leakage inductance energy reset voltage.

V_{OCV} regulated output voltage of the converter.

V_{OCC} target lowest converter output voltage in constant-current regulation.

V_{OVL} The output voltage reaches V_{OVL} when output current reaches its limit I_{OCC} ; V_{OVL} is determined by I_{OCC} and the expected minimum load resistance R_{LOAD} at I_{OCC} , *i.e.*, $V_{OVL} = I_{OCC} \times R_{LOAD}$.

V_{RIPPLE} output peak-to-peak ripple voltage at full-load.

V_{VSR} CV regulating level at the VS input (see the [Electrical Characteristics](#) table).

11.1.2.11 AC Voltage Terms in V_{RMS}

$V_{IN(max)}$ maximum input voltage to the converter.

$V_{IN(min)}$ minimum input voltage to the converter.

$V_{IN(run)}$ converter input start-up (run) voltage.

11.1.2.12 Efficiency Terms

η converter overall efficiency.

η_{10} efficiency at 10% load.

η_{AVG} arithmetic average of efficiency at load level 25%, 50%, 75%, and 100% .

η_{XFMR} transformer primary-to-secondary power transfer efficiency.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [Using the UCC28742-1EVM-724, Evaluation Module, SLUUBF1](#)
- [UCC28742 Design Calculator SLUC652](#)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28742DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742	Samples
UCC28742DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U742	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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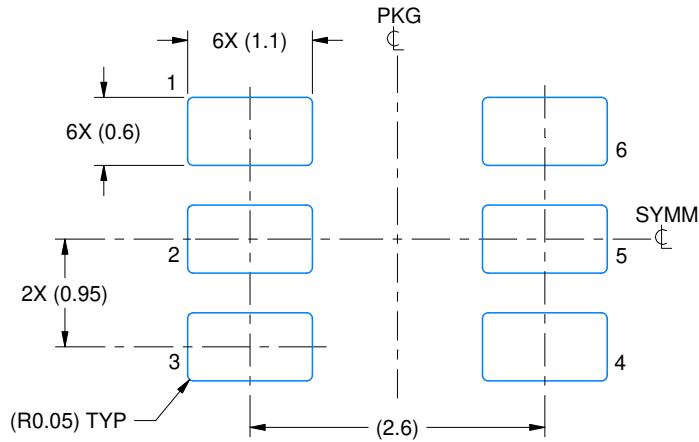
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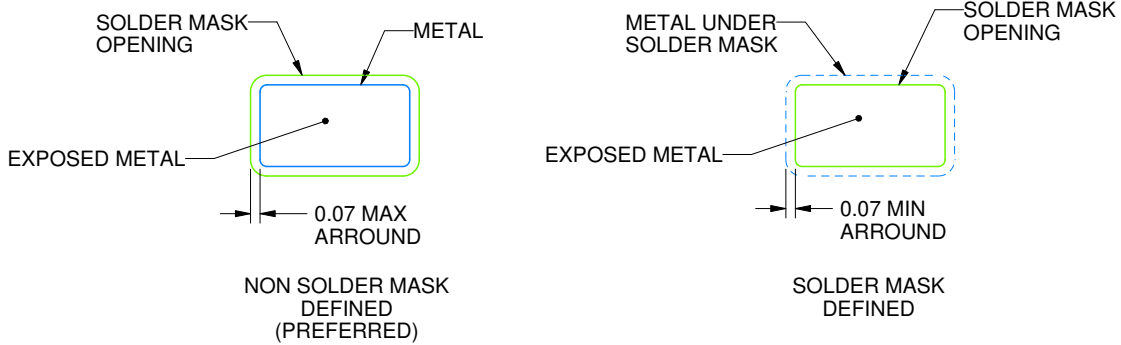
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/D 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

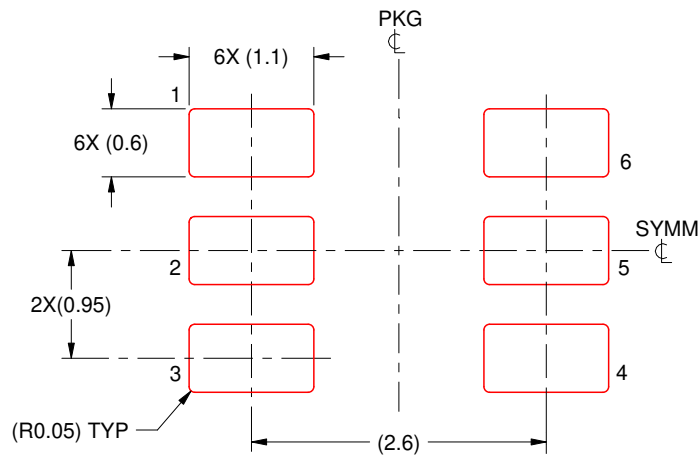
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/D 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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