3.3V HCSL PCIe 2.0 Low Jitter XO

SH

7.0 x 5.0mm Ceramic SMD

Product Features

- Provides 100 MHz HCSL output for interfacing to standard PCIe devices
- <2.5 ps max, 1.8ps typ RMS jitter (measured per PCI-SIG for PCIe 2.0 reference clock) with advanced non-PLL, patented XP Technology. Tight stability over a broad range of operating conditions
- Thicker crystal than conventional overtone for improved reliablity
- RoHS compliant

Product Description

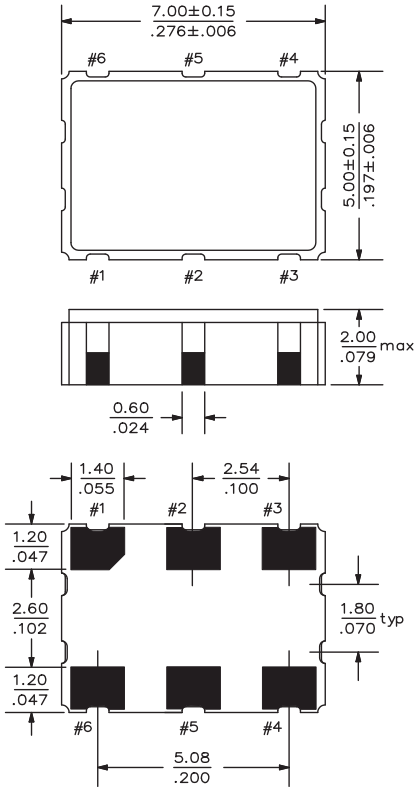
The SH Series 3.3V HCSL PCIe 2.0 crystal clock oscillator achieves superb jitter and stability over a broad range of operating conditions. The output clock signal, generated internally with a patented oscillator design, provides HCSL differential levels. The device, available on tape and reel, is contained in a 7.0 x 5.0mm surface-mount ceramic package.

Applications

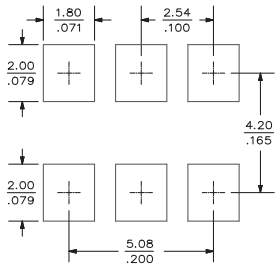
The SH Series is an ideal reference clock for high-speed applications requiring low jitter, 100 MHz HCSL Reference Clock, including:

- Server
- SAS
- SATA
- Graphics Card
- Network Switch/Router
- Telecom Switch
- Media Box

Package:



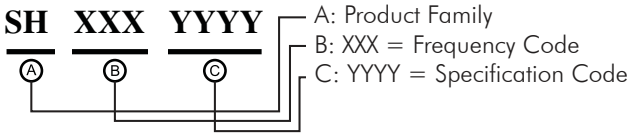
Recommended Land Pattern:



Pin Functions:

Pin	Function
1	OE
2	NC
3	V_{EE}
4	Q Output
5	$\overline{Q}$ Output
6	V_{CC}

Part Ordering Information:



Following the above format, Saronix-eCera part numbers will be assigned upon confirmation of exact customer requirements.

Electrical Performance (Over -40 to 85°C)

Parameter	Min.	Typ.	Max.	Units	Notes
Output Frequency		100		MHz	As specified
Supply Voltage	2.97	3.3	3.63	V	
Supply Current, Output Enabled		50	60	mA	100 MHz
Supply Current, Output Disabled			25	mA	100 MHz
Frequency Stability			±50	ppm	See Note 1 below
Operating Temperature Range	-40		+85	°C	As specified
Output Logic 0, V_{OL}	-0.15		0.15	V	
Output Logic 1, V_{OH}		0.7	0.85	V	
Output Load	See Test Diagram				output requires termination
Duty Cycle	45		55	%	measured 50% of waveform
Rise and Fall Time			700	ps	measured from V_{OL}=0.175V to V_{OH} = 0.525V
Jitter, Phase		1.8	2.5	ps RMS	As defined by PCI-SIG for PCIeG2 reference clock

Notes:
1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (5 years at 40°C average effective ambient temperature), shock and vibration
2. Note: For specifications other than those listed, please contact sales.

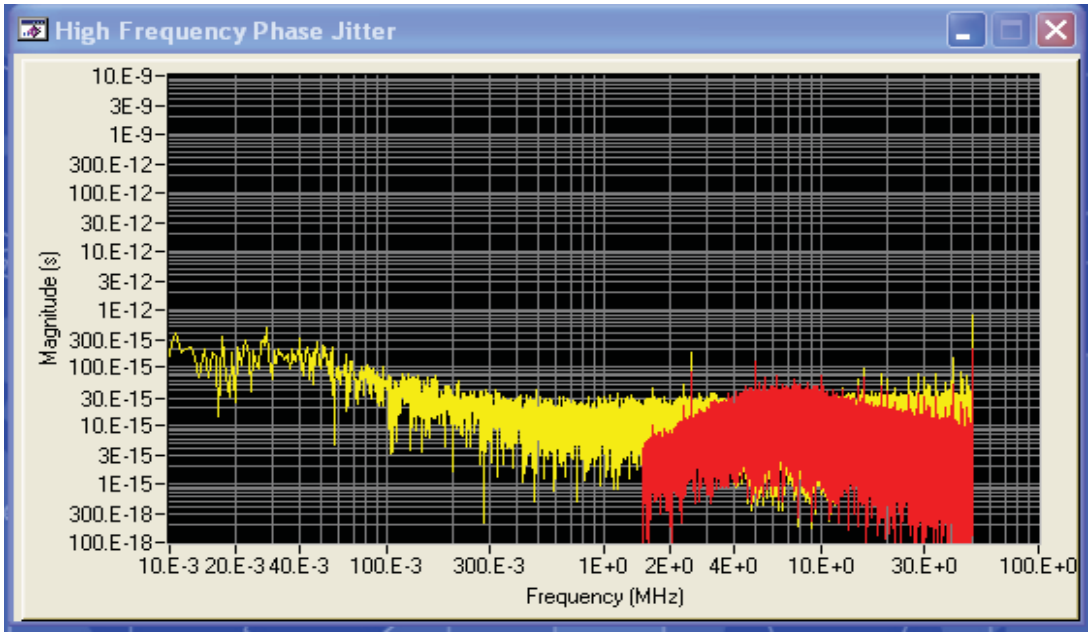
Output Enable / Disable Function

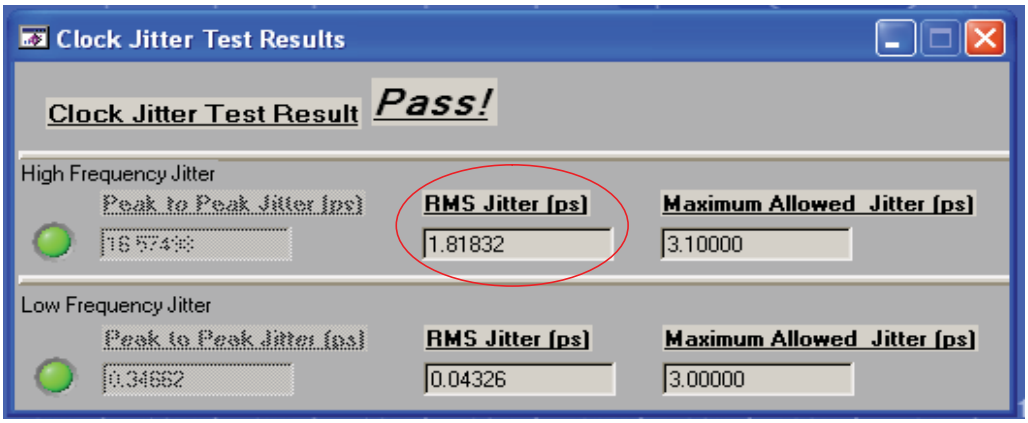
Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (OE pin), Output Enable	2.2			V	or open
Input Voltage (OE pin), Output Disable			0.8	V	Outputs disabled to Hi-Z
Internal Pull-up Resistance	50			kΩ	
Output Disable Delay			200	ns	
Output Enable Delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage Temperature	-55		+125	°C	

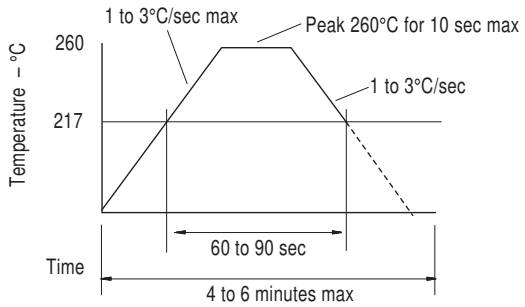
High Frequency Phase Jitter



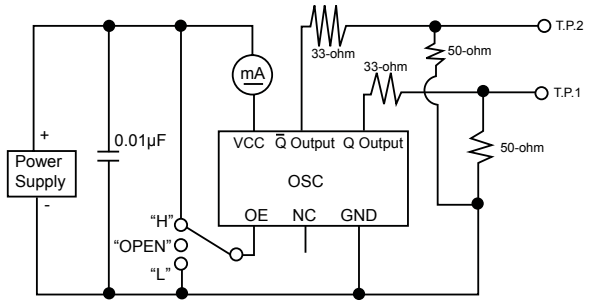


Reflow Soldering Profile

As per IPC/JEDEC J-STD-020C

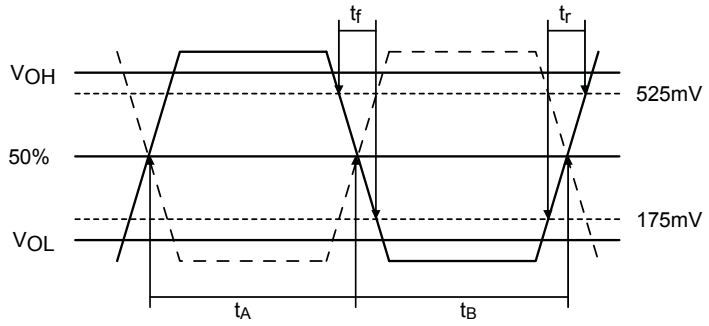


Test Circuit



Reset Function:
Logic 0 On Pad 1 - Disable Output to High Impedance
Logic 1 or Open On Pad 1 - Oscillator Output Enabled

Output Waveform



Duty cycle = 100% × (t_A) / (t_A + t_B)

Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2x10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)