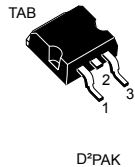
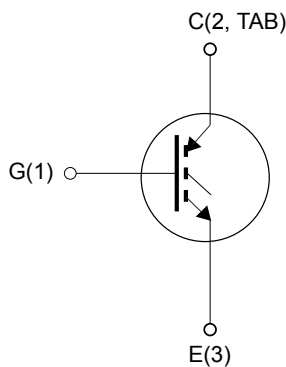


## Trench gate field-stop, 650 V, 20 A, high-speed HB2 series IGBT in a D<sup>2</sup>PAK package


 D<sup>2</sup>PAK


G1C2TE3



### Features

- Maximum junction temperature :  $T_J = 175\text{ }^\circ\text{C}$
- Low  $V_{CE(sat)} = 1.65\text{ V (typ.) @ } I_C = 20\text{ A}$
- Minimized tail current
- Tight parameter distribution
- Low thermal resistance
- Positive  $V_{CE(sat)}$  temperature coefficient

### Applications

- Welding
- Power factor correction
- UPS
- Solar inverters
- Chargers

### Description

The newest IGBT 650 V HB2 series represents an evolution of the advanced proprietary trench gate field-stop structure. The performance of the HB2 series is optimized in terms of conduction, thanks to a better  $V_{CE(sat)}$  behavior at low current values, as well as in terms of reduced switching energy. The result is a product specifically designed to maximize efficiency for a wide range of fast applications.

#### Product status link

[STGB20H65FB2](#)

#### Product summary

<b>Order code</b>	STGB20H65FB2
<b>Marking</b>	G20H65FB2
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{GE} = 0$ V)	650	V
$I_C$	Continuous collector current at $T_C = 25$ °C	40	A
	Continuous collector current at $T_C = 100$ °C	25	
$I_{CP}^{(1)(2)}$	Pulsed collector current	60	
$V_{GE}$	Gate-emitter voltage	$\pm 20$	V
	Transient gate-emitter voltage ( $t_p \leq 10$ $\mu$ s)	$\pm 30$	
$P_{TOT}$	Total power dissipation at $T_C = 25$ °C	147	W
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_J$	Operating junction temperature range	-55 to 175	

1. Defined by design, not subject to production test.
2. Pulse width is limited by maximum junction temperature.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case	1.02	°C/W
$R_{thJA}$	Thermal resistance junction-ambient	62.5	

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 3. Static characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}, I_C = 1\text{ mA}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}, I_C = 20\text{ A}$		1.65	2.1	V
		$V_{GE} = 15\text{ V}, I_C = 20\text{ A}, T_J = 125\text{ °C}$		1.95		
		$V_{GE} = 15\text{ V}, I_C = 20\text{ A}, T_J = 175\text{ °C}$		2.1		
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 1\text{ mA}$	5	6	7	V
$I_{CES}$	Collector cut-off current	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$			25	$\mu\text{A}$
$I_{GES}$	Gate-emitter leakage current	$V_{CE} = 0\text{ V}, V_{GE} = \pm 20\text{ V}$			$\pm 250$	nA

**Table 4. Dynamic characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ies}$	Input capacitance	$V_{CE} = 25\text{ V}, f = 1\text{ MHz}, V_{GE} = 0\text{ V}$	-	1010	-	$\mu\text{F}$
$C_{oes}$	Output capacitance		-	81	-	
$C_{res}$	Reverse transfer capacitance		-	26	-	
$Q_g$	Total gate charge	$V_{CC} = 520\text{ V}, I_C = 20\text{ A}, V_{GE} = 0\text{ to }15\text{ V}$ (see Figure 22. Gate charge test circuit)	-	56	-	nC
$Q_{ge}$	Gate-emitter charge		-	9.4	-	
$Q_{gc}$	Gate-collector charge		-	27.8	-	

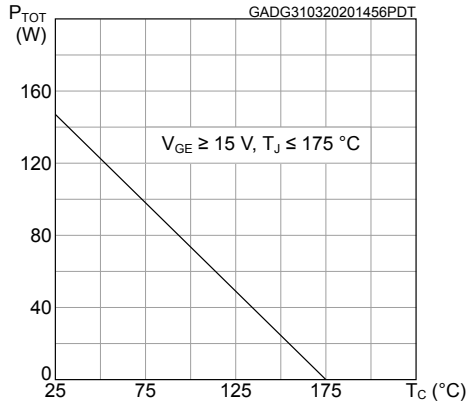
**Table 5. Switching characteristics (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$ , $I_C = 20\text{ A}$ , $V_{GE} = 15\text{ V}$ , $R_G = 10\ \Omega$ (see Figure 21. Test circuit for inductive load switching)	-	16	-	ns
$t_r$	Current rise time		-	8	-	ns
$E_{on}^{(1)}$	Turn-on switching energy		-	265	-	$\mu\text{J}$
$t_{d(off)}$	Turn-off delay time		-	78.8	-	ns
$t_f$	Current fall time		-	35	-	ns
$E_{off}^{(2)}$	Turn-off switching energy		-	214	-	$\mu\text{J}$
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$ , $I_C = 20\text{ A}$ , $V_{GE} = 15\text{ V}$ , $R_G = 10\ \Omega$ , $T_J = 175\text{ }^\circ\text{C}$ (see Figure 21. Test circuit for inductive load switching)	-	17	-	ns
$t_r$	Current rise time		-	9	-	ns
$E_{on}^{(1)}$	Turn-on switching energy		-	556	-	$\mu\text{J}$
$t_{d(off)}$	Turn-off delay time		-	98	-	ns
$t_f$	Current fall time		-	80	-	ns
$E_{off}^{(2)}$	Turn-off switching energy		-	378	-	$\mu\text{J}$

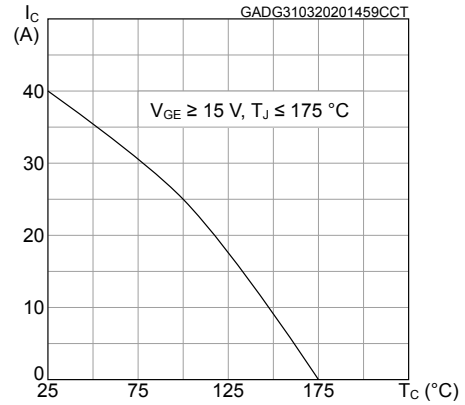
1. Including the reverse recovery of the external diode. The diode is the same of the co-packed STGWA20H65DFB2.
2. Including the tail of the collector current.

## 2.1 Electrical characteristics (curves)

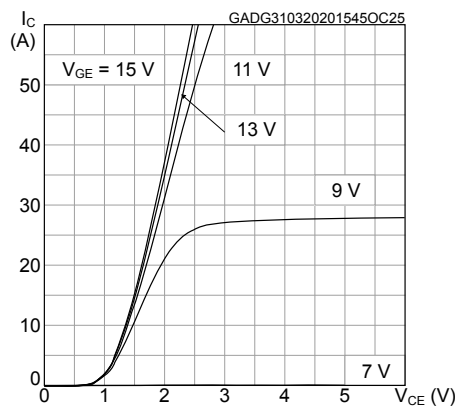
**Figure 1. Power dissipation vs case temperature**



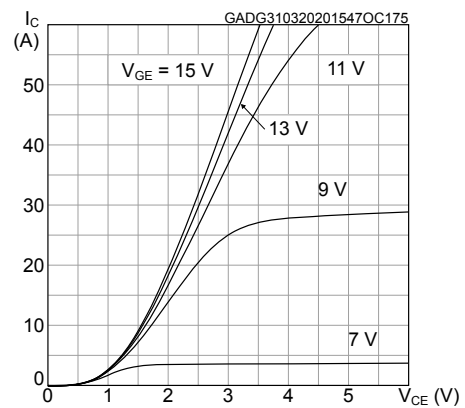
**Figure 2. Collector current vs case temperature**



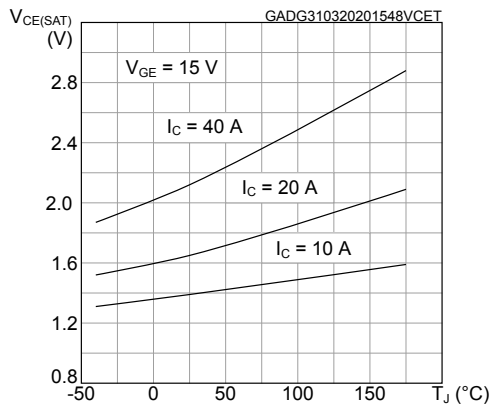
**Figure 3. Output characteristics (T<sub>J</sub> = 25 °C)**



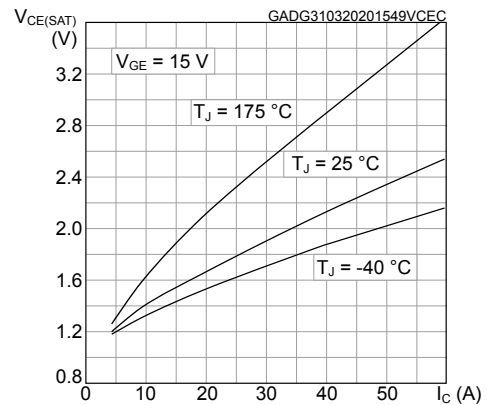
**Figure 4. Output characteristics (T<sub>J</sub> = 175 °C)**



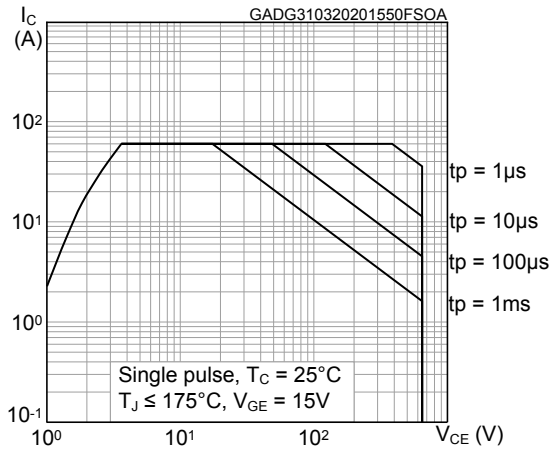
**Figure 5. V<sub>CE(sat)</sub> vs junction temperature**



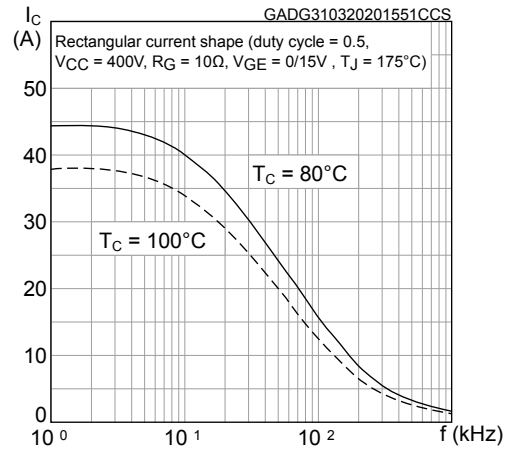
**Figure 6. V<sub>CE(sat)</sub> vs collector current**



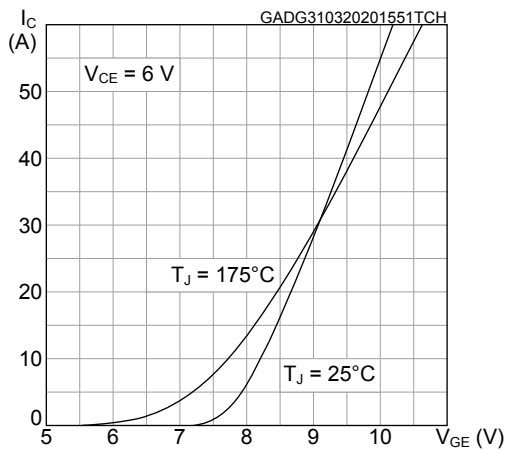
**Figure 7. Forward bias safe operating area**



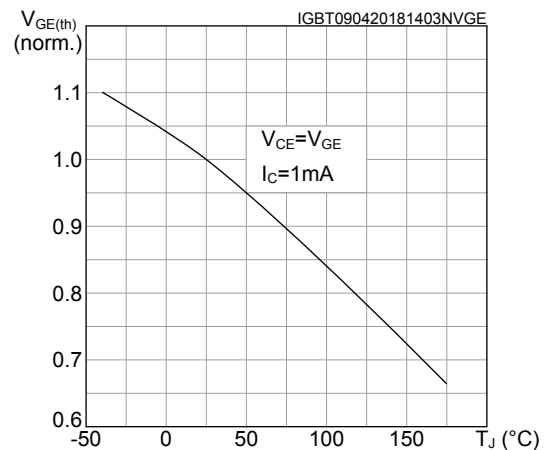
**Figure 8. Collector current vs switching frequency**



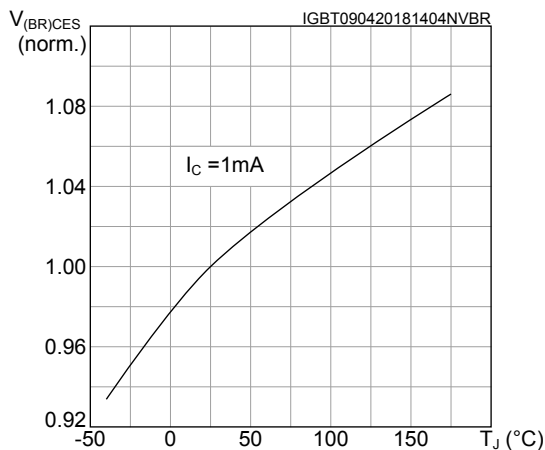
**Figure 9. Transfer characteristics**



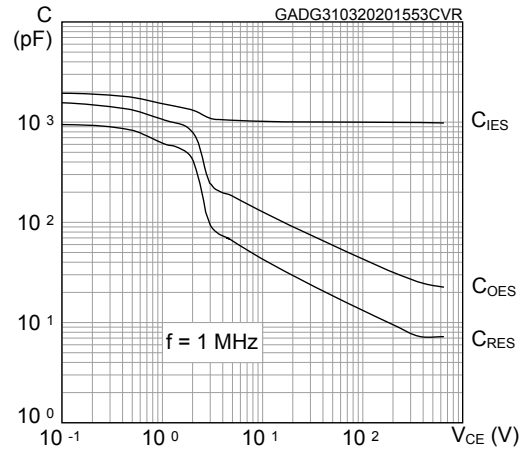
**Figure 10. Normalized V\_GE(th) vs junction temperature**



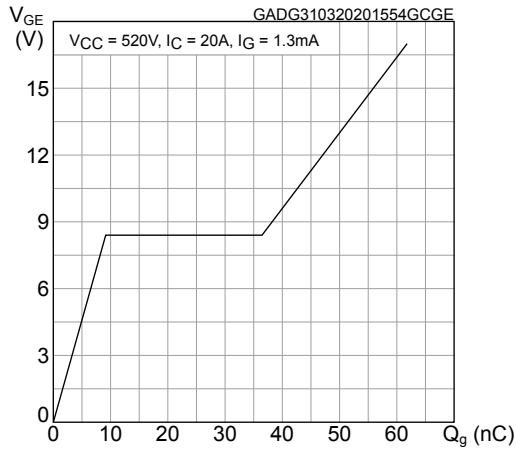
**Figure 11. Normalized V\_(BR)CES vs junction temperature**



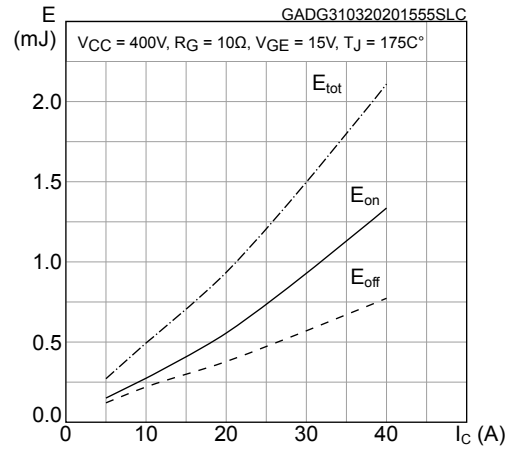
**Figure 12. Capacitance variations**



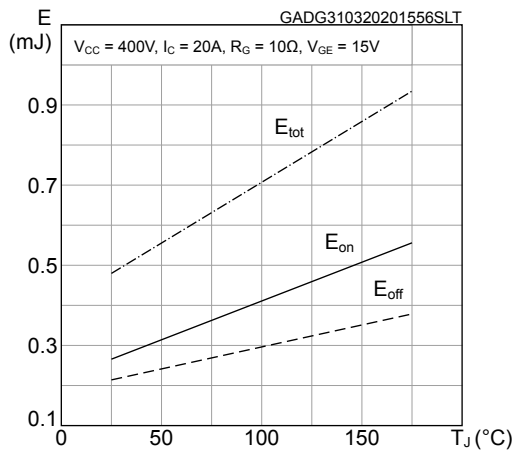
**Figure 13. Gate charge vs gate-emitter voltage**



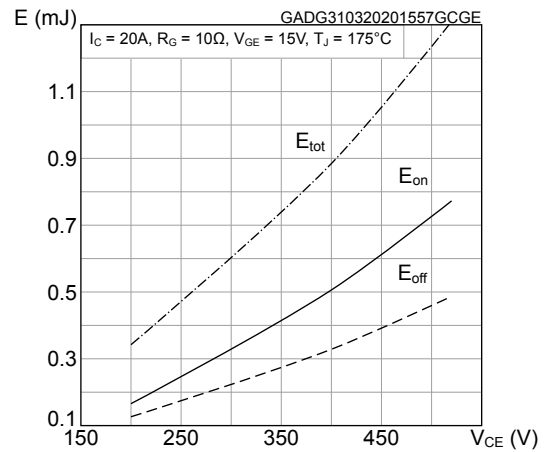
**Figure 14. Switching energy vs collector current**



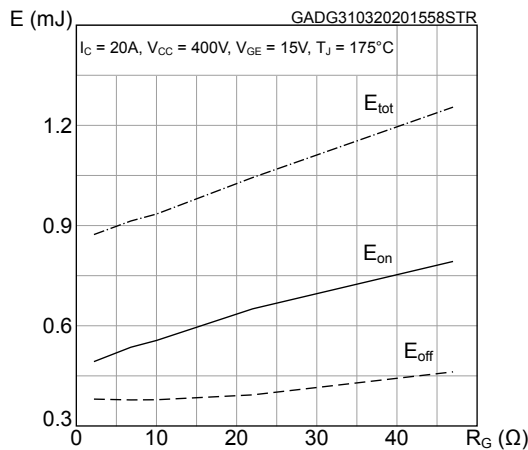
**Figure 15. Switching energy vs temperature**



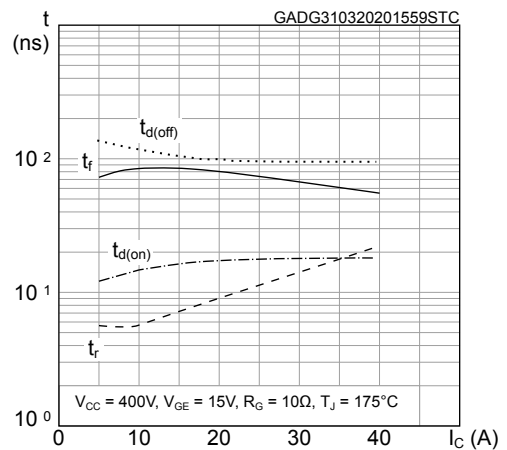
**Figure 16. Switching energy vs collector emitter voltage**



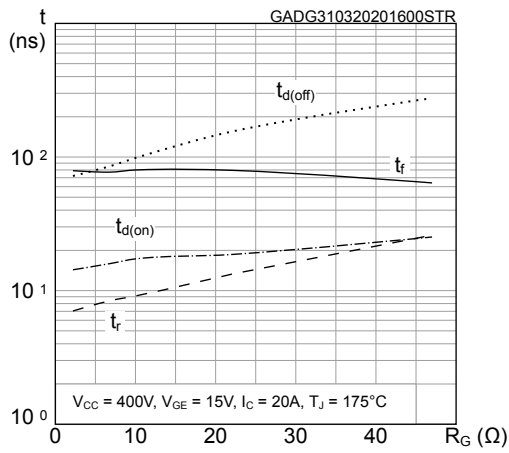
**Figure 17. Switching energy vs gate resistance**



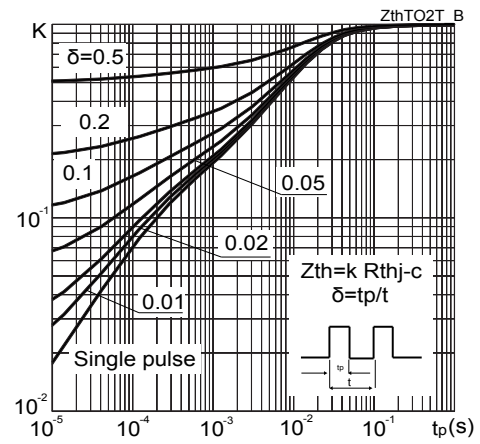
**Figure 18. Switching times vs collector current**



**Figure 19. Switching times vs gate resistance**

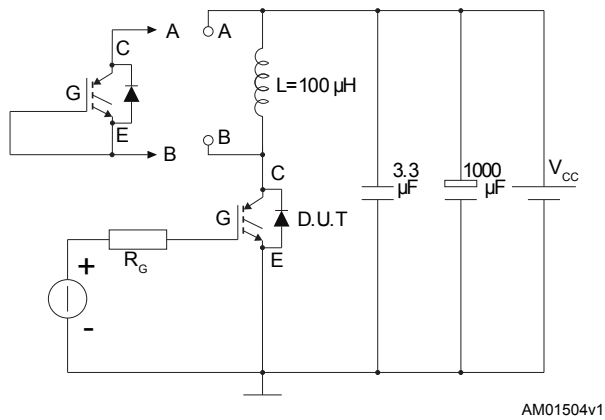
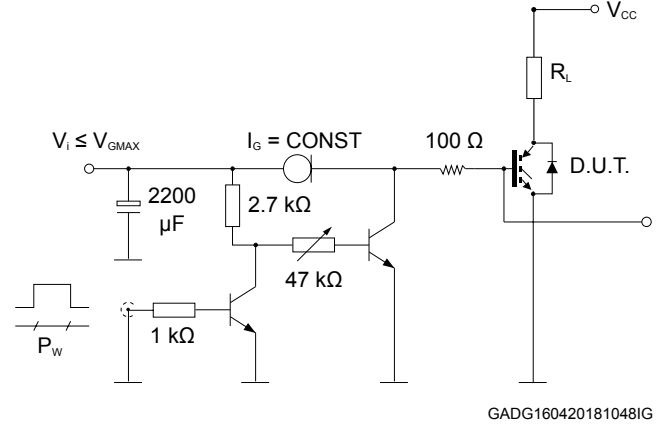
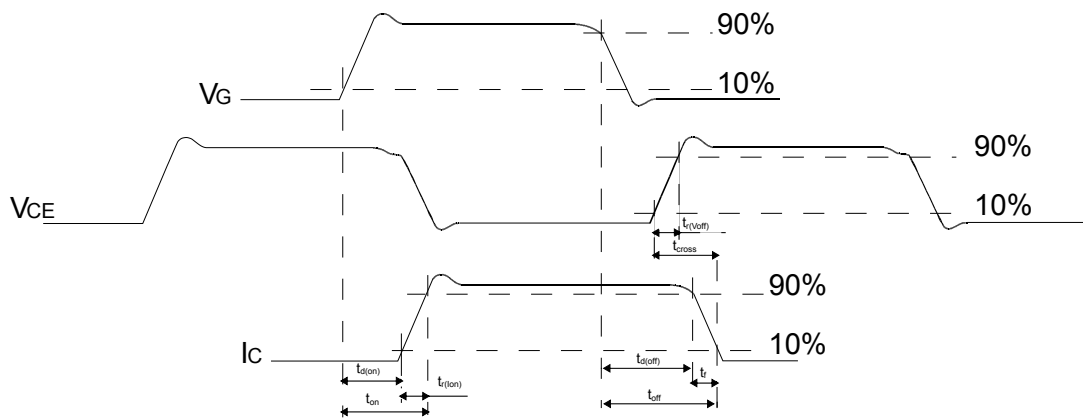


**Figure 20. Thermal impedance**





### 3 Test circuits

**Figure 21. Test circuit for inductive load switching**

**Figure 22. Gate charge test circuit**

**Figure 23. Switching waveform**


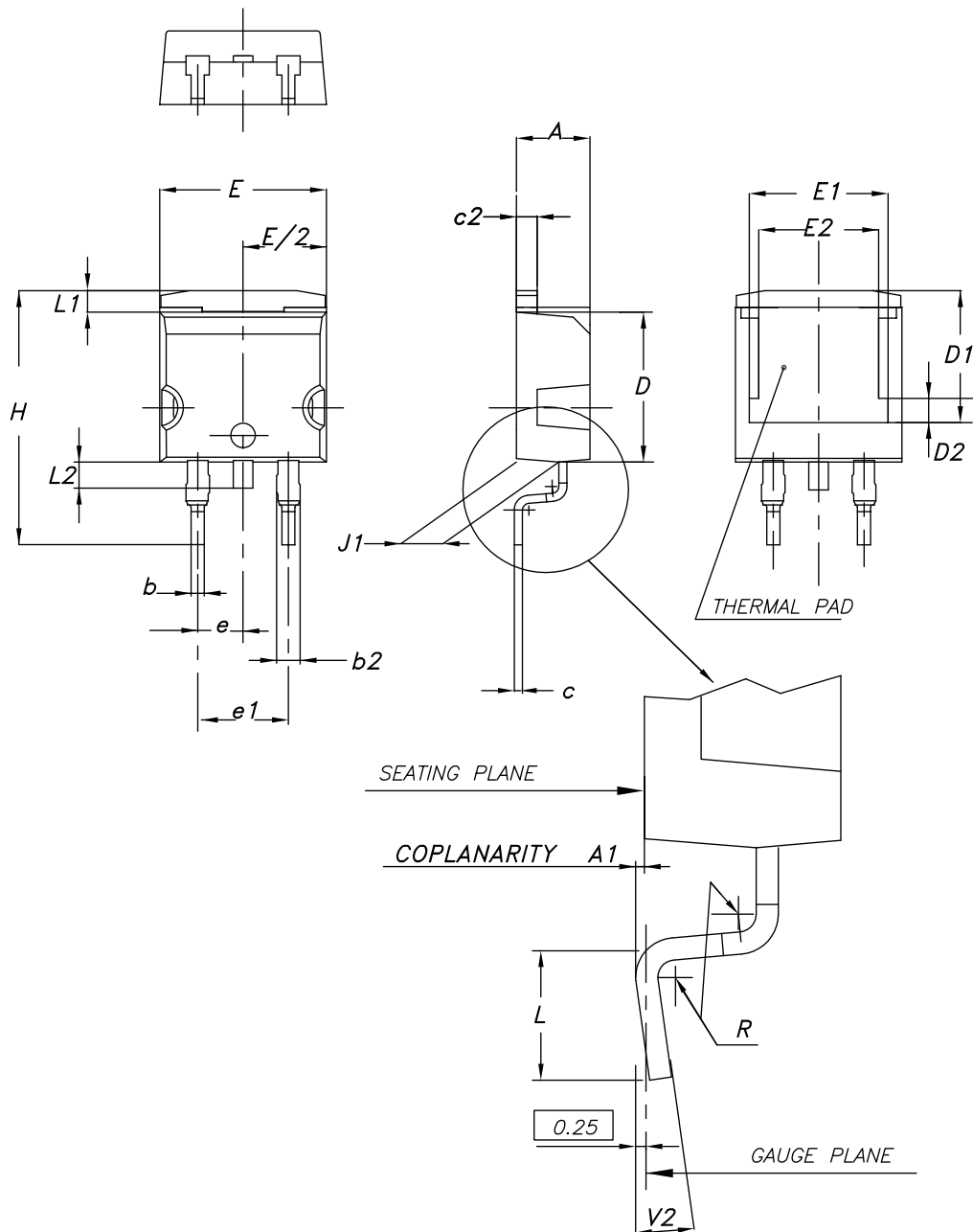
AM01506v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information

Figure 24. D<sup>2</sup>PAK (TO-263) type A2 package outline

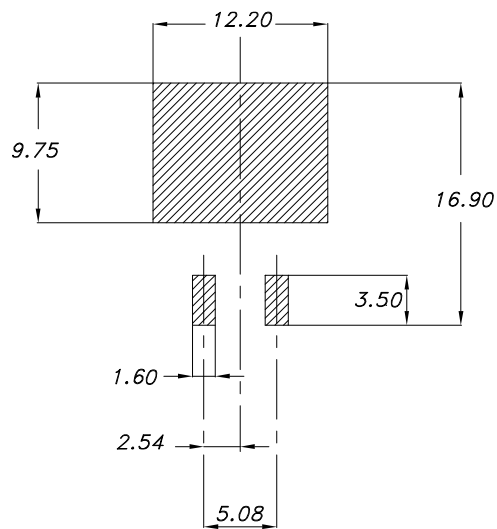


0079457\_A2\_26

**Table 6. D<sup>2</sup>PAK (TO-263) type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

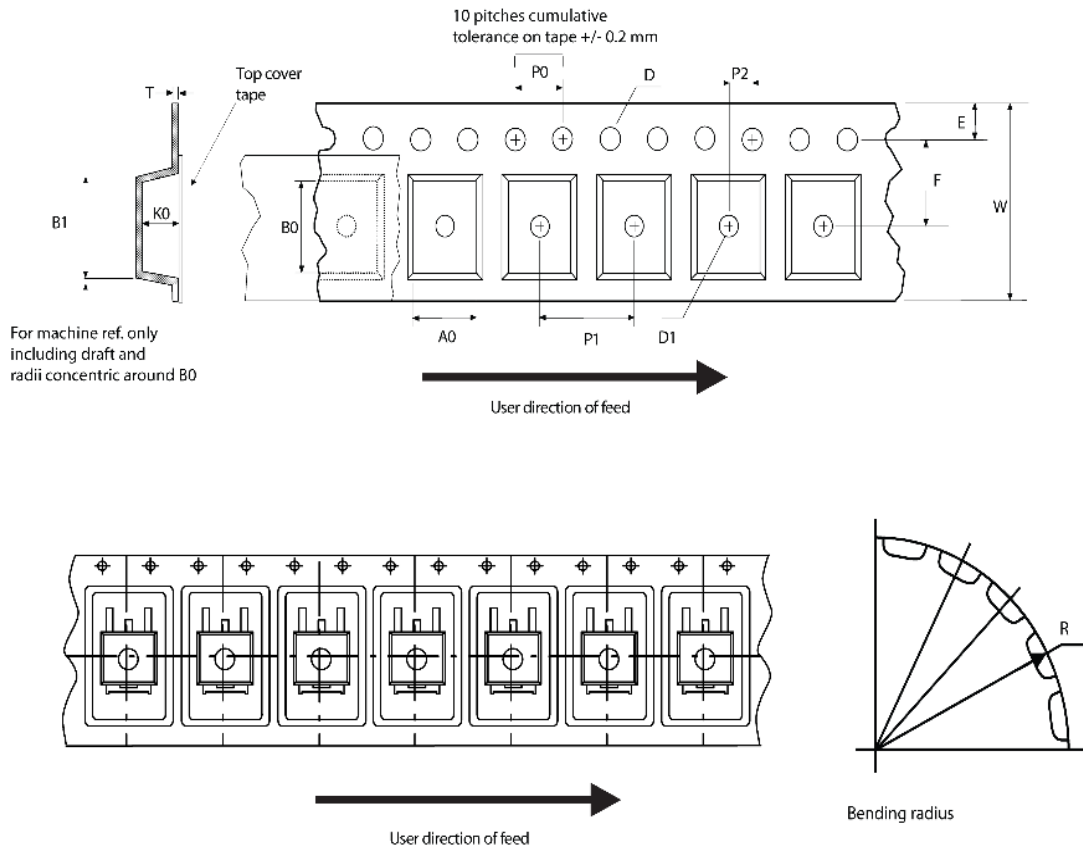
**Figure 25. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**



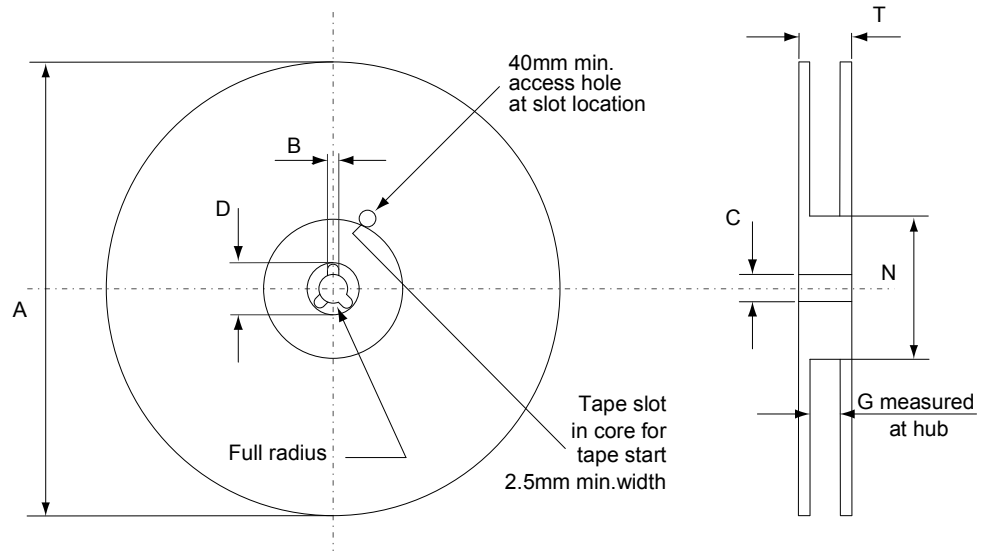
Footprint\_26

## 4.2 D<sup>2</sup>PAK packing information

Figure 26. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 27. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 7. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel			
Dim.	mm		Dim.	mm		
	Min.	Max.		Min.	Max.	
A0	10.5	10.7	A		330	
B0	15.7	15.9	B	1.5		
D	1.5	1.6	C	12.8	13.2	
D1	1.59	1.61	D	20.2		
E	1.65	1.85	G	24.4	26.4	
F	11.4	11.6	N	100		
K0	4.8	5.0	T		30.4	
P0	3.9	4.1	Base quantity Bulk quantity			
P1	11.9	12.1				1000
P2	1.9	2.1				1000
R	50					
T	0.25	0.35				
W	23.7	24.3				

## Revision history

**Table 8. Document revision history**

Date	Version	Changes
22-May-2020	1	First release.

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