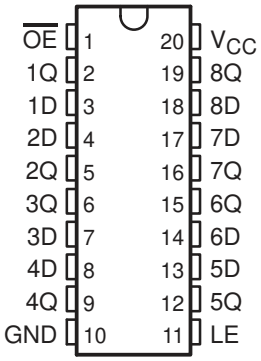
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **High-Impedance State During Power Up and Power Down**
- **3-State True Outputs Drive Bus Lines or Buffer-Memory Address Registers**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



description

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the SN64BCT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the enable is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

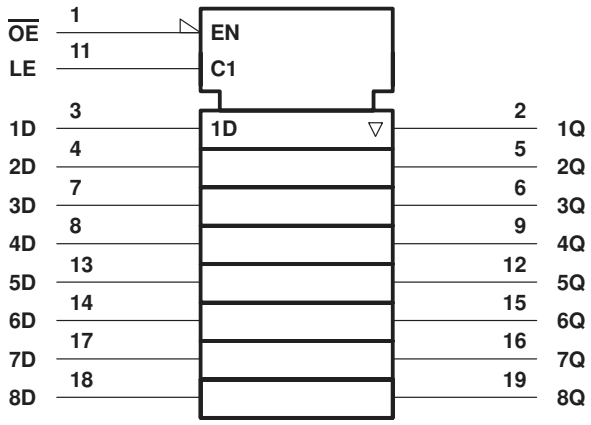
The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT373 is characterized for operation from –40°C to 85°C and 0°C to 70°C.

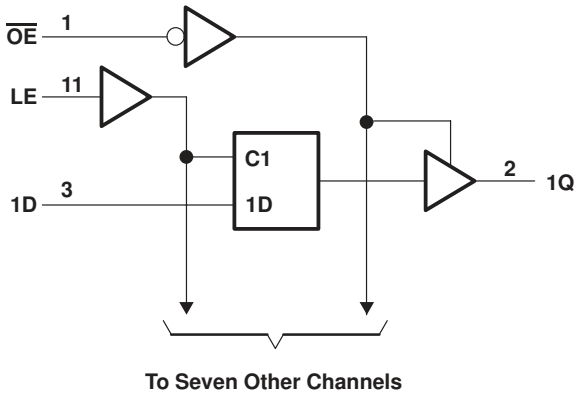
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O . . . . . 128 mA
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	2			μs/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –3 mA		2.4	3.3		V
		I_{OH} = –15 mA		2	3.1		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 64 mA			0.42	0.55	V
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				0.4	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V				–0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0		–100		–225	mA
I_{OZ}	V_{CC} = 0 to 2.3 V (power up)	V_O = 2.7 V or 0.5 V,	$\overline{OE}$ = 0.8 V			±50	µA
	V_{CC} = 1.8 V to 0 (power down)					±50	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–50	µA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open			37	60	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open			2	5	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open			5	8	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V			11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended range of supply voltage (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V				UNIT
				T_A = –40°C to 85°C		T_A = 0°C to 70°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	7.5		7.5		7.5		ns
t_{su}	Setup time, data before LE↓	2		2		2		ns
t_h	Hold time, data after LE↓	5.5		5.5		5.5		ns

switching characteristics over recommended range of supply voltage, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			T_A = –40°C to 85°C		T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	5.9	7.7	1.5	10.1	2	9.3	ns
t_{PHL}			2	6.7	8.5	1	10.3	1.5	9.5	
t_{PLH}	LE	Q	2	6.2	8.2	2	10.1	2	9.3	ns
t_{PHL}			2	5.9	7.8	2	9.2	2	8.8	
t_{PZH}	$\overline{OE}$	Q	1	7.8	9.6	1	12.3	1	11.8	ns
t_{PZL}			1	8.2	10.2	1	12.5	1	12	
t_{PHZ}	$\overline{OE}$	Q	1	4.9	6.6	1	7.4	1	7	ns
t_{PLZ}			1	5	6.7	1	8.1	1	7.4	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN64BCT373DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN64BCT373N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265