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April 1, 2003

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SuperH™ RISC engine Peripheral LSI

HD64413A Q2SD

Quick 2D Graphics Renderer with Synchronous DRAM Interface

User's Manual

HITACHI

ADE-602-204A

Rev. 2.0
09/24/02
Hitachi, Ltd.

Shaping intelligence
HITACHI SEMICONDUCTOR

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General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Pins
   - Pin configuration
   - Pin Arrangement
   - Pin Functions
7. Description of UGM Architecture
8. Description of Display List

   The configuration of the functional description of each command differs according to the command. However, the generic style includes the following items:

   i) Function
   ii) Command Format
   iii) Command Description
   iv) Example
9. Descriptions of Registers
   - List of Registers
   - Descriptions of Registers
10. Usage Notes

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given.

11. Electrical Characteristics
12. Appendix

Preface

The Q2SD (Quick 2D Graphics Renderer with Synchronous DRAM Interface) is a 2D graphics renderer that supports SDRAM interface in the SH microcomputer graphics accelerator "Quick" series (Q Series), based on the concepts of simplicity, realtime operation, and upgradability.

The Q2SD is a high-performance graphics rendering LSI for multimedia applications, which provides both drawing and display, video input functions integrated into a single chip.

Target Users: This manual was written for users who will be using the Q2SD Series in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the Q2SD Series to the target users. In this revised version, descriptions of the video input function, the list of related manuals, and points to have gotten questions from customers are reviewed.

Notes on reading this manual:

- Read the manual according to the contents.
  This manual can be roughly categorized into parts on overview, descriptions of the UGM architecture, display list, and registers, and usage notes. These are arranged in that order.

  Rules: Number notation: Binary is B′xxxx, hexadecimal is H′xxxx.
  Signal notation: An overbar is added to a low-active signal: $\overline{xxxx}$

Related Manuals: The latest versions of all related manuals are available from our web site. Please ensure you have the latest versions of all documents you require. http://www.hitachisemiconductor.com/

Q2SD Series manuals:

Manual Title	ADE No.
Q2SD Series Hardware Manual	This manual

Application notes:

Manual Title	ADE No.
HD64413A Q2SD Application Notes/Q & A	ADE-502-070

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Section 7 Electrical Characteristics

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Section 1 Overview

The Q2SD (Quick 2D Graphics Renderer with Synchronous DRAM Interface) is a 2D graphics renderer that supports SDRAM interface in the SH microcomputer graphics accelerator "Quick" series (Q Series), based on the concepts of simplicity, realtime operation, and upgradability.

The use of unified graphics memory (UGM), a double-buffering system that switches drawing and display buffers in frame units, and the video-input function, providing a high-speed drawing performance of 60 screens per second, has made possible minimization of graphics memory (with the minimum configuration of a single 16-Mbit SDRAM memory), unified handling of graphics and natural images, and realtime software 3D graphics drawing. The separation of geometric operations (handled by the CPU) and rendering operations (handled by the Q2SD) has also resulted in improved system bus utilization.

The Q2SD is a high-performance graphics rendering LSI for multimedia applications, which provides both drawing and display, video input functions integrated into a single chip.

A sample Q2SD system configuration is shown in figure 1.1.

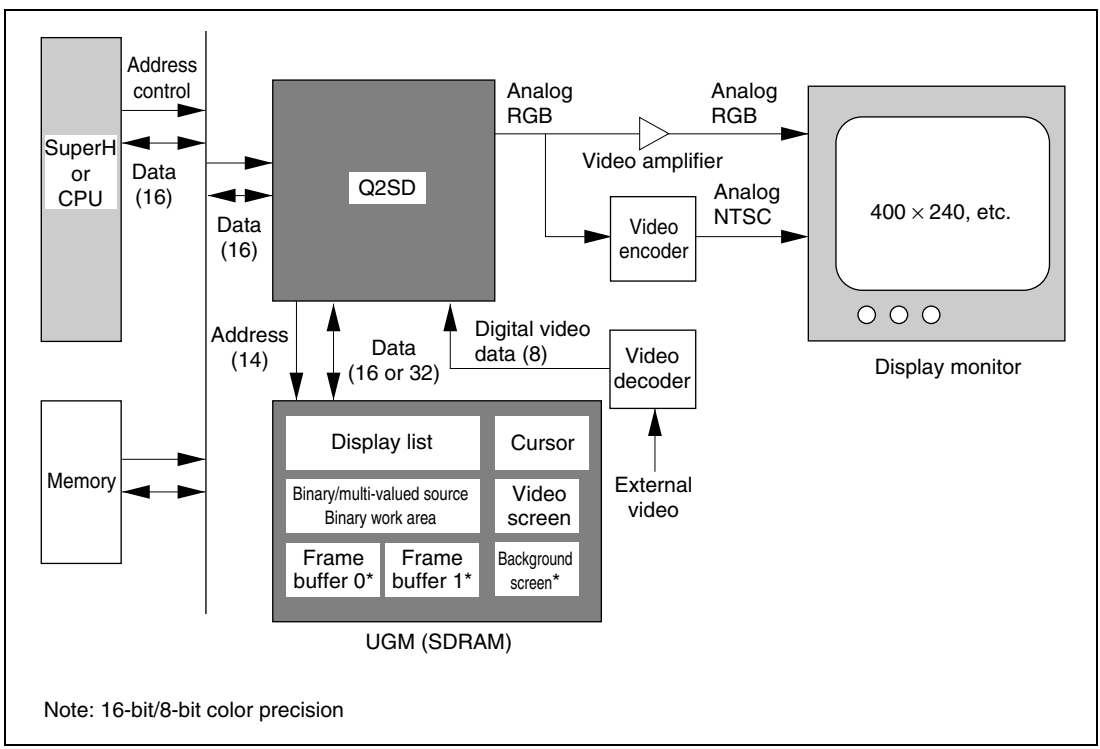


Figure 1.1 Sample System Configuration

1.1 Features

Simple (Optimized System Configuration):

(1) Use of Unified Graphics Memory (UGM) Architecture

- Unified handling of image data (unified graphics memory (UGM) architecture)
  Data in various formats can be stored and managed in the same unified graphics memory (see figure 1.2).

- Minimum necessary UGM
  Minimum UGM configuration: One 16-bit-data-bus type 16-Mbit synchronous DRAM

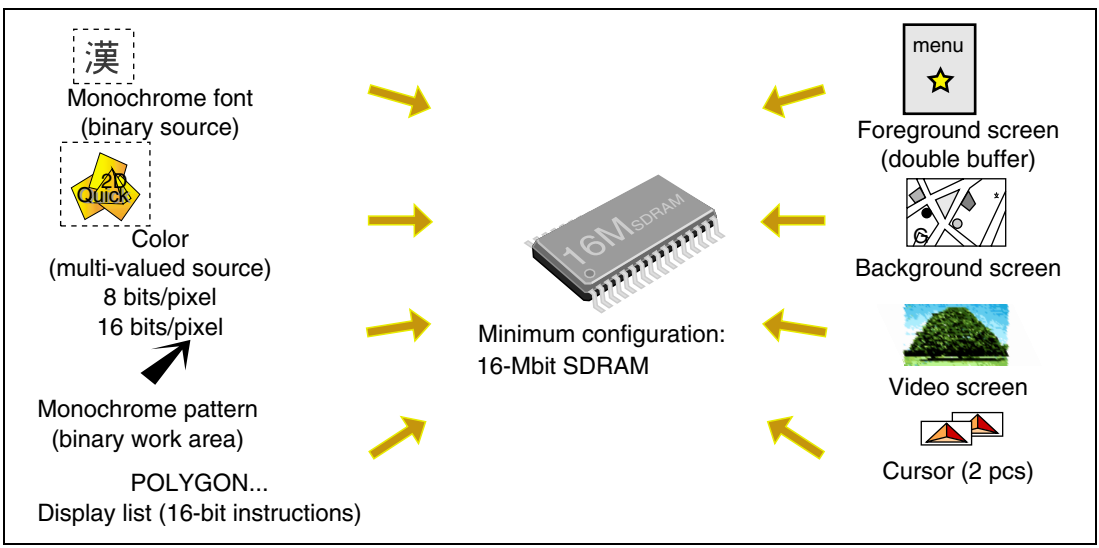


Figure 1.2 Reduced System Size Through Use of UGM Architecture

- Allocating the UGM in the CPU's memory space

  A CPU interface circuit is incorporated to provide a unified interface. The UGM is allocated in the CPU's memory space (see figure 1.3). This simplifies the UGM management by the CPU.

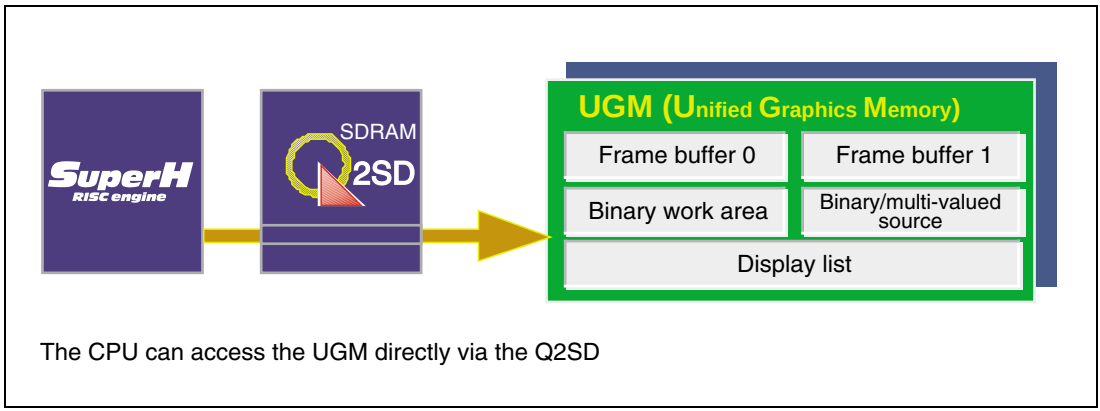


Figure 1.3 Unified System Bus Interface

Realtime:

(1) Use of Double-Buffering Architecture

The use of a double-buffering architecture that allows switching between the drawing buffer and display buffer in frame or field units enables realtime operation by synchronous with display processing with high-speed drawing processing (see figure 1.4).

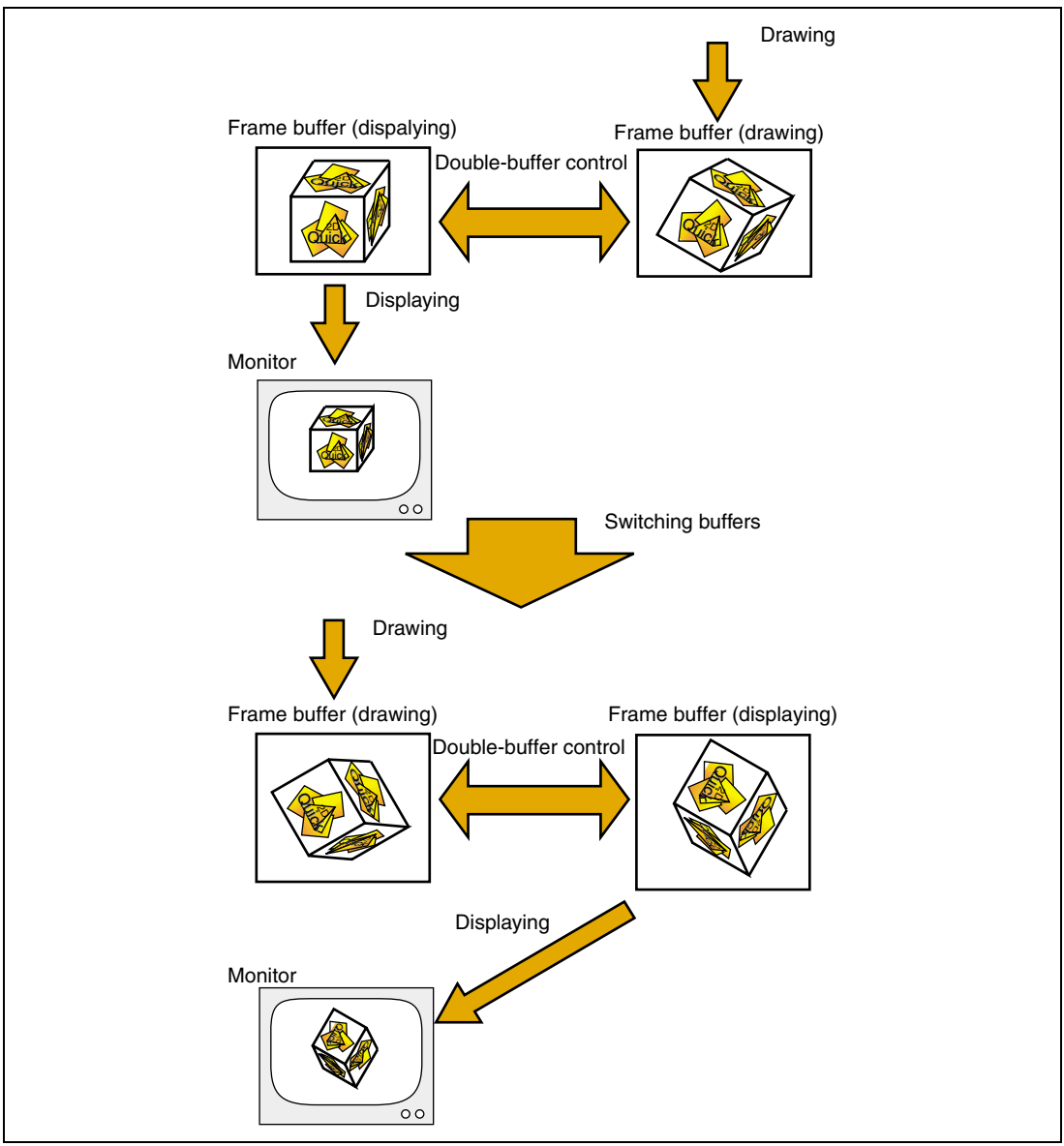


Figure 1.4 Double-Buffering Architecture

(2) Graphics Accelerator

A Dedicated hardware is used for the inefficient processing in the CPU. Thus, CPU bus efficiency is improved and high-speed realtime drawing is realized (see figure 1.5).

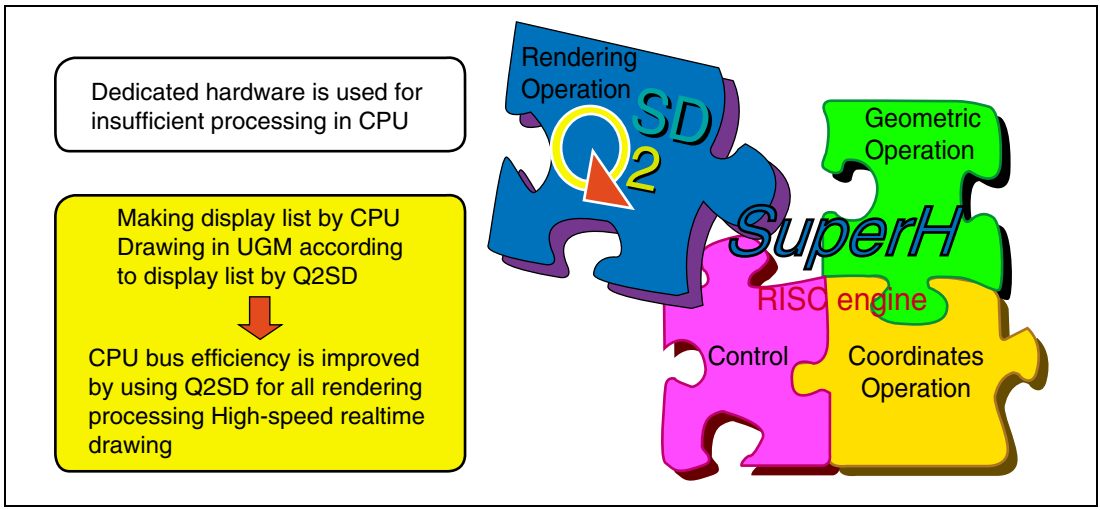


Figure 1.5 Graphics Accelerator

(3) Pipeline Graphics Processing:

High-speed graphics processing is enabled by pipelining the CPU geometry processing and Q2SD rendering processing (see figure 1.6).

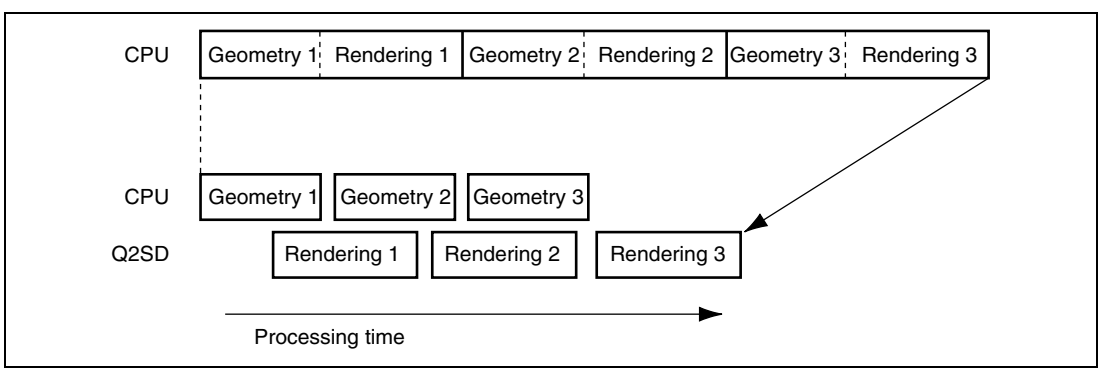


Figure 1.6 Pipeline Graphics Processing

(4) Use of Write-Only Drawing:

Write-only drawing (a drawing method using only write operations) is used to improve drawing performance.

(5) Display Composite Function

The drawing time can be reduced by changing only the images that have been modified (see figure 1.7).

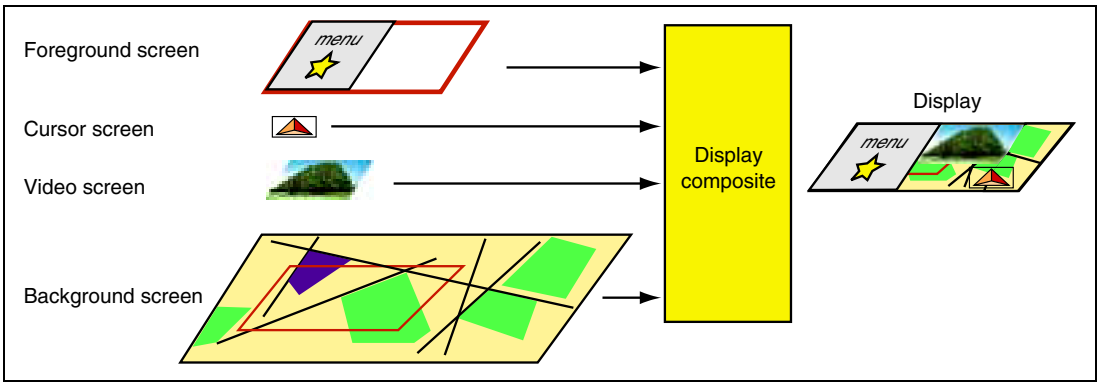


Figure 1.7 Display Composite Function

(6) Digital Video Capture

Realtime expression of digital video images in various types can be achieved.

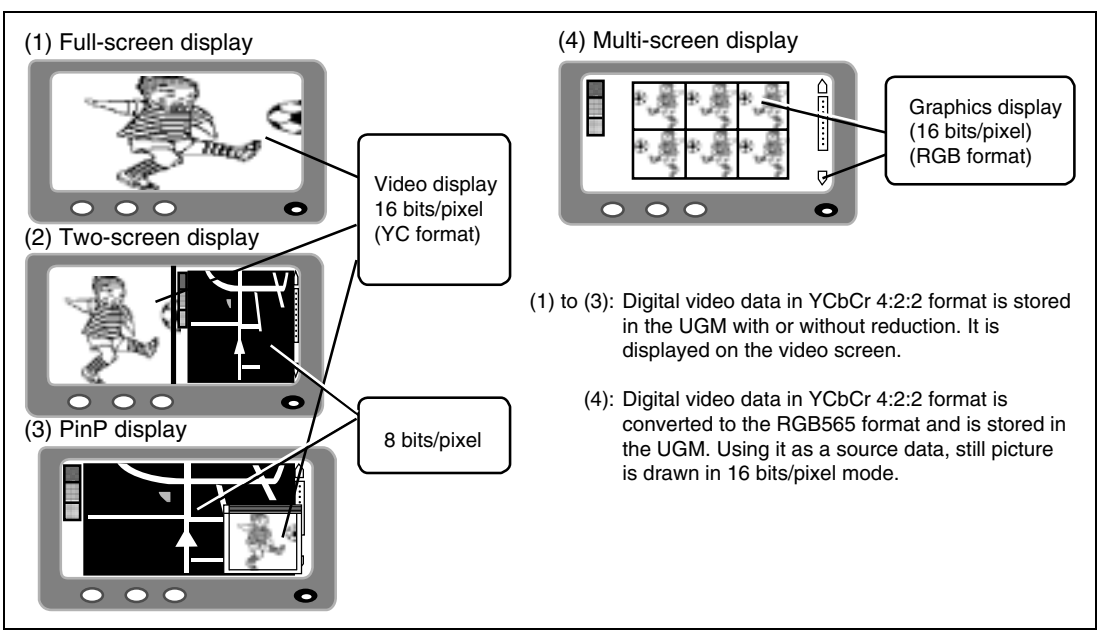


Figure 1.8 Digital Video Images

(7) Support for SDRAM

SDRAM can be used for the UGM. This enables the Q2SD to use burst access to the UGM and perform high-speed drawing.

Upgradability:

(1) Algorithm Upgrading

In the Q2SD's drawing system, algorithms for coordinate conversion, etc., are executed by the CPU, using a systematized data base containing coordinates and other data, and the results are represented in graphical form. Thus, the graphics for a variety of shapes can be implemented simply by upgrading the algorithms, without having to modify the data base (see figure 1.9).

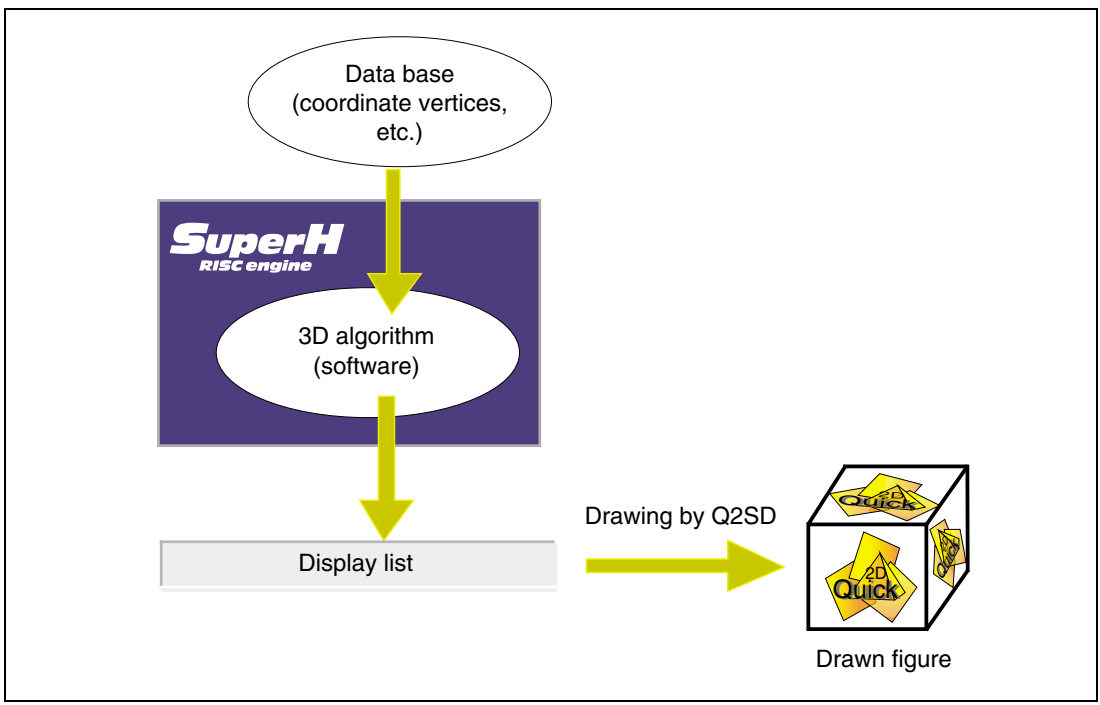


Figure 1.9 Data Flow when Using a 3D Algorithm

(2) Drawing System Upgrading

The Q2SD has been developed as a member of the Q Series, enabling the user to select the most appropriate model from the series for a particular application. The user's drawing system can also be upgraded as necessary by changing the Q2SD or CPU combination.

(3) Consistency of Application Interface

The Q2SD's carefully selected drawing commands are of four kinds: four-vertex screen drawing, line drawing, work screen drawing, and work line drawing. This makes it possible to reduce the parts dependent upon drawing commands within an application, and so achieve a more consistent interface between applications.

1.2 A List of Specifications

Table 1.1 summarizes the specifications of the Q2SD.

Table 1.1 A List of Specifications

Item		Function/Performance
Drawing	Drawing performance	Polygon drawing performance (20 × 25 pixels): 91,000/sec (2-screen composite mode: 60,000/sec)
		Line drawing performance (10 pixels): 1,200,000/sec (2-screen composite mode: 400,000/sec)
	Color representation	Source: 1/8/16 bits/pixel; drawing: 8/16 bits/pixel; work: binary
	Drawing commands	4-vertex screen drawing, line drawing, work screen drawing, work line drawing
	Register setting commands	Current pointer setting, local offset setting, clipping, specific address-mapped register setting
	Sequence control commands	Jump, subroutine, vertical blanking interval wait, no operation, display list end
Display functions	Sample screen sizes	320 × 240, 400 × 240, 480 × 240, 640 × 480, NTSC, PAL, etc.
	CRT scanning system	Non-interlace, interlace, interlace sync & video
	External synchronization	Master, TV synchronization
	Color palette	Simultaneous display of 256 colors out of 260,000
	Cursors	Two cursors, 32 × 32 pixels, display color selectable from color palette
	Display screen	Foreground, background, and video screens
Video input		8-bit multiplexed YCbCr 4:2:2 digital input
System	Drawing system internal operation maximum clock frequency (Q2SD operating frequency)	66 MHz × 1, 33 MHz × 2, 16.5 MHz × 4 (using multiplier)
	Display system internal operation clock frequency (display operation clock frequency)	Operating frequency/2 (max. 33 MHz)

Table 1.1 Summary of Q2SD Functions (cont)

Item			Function/Performance
System	SH interface	Command/ data transfer	DMA transfer (single address, dual address), or performed by SuperH
		YUV → RGB conversion	16-bit input, 4:2:2 (8 bits each for Y, U, V) 16-bit output (R: 5, G: 6, B: 5 bits)
		ΔYUV → RGB conversion	8-bit input (4 bits each for d-Y, d-U, d-V) 16-bit output (R: 5, G: 6, B: 5 bits)
		Interrupt output	TV sync signal error flag, frame flag, DMA flag, command error flag, vertical blanking flag, trap flag, command suspend flag, drawing break flag
		SuperH supported	Can be allocated to the SRAM area of the SuperH with 3.3-V power supply.
	UGM interface	32/16-bit-bus-width SDRAM	Minimum 16 Mbits (choice of one 16-Mbit (×16) memory, two parallel 16-Mbit (×16) memories, one 64-Mbit (×16) memory, or one 64-Mbit (×32) memory)
	DAC	Analog RGB output	6-bit resolution for each of R, G, and B (8-bit resolution for each of R, G, and B for video stored in UGM in YCbCr format)
Process/package			0.35-μ CMOS/176-pin LQFP
Power supply voltage/temperature range			3.3 V ± 0.3 V/0°C to 70°C (Details of a –40°C to 85°C special-specification model are also available from Hitachi sales representatives)

1.3 Block Diagram

Figure 1.10 shows a block diagram of the Q2SD. The functions of the various blocks in figure 1.10 are as follows.

- CPU interface unit

  Performs UGM access by the CPU, Q2SD on-chip register accesses by the CPU, and UGM write access by the external DMAC. Converts input data ΔYUV (260,000 colors) or YUV (260,000 colors) to RGB data (60,000 colors), and stores it in the UGM. Interrupts are output.
- UGM interface unit

  Controls the connection relating to the SDRAM that is used for the UGM.
- Chip manager

  Controls the operation of each unit in the UGM architecture.

- Clock generator (CPG0, CPG1)

  The Q2SD operating clock is generated in the CPG0, and it is provided to each unit excluding the display unit. The display dot clock is generated in the CPG1 and it is provided to the display unit.
- Rendering unit

  Performs fetching and interpretation of the display list in the UGM.
- Rendering buffer unit

  Buffers data and addresses between the rendering unit and the UGM to improve the efficiency to the UGM access in the rendering unit.
- Display unit

  Generates the CRT control signals and outputs analog RGB signals.
- Display buffer unit

  Composes the foreground, background, video and cursor screens. Accesses data to be displayed in synchronization with the display timing. By the color palette (6 bits per color), converts 8-bits/pixel data to display data of 256 colors out of 262,144 to the RGB data, based on the color conversion table, and when the video screen data is the YCbCr data, it is converted to the RGB data.
- Video-in unit

  Fetches 4:2:2 YCbCr data and stores it in the UGM in YCbCr or RGB format. The image data can also be stored with reduction.

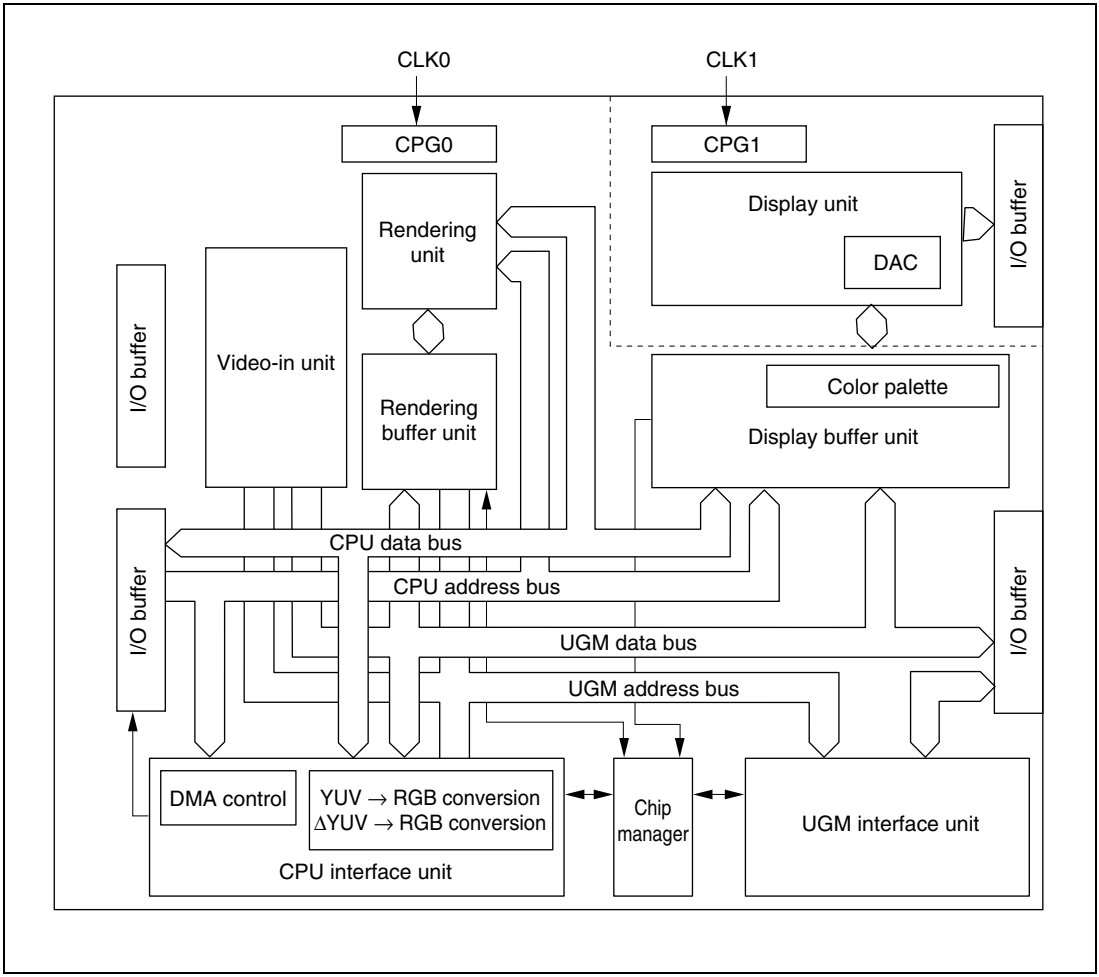


Figure 1.10 Internal Block Diagram

1.4 Processing States

The Q2SD has five main processing states: the power-on state, initial state, reset state, UGM initialization state, and normal states. Figure 1.11 shows the state transitions.

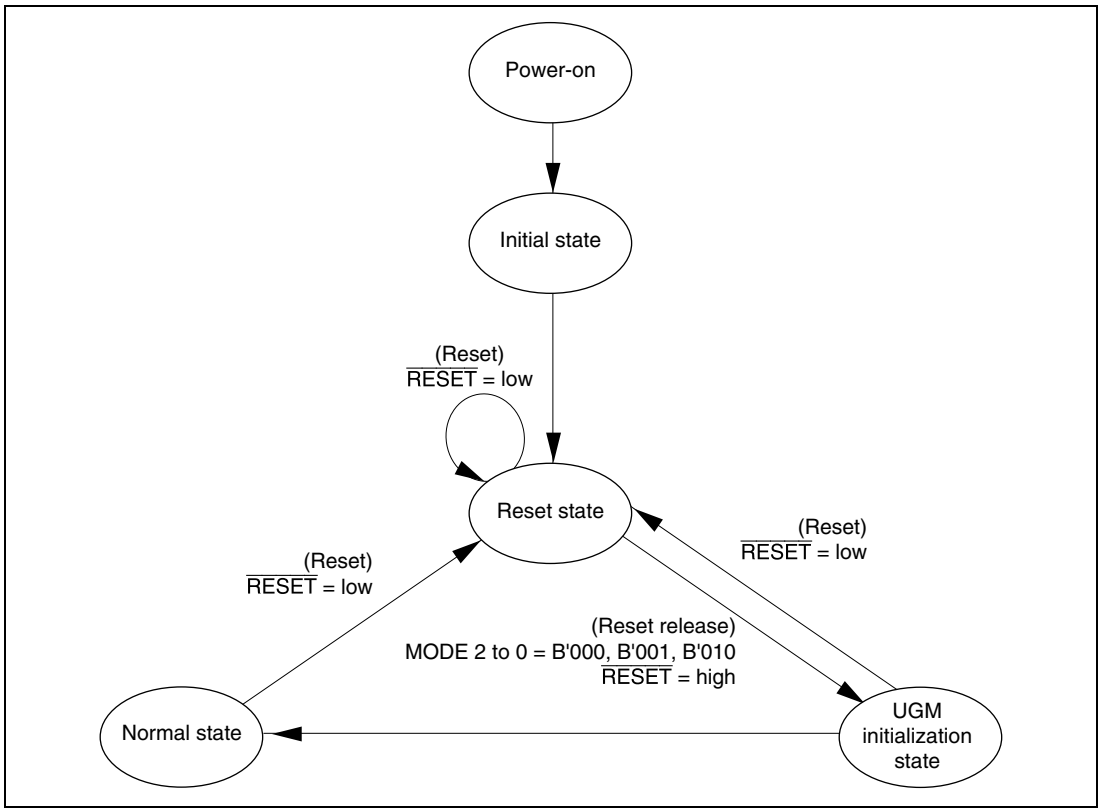


Figure 1.11 State Transition Diagram

1.4.1 Power On

For details, refer to section 6.1, Power-On Sequence.

1.4.2 Initial States (when Specified Power is Supplied)

Initial states are undefined.

Registers: Undefined
I/O pins: Undefined
Output pins: Low/high-level output

1.4.3 Reset State (when Low Level is Input to $\overline{\text{RESET}}$ Pin)

Table 1.2 shows the Q2SD pin states immediately after a reset. UGM refreshing is not performed when the $\overline{\text{RESET}}$ pin is low. The levels of pins MODE2 to MODE0 are latched at the rising edge of the $\overline{\text{RESET}}$ pin. At this time, they must be fixed at a level of B′000, B′001, or B′010. Other levels must not be used because those setting makes the Q2SD enter in test mode.

Table 1.2 Pin States After Reset

I/O Pins	Input state	D0 to D15*, $\overline{\text{VSYNC}}$/$\overline{\text{EXVSYNC}}$, $\overline{\text{HSYNC}}$/ $\overline{\text{EXHSYNC}}$, $\overline{\text{ODDF}}$
	Output state (low-level output)	MD0 to MD31
Output Pins	Low-level output	DISP, CDE
	High-level output	$\overline{\text{DREQ}}$, $\overline{\text{IRL}}$, $\overline{\text{WAIT}}$
	Low/high-level output	$\overline{\text{CSYNC}}$, MA0 to MA13, $\overline{\text{MWE}}$, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, LDQM0, LDQM1, UDQM0, UDQM1, MCLK

Note: Pins D0 to D15 are in the output state when $\overline{\text{RD}}$ is a low-level input.

1.4.4 UGM Initialization State

Initializes the SDRAM which is used for the UGM. For details on initialization, refer to section 6.6, SDRAM Mode Register Values for UGM Set by Q2SD.

1.4.5 Normal Operating State

In the normal operating state, the Q2SD executes drawing commands and performs display control.

2.1 Pin Configuration

Figure 2.1 shows an overview of the Q2SD's pins. Unused input pins should be made inactive by pulling them up or down.

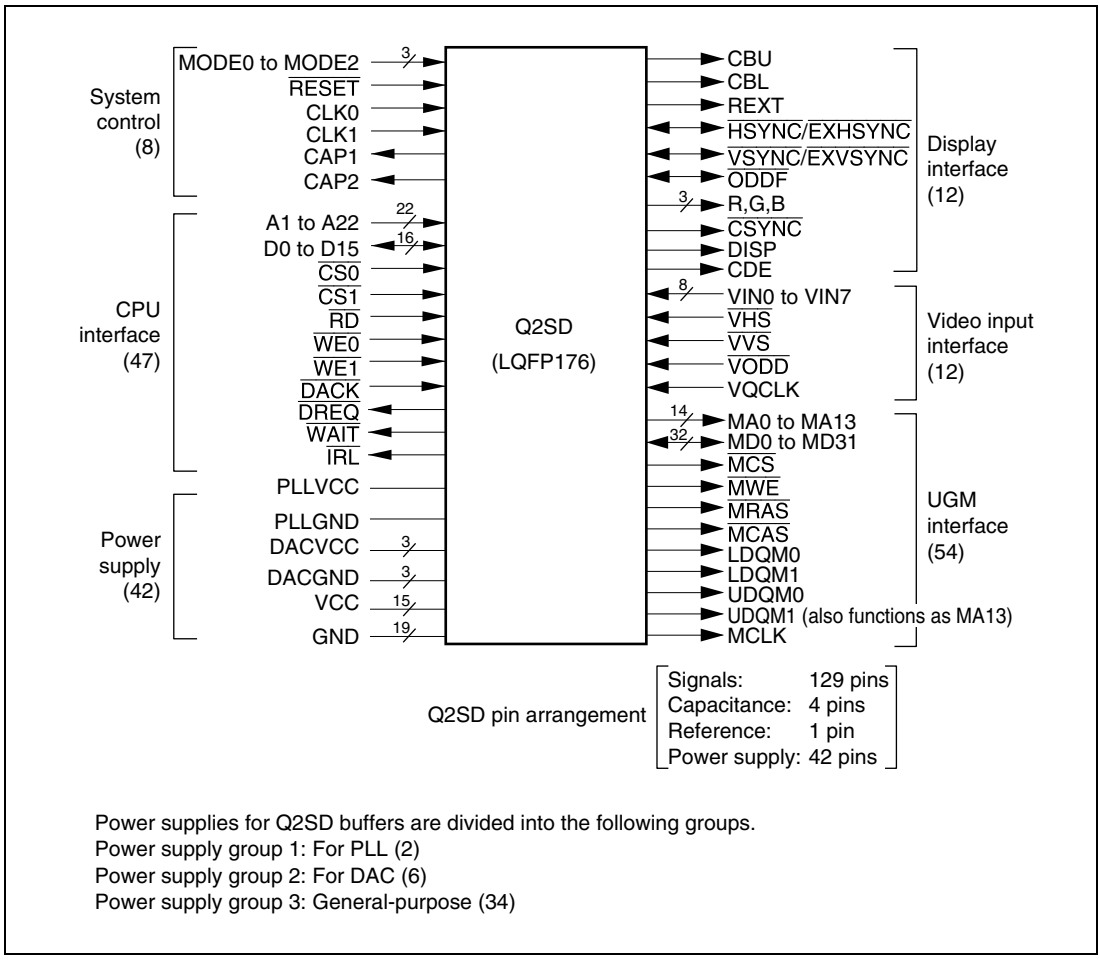


Figure 2.1 Pin Configuration

2.2 Pin Arrangement

Figure 2.2 shows the pin arrangement of the Q2SD.

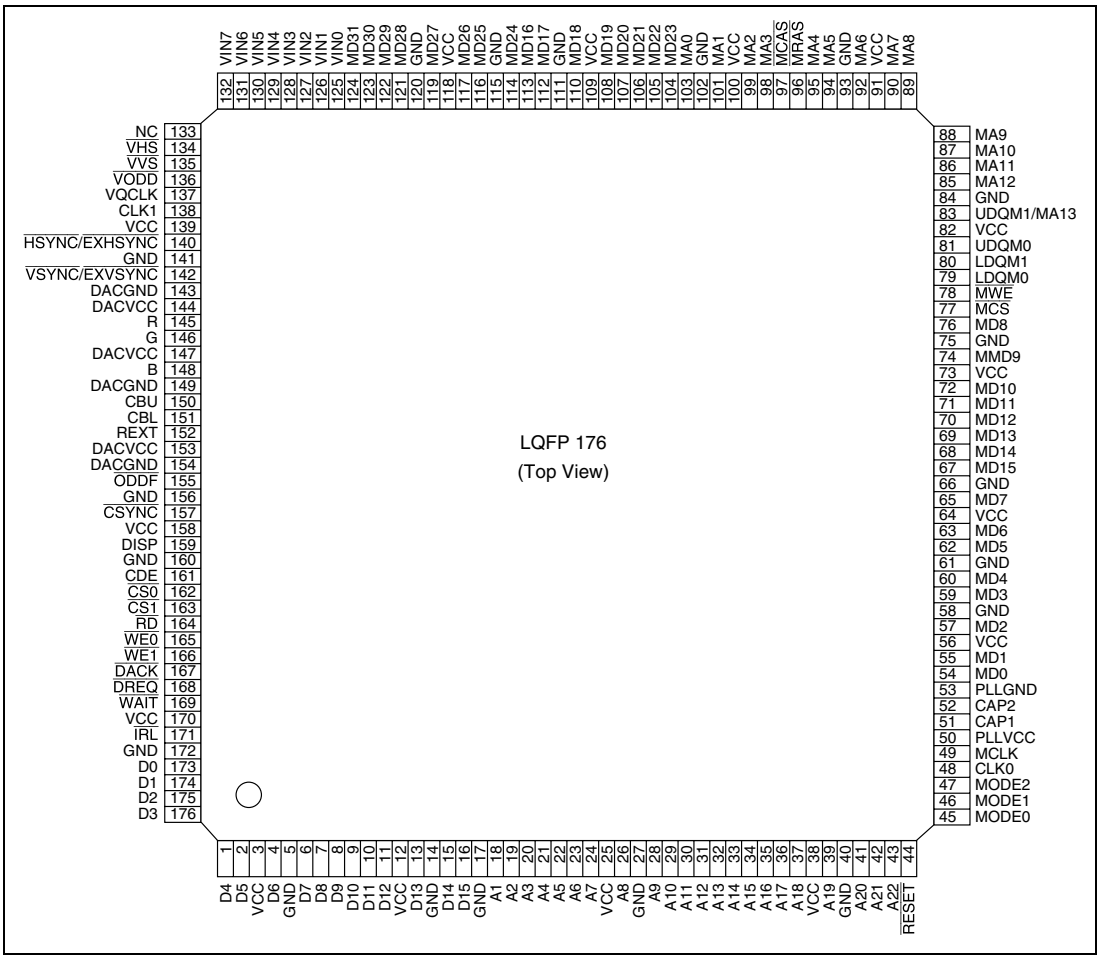


Figure 2.2 Pin Arrangement

2.3 Pin Functions

Table 2.1 shows the Q2SD pin functions.

Table 2.1 Pin Functions

Type	Symbol	Pin No.	I/O	Function
System control	MODE0	45	Input	Operating mode pin 0
	MODE1	46	Input	Operating mode pin 1
	MODE2	47	Input	Operating mode pin 2
	CLK0	48	Input	Q2SD operating clock
	CLK1	138	Input	Display operating clock
	$\overline{\text{RESET}}$	44	Input	Reset
	CAP1	51	Output	Multiplication circuit external capacitance pin
	CAP2	52	Output	Multiplication circuit external capacitance pin
CPU interface	A1	18	Input	CPU address 1
	A2	19	Input	CPU address 2
	A3	20	Input	CPU address 3
	A4	21	Input	CPU address 4
	A5	22	Input	CPU address 5
	A6	23	Input	CPU address 6
	A7	24	Input	CPU address 7
	A8	26	Input	CPU address 8
	A9	28	Input	CPU address 9
	A10	29	Input	CPU address 10
	A11	30	Input	CPU address 11
	A12	31	Input	CPU address 12
	A13	32	Input	CPU address 13
	A14	33	Input	CPU address 14
	A15	34	Input	CPU address 15
	A16	35	Input	CPU address 16
	A17	36	Input	CPU address 17
	A18	37	Input	CPU address 18
	A19	39	Input	CPU address 19
	A20	41	Input	CPU address 20

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
CPU interface	A21	42	Input	CPU address 21
	A22	43	Input	CPU address 22
	D0	173	I/O	CPU data 0
	D1	174	I/O	CPU data 1
	D2	175	I/O	CPU data 2
	D3	176	I/O	CPU data 3
	D4	1	I/O	CPU data 4
	D5	2	I/O	CPU data 5
	D6	4	I/O	CPU data 6
	D7	6	I/O	CPU data 7
	D8	7	I/O	CPU data 8
	D9	8	I/O	CPU data 9
	D10	9	I/O	CPU data 10
	D11	10	I/O	CPU data 11
	D12	11	I/O	CPU data 12
	D13	13	I/O	CPU data 13
	D14	15	I/O	CPU data 14
	D15	16	I/O	CPU data 15
	$\overline{CS0}$	162	Input	Chip select 0 (UGM)
	$\overline{CS1}$	163	Input	Chip select 1 (internal registers)
	$\overline{RD}$	164	Input	Read strobe
	$\overline{WE0}$	165	Input	Write pulse 0 (lower)
	$\overline{WE1}$	166	Input	Write pulse 1 (upper)
	$\overline{DACK}$	167	Input	DMA acknowledge
	$\overline{DREQ}$	168	Output	DMA request
	$\overline{WAIT}$	169	Output	CPU wait
	$\overline{IRL}$	171	Output	Interrupt request
Display interface	CBU	150	Output	DAC external capacitance pin
	CBL	151	Output	DAC external capacitance pin
	REXT	152	Output	DAC external reference pin
	R	145	Output	Display data analog output R

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
Display interface	G	146	Output	Display data analog output G
	B	148	Output	Display data analog output B
	$\overline{\text{CSYNC}}$	157	Output	Composite sync output signal
	$\overline{\text{HSYNC}}$/ $\overline{\text{EXHSYNC}}$	140	I/O	Horizontal sync output/external horizontal sync input
	$\overline{\text{VSYNC}}$/ $\overline{\text{EXVSYNC}}$	142	I/O	Vertical sync output/external vertical sync input
	DISP	159	Output	Signal indicating display period (high during display period)
	CDE	161	Output	Color detection (high in case of specific color output)
	$\overline{\text{ODDF}}$	155	I/O	Signal indicating odd field (low when odd)
Video input	VIN0	125	Input	Video input data 0
interface	VIN1	126	Input	Video input data 1
	VIN2	127	Input	Video input data 2
	VIN3	128	Input	Video input data 3
	VIN4	129	Input	Video input data 4
	VIN5	130	Input	Video input data 5
	VIN6	131	Input	Video input data 6
	VIN7	132	Input	Video input data 7
	$\overline{\text{VHS}}$	134	Input	Video horizontal sync input
	$\overline{\text{VVS}}$	135	Input	Video vertical sync input
	$\overline{\text{VODD}}$	136	Input	Signal indicating video input odd field
	VQCLK	137	Input	Video input valid data capture clock
UGM interface	MA0	103	Output	Memory address 0
	MA1	101	Output	Memory address 1
	MA2	99	Output	Memory address 2
	MA3	98	Output	Memory address 3
	MA4	95	Output	Memory address 4
	MA5	94	Output	Memory address 5
	MA6	92	Output	Memory address 6
	MA7	90	Output	Memory address 7

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
UGM interface	MA8	89	Output	Memory address 8
	MA9	88	Output	Memory address 9
	MA10	87	Output	Memory address 10
	MA11	86	Output	Memory address 11
	MA12	85	Output	Memory address 12
	MA13	83	Output	Memory address 13 (also functions as UDQM1)
	MD0	54	I/O	Memory data 0
	MD1	55	I/O	Memory data 1
	MD2	57	I/O	Memory data 2
	MD3	59	I/O	Memory data 3
	MD4	60	I/O	Memory data 4
	MD5	62	I/O	Memory data 5
	MD6	63	I/O	Memory data 6
	MD7	65	I/O	Memory data 7
	MD8	76	I/O	Memory data 8
	MD9	74	I/O	Memory data 9
	MD10	72	I/O	Memory data 10
	MD11	71	I/O	Memory data 11
	MD12	70	I/O	Memory data 12
	MD13	69	I/O	Memory data 13
	MD14	68	I/O	Memory data 14
	MD15	67	I/O	Memory data 15
	MD16	113	I/O	Memory data 16
	MD17	112	I/O	Memory data 17
	MD18	110	I/O	Memory data 18
	MD19	108	I/O	Memory data 19
	MD20	107	I/O	Memory data 20
	MD21	106	I/O	Memory data 21
	MD22	105	I/O	Memory data 22
	MD23	104	I/O	Memory data 23
	MD24	114	I/O	Memory data 24

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
UGM interface	MD25	116	I/O	Memory data 25
	MD26	117	I/O	Memory data 26
	MD27	119	I/O	Memory data 27
	MD28	121	I/O	Memory data 28
	MD29	122	I/O	Memory data 29
	MD30	123	I/O	Memory data 30
	MD31	124	I/O	Memory data 31
	$\overline{\text{MCS}}$	77	Output	Memory chip select
	$\overline{\text{MWE}}$	78	Output	Memory write pulse
	$\overline{\text{MRAS}}$	96	Output	Row select signal
	$\overline{\text{MCAS}}$	97	Output	Column select signal
	LDQM0	79	Output	Lower word, lower byte I/O mask
	LDQM1	80	Output	Lower word, upper byte I/O mask
	UDQM0	81	Output	Upper word, lower byte I/O mask
	UDQM1	83	Output	Upper word, upper byte I/O mask (also functions as MA13)
	MCLK	49	Output	Memory clock
Power supply	VCC	3	Power supply	Buffer/internal VDD
	VCC	12	Power supply	Buffer/internal VDD
	VCC	25	Power supply	Buffer/internal VDD
	VCC	38	Power supply	Buffer/internal VDD
	VCC	56	Power supply	Buffer/internal VDD
	VCC	64	Power supply	Buffer/internal VDD
	VCC	73	Power supply	Buffer/internal VDD
	VCC	82	Power supply	Buffer/internal VDD
	VCC	91	Power supply	Buffer/internal VDD
	VCC	100	Power supply	Buffer/internal VDD
	VCC	109	Power supply	Buffer/internal VDD
	VCC	118	Power supply	Buffer/internal VDD
	VCC	139	Power supply	Buffer/internal VDD
	VCC	158	Power supply	Buffer/internal VDD
	VCC	170	Power supply	Buffer/internal VDD

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
Power supply	GND	5	Ground	Buffer VSS
	GND	14	Ground	Buffer VSS
	GND	27	Ground	Buffer VSS
	GND	40	Ground	Buffer VSS
	GND	58	Ground	Buffer VSS
	GND	66	Ground	Buffer VSS
	GND	75	Ground	Buffer VSS
	GND	84	Ground	Buffer VSS
	GND	93	Ground	Buffer VSS
	GND	102	Ground	Buffer VSS
	GND	111	Ground	Buffer VSS
	GND	120	Ground	Buffer VSS
	GND	141	Ground	Buffer VSS
	GND	160	Ground	Buffer VSS
	GND	172	Ground	Buffer VSS
	GND	17	Ground	Internal VSS
	GND	61	Ground	Internal VSS
	GND	115	Ground	Internal VSS
	GND	156	Ground	Internal VSS
	PLL VCC	50	Power supply	Multiplication circuit VDD
	PLL GND	53	Ground	Multiplication circuit VSS
	DAC VCC	144	Power supply	DAC VDD
	DAC VCC	147	Power supply	DAC VDD
	DAC VCC	153	Power supply	DAC VDD
	DAC GND	143	Ground	DAC VSS
	DAC GND	149	Ground	DAC VSS
	DAC GND	154	Ground	DAC VSS
Other	NC	133		No-connection (should be open.)

2.4 System Control Pins

2.4.1 Operating Mode Pins

- MODE0, MODE1, and MODE2

These pins control the Q2SD's operating mode. The mode is fixed in a reset-startup and cannot be changed after reset.

Table 2.2 Operating Mode Selection

MODE2	MODE1	MODE0	Description
L	L	L	Normal operation state. Multiplication on. The external input clock is duty-free. The internal operating clock has the same frequency as the external input clock.
L	L	H	Normal operation state. Multiplication on. The external input clock is duty-free. The internal operating clock has twice the frequency of the external input clock.
L	H	L	Normal operation state. Multiplication on. The external input clock is duty-free. The internal operating clock has four times the frequency of the external input clock.
L	H	H	Setting prohibited.
H	*	*	Setting prohibited.

Legend

H: High level

L: Low level

*: Either high or low level

2.4.2 Clock Pins

- CLK0, CLK 1, CAP1, and CAP2

There are two Q2SD clocks, CLK0 and CLK1. The clock used as the base for the Q2SD operating clock is input to the CLK0 pin, and the clock used as the display operating clock is input to the CLK1 pin.

The Q2SD operating clock is the base clock for Q2SD's operations, and is also used as the base clock for UGM access. The Q2SD includes an operating clock multiplication circuit that enables a ×1, ×1/2, or ×1/4 multiple of the operating clock to be selected for input to the CLK0 pin.

The display operating clock is the base clock for display operations, and is used to control display dot clock, display data output and generate horizontal and vertical sync signals.

The relationship between the clocks and operating frequencies is summarized in table 2.3.

Table 2.3 Input Clocks and Operating Frequencies

Clock Input Pin	Clock Type	Input Clock
CLK0	One of the clocks on the right is the Q2SD operating clock.	Clock with the CLK0 frequency, and duty cycle adjusted to 50%
		Clock with twice the CLK0 frequency, and duty cycle adjusted to 50%
		Clock with four times the CLK0 frequency, and duty cycle adjusted to 50%
CLK1	The clock on the right is the display operating clock.	Clock with the CLK1 frequency

The Q2SD operating clock and display operating clock frequencies can be set to any values within the following range. This enables to perform drawing at a maximum operating clock independently of the characteristics of the display device.

Q2SD operating clock ≥ 2 × display operating clock
(where display operating clock ≤ 33 MHz)

CAP1 and CAP2 are external capacitance pins for the multiplication circuit. Figure 2.3 shows an example circuit for connection of pins CAP1 and CAP2. The capacitor C0 and resistor R0 of the internal PLL for oscillation settling must be placed near pins CAP1 and CAP2, and must not cross with other signals. The C0 ground must be provided from the PLLGND. C0 and R0 are an external capacitor and a noise-reduction resistor for a PLL charge pump.

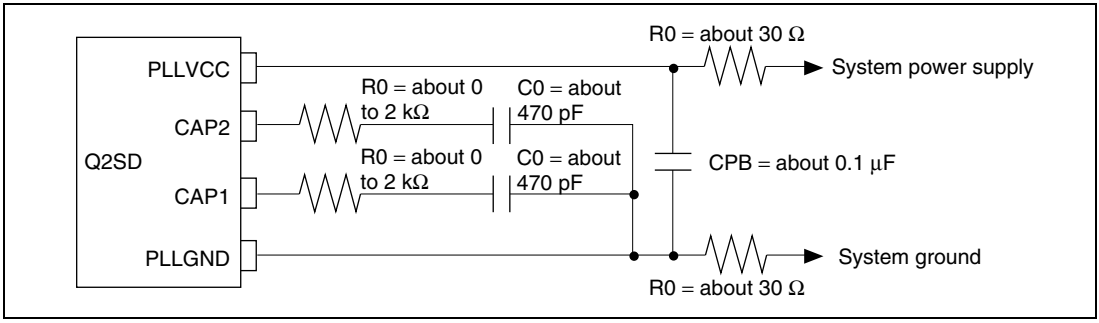


Figure 2.3 Example of Circuit for Connection of Pins CAP1 and CAP2

2.4.3 Reset Pin

- $\overline{\text{RESET}}$

A hardware reset signal is input to this pin. When the signal is at a low level, the Q2SD enters the hardware reset state. At this time, pin states are initialized as shown in table 1.2 and register contents are also initialized.

2.4.4 Power Supply Pin

- VCC, GND, PLLVCC, PLLGND, DACVCC, DACGND

The normal power supply, DAC power supply, and PLL power supply are connected to 3.3 V. There are several normal power supply and DAC power supply pins and power must be supplied to all those pins.

Normal power supply (VCC, GND), PLL power supply (PLLVCC, PLLGND), and DAC power supply (DACVCC, DACGND) must be separated from the board's power supply source, and bypass capacitors CPB, CB1, and CB2 must be inserted near the pins.

Since the DAC outputs signals with high resolution, external noise should be reduced. It is recommended that at least one electrolytic capacitor should be placed each of between power supply and GND pins other than capacitors CPB, CB1, and CB2. It is also recommended that differences of voltage levels for each power supply pin should be reduced to avoid DAC's latch-up and an inductance with about 100 µH or a noise filter should be inserted between the DACVCC and VCC pins to cut out high frequency noise.

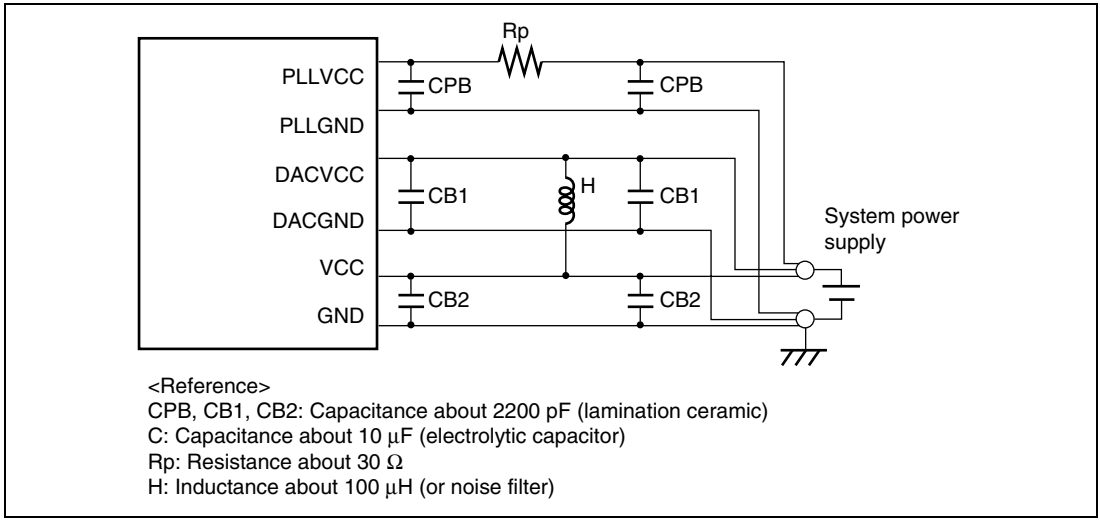


Figure 2.4 Connections of Bypass Capacitors between Power Supplies Near the Pins

2.5 CPU Interface Pins

- A1 to A22, D0 to D15, $\overline{CS0}$, $\overline{CS1}$, $\overline{RD}$, $\overline{WE0}$, $\overline{WE1}$, $\overline{DACK}$, $\overline{DREQ}$, $\overline{WAIT}$, $\overline{IRL}$

2.5.1 CPU Writes

The CPU can access the UGM or a Q2SD internal registers. In a UGM access, a low-level signal is input to $\overline{CS0}$; in a Q2SD internal register access, a low-level signal is input to $\overline{CS1}$. $\overline{CS0}$ and $\overline{CS1}$ must not be driven low at the same time. The UGM or Q2SD internal register address is input to A1 to A22. Input the addresses of the UGM within the range specified by the memory mode register (MEMR) to pins A1 to A22. Route the wire so that pins A22 and A21 are fixed at low levels when a single memory of 16 Mbits is in use and route the wire so that pin A22 is fixed at a low level when two memories of 16 Mbits are in use. The address is a byte address. Only word (2-byte) access can be used in the Q2SD for registers, while word access or byte access can be used for the UGM. In word access, input a low-level signal to both $\overline{WE0}$ and $\overline{WE1}$; in byte access, drive $\overline{WE0}$ low for an access to bits 7 to 0, or drive $\overline{WE1}$ low for an access to bits 15 to 8.

The Q2SD uses the $\overline{WAIT}$ signal to notify the CPU of a delay in CPU access due to an internal Q2SD operation. However, because of the high-level width specification for the $\overline{WE0}$ and $\overline{WE1}$ signals, the CPU external bus operating frequency should be set equal to or lower than the Q2SD's internal operating frequency. Following detection of a low level of $\overline{CS0}$ or $\overline{CS1}$ and a low level of $\overline{RD}$, $\overline{WE0}$, or $\overline{WE1}$, there is a maximum interval of 3 cycles, followed by an output buffer delay (max. 15 ns), before the Q2SD's $\overline{WAIT}$ signal is asserted. The number of software waits should be adjusted by software according to the frequency ratio between the CPU and Q2SD, and system specifications such as synchronous or asynchronous operation.

In some SuperH RISC engine family products, the $\overline{CS}$ pin is initially set as an input port. If this signal is connected directly to the $\overline{CS0}$ or $\overline{CS1}$ signal of the Q2SD, pull up the SuperH's $\overline{CS}$ pin externally to prevent the voltage level from becoming unstable in a reset.

When using a CPU that uses an $\overline{RDY}$ signal for interfacing, invert the Q2SD's $\overline{WAIT}$ signal and use it as the $\overline{RDY}$ signal.

The $\overline{WAIT}$ signal is output for a minimum of 1 tcyc0 when accessing the Q2SD.

2.5.2 CPU Reads

A read operation is basically the same as a write operation. Reads are performed in word units. Although write operations are indicated by signals $\overline{WE0}$ and $\overline{WE1}$, read operations are indicated by the low level of the $\overline{RD}$ signal.

2.5.3 DMA Writes

The CPU can perform write DMA access, using cycle stealing, to the UGM or a Q2SD address-mapped register (the image data entry register (IDE)). To perform DMA access, DMA transfer start address, DMA transfer word count, and system control register DMA mode and DMA address mode settings must be made. After the DMA mode settings are made, the Q2SD dives the $\overline{\text{DREQ}}$ signal low as soon as its preparations are completed. When the DMA controller receives this signal, it drives the $\overline{\text{DACK}}$ signal low and begins DMA access. DMA access is performed in word units.

Use a DMA mode setting of B′01 (DMA transfer to the UGM) when performing DMA writes with a YUV mode (YUV2, YUV1, YUV0 in the input data conversion mode register (IEMR)) setting of B′000, and a DMA mode setting of B′11 (DMA transfer to the image data entry register (IDER)) when performing DMA writes with a YUV mode setting other than B′000.

When DMA address mode bits DAA1 and DAA0 in the system control register (SYSR) are is set to B′00 or B′01, transfer is performed using single address transfer timing.

When the DMA address mode (DAA1, DAA0) is set to B′10, transfer is performed using dual address transfer timing. In this case, access to the Q2SD should be performed by driving $\overline{\text{DACK}}$ low. $\overline{\text{CS0}}$ is ignored. The DMA mode is set to B′01 for UGM access, and to B′11 for Q2SD address-mapped register (image data entry register (IDE)) access. Other address-mapped registers cannot be accessed. The destination address (UGM address) is set as the DMA transfer start address (DMSARH, DMSARL), and the number of words set as the DMA transfer word count (DMAWRH, DMAWRL) are transferred. The Q2SD controls the UGM addresses using the on-chip address counter. Addresses input from off-chip are not used.

When making another DMA mode setting after DMA transfer ends, first check that the DMF bit is set to 1 in the status register.

In DMA transfer from synchronous DRAM to the Q2SD, the D0 to D15 setup time (t_{WRDRS}) relative to the rise of the $\overline{\text{RD}}$ signal must be at least two Q2SD system operating clock cycles, and therefore the external bus operating frequency must be no higher than 1/2 the system operating clock frequency.

When using the DMAC, make the following DMAC settings.

- For DMA transfer in dual address mode
  - $\overline{\text{DACK}}$ output in write cycle
  - Active-low $\overline{\text{DACK}}$ output
  - Fixed destination address (set any UGM address)
  - Source address incremented
  - External request, dual address mode
  - $\overline{\text{DREQ}}$ falling-edge detection

— Cycle stealing

- For DMA transfer in single address mode
  — $\overline{\text{DACK}}$ output in read cycle
  — Active-low $\overline{\text{DACK}}$ output
  — Fixed destination address
  — Source address incremented
  — External request, single address mode
  — $\overline{\text{DREQ}}$ falling-edge detection
  — Cycle stealing

The SuperH family includes models in which the initial DACK pin setting is active-high. In this case, leave the DACK pin at its initial setting (active-high) and use an external circuit to invert the DACK pin signal before connection to the Q2SD's $\overline{\text{DACK}}$ pin.

2.5.4 Interrupts

The Q2SD requests interrupts to the CPU by means of internal sources. Interrupt sources are set in the interrupt enable register (IER).

2.6 UGM Interface Pins

- MA0 to MA13, MD0 to MD31, $\overline{\text{MCS}}$, $\overline{\text{MWE}}$, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, LDQM0, LDQM1, UDQM0, UDQM1, MCLK

The Q2SD allows synchronous DRAM to be used as the UGM, and has a direct interface for synchronous DRAM. When connecting only one synchronous DRAM with a data bit width of 16, use pins MD0 to MD15, and leave pins MD16 to MD31 open.

The operating mode of the synchronous DRAM (write mode, $\overline{\text{CAS}}$ latency, burst type, and burst length) is set automatically by the Q2SD. For refreshing, auto-refresh mode is used. Synchronous DRAM precharging is carried out using the Precharge All Banks (PALL) command.

2.7 Display Interface Pins

The signals output from the display interface pins are all synchronized with the display operating clock.

2.7.1 Display Signal Output

- R, G, B

RGB analog display signals are output. The pixel data resolution is 6 bits for each of R, G, and B. Outside the display period, the image data (R, G, B) goes to the level corresponding to H′000.

2.7.2 Video Encoder Interface

- CSYNC

Outputs the composite sync signal ($\overline{\text{CSYNC}}$). In master mode, equalizing pulses can also be added to the composite sync signal.

2.7.3 CRT Interface

- HSYNC/$\overline{\text{EXHSYNC}}$, $\overline{\text{VSYNC}}$/$\overline{\text{EXVSYNC}}$, DISP, CDE, $\overline{\text{ODDF}}$

Inputs/outputs the horizontal and vertical sync signals to the HSYNC/$\overline{\text{EXHSYNC}}$ and $\overline{\text{VSYNC}}$/$\overline{\text{EXVSYNC}}$ pins. Inputs/outputs the signal indicating whether the current field is odd or even for interlace control to the $\overline{\text{ODDF}}$ pin. When the Q2SD has a mastership for synchronization, these signals are outputs. When an external device (TV or VCR) has a mastership, these signals are inputs. Since these signals are input during the reset state, they must be pulled up to fix the levels, meaning that the direction is a non-significant. The TV sync mode bits in the display mode register (bits TVM1 and TVM0 in DSMR) select either master (output) or TV sync (input).

The CDE pin outputs a high level when a specified color in a display area in the UGM is detected. CDER specifies the color to be detected. Display synthesis of external video and Q2 graphics image in one pixel units is enabled by using the CDE pin for selecting the external selection circuit for the external video or Q2 graphics image. The DISP signal indicates the display period in which the high level is output.

2.7.4 D/A Converter

- CBU, CBL, and REXT

The D/A converter changes output levels linearly in accordance with the display data. Connect the specified resistors or capacitors to the REXT, CBU, and CBL pins.

Connect resistive load RL to the R, G, and B output pins. The relationship between Ioutmax which is the maximum value of the output current Iout and REXT can be given in the following expression.

REXT = (2.842/Iout) × DACVCC.

Where Vout is an amplitude when the current of Ioutmax is flowing in the resistive load RL, REXT can given in the following expression.

REXT = (2.842/(Vout/RL)) × DACVCC

Therefore, to obtain Vout = 1 Vpp when RL = 330 Ω and DACVCC = 3.3 V, REXT = 3.1 kΩ.

The range of maximum output current Ioutmax must be set within the range from 2.0 mA to 3.0 mA.

The D/A converter has 8-bit resolution, but the dynamic settling error is determined by resistive load RL, output pin load C (total of routing and video amp input capacitances), and display operating frequency f.

For example, when RL = 330 Ω, C = 20 pF, and f = 33 MHz, the value of n when the following equation is satisfied is the D/A converter accuracy.

$$\exp\left(\frac{-1}{RL \cdot C \cdot f}\right) \leq \frac{1}{2^n} \qquad \text{(Where n is an integer)}$$

Since n is 6 in this case, the D/A converter has 6-bit accuracy. (The dynamic settling error is $1/2^6$ = 1.56% full-scale.)

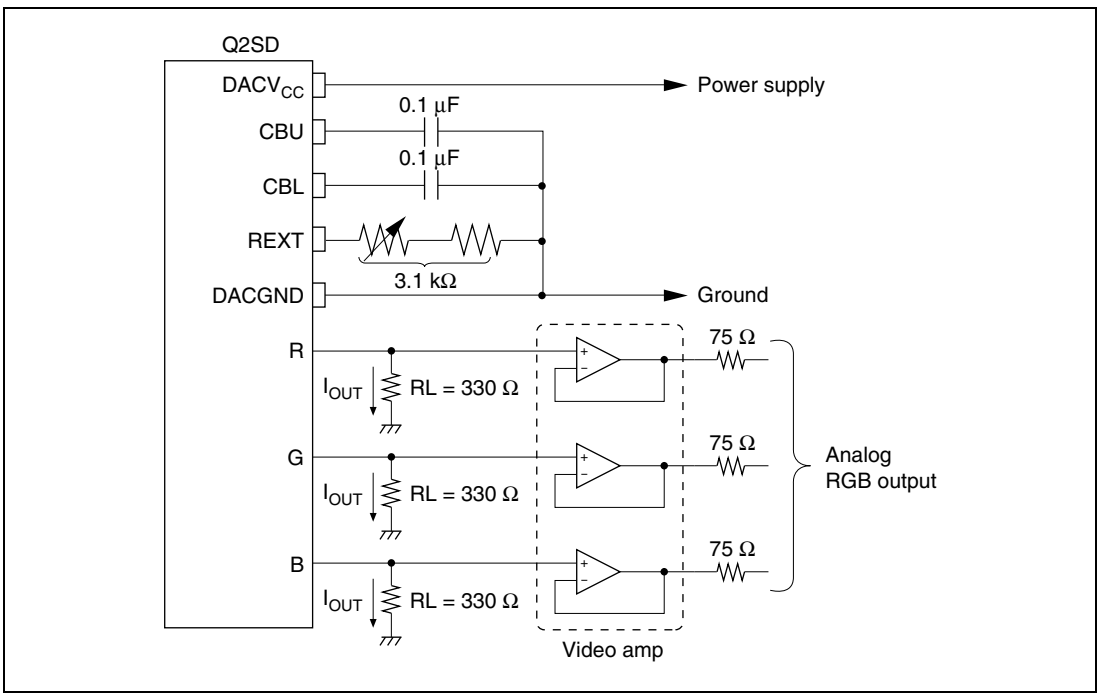


Figure 2.5 Example of Circuit for Connection of REXT, CBU, and CBL Pins

2.8 Video Interface Pins

- VIN0 to VIN7, $\overline{\text{VHS}}$, $\overline{\text{VVS}}$, $\overline{\text{VODD}}$, VQCLK

2.8.1 Video Input Interface

An 8-bit YCbCr 4:2:2 video data that is synchronous with the VQCLK must be input to VIN0 to VIN7. Input must be made to the VQCLK only when there is a valid data in data pairs. A horizontal and vertical synchronous signals must be input to $\overline{\text{VHS}}$ and $\overline{\text{VVS}}$. The start position of

the data fetching is determined by these signals. A signal indicating the video input field must be input to $\overline{\text{VODD}}$. A low-level signal indicates the odd field and a high-level signal indicates the even field.

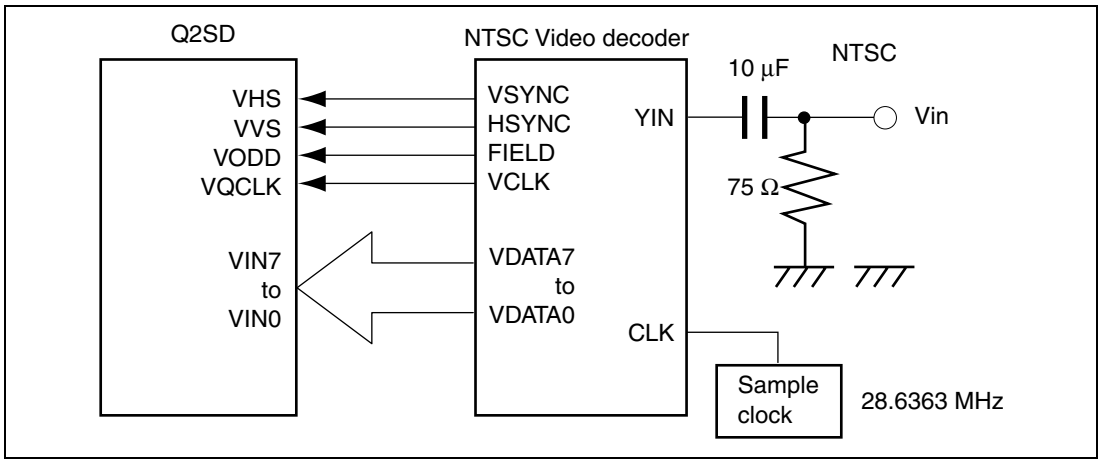


Figure 2.6 Example of Connection of Video Input Pins

Section 3 UGM Architecture

3.1 Features

The unified graphics memory (UGM) connected to the Q2SD is used for the following purposes.

- Foreground (FG), background (BG), and cursor screen areas

  Areas that perform drawing and displaying. Double-buffering architecture (Frame buffer 0: FB0, frame buffer 1: FB1) is used for the foreground screens.

- Display list area

  Area that stores the Q2SD command list. The Q2SD fetches commands from this area while carrying out drawing operations.

- Work, Source, and rendering areas,

  Used as the work area that stores patterns for painting or cutting-out and is for drawing with FTRAP command, as the binary source area that stores font data, as the multi-valued source area that stores natural images and icons, and as the rendering area that is specified by RSAR.

- Video area

  Stores video data for three screens taken by the video capture function (the size of a single screen is a video-window size).

- Others

  The UGM can be allocated to part of the CPU's main memory area, enabling it to be used as CPU work areas as well as for the above purposes.

Figure 3.1 shows a sample system configuration using the UGM, and figure 3.2 shows an example of UGM mapping onto the CPU memory space.

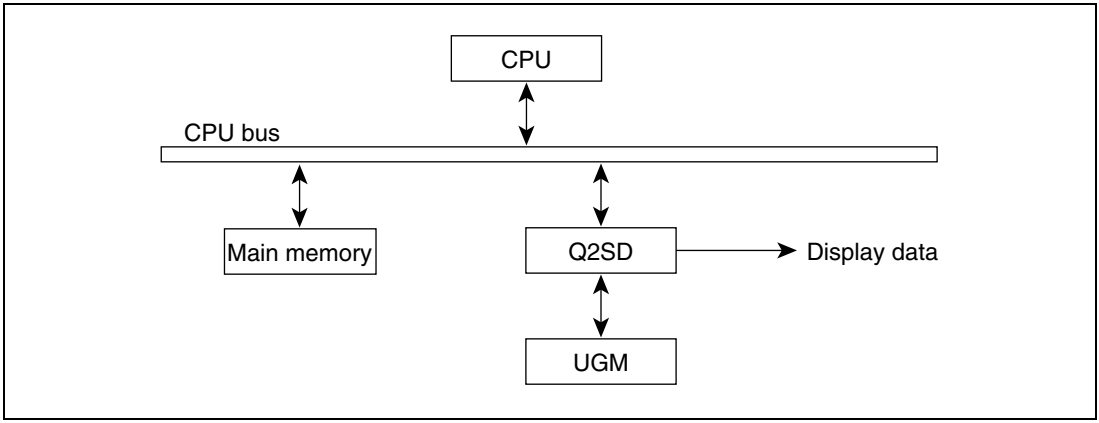


Figure 3.1 Example of System Configuration Using UGM

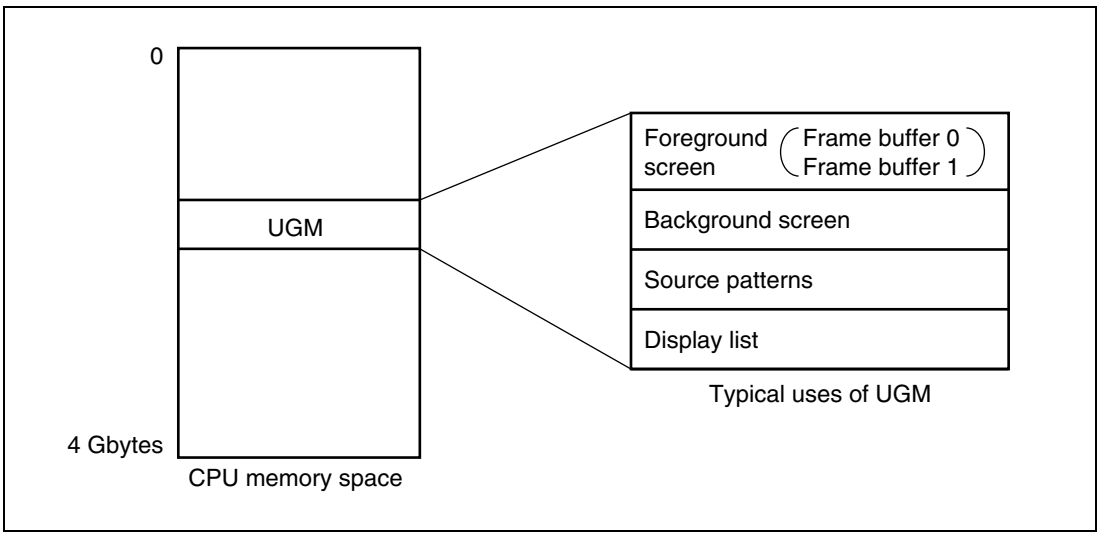


Figure 3.2 Example of UGM Mapping onto CPU Memory Space

3.2 Q2SD Access

3.2.1 UGM Access Priority

The priority order for control of UGM access is as follows:

1. Refreshing
2. Display
3. Video capture
4. CPU

5. Others (command fetches, drawing, source referencing, etc.)

To enable these different kinds of processing to be performed in parallel, after performing access for a fixed period, the Q2SD passes the access control to another source. So if three sources are requesting access, for example, they will perform accesses alternately.

3.2.2 UGM Access by the CPU

The CPU can access the UGM as part of the memory space for the CPU.

In a write operation, access is possible with a minimum number of wait cycles if there is empty space in the Q2SD's built-in 32-byte FIFO buffer.

In a read operation, a number of wait cycles are inserted. The number of wait cycles varies depending on the relationship between the Q2SD operating clock and the display operating clock, and the screen size.

The data stored in the FIFO is transferred to the UGM when the rendering start bit in the system control register (the RS bit in SYSR) is set to 1, when the UGM has not been accessed by the CPU for 32 tcyc0 or more, when the FIFO is full, or when the UGM is accessed by the CPU.

If a SuperH with MMU is used as the CPU, the UGM should be mapped onto a normal space as SRAM. Data transfer between the CPU and Q2SD is synchronized with the Q2SD's system operating clock.

3.2.3 UGM Access by DMAC

Data in the memory connected to the CPU bus can be transferred between the memory and the UGM using the DMAC. DMA transfer can be used to transfer display list or image data.

Single address mode or dual address mode can be used in DMA transfers, since UGM memory addresses are controlled by the Q2SD's built-in address counter. The address mode is specifiable as single address mode or dual address mode. However, only cycle-steal mode can be used as the bus mode. Note that the burst mode is not supported. See section 2.5.3, DMA Writes.

3.2.4 UGM Access by Q2SD

SDRAM can be connected directly to the Q2SD as the UGM. Use of the SDRAM enables the Q2SD to perform memory access in one-cycle (operating clock).

SDRAMs that can be used for the UGM are those that have a power supply voltage of 3.3 V and meet the electrical characteristics and the initialization sequence of the Q2SD. When the bus width of the SDRAM is 16 bits, up to two SDRAMs can be used. The following memory configurations can be used:

- 64-Mbit capacity (1-Mbit × 16 × 4-bank configuration)
- 64-Mbit capacity (512-kbit × 32 × 4-bank configuration)
- 16-Mbit capacity (512-kbit × 16 × 2-bank configuration)

The type of memory is set in the memory mode register (MEMR).

3.2.5 Register Access from the CPU

The Q2SD has address-mapped registers mapped onto the CPU byte address space (H'000 to H'7FF). These registers are divided into five groups—interface control registers, memory control registers, display control registers (including the color palette registers), rendering control registers, and input data control registers. The color palette registers should be access in longwords. The address specification is made by inputting the address from pins A10 to A1 while the $\overline{CS1}$ pin is in the 0 state.

A reserved addresses must not be read from or written to. Reading or writing to these addresses may result in the loss of address-mapped register values, and unpredictable operation by the Q2SD.

To control UGM accesses, initial values must be set in the address-mapped registers by the CPU before it accesses the UGM.

The setting procedure is shown in 1 to 3 below.

1. Set initial values in the system control register (SYSR). Set SRES = 0, DRES = 1, and DEN = 0.
2. Set initial values in other registers.
3. Set SRES = 0 and DRES = 0.

Also, since video control related registers (video area start address register 0 to 2 (VSAR0 to VSAR2), video window size registers (VSIZER), and video incorporation mode register (VIMR)) are externally updated for video capture operations, they should only be rewritten when the VIE bit is cleared to 0 in the video incorporation mode register. The same also applies when updating bits other than VIE in VIMR. The procedure is shown below.

1. Clear the VIE bit to 0 in VIMR. Retain bits other than VIE to the values to which they are set at that time.
2. Modify the contents of VSAR0 to 2 and VSIZER, and bits other than the VIE bit in VIMR after the elapse of one $\overline{VVS}$ cycle.
3. Set the VIE bit to 1 in VIMR. Retain bits other than VIE to the values to which they are set at that time.

3.2.6 Register Updating

External Updating: In external updating, values set in address-mapped registers by the CPU become effective after the end of the CPU access. When the VBK flag and FRM flag in the status register (SR) are set to 1 at the start of vertical blanking, display control related registers which are updated by the external updating, such as the color palette registers, are updated without causing display flicker.

Internal Updating: In internal updating, values set in address-mapped registers become effective when Q2SD internal updating is performed. In the case of registers with an internal update function, therefore, display flicker can be prevented even if the CPU modifies address-mapped registers relating to display operations without being aware of the display timing.

Internal updating is carried out while the DRES bit is set to 1 in the system control register (SYSR) and at the beginning of each frame. Internal updating is also performed at the beginning of each field for WRAP and BG bits in the display mode register (DSMR), and BGSX and BGSY bits in interlace sync & video mode. The update is performed at the falling edge of $\overline{\text{VSYNC}}$ when the TV sync mode setting in DSMR is TVM1 = 0, TVM0 = 0 (master mode), and on detection of the fall of $\overline{\text{EXVSYNC}}$ when TVM1 = 1 and TVM0 = 0 (TV mode). Internal updating is not performed when TVM1 = 0 and TVM0 = 1.

The address-mapped registers provided with an internal update function are shown in table 3.1. The initial values of these registers should be set while the DRES bit is set to 1. However, internal updating is used for display start address registers 0, display start address register 1, and the GBM bits in the rendering mode register in display operations. In drawing operations, external updating is used.

Internal updating is used for the video area start address (VSAR 0 to 2), video area start coordinates (VPR), and video display size (VSIZE) in display operations. In video capture operations, external updating is used.

Table 3.1 Registers with Internal Update Function

- Q2 Control Registers

Address A[10:0]	Name	Abbreviation	Bits with Internal Update Function
H'000	System control register	SYSR	DEN (bit 13)
H'00A	Display mode register	DSMR	WRAP (bit 11) BG (bit 10)
H'00C	Rendering mode register	REMR	GBM (bits 2–0)
H'056	Display mode 2 register	DSMD2	All bits

- Memory Control Registers

Address A[10:0]	Name	Abbreviation	Bits with Internal Update Function
H'010	Display size register X	DSRX	All bits
H'012	Display size register Y	DSRY	All bits
H'014	Display start address register 0	DSAR0	All bits
H'016	Display start address register 1	DSAR1	All bits
H'04C	Background start coordinate register X	BGSRX	All bits
H'04E	Background start coordinate register Y	BGSRY	All bits

- Display Control Registers

Address A[10:0]	Name	Abbreviation	Bits with Internal Update Function
H'026	Display window register (horizontal display start position)	DSWR (HDS)	All bits
H'028	Display window register (horizontal display end position)	DSWR (HDE)	All bits
H'02A	Display window register (vertical display start position)	DSWR (VDS)	All bits
H'02C	Display window register (vertical display end position)	DSWR (VDE)	All bits
H'02E	Horizontal sync pulse width register	HSWR	All bits
H'030	Horizontal scan cycle register	HCR	All bits
H'032	Vertical sync position register	VSPR	All bits
H'034	Vertical scan cycle register	VCR	

- Display Control Registers (cont)

Address A[10:0]	Name	Abbreviation	Bits with Internal Update Function
H'03A	Color detection register H	CDERH	All bits
H'03C	Color detection register L	CDERL	All bits
H'058	Video display position register (horizontal display start position)	VPR (HVP)	All bits
H'05A	Video display position register (vertical display end position)	VPR (VVP)	All bits
H'062	Video area start address register 0H	VSA0H	All bits
H'064	Video area start address register 0L	VSA0L	All bits
H'066	Video area start address register 1H	VSA1H	All bits
H'068	Video area start address register 1L	VSA1L	All bits
H'06A	Video area start address register 2H	VSA2H	All bits
H'06C	Video area start address register 2L	VSA2L	All bits
H'06E	Video window size register X	VSIZERX	All bits
H'070	Video window size register Y	VSIZERY	All bits
H'074	Cursor register (horizontal start position 1)	CSR (HCS1)	All bits
H'076	Cursor register (vertical start position 1)	CSR (VCS1)	All bits
H'078	Cursor register (horizontal start position 2)	CSR (HCS2)	All bits
H'07A	Cursor register (vertical start position 2)	CSR (VCS2)	All bits
H'07C	Cursor area start address register 1	CSAR1	All bits
H'07E	Cursor area start address register 2	CSAR2	All bits

3.2.7 Byte Exchange Function

The word data can be replaced between upper and lower data in byte units by using the DTP and MDTP of the input data transfer mode register (IEMR). MDTP is referenced when the data is directly transmitted to the UGM, and DTP is referenced when the data is transmitted to the UGM via the image data entry register (IDER).

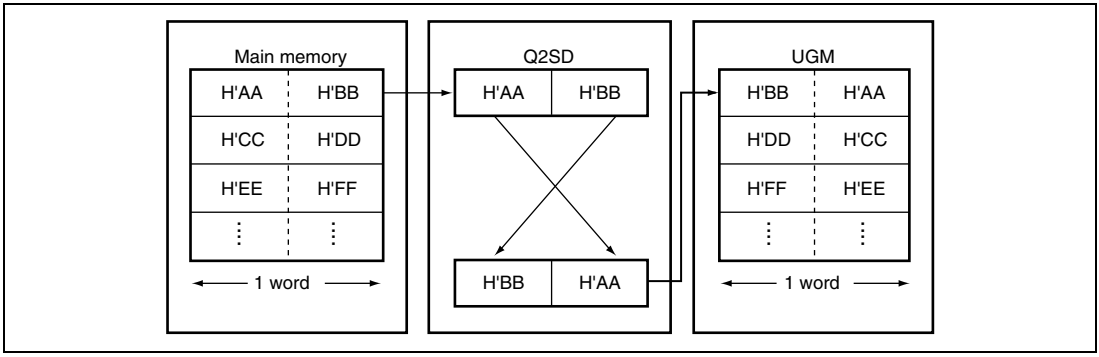


Figure 3.3 Byte Exchange Diagram

3.2.8 2-Dimensional Image Data Exchange Function

Conversion of 2-dimensional image data: Image data which is stored in the linear address format in the main memory, etc., can be converted to the two-dimension image data and transferred to UGM. When the image data is transmitted to the image data entry register (IDER) using the CPU, the Q2SD converts the data to the two-dimension image data and stores it in UGM. The supported data format is shown below. For details of the data format, section 3.2.9, Input Color Data Configurations, and section 3.2.10, Configurations of Data in UGM.

IDER Input Data		**UGM Data**
Linear address ΔYUV data (ΔY, ΔU, ΔV 4 bits each)	→	Two-dimension RGB data (R: 5 bits, G: 6 bits, B 5 bits)
Linear address (YUV data (4:2:2 format))	→	Two-dimension RGB data (R: 5 bits, G: 6 bits, B 5 bits)
Linear address (16 bits/pixel data)	→	Two-dimension 16 bits/pixel data
Linear address (8 bits/pixel data)	→	Two-dimension 8 bits/pixel data

The converted RGB data can be used for the source data of the 4-vertex screen drawing command and the data for each display screen.

Q2SD registers that should be set by the CPU are shown in figure 3.4. Make the register settings in the order shown in figure 3.5.

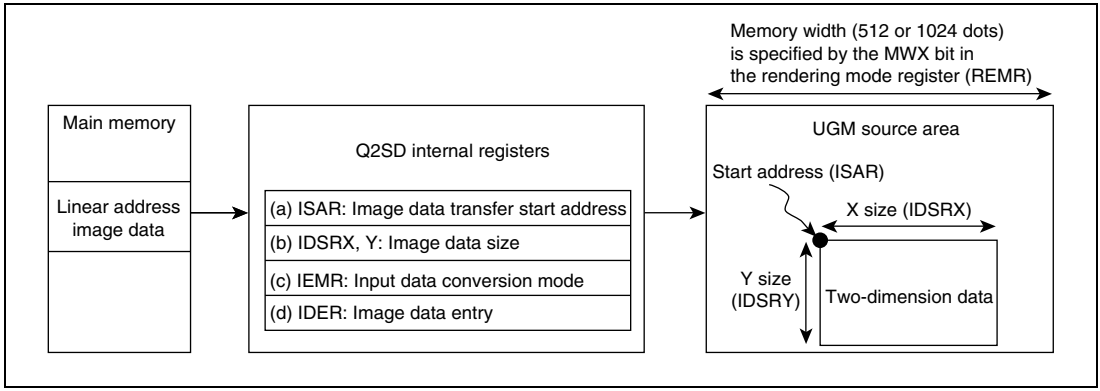
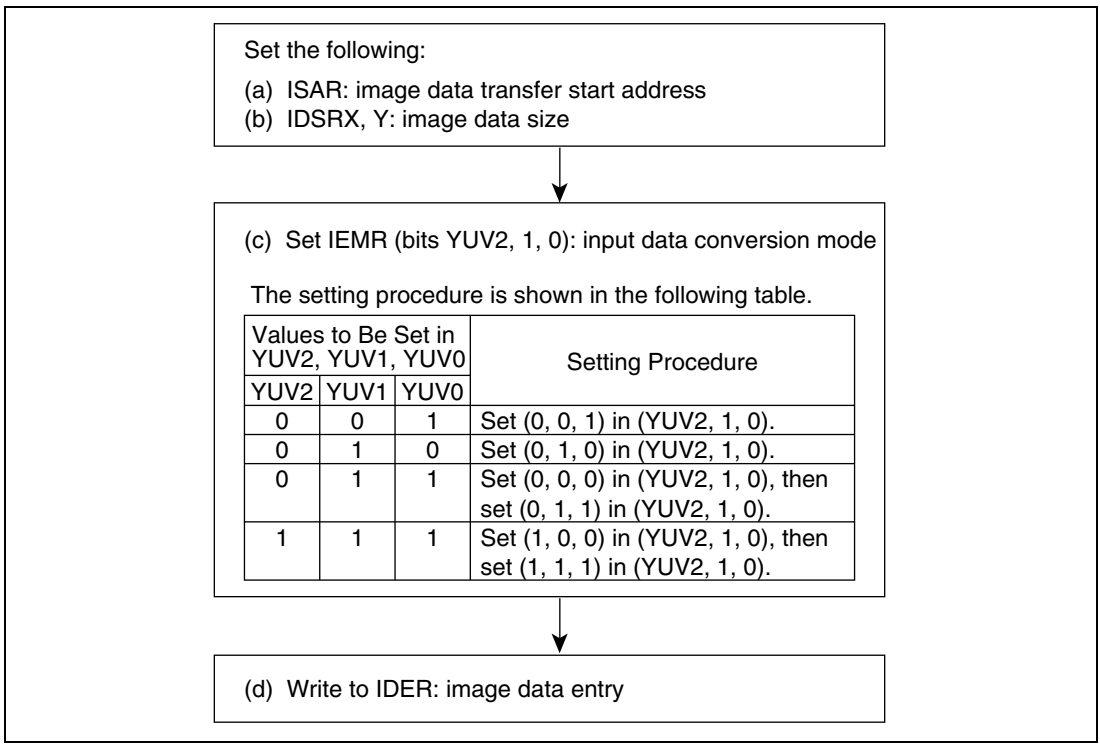


Figure 3.4 Image Data Specifications



Values to Be Set in YUV2, YUV1, YUV0			Setting Procedure
YUV2	YUV1	YUV0	
0	0	1	Set (0, 0, 1) in (YUV2, 1, 0).
0	1	0	Set (0, 1, 0) in (YUV2, 1, 0).
0	1	1	Set (0, 0, 0) in (YUV2, 1, 0), then set (0, 1, 1) in (YUV2, 1, 0).
1	1	1	Set (1, 0, 0) in (YUV2, 1, 0), then set (1, 1, 1) in (YUV2, 1, 0).

Figure 3.5 Register Setting Procedure for ΔYUV/YUV-to-RGB Conversion

2. Sample settings for two-dimension image by DMA transfer

When performing two-dimension image conversion by DMA transfer, ensure that the number of pixels corresponding to DMA transfer word count registers H and L (DMAWRH, DMAWRL) is the same as the total number of pixels specified by image data size registers X and Y (IDSRX, IDSRY).

If these two values are not the same, DMA transfer will end at the smaller of the two values, and then bits YUV2, YUV1, and YUV0 will be cleared to 000, and bits DMA1 and DMA0 will be cleared to 00 again.

Therefore, if the total transfer word count of the source data is larger than the DMA transfer word count, DMAWR, the DMA setting must be divided into a number of stages. The image data transfer start address register (ISAR) must be set each time this conversion is performed.

3. An example of the settings for transferring 320 × 240 YUV source data to UGM by means of four DMA_YUV operations

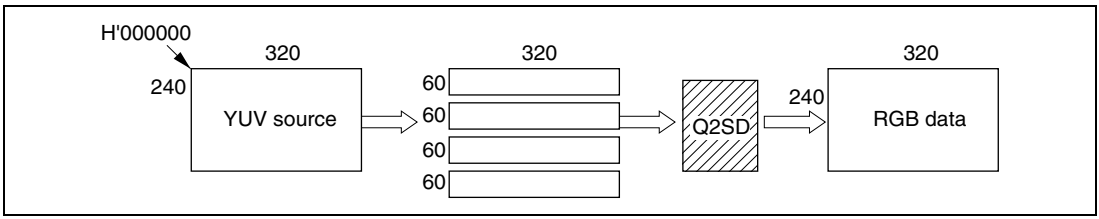


Figure 3.6 Example of Settings for Transferring 320 × 240 YUV Source Data to UGM by Means of Four DMA Operations

Conditions:
- YUV source size: 320 × 240 dots
- Number of setting stages: 4
- UGM transfer destination address: H'000000
- YUV mode: YUV-RGB conversion

- 1st time
  (1) Image data transfer start address setting
  ISAR = H'000000
  (2) Image data transfer size register settings[*1]
  IDSRX = 320
  IDSRY = 60
  (3) DMA transfer word count setting[*2]
  DMAWR = 19200
  (4) YUV mode setting
  IEMR = H'01
  (5) DMA mode setting
  DMA in SYSR = H'11
  (6) Wait until the DMF bit in the status register (SR) changes to 1.

- 2nd time onward
  (7) Image data transfer start address re-setting[*3]
  ISAR = current ISAR + transfer word count (Y) = H'C180

(8) Image data transfer size register settings[*4]
IDSRX = 320
IDSRY = 60

(9) DMA transfer word count setting[*5]
DMAWR = 19200

(10) YUV mode setting
IEMR = H'01

(11) DMA mode setting
DMA in SYSR = H'11

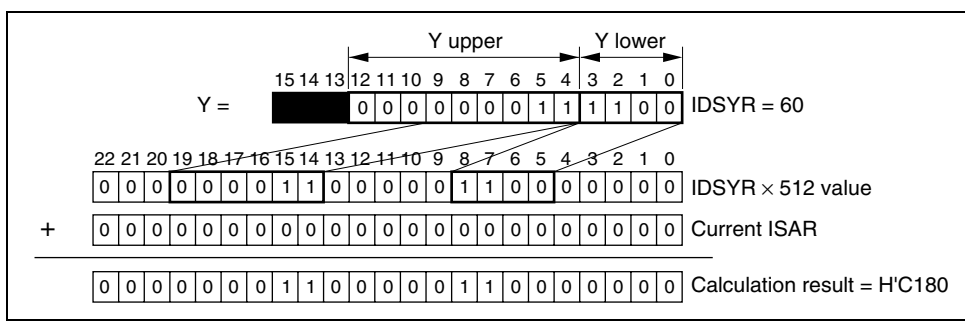
Steps (6) to (11) are then repeated until the end of the YUV transfer source. Settings for YUV-RGB conversion are also made as shown in the above example.

Notes: 1. Where IDSRX and IDSRY satisfy the following conditions:
- The transfer unit is a line.
- One transfer is within the DMAWR range.

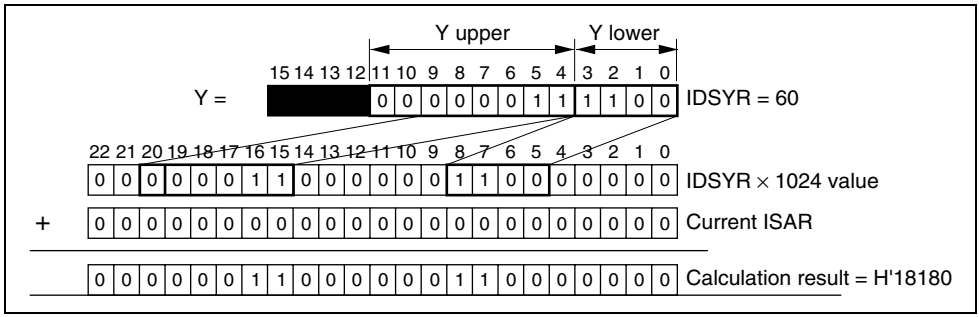
2. Set the transfer word count corresponding to IDSRX/IDSRY.
3. In the Q2SD, addresses of the foreground screen area are allocated as shown in section 3.3.2, Memory Map. Therefore, set the drawing data transfer start address in ISAR with reference to the relationship between memory physical addresses and coordinates shown in figure 3.9).

   In this setting example, the start position of the second image data transfer is at the [X = 0, Y = 60] dot position. This position is divided into the upper and lower coordinates of X and Y, respectively, and the value assigned in figure 3.9 is the value set in ISAR the second time.

   Example: Method of calculating second ISAR, with memory width of 512 (from figure 3.9)



Example: Method of calculating second ISAR, with memory width of 1024 (from figure 3.9)



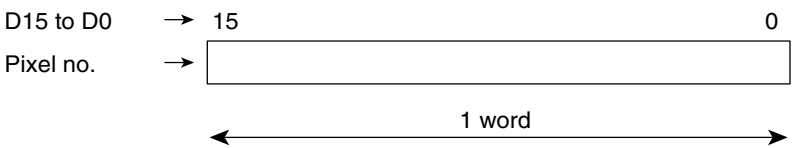
Notes: 4. Same setting conditions as for (2).

5. Same setting conditions as for (3).

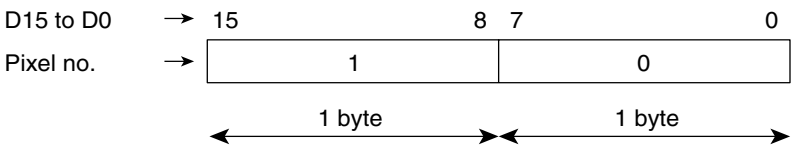
3.2.9 Input Color Data Configurations

Input data configurations are shown below. The pixel number starting with 0 runs from left to right in ascending order.

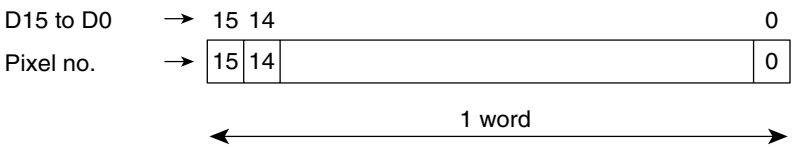
- 16-bit data



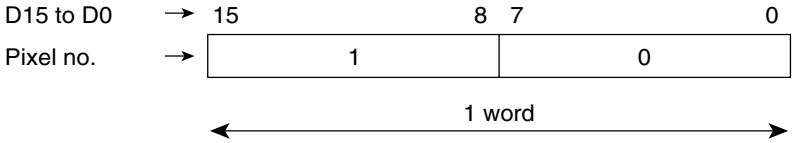
- 8-bit data



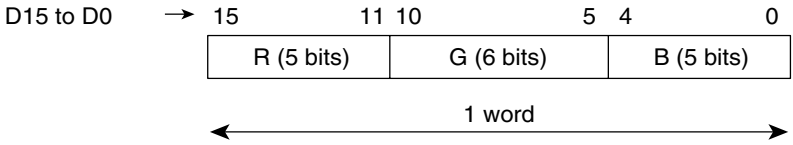
- 1 bit/pixel data



- 8-bit/pixel data

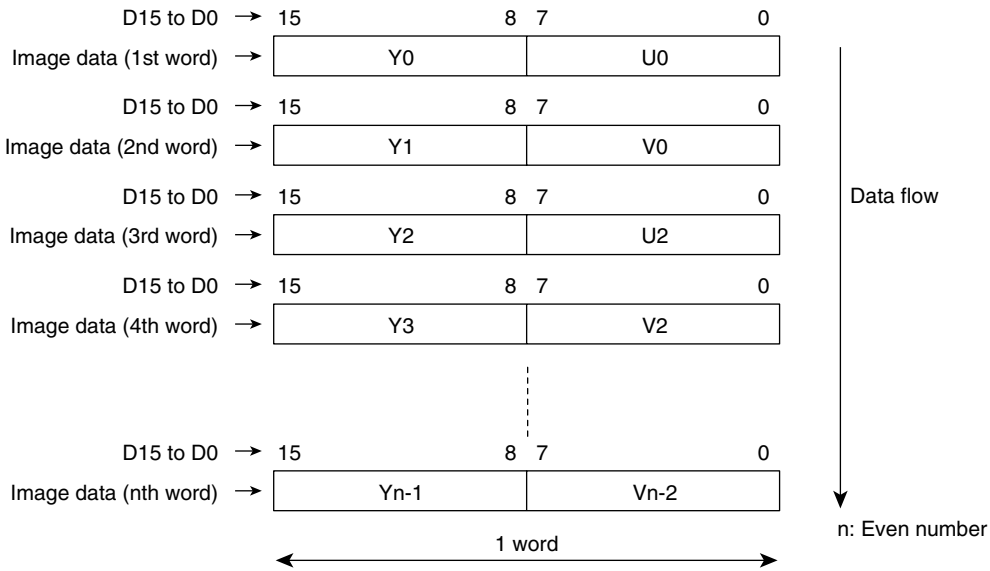


- RGB data (16-bit/pixel data)



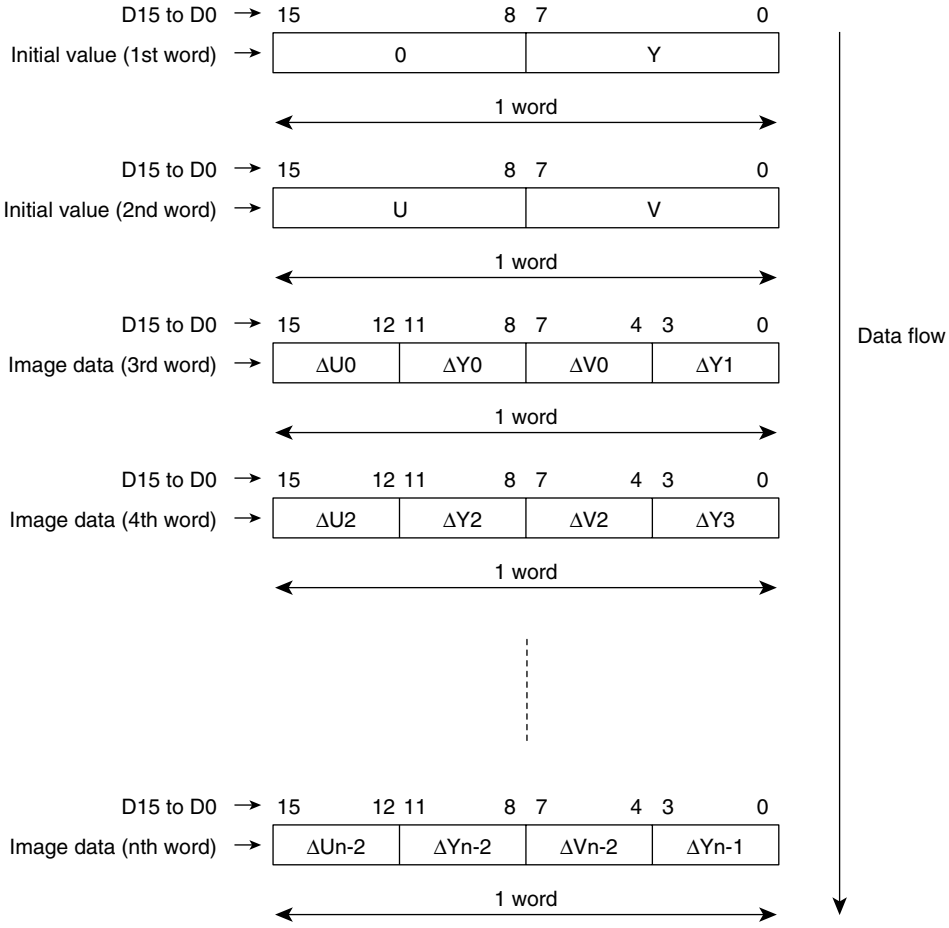
- YUV data

YUV data uses a 4:2:2 format. The U and V data is horizontally reduced data.



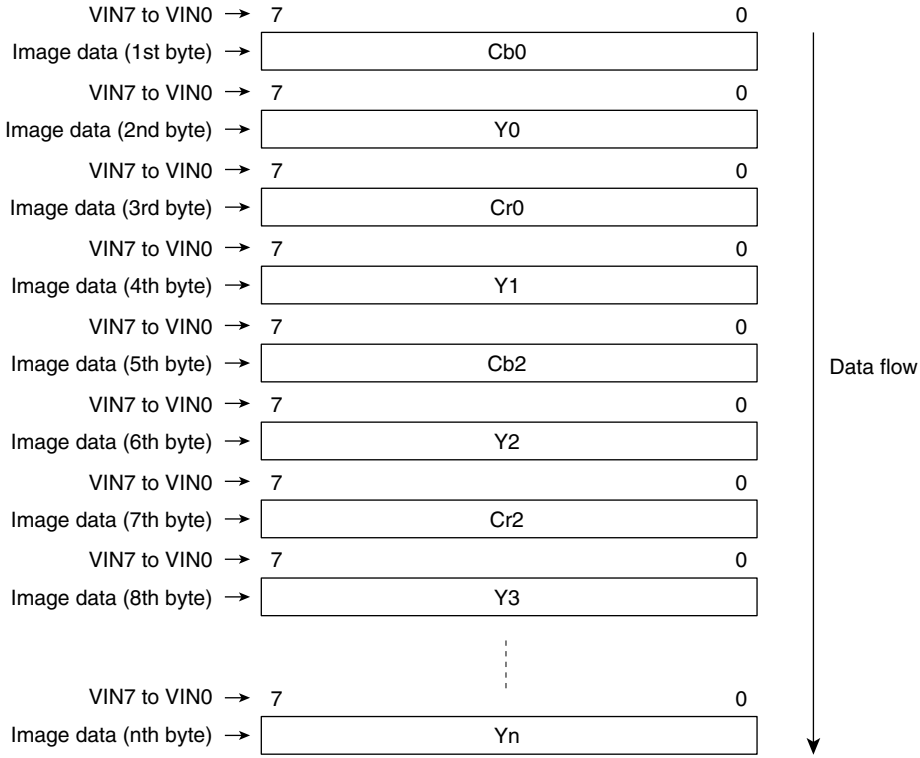
- ΔYUV data

  ΔYUV data uses a raster as the basic unit. The data configuration for one raster consists of the initial value in the first two words and compressed image data in the remaining words.



- YCbCr data

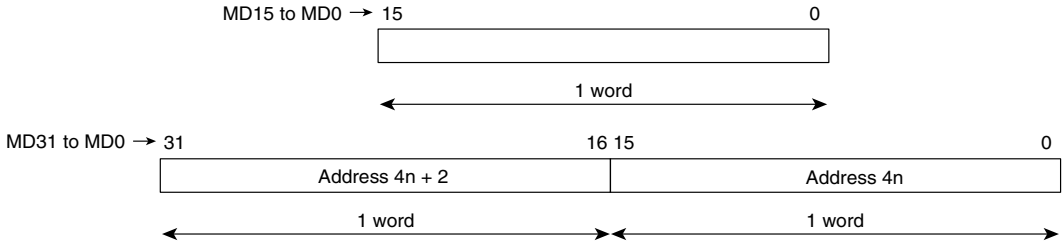
The data is input from the video capture input. The YCbCr data is eight bits in 4:2:2 format.



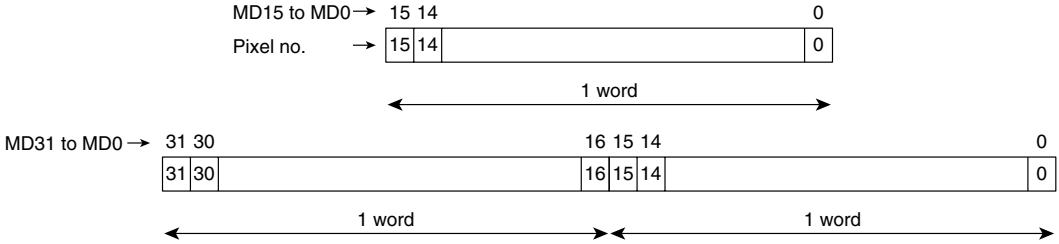
3.2.10 Configurations of Data in UGM

The UGM data configuration is shown below (first for a UGM 16-bit bus, then for a 32-bit bus). The image data is handled as little endian format by the Q2SD. The pixel number starting with 0 runs from left to right in ascending order.

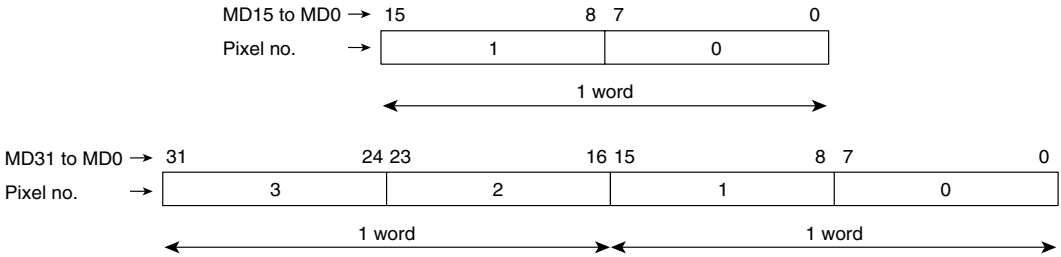
- 16-bit data



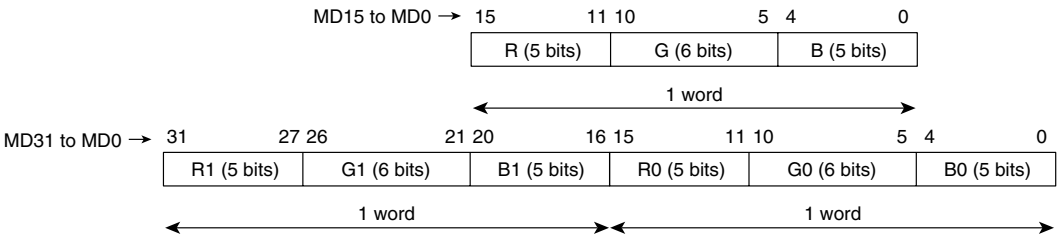
- 1-bit/pixel data



- 8-bit/pixel data

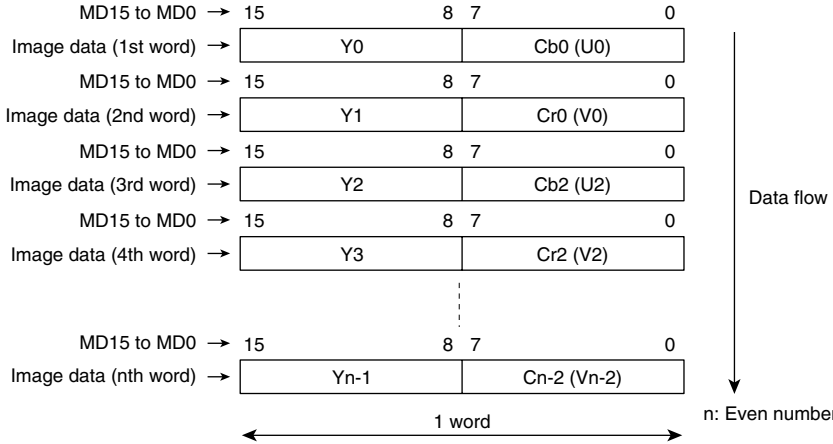


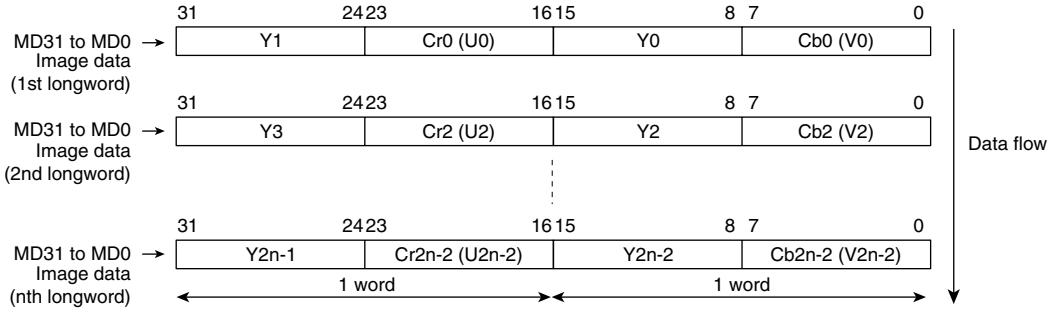
- RGB data (16-bit/pixel data)



- YCbCr data (YUV data)

  YCbCr (YUV) data uses a 4:2:2 format. Cr and Cb (U and V) data is horizontally reduced data.





3.2.11 Q2SD Internal Data Format

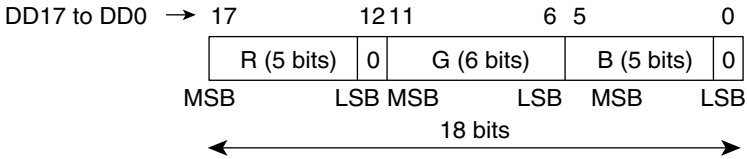
Color data configurations in the Q2SD are shown below.

- RGB data

  The display data configurations used in the display unit is shown below.

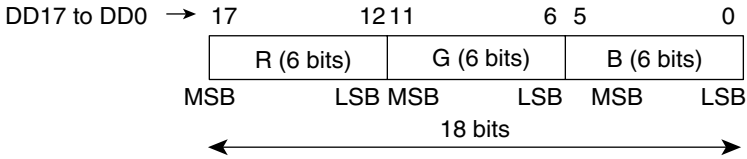
  — When the UGM data is 16 bits/pixel and the color palette is not used

  A pixel with H'0000 on the foreground or cursor screen is a transparent color and the data on the lower screens shows through regions set to this color.



— When the UGM data is 8 bits/pixel and the color palette is used, or the UGM data is YCbCr format

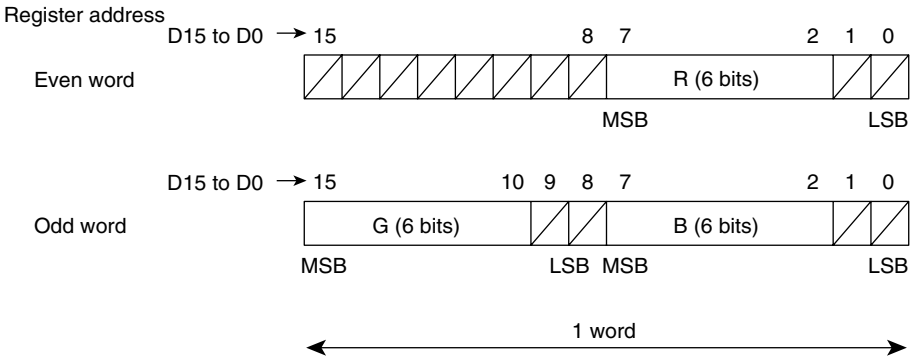
A pixel with H'00000000 on the foreground or cursor screen is a transparent color and the data on the lower screens shows through regions set to this color.



DD17 to DD0 are internal signals. Q2SD analog output is the result of D/A conversion of the above data.

- **Color palette register color data configuration**

— The color palette register color data configuration is shown below. H'0000 0000 is a transparent color and the data on the lower screens shows through regions set to this color.



3.2.12 Interrupt Output Function

The Q2SD outputs interrupt output signal caused by various sources. The generation of interrupt source is reflected in the status register (SR). The selection of interrupt source is set in the interrupt enable register (IER) for use by transfer of the display list or source data to UGM, controlling cursor blinking, controlling DMA transfer, and error processing, etc.

Table 3.2 Interrupt Output Function

Status Register (SR) Bit	Description	Processing
TVR	The expected signal ($\overline{\text{EXVSYNC}}$) is not input	Error processing
FRM	The display frame is switched	Drawing processing, display processing, and data transfer processing
DMF	DMA transfer is completed	Data transfer processing
CER	Invalid command is detected	Error processing
VBK	The display field is switched	Drawing processing, display processing, and data transfer processing
TRA	The TRAP command is executed	Drawing processing, display processing, and data transfer processing
CSF	The frame is changed before the completion of the command	Error processing
BRK	Command execution is aborted by the RBRK bit of the system control register (SYSR)	Drawing is aborted and restarted. Debugging by software is performed.

3.3 Unified Graphics Memory (UGM)

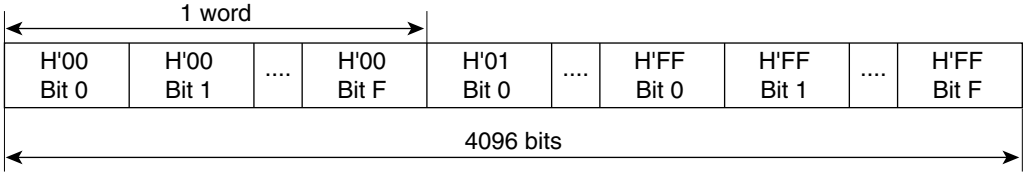
3.3.1 Memory Address

(1) One Memory Unit

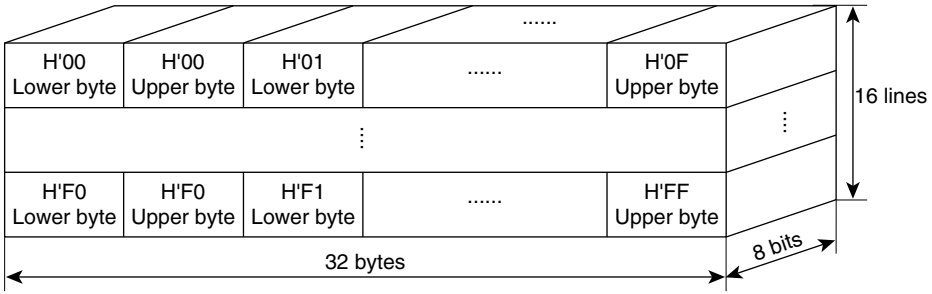
The Q2SD performs UGM address control. The UGM includes the display list area, binary source area, 8-bit/pixel or 16-bit/pixel source area, 8-bit/pixel or 16-bit/pixel rendering area, binary work area, and video area. The UGM is configured in 512-byte units, and a different memory configuration is used for each area. The memory configuration for each of the areas is shown in figure 3.7.

The UGM consists of addresses that are consecutive within one memory unit (linear addresses), as shown in figure 3.8.

1-bit/pixel (work, binary source, display list):



8 bits/pixel (multi-valued source, multi-valued destination):



16 bits/pixel (multi-valued source, multi-valued destination, video):

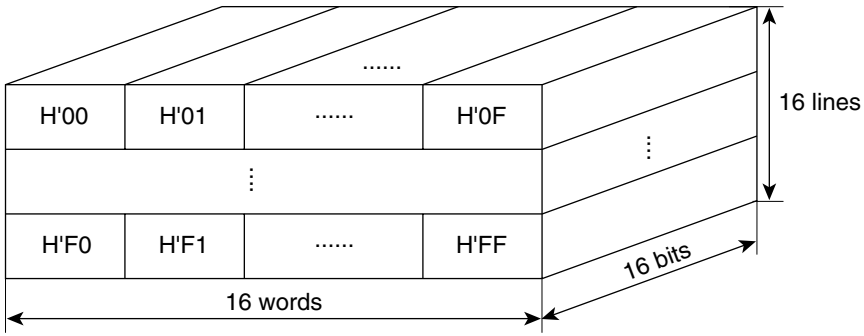


Figure 3.7 Configuration of One Memory Unit (512 Bytes)

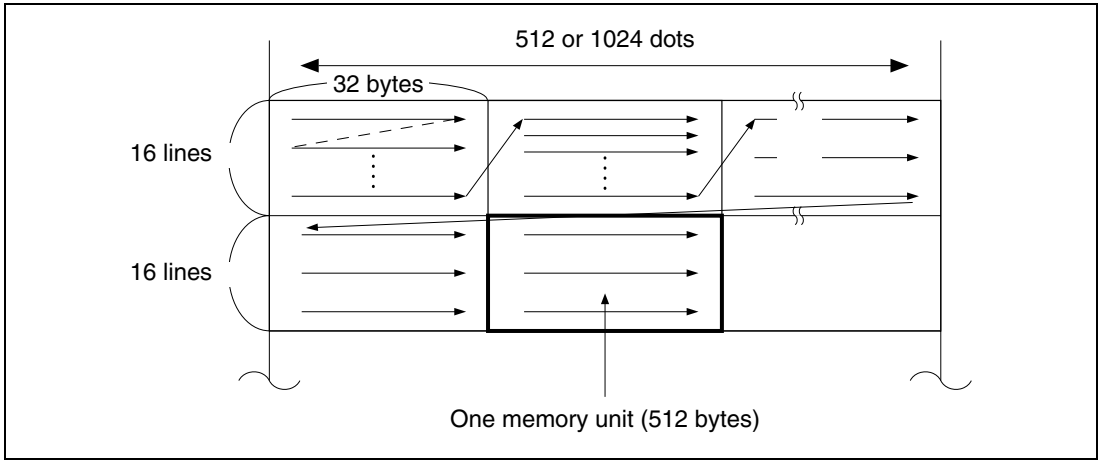


Figure 3.8 UGM Address Transitions

(2) 2-dimensinal Virtual Addresses

The Q2SD handles the UGM as a 2-dimensinal virtual address space. The 2-dimensinal virtual address space is represented by the X-axis corresponding to the horizontal direction of the display and the Y-axis corresponding to the vertical direction. The original corresponds to a physical address of H′00 in the UGM. The possible range on the X-axis is from 0 to 511 or from 0 to 1023, and that on the Y-axis is 0 or greater. The Q2SD processes displaying and drawing based on the 2-dimensinal virtual addresses. Conversion between 2-dimensinal virtual addresses and UGM physical addresses shown in figure 3.9 is performed by the Q2SD. The upper bits of the X coordinate and lower bits of the X coordinate refer to the values when the X values are divided into the respective bit widths. Similarly, the Y upper coordinate and Y lower coordinate are the values when the Y values are divided. When the CPU directly accesses the UGM to modify the image data, take this conversion account into consideration.

(3) Linear Addresses

The Q2SD can handle part of the UGM as a linear address space. The area should be specified to the linear address space and the start address in the UGM should be specified. The addresses of this area is represented by physical addresses.

8 bits/pixel, MWX = 0 (512 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Upper bits of Y coordinate										Upper bits of X coordinate				Lower bits of Y coordinate				Lower bits of X coordinate				

8 bits/pixel, MWX = 1 (1024 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Upper bits of Y coordinate										Upper bits of X coordinate				Lower bits of Y coordinate				Lower bits of X coordinate				

16 bits/pixel, MWX = 0 (512 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Upper bits of Y coordinate										Upper bits of X coordinate				Lower bits of Y coordinate				Lower bits of X coordinate				0

16 bits/pixel, MWX = 1 (1024 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Upper bits of Y coordinate										Upper bits of X coordinate				Lower bits of Y coordinate				Lower bits of X coordinate				0

Upper line: UGM physical addresses (bytes) A22 to A1, A0
Lower line: 2-dimensional virtual addresses (X, Y)

Note: A0 is an LSI internal signal, indicating the least significant bit of the byte address. The least significant bit of the byte address is decoded and output to pins UDQM0, UDQM1, LDQM0 and LDQM1.

Figure 3.9 Correspondence between UGM Physical Addresses (Bytes) and 2-Dimensinal Virtual Addresses

(4) Work Addresses

The Q2SD handles part of the UGM as a work address space. Work addresses are 2-dimensinal addresses and one dot corresponds to one address.

The work address space starts from the address specified by the work area start address register (WSAR). The work address space configures a 2-dimensional space by wrapping around at every 512 or 1024 pixels. The number of pixels for wrap-around is specified by the memory width bit in the rendering mode register (the MWX bit in REMR). Figures 3.10 and 3.11 show the examples.

The memory capacity required for the work address space is (the number of pixels specified by the MWX bit) × (YMAX in the SCLIP command + 1)/8 [bytes]. In general, one less than the number of display lines in the vertical direction should be set as YMAX in the SCLIP command.

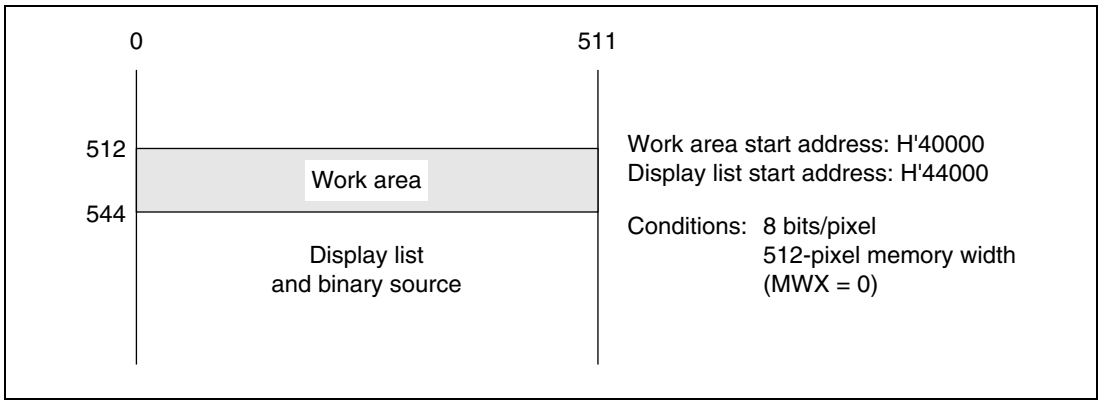


Figure 3.10 Work Address Space

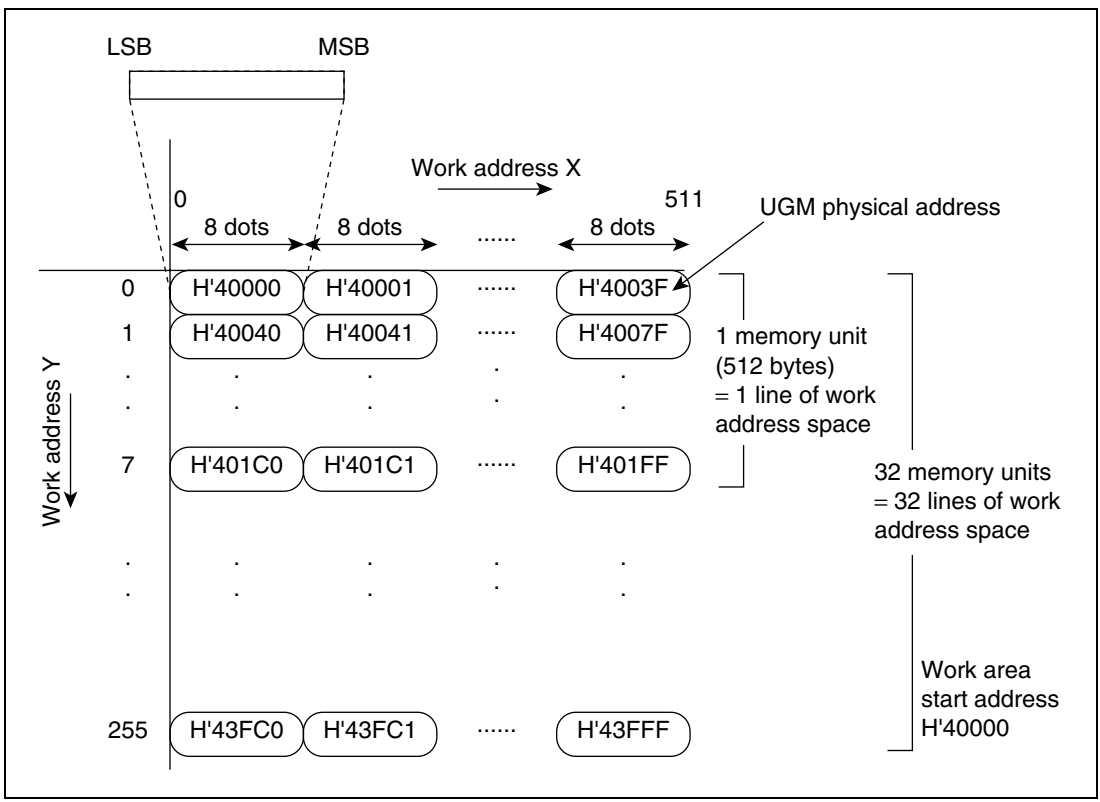


Figure 3.11 Relationship between UGM Physical Addresses (Byte) and Work Addresses

(5) UGM Physical Addresses

The UGM addresses range from H′000000 to H′37FFFE when two memories of 16 Mbits × 16 or from H′000000 to H′7FFFFE when a single memory of 64 Mbits × 32.

3.3.2 Memory Map

Figure 3.12 shows a memory map of the UGM. A combination of 8-bit/pixel and 16-bit/pixel areas can be used in the UGM, but area allocation must be carried out so that areas do not overlap. For this purpose, 8-bit/pixel and 16-bit/pixel areas should virtually be considered as shown in figure 3.13 when performing area allocation. In terms of the number of Y-direction dots, there is a 2-to-1 relationship between the 8-bit/pixel and 16-bit/pixel memory maps.

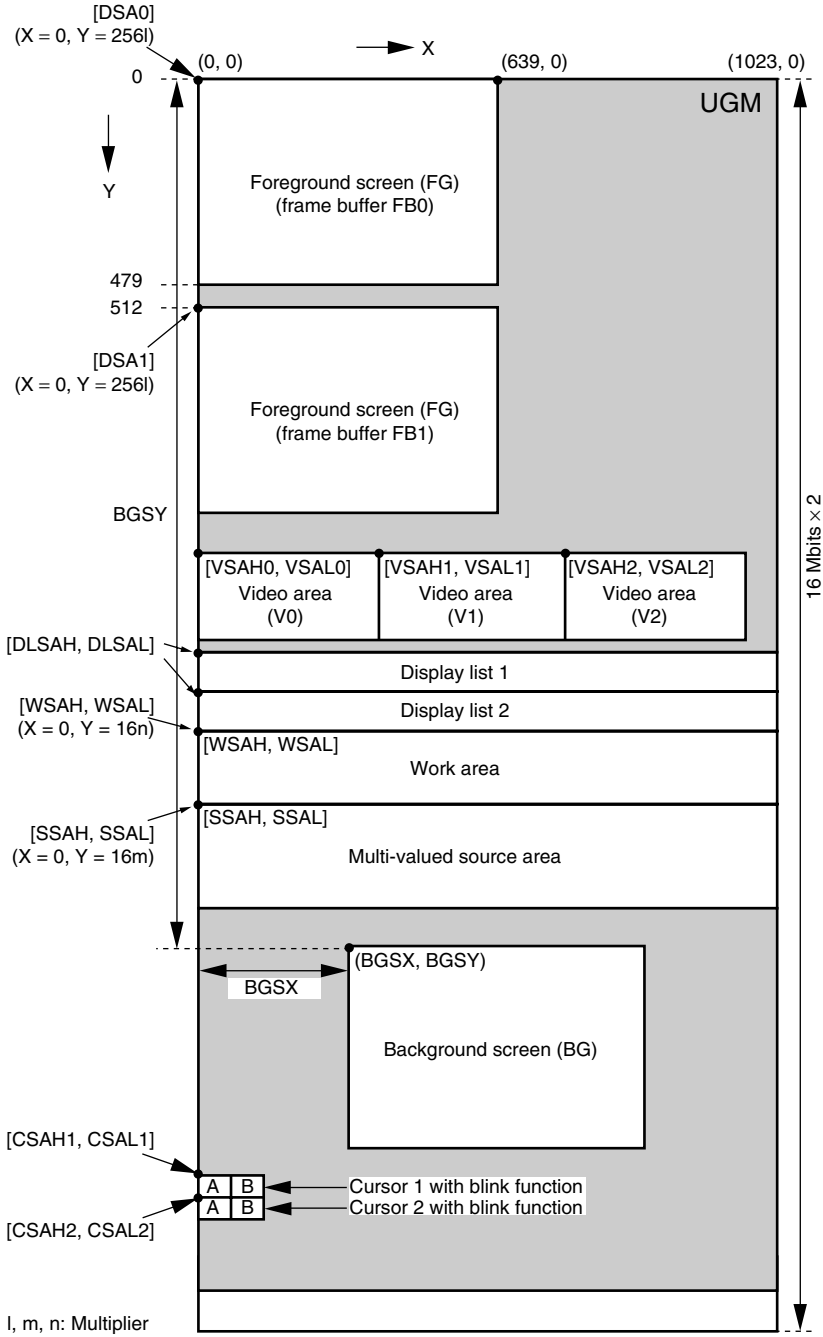


Figure 3.12 Sample Memory Map
(Corresponding to 640 × 480 Screen Size, with 16 Bits/Pixel)

- [WSAH, WSAL]: Addresses which can be specified by bits A22 to A13
- [SSAH, SSAL]: Addresses which can be specified by bits A22 to A13
- [DSA0], [DSA1]: Addresses which can be specified by bits A22 to A16
- [DLSAH, DLSAL]: Addresses which can be specified by bits A22 to A5
- [VSAHn, VSALn]: Addresses which can be specified by bits A22 to A10 (n = 0, 1, and 2)

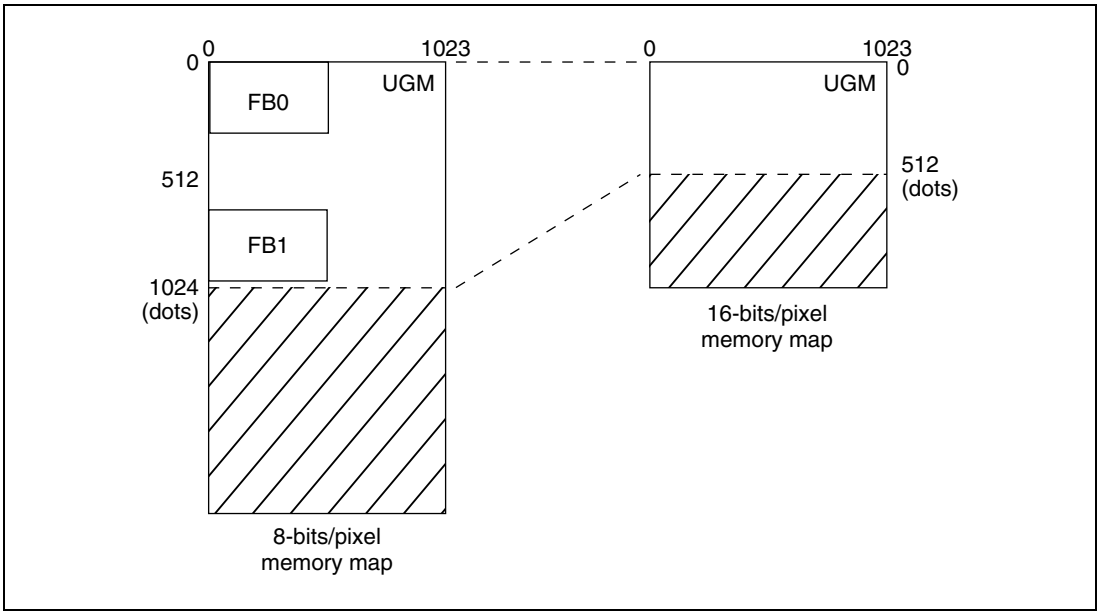


Figure 3.13 Relationship between 8-Bits/Pixel and 16-Bits/Pixel Memory Maps

If a 1024-pixel memory width configuration is used when the horizontal screen size is 512 pixels or less (e.g. 320 × 240 equivalent), the foreground screen FB1 can be set from position X = 512 by setting the HDIS bit in display mode register 2 (DSMR2) to 1. In this case, the same value is set in DSA0 and DSA1. When the HDIS bit is set to 1, use the following settings: GBM2 = 0, BM1 = 0, and RSAE = 0.

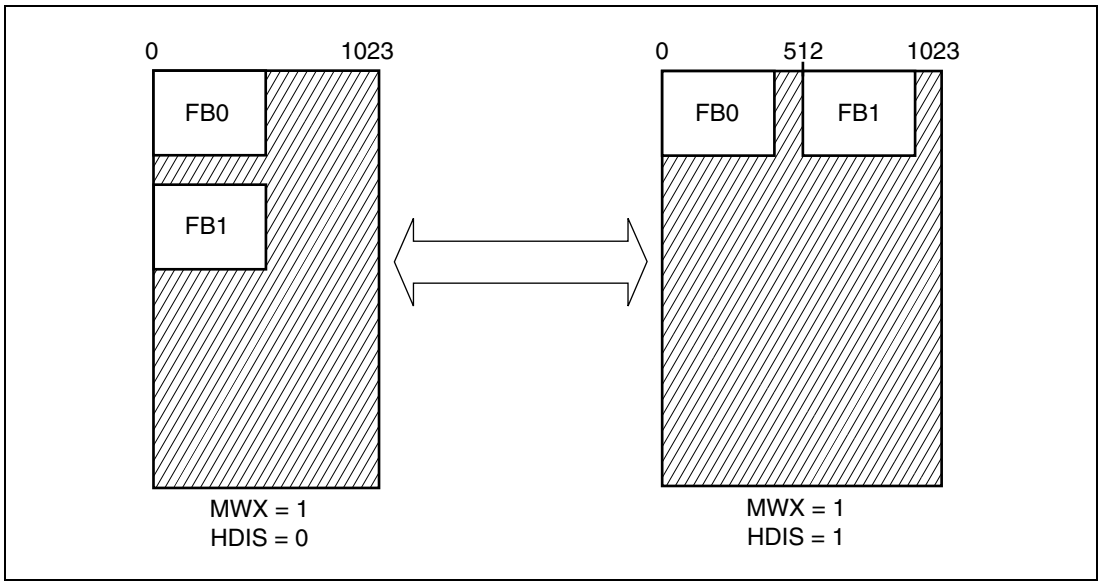


Figure 3.14 Example of Frame Buffer FB1 Location When HDIS = 1

3.3.3 Coordinate Systems

(1) Coordinates

The Q2SD has screen coordinates for display control, rendering, work, multi-valued source, and binary source coordinates for drawing control, and foreground screen, background screen, video screen, and cursor coordinates for display screen.

In the Q2Sd 2-dimensional coordinates, a set of coordinates indicates a single pixel (except for video coordinates in YCbCr format). An X coordinate corresponds to the horizontal direction of the display screen and a Y coordinate corresponds to the vertical direction. The positive coordinates indicate the right direction for X coordinates and the lower direction for Y coordinates.

There are three types of the correspondences between coordinates and UGM addresses: 2-dimensional virtual addresses, linear addresses, and work addresses. The coordinates in which addresses can be handled as 2-dimensional virtual addresses are screen, rendering, multi-valued source, foreground screen, background screen, and video screen coordinates. However, the multi-valued source coordinates are handled as 2-dimensional virtual addresses only when LNi = 0

(source linear specification of the rendering attribute). The coordinates in which addresses can be handled as linear addresses are multi-valued source, binary source, and cursor coordinates. The coordinates in which addresses can be handled as work addresses are work coordinates. For details of the 2-dimensional virtual, linear, and work addresses, see section 3.3.1, Memory Address.

(2) Screen Coordinates

The screen coordinates are for display control. The origin of this coordinates corresponds to the upper-left of the display area. A step of the X coordinates corresponds to a dot and a step of the Y coordinates corresponds to a line (one raster). For example, the upper-left and lower-right coordinates of the yw-by-xw display area are (0, 0) and (xw – 1, yw – 1) in the screen coordinates. The correspondences vary in each display screen. The origin of the foreground screen corresponds to that of the screen coordinates. The start coordinates of the background screen are the same as that of the screen coordinates. The origins of the video and cursor screens are within the screen coordinates specified by the video display start position registers (VPR) and cursor display start position registers (CSR).

The maximum X values in the screen coordinate is 1023 or 511 which is specified by the memory width bit in the rendering mode register (the MWX bit in REMR).

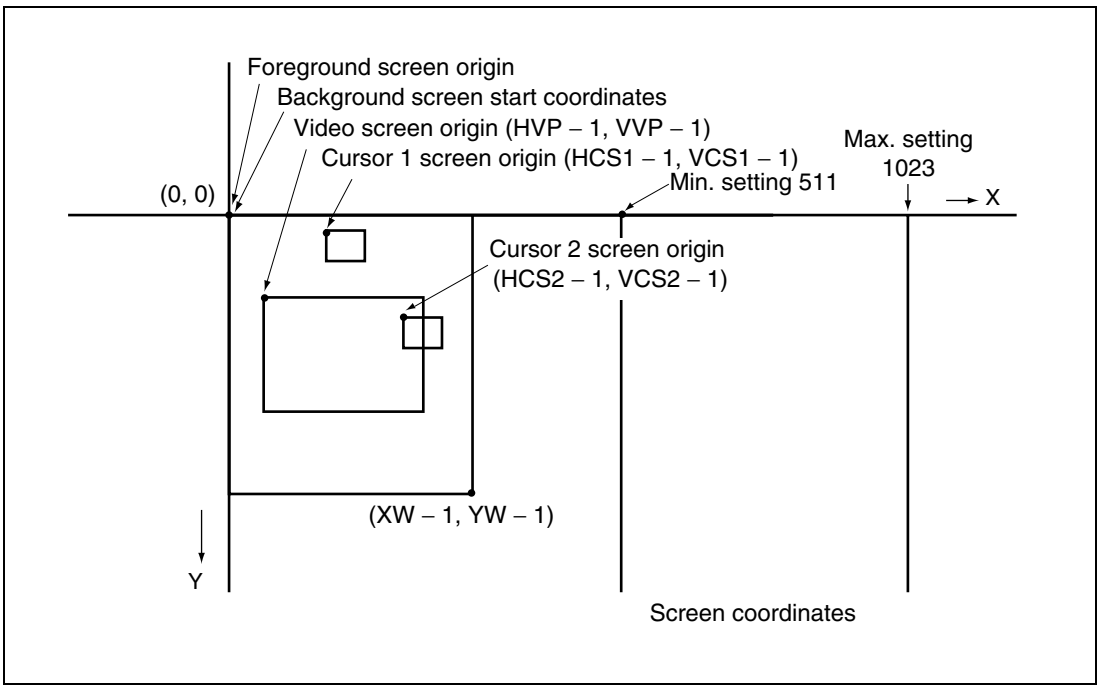


Figure 3.15 Screen Coordinates

(3) Rendering Coordinate System

This is the coordinate system used for drawing control as destination coordinates for drawing commands. It has a fixed size as shown in figure 3.15. The coordinates which exceeds the fixed size cannot be handled. The origin of the rendering coordinates corresponds to the display address register (DSAR0 and DSAR1) contents when the RSAE bit in the rendering mode register (REMR) is cleared to 0, and the rendering start address register (RSAR) contents when the RSAE bit in the rendering mode register (REMR) is set to 1. Eight bits or 16 bits of data width (8 bits/pixel or 16 bits/pixel) for a set of the rendering coordinates can be selected by the graphic bit mode bits in the rendering mode register (bits GBM 2 to GBM 0 in REMR).

Drawing operations for coordinates outside the clipping area are performed. However, accesses to the UGM are not performed. The rendering coordinates origin can be shifted in both horizontal and vertical directions by the offset specified by the local offset command (LCOFS). In this case, the coordinates to which the offset values XO and YO specified by the LCOFS command are added must be within the range shown in the following expressions. Of all drawing commands, the commands which specifies clipping (SCLIP and UCLIP) are handled as the rendering coordinates without offset.

(When bold line attribute is specified)

$$-2045 \leq X + XO \leq 2044$$
$$-2045 \leq Y + YO \leq 2044$$

(When bold line attribute is not specified)

$$-2048 \leq X + XO \leq 2047$$
$$-2048 \leq Y + YO \leq 2047$$

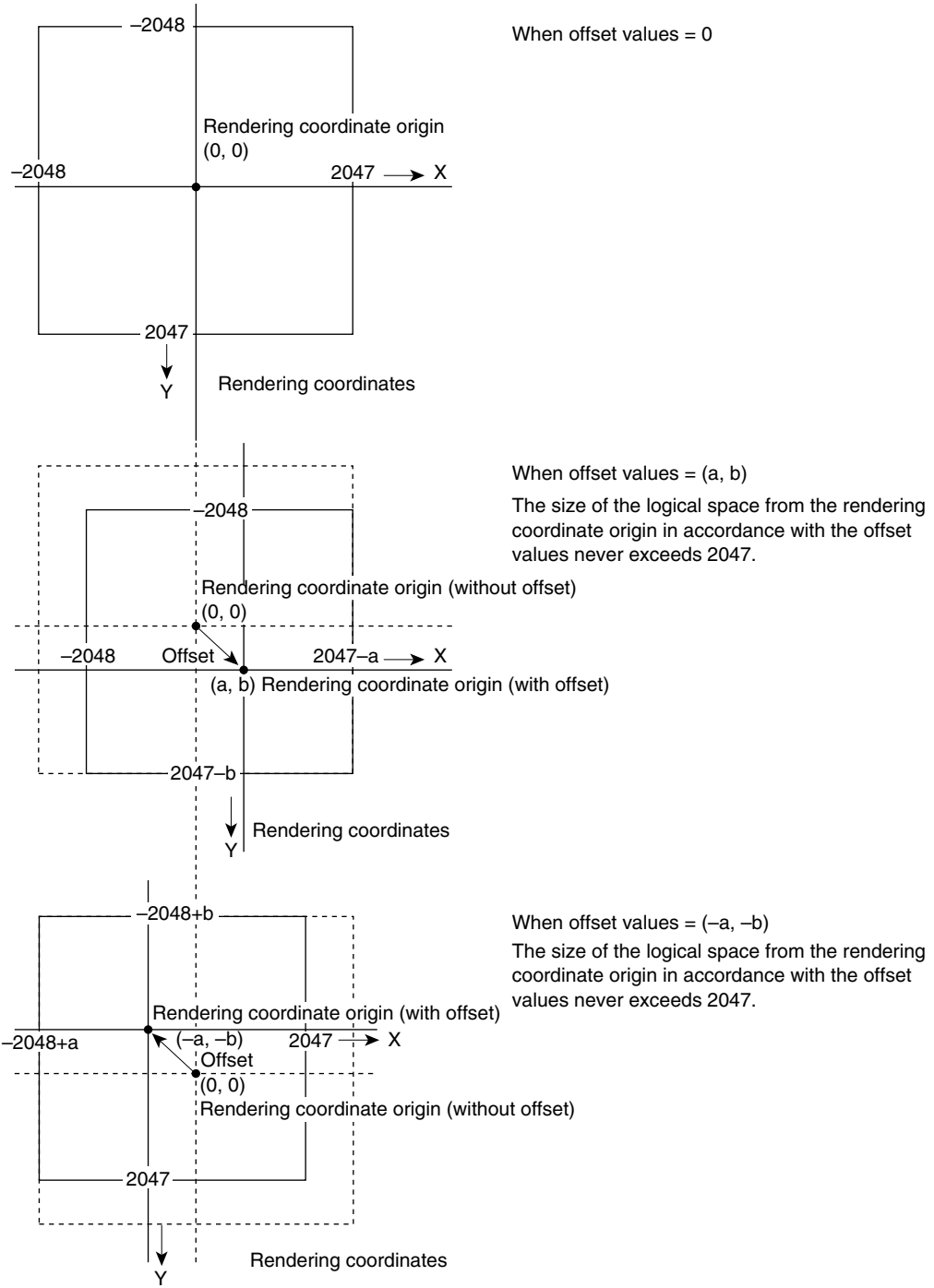


Figure 3.16 Rendering Coordinates

(4) Multi-Valued Source Coordinates

This is the coordinate system used for drawing control and handles multi-valued source data (graphics bit map data and natural images) specified by drawing commands. Data width of 8 bits or 16 bits for a set of the multi-valued source data coordinates (8 bits/pixel or 16 bits/pixel) can be selected by the graphic bit mode bits in the rendering mode register (bits GBM 2 to GBM 0 in REMR). Data width of the multi-valued source coordinates is determined by the bit configuration specified by this register setting.

The Q2SD can use two kinds of multi-valued source coordinates according to the value of linear attribute LNi.

When LNi = 0, the coordinate origin is specified by the multi-valued source area start address. Figure 3.17 shows the multi-valued source coordinates when LNi = 0. As shown in this figure, the maximum coordinate system size is represented by 1024×1024 positive coordinates, but the size depends on the installed memory capacity, screen size, and multi-valued source area start address. Depending on the multi-valued source start address, this coordinate system may entirely or partially overlap another coordinate system. When data is transferred from the CPU, address conversion shown in figure 3.9 is needed. If the function of 2-dimensional image data conversion is used (see section 3.2.8, 2-Dimensional Image Data Exchange Function), the address conversion shown in figure 3.9 is performed by the Q2SD.

When LNi = 1, it is possible to use multi-valued source arranged in linear fashion in the UGM. The physical address of the origin and the range of the coordinates are specified by the parameters in a drawing command. Each multi-valued source data indicates one physical address (origin: upper-left of the multi-valued source data coordinates) and specify the area (length and width) by the source address parameters (TDX and TDY) in the POLYGON4A command. This area can overlap another coordinate system such as a display list. Figure 3.18 shows the multi-valued source coordinates when LNi = 1.

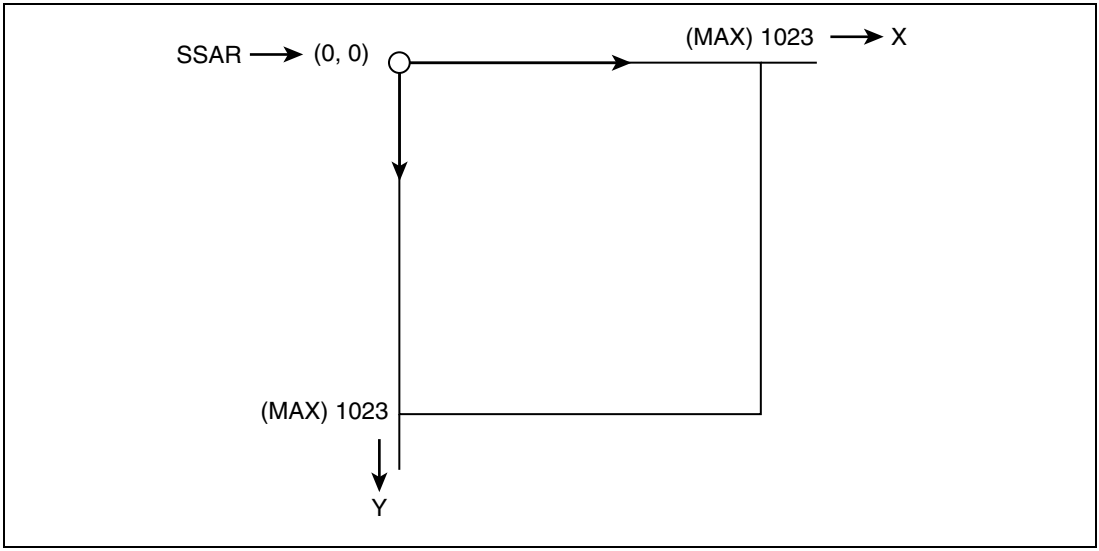


Figure 3.17 Multi-Valued Source Coordinates (LNi = 0)

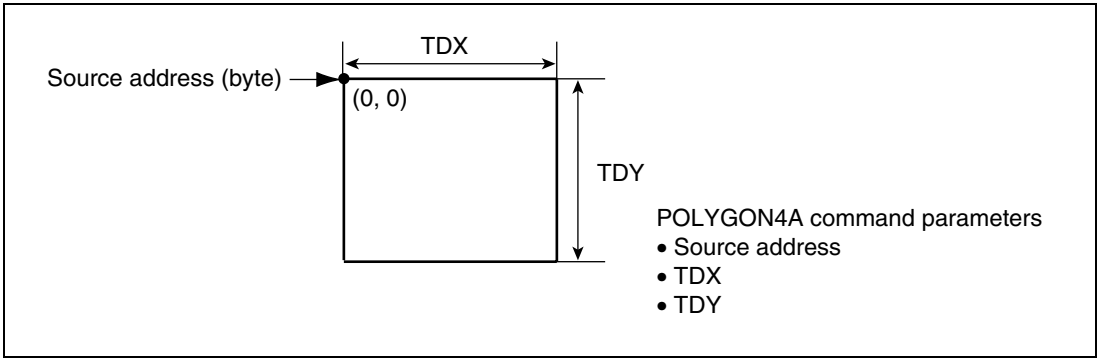


Figure 3.18 Multi-Valued Source Coordinates with LNi = 1 Specified (Linear Address)

(5) Binary Source Coordinates

This is the coordinate system used for drawing control and handles binary source data (character and line patterns) specified by drawing commands. Data width of a single bit for a set of the binary source data coordinates (1 bit/pixel) is used.

The physical address of the origin and the range are specified by the parameters in a drawing command. Each binary source data indicates one physical address (origin: upper-left of the binary source data coordinates) and specify the area (length and width) by the source address parameters (TDX and TDY) in the POLYGON4B command. This area can overlap another coordinate system such as a display list. However, the start address of the source pattern must be a byte address.

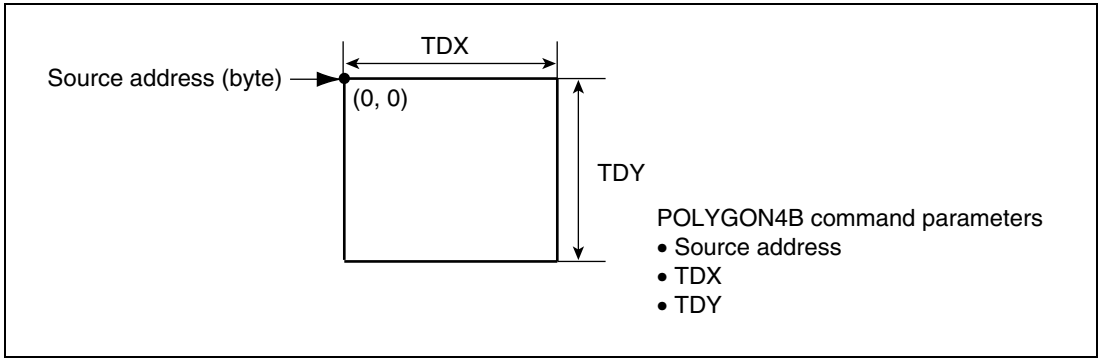


Figure 3.19 Binary Source Coordinates

(6) Work Coordinate System

This coordinate system is for drawing control and corresponds on a one-to-one basis to the rendering coordinate system, as shown in figure 3.20. When the work specification in the rendering attributes is set, a pattern is controlled using this coordinates. Drawing commands for work data use this coordinates for drawing. Data width of a single bit for a set of the work coordinates is used. The physical address of the origin, clipping, and offset are controlled the same way as the rendering coordinates. The physical address of the origin is specified by the work area start address register (WSAR)

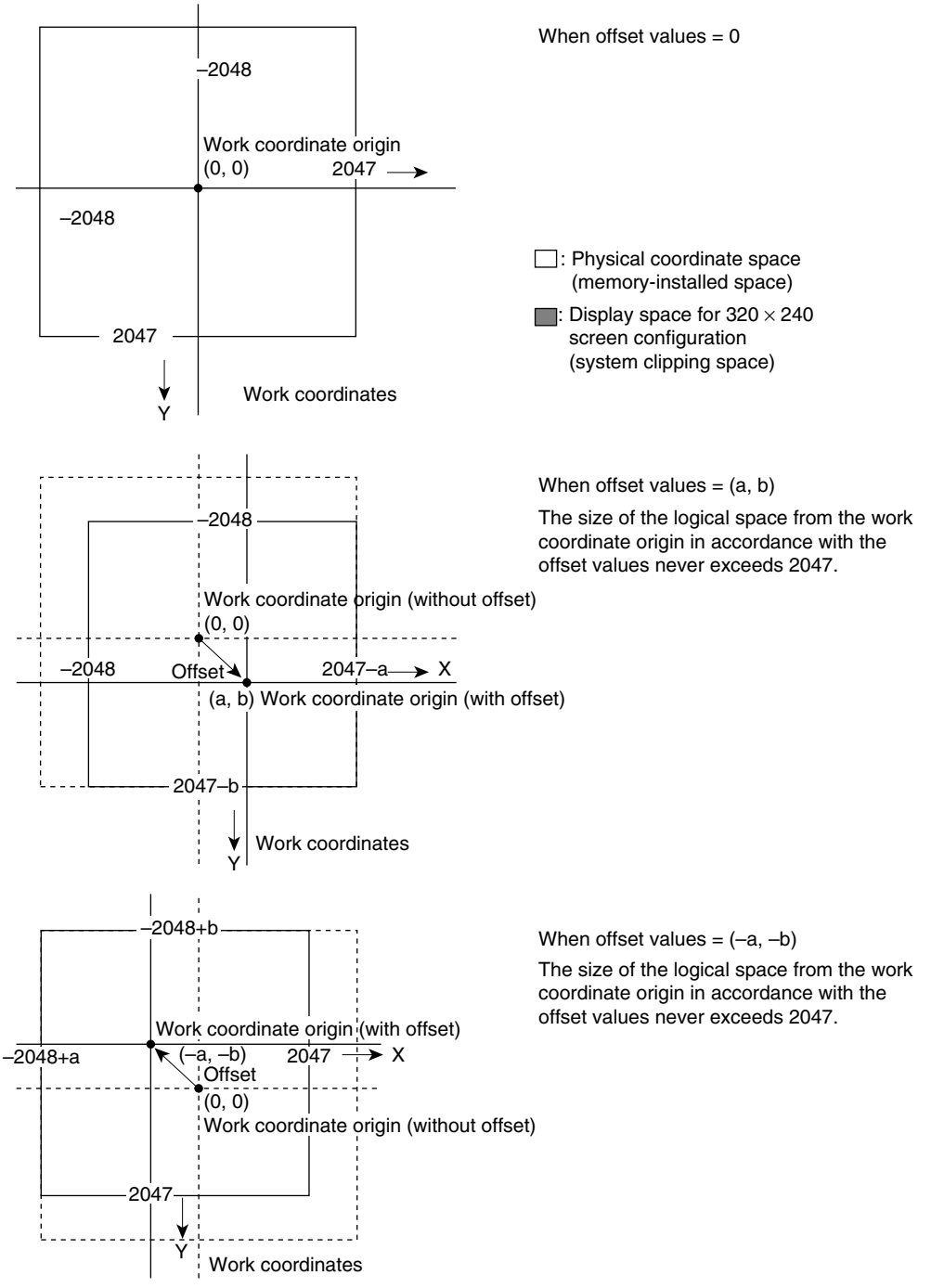


Figure 3.20 Work Coordinates

(7) Foreground Screen Coordinate System

This coordinate system is for display control and the foreground screen (FG(FB0 and FB1)) is handled by this coordinate system. The physical address of the origin is specified by the display start address register (DSAR0 and DSAR1). The display buffer uses the double buffer configuration by which the origin of this coordinates specified by DSAR0 or by DSAR1 as a display start address can be switched. Data width of 8 bits or 16 bits for a set of this coordinates (8 bits/pixel or 16 bits/pixel) can be selected and a maximum value of the X coordinate of 511 or 1023 can also be selected. These settings are specified by the graphic bit mode and memory width bits in the rendering mode register (bits GBM 2 to GBM 0 and the MWX bit in REMR).

(8) Background Screen Coordinate System

This coordinate system is for display control and the background screen (BG) is handled by this coordinate system. The physical address of the origin is fixed at H′0. Display starts from the coordinate specified by the background start coordinate registers (BGSR). Data width of 8 bits or 16 bits for a set of this coordinates (8 bits/pixel or 16 bits/pixel) can be selected and a maximum value of the X coordinate of 511 or 1023 can also be selected. These settings are specified by the graphic bit mode and memory width bits in the rendering mode register (bits GBM 2 to GBM 0 and the MWX bit in REMR).

(9) Video Screen Coordinate System

This coordinate system is for display control and the video screen is handled by this coordinate system. The physical address of the origin is specified by the video area start address registers (VSR0 to VSR2). The buffer for video capture and display uses the triple buffer configuration by which the origin of this coordinates specified by VSR0, VSR1, or VSR2 as a display (video capture) start address can be switched. Data width of YCbCr and RGB format are 8 bits or 16 bits for a set of this coordinates (8 bits/pixel or 16 bits/pixel), respectively. This is specified by the RGB bit in the video incorporation mode register (VIMR). The area of this coordinates is specified by the video window size registers (VSIZER).

(10) Cursor Coordinate System

This coordinate system is for display control and the cursor is handled by this coordinate system. The physical address of the origin is specified by the cursor area start address registers (CSAR1 and CSAR2). Display for cursor 1 starts from the origin specified by CSAR1 and display for cursor 2 starts from the origin specified by CSAR2. Data width for a set of this coordinates is 8 bits (8 bits/pixel). Both the X and Y coordinates range from 0 to 31.

3.3.4 Double-Buffering Control

The Q2SD uses double-buffering control to alternately switch the display and drawing areas located in the UGM. An area switching operation is called a display change. There are three types of mode for double-buffering control: auto display change mode, auto rendering mode, and manual display change mode. These are specified by the double-buffering mode bits (DBM) in the system control register. The start of drawing is specified by the RS bit.

When double-buffering control is performed, frame changes are performed in frame units when the Q2SD is operating in non-interlace or interlace mode, and in field units when operating in interlace sync & video mode.

When the Q2SD is operated in interlace mode, the frame flag (FRM) in the status register is used for $\overline{\text{VSYNC}}$ synchronization pulse detection by the CPU. When the Q2SD is operated in non-interlace mode, synchronization pulses are detected using the vertical blanking flag (VBK). When the Q2SD is operating in interlace sync & video mode, since the first field corresponds to the even field and the second field to the odd field, synchronization pulses are detected using VBK or FRM.

The same results can also be achieved by using the VBKEM command.

- Double-buffer switching timing:

  — Non-interlace mode

    Scanning system in which one frame is composed of one field. Double-buffer switching is performed in units of a frame.

  — Interlace mode

    Scanning system in which one frame is composed of two fields. Double-buffer switching is performed in units of a frame.

  — Interlace sync & video mode

    Scanning system in which one frame is composed of two fields. Double-buffer switching is performed in units of a field.

Examples are given below for Q2SD non-interlace operation, with a description of the operation in each mode.

(1) Auto Display Change Mode

In auto display change mode, display changes have priority. Display is changed on completion of the frame. When drawing is completed within a frame periods, this mode can be used.

If drawing is in progress when the frame is changed, drawing is aborted midway through that display list. It is therefore essential for drawing to be finished before the arrival of a $\overline{\text{VSYNC}}$ synchronization pulse.

An outline of operation in this mode is shown in figure 3.21. Drawing cannot be started with the VBKEM command in this mode, so the VBK or FRM flag must be used. Drawing is started by the rendering start bit (RS).

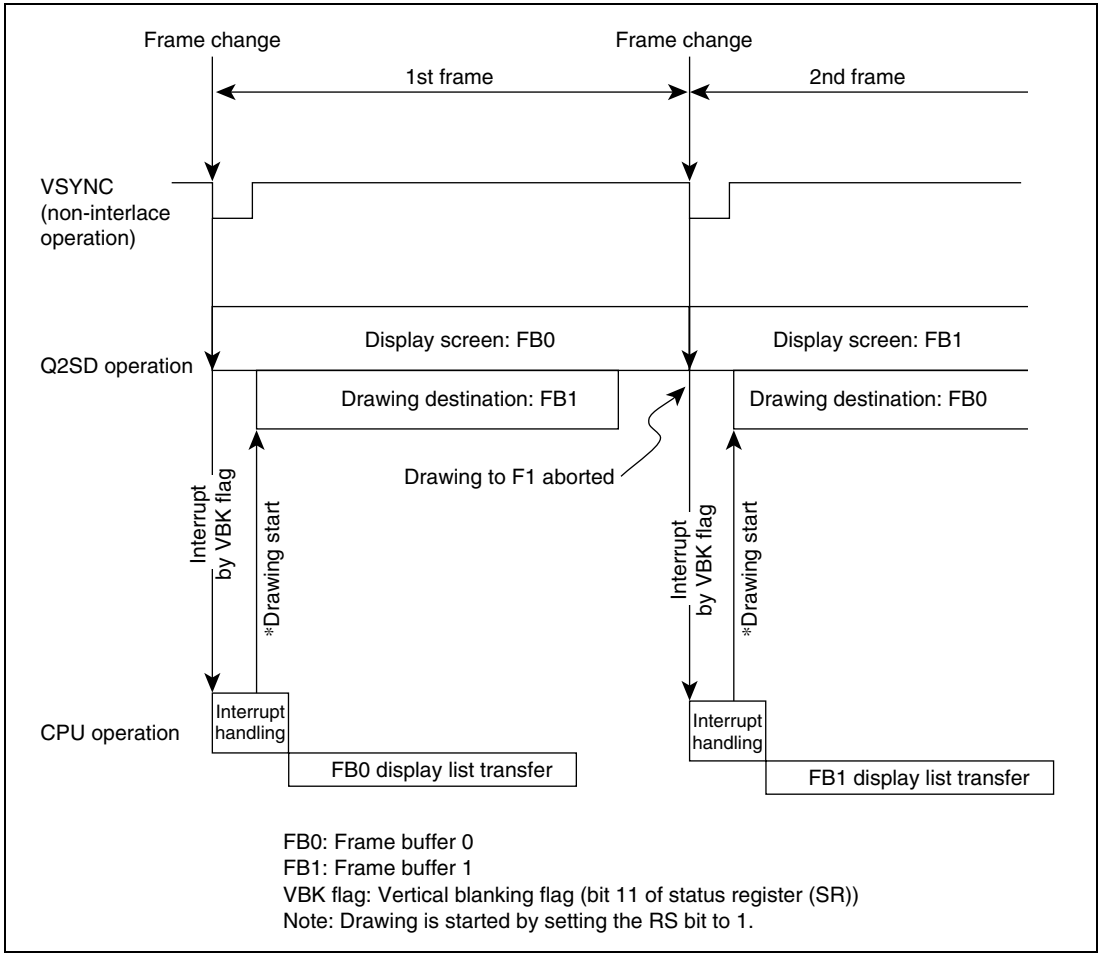


Figure 3.21 Operation in Auto Display Change Mode

(2) Auto Rendering Mode

In auto rendering mode, display switching is not performed until execution of a TRAP command is completed. If drawing does not end within one frame, it is continued without interruption and display is changed in the frame on completion of drawing. An outline of operation in this mode is shown in figure 3.22. Drawing is started by the rendering start bit (RS).

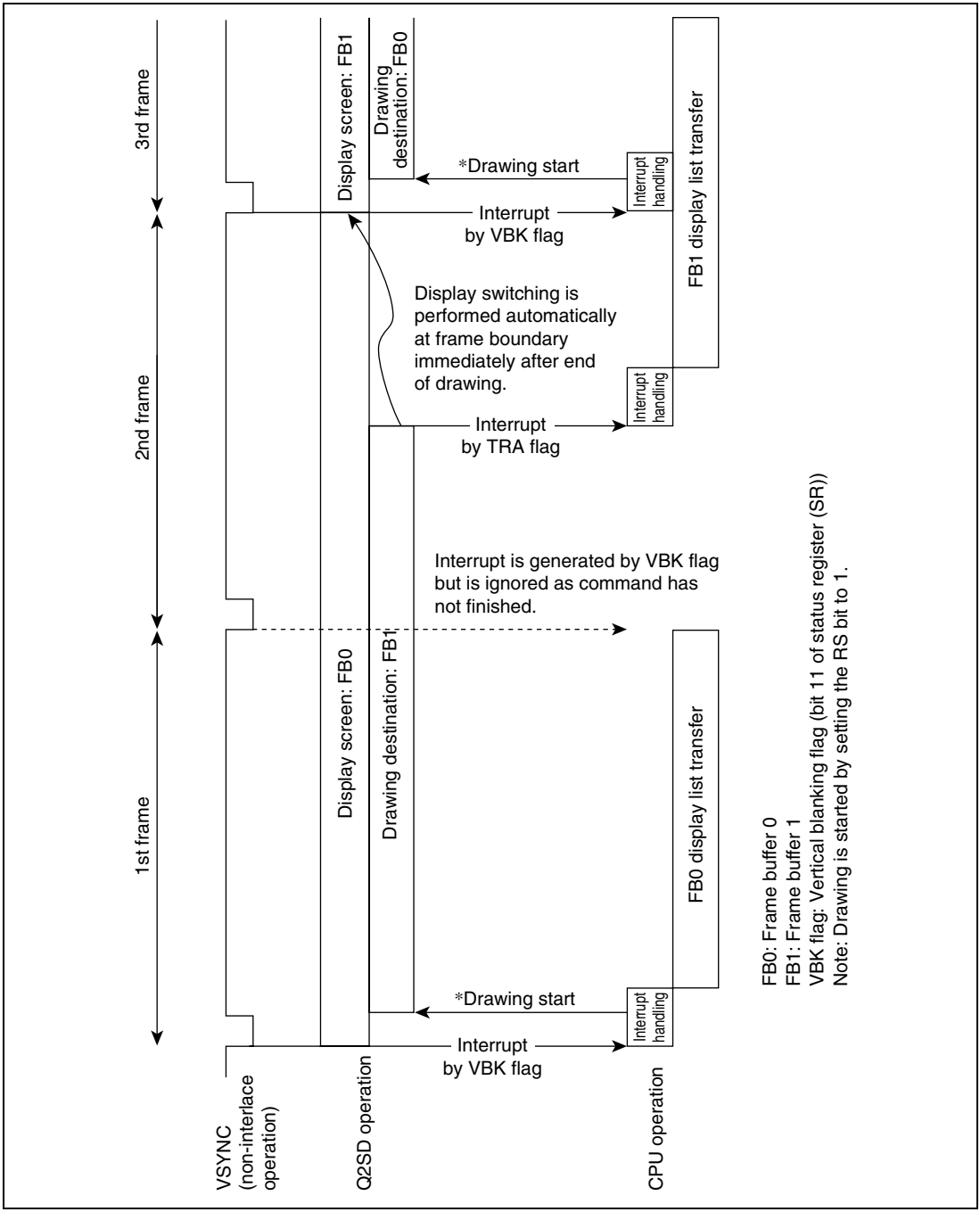


Figure 3.22 Operation in Auto Rendering Mode

(3) Manual Display Change Mode

In manual display change mode, display changes and the start of drawing are controlled independently by software. Frame changes can be performed by software by switching between FB0 and FB1 according to the setting of the DC bit in SYSR, or by using the WPR command to set the FB0 or FB1 start address in the display start address register indicated by DBF in the status register. The start of drawing is controlled by the RS bit in the system control register. Interrupts by means of the VBKEM command or the TRA flag are used for the control timing. An outline of operation in this mode when using the DC bit is shown in figure 3.23. When changing from this mode to another double-buffering control mode, first check that the DC bit has been set to 1 and has then returned to 0. If this is not done, a display change will occur at a timing of VSYNC during display processing. Confirm that the DC bit is cleared to 0 before setting it to 1.

(4) Control by Means of VBKEM and WPR Commands

The VBKEM command holds fetching and execution of the display list waiting following this command. With the VBKEM command , the waiting state is cleared at the next VSYNC in non-interlace mode display or interlace sync & video mode display, and at the start of the next frame in interlace sync mode display. Use of this command allows drawing processing to be started without using a VBK or FRM interrupt. Control is carried out by a combination of the WPR command, which performs drawing-related register setting, and the VBKEM command, which ends in synchronization with VBK, as shown in figure 3.24. The CPU only has to monitor drawing end interrupts; monitoring of VBK interrupts is no longer necessary.

This kind of double-buffering control can be used only in auto-rendering mode and manual display change mode.

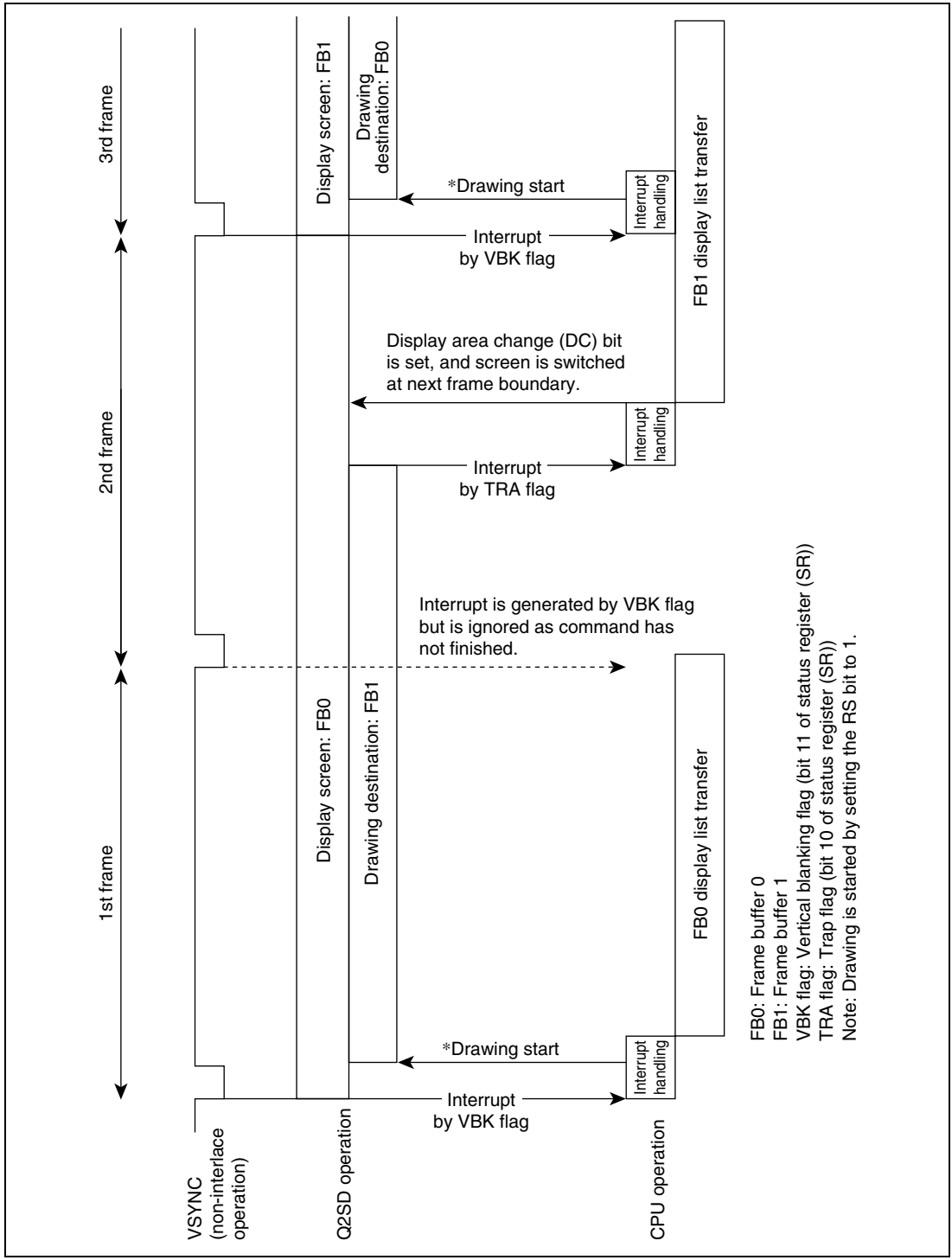


Figure 3.23 Operation in Manual Display Change Mode

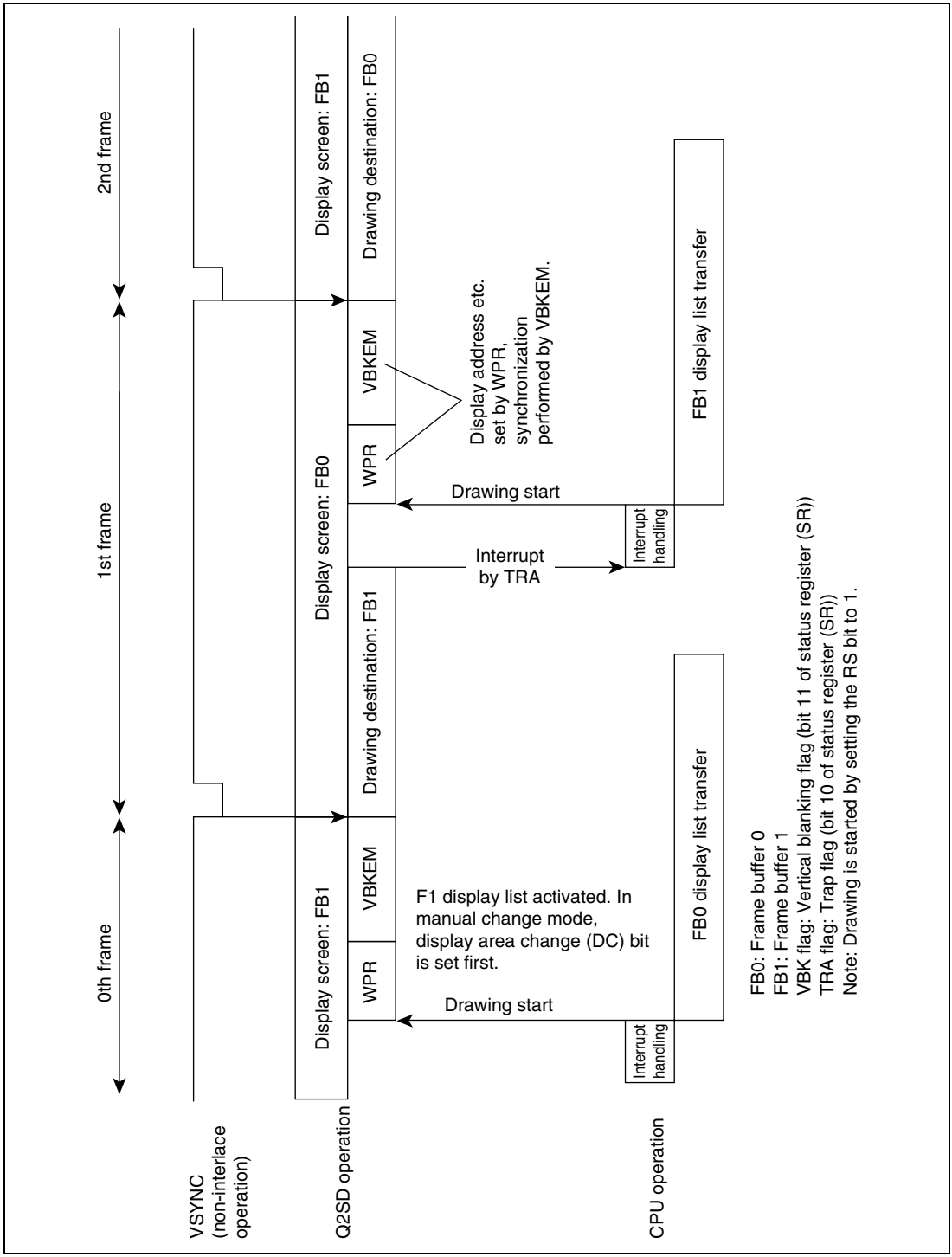


Figure 3.24 Operation when Using VBKEM Command

3.3.5 Refresh Control

The number of refresh cycles for the UGM connected to the Q2SD is set in bits REF3 to REF0 (refresh cycle count) in the display mode register (DSMR). The setting made in bits REF3 to REF0 is the number of refreshes per line (raster).

For example, if the refreshing specification of the memory used is 4096 cycles/64 ms and one field is 1/60 sec, the necessary number of refresh cycles in one field is 1067 cycles. Since the value set in DSMR is the number of refresh cycles per lines (rasters), it is the quotient when 1067 is divided by the number of lines (rasters) in one field. The number of refresh cycles should therefore be set so that the following expression is satisfied:

$$1067 \leq \text{number of lines (rasters)} \times \text{number of refresh cycles set in DSMR}$$

The Q2SD supports CAS-before-RAS refresh mode. The number of refreshes set in bits REF3 to REF0 are executed from the fall of the DISP signal.

Table 3.4 shows sample settings.

Table 3.3 Setting for Number of Refreshes

Bit 3: REF3	Bit 2: REF2	Bit 1: REF1	Bit 0: REF0	Operation
0	0	0	0	Refresh timing is not output.
*	*	*	*	Refresh timing is set to any value from 1 to 15 cycles, and output.

Table 3.4 Sample Estimations of Number of Refresh Cycles

Display Screen Size	Frame Rate	Number of Lines	Number of Refreshes Required Per Line	REF Set Value
320 × 240	1/60 s	525/2 lines	(1/60) (2/525) (4096/0.064) = 4.06	5
480 × 240	1/60 s	525/2 lines	(1/60) (2/525) (4096/0.064) = 4.06	5
640 × 480	1/60 s	525 lines	(1/60) (1/525) (4096/0.064) = 2.03	3

3.4 Display

3.4.1 Display Functions

The Q2SD has functions for outputting image data, drawn in the UGM, in synchronization with externally or internally generated display timing.

In the Q2SD, horizontal and vertical display timing for the display screen is set in the display control registers (see section 5.4, Display Control Registers).

The display control register settings depend on the scanning and synchronization systems used. Table 3.5 shows the display control register settings.

Figure 3.25 shows the display timing in non-interlace mode. The display screen is defined by the variables shown in table 3.6. Set each of VDC, VDE, VSP, and VC to the number of rasters within one $\overline{\text{VSYNC}}$ cycle for, regardless of the scan mode in the display mode register. Set DSY to the number of rasters within one $\overline{\text{VSYNC}}$ cycle (one field) in non-interlace or interlace mode, or set DSY to two $\overline{\text{VSYNC}}$ cycles (one frame) in interlace sync & video mode.

For the display operating clock (display dot clock) frequency, use the value obtained by dividing the number of pixels to be displayed in the xw period by the duration of the xw period. Input the dot clock to the CLK1 pin.

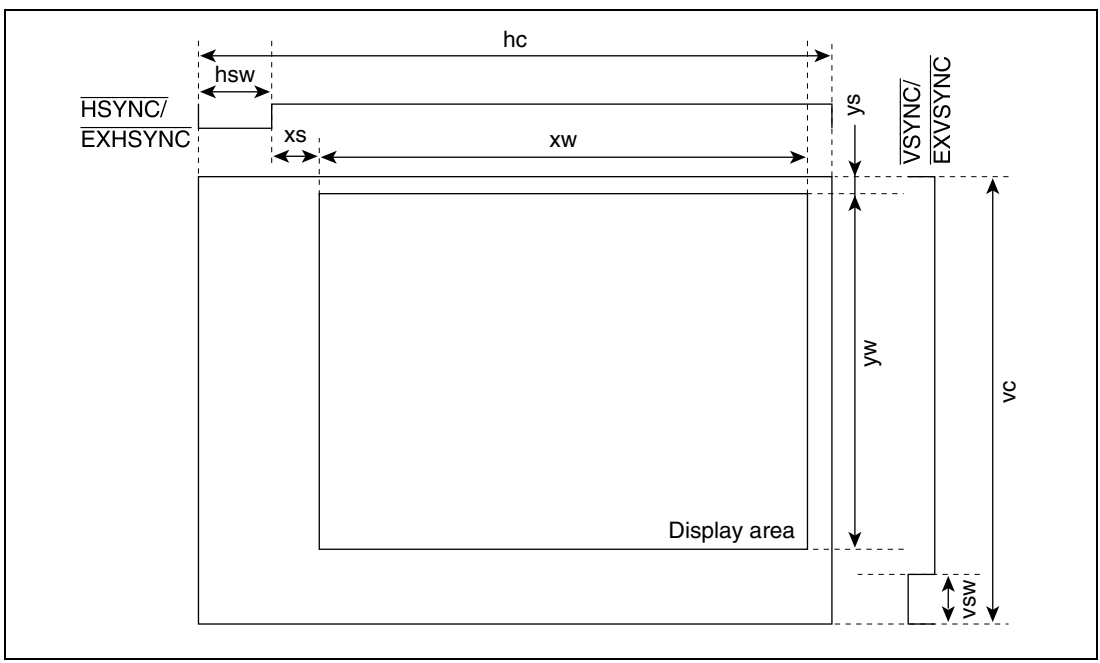


Figure 3.25 Display Timing

Table 3.5 Variables Defined by Display Screen

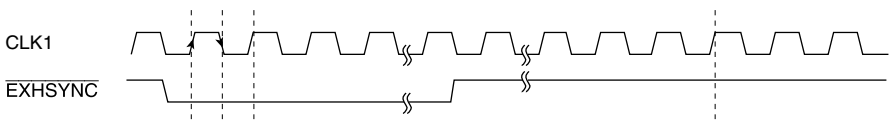
Variable	Description	Unit
hc	Horizontal scan cycle	Dot clock
hsw	Horizontal sync pulse width	Dot clock
xs	Interval between $\overline{\text{HSYNC}}$ rise and display screen horizontal display start position	Dot clock
xw	Display screen display width per raster	Dot clock
vc	Vertical scan cycle	Raster lines
vsw	Vertical sync pulse width	Raster lines
ys	Interval between $\overline{\text{VSYNC}}$ rise and display screen vertical display start position	Raster lines
yw	Display screen vertical display interval	Raster lines

Table 3.6 Register Settings

Register Address (A10–A0)	Register Name		Bit Name	Operating Mode: Master Mode	Operating Mode: TV Sync Mode
010	Display size register X (DSRX)		DSX*[5]	xw	xw
012	Display size register Y (DSRY)		DSY	yw (2yw)*[6]	yw (2yw)*[6]
026	Display window	Horizontal display start position register (DSWR)	HDS*[2]*[3]	hsw + xs – 11	hsw + xs – 14
028		Horizontal display end position register (DSWR)	HDE*[2]	hsw + xs – 11 + xw	hsw + xs – 14 + xw
02A		Vertical display start position register (DSWR)	VDS*[1]*[4]	ys – 2	ys – 2
02C		Vertical display end position register (DSWR)	VDE*[1]	ys – 2 + yw	ys – 2 + yw
02E	Horizontal sync pulse width register (HSWR)		HSW	hsw – 1	hsw – 1
030	Horizontal scan cycle register (HCR)		HC	hc – 1	hc
032	Vertical sync position register (VSPR)		VSP*[1]	vc – vsw – 1	vc – vsw – 1
034	Vertical scan cycle register (VCR)		VC*[1]	vc – 1	vc + 2

Notes: 1. In all scanning mode the settings of the VDS, VDE, VSP, and VC bits are made for a one-field unit.

2. Timing for the HDS and HDE are stipulated from the fourth rising edge of CLK1 after the low level of $\overline{\text{EXHSYNC}}$ is detected at the rising edge of CLK1.



3. The setting for the lower limit of the HDS bits is as follows: when MCLK = 2 × CLK1, HDS ≥ 64 × (CLK1/MCLK); when MCLK > 2 × CLK1, HDS ≥ (64 + 80) × (CLK1/MCLK). The unit for MCLK and CLK1 is MHz. When MCLK = 2 × CLK1, use a clock with which MCLK and CLK1 are synchronized. With a multiplication factor of N, MCLK is N × CLK0.
4. In interlace and interlace sync & video mode, the setting is: VDS ≥ 1.
5. Use a value of 4 or more for DSX.

   If the cursor 1 horizontal display start position (HCS1) and cursor 2 horizontal display start position (HCS2) in the cursor registers are DSX, DSX – 1, DSX – 2, DSX – 3, DSX – 4, DSX – 5, then set DSX = XW + 6.
6. In interlace sync & video mode

3.4.2 Screen Display Composition

In the Q2SD, the DEN (display enable) bit in the system control register (SYSR) can be used to select whether or not display data is to be output to the screen. When display data is not output, the display off output register (DOOR) settings are displayed.

The Q2SD is capable of composing a screen from two cursor screens, a foreground screen (FG), a video screen, and a background screen (BG), and of displaying the screen thus composed. See figure 3.26.

The data on the lower screens shows through regions of black (H′0) in the cursor and FG screens, since black is the transparent color for these screens. Therefore, characters and pictures drawn on these screens using color other than black are composed with the image on the video screen.

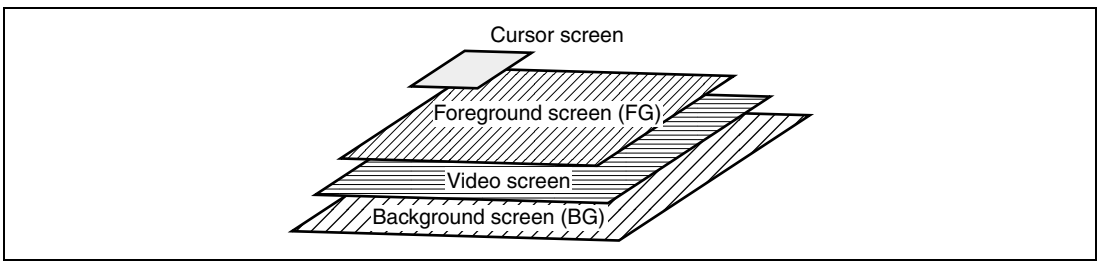


Figure 3.26 Configuration of the Display Screen for Q2SD

(1) Composed Screen Types

- Foreground screen: FG (frame buffer FB0 or FB1)
- Video screen: VW
- Background screen: BG
- Cursors (cursor1 and cursor2)

The foreground screens, video screens, and background screens that can actually be composed depend on the UGM bus width, the Q2SD operating frequency, and the display operating clock frequency. See appendix E.

(2) Priority Order of Composed Screens

Screens are displayed in the priority order shown below. With the cursors, display can be performed according to the priority order set in the window priority bits (PRI) in display mode register 2 (DSMR2).

Foreground screen > video screen > background screen (in front-to-rear order)

(3) Features of Each Screen

- Foreground screen (FG)

  If the data for a foreground screen pixel is H′0 (color-expanded data by the color palette when 8 bits/pixel is selected), a low-priority screen such as the video window is displayed through that pixel.

- Video screen (VW)

  In the video screen, the data in the UGM which is specified by the contents of the video area start address registers (VSAH and VSAL) is displayed on a rectangular area specified by the contents of the video window size registers (VSIZE). The video screen is not transparent to a low-display-priority screen such as the background screen and is displayed as a rectangular area. This window displays the video area specified by the video area start address registers (VSAH and VSAL) pointed to by the video window status bit (VID) regardless of whether the video incorporation enable bit in the video incorporation mode register (the VIE bit in VIMR) is set to 1 or cleared to 0.

- Background screen (BG)

  The display start position can be set in background coordinate display start registers X and Y (BGSX, BGSY) in pixel units from address H′0 in the UGM. The background screen is suitable for performing scroll display. Setting the wrap around bit in the display mode register (the WRAP bit in DSMR) to 1 enables to access the display area in wrapping around way. When displaying the background screen, ensure that the frame screen and background screen locations in the UGM do not overlap.

- Cursors

  Two 32 × 32-pixel cursors with a hardware blink function can be displayed. If the cursor pixel data color-expanded by the color palette is H′0, a low-priority screen is displayed through that pixel. The blink cycle is specified by the cursor blink shape A display interval length or cursor blink shape B display interval length in the cursor display start position registers (the BLINKA or BLINKB bit in CSR).

(4) Display on/off control

The bits that control whether or not each screen is displayed are shown below. With the foreground and background screens, set either or both to be displayed. When the foreground screen is set to 16-bit/pixel mode with bits GBM2 to GBM0, the Q2SD's internal display data increases and other screens cannot be displayed. Therefore, to disable display of the video window, background screen, and cursors, the bits controlling whether or not each screen is to be displayed should be cleared to 0. In this case, also, clear the VIE bit to 0 in the video incorporation mode register (VIMR) to disable video capture.

Register updating for each screen should be carried out in the register update interval shown in section 3.2.6, Register Updating. The display contents differ according to the setting of the background screen wraparound mode (WRAP) bit.

- Foreground screen: Can be set with the FBD bit in display mode register 2 (DSMR2).
- Video screen: Can be set with the VWE bit in display mode register 2 (DSMR2).
- Background screen: Can be set with the BG bit in the display mode register (DSMR).
- Cursors: Can be set with bits CE1 and CE2 in display mode register 2 (DSMR2).

Table 3.7 Background Screen Related Register Settings

Register	Field			
Name	**Bit No.**	**Name**	**Set Value**	**Notes**
DSMR	10	BG	1/0	Combination on/off
	11	WRAP	1/0	Wraparound on/off
REMR	2 to 0	GBM	000 to 111	8 or 16 bits/pixel
BGSRX	9 to 0	BGSX	BG starting point X coordinate	According to screen coordinates
BGSRY	13 to 0	BGSY	BG starting point Y coordinate	

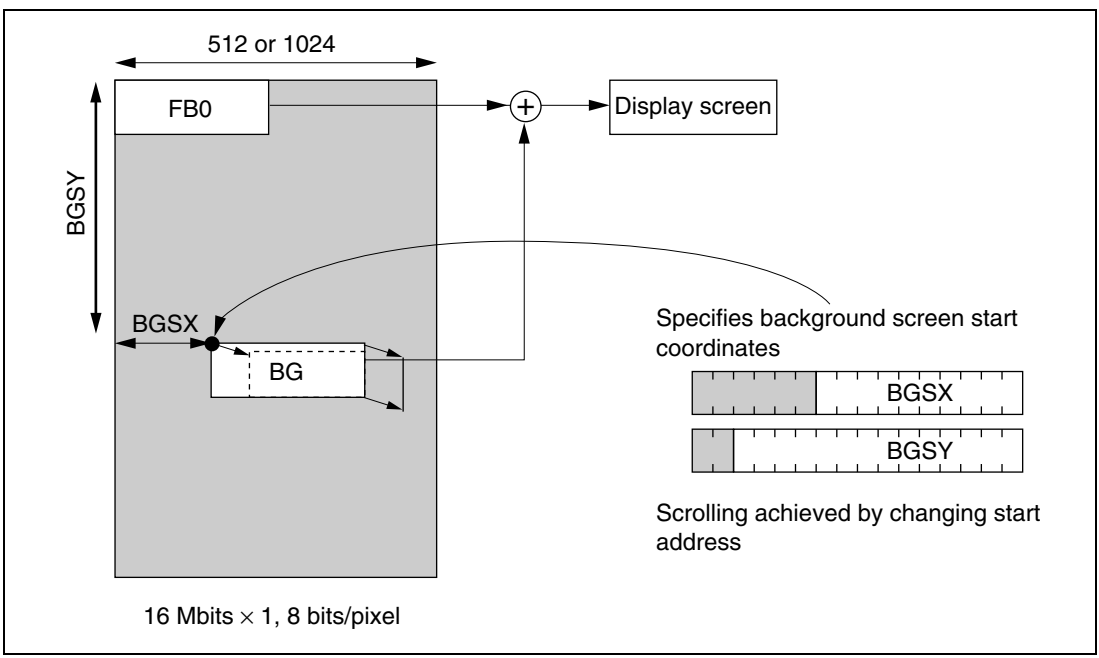


Figure 3.27 Example of Background Screen Simple Scroll (WRAP = 0)

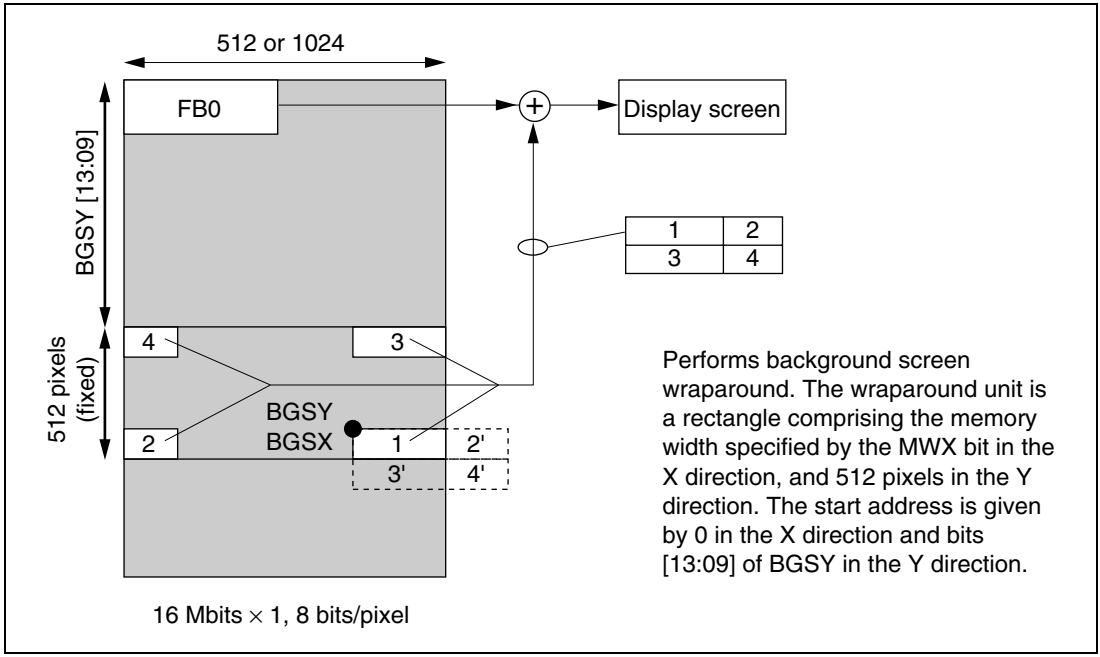


Figure 3.28 Example of Background Screen Wraparound Scroll (WRAP = 1)

3.4.3 Scanning Systems

(1) Q2SD Scanning Systems

The Q2SD allows selection of non-interlace mode, interlace mode, or interlace sync & video mode as the scanning system. The mode setting is made in the SCM (scan mode) bits in the display mode register (DSMR).

In non-interlace mode, one frame is composed of one field. In interlace mode, one frame is composed of two fields, even and odd, in which the same data is displayed. In interlace sync & video mode, also, one frame is composed of two fields, even and odd, but in this mode different data is displayed in these two fields. When the ODEV bit is cleared to 0 in display mode register 2 (DSMR2), the $\overline{\text{ODDF}}$ pin signal functions as follows.

The order of fields to be displayed in interlace and interlace sync & video mode is specified by the ODEV bit in the display mode 2 register (DSMR2). When the ODEV bit is cleared to 0, an odd field and an even field for the same frame are displayed in that order. When the ODEV bit is set to 1, an even field and an odd field for the same frame are displayed in that order.

In master mode, the Q2SD outputs a high-level signal from the $\overline{\text{ODDF}}$ pin during even field display, and a low-level signal during odd field display. In TV sync mode, a high-level signal is input at the $\overline{\text{ODDF}}$ pin to display the even field, and a low-level signal to display the odd field.

When the ODEV bit is set to 1 in DSMR2, the polarity of the $\overline{\text{ODDF}}$ pin is the opposite of that described above. Figure 3.29 shows examples of raster scan control display.

- Vertical scan synchronization example

  Non-interlace mode: 1/60 second/field, 1/30 second/field

  Interlace mode: 1/30 second/frame

  Interlace sync & video mode: 1/30 second/frame

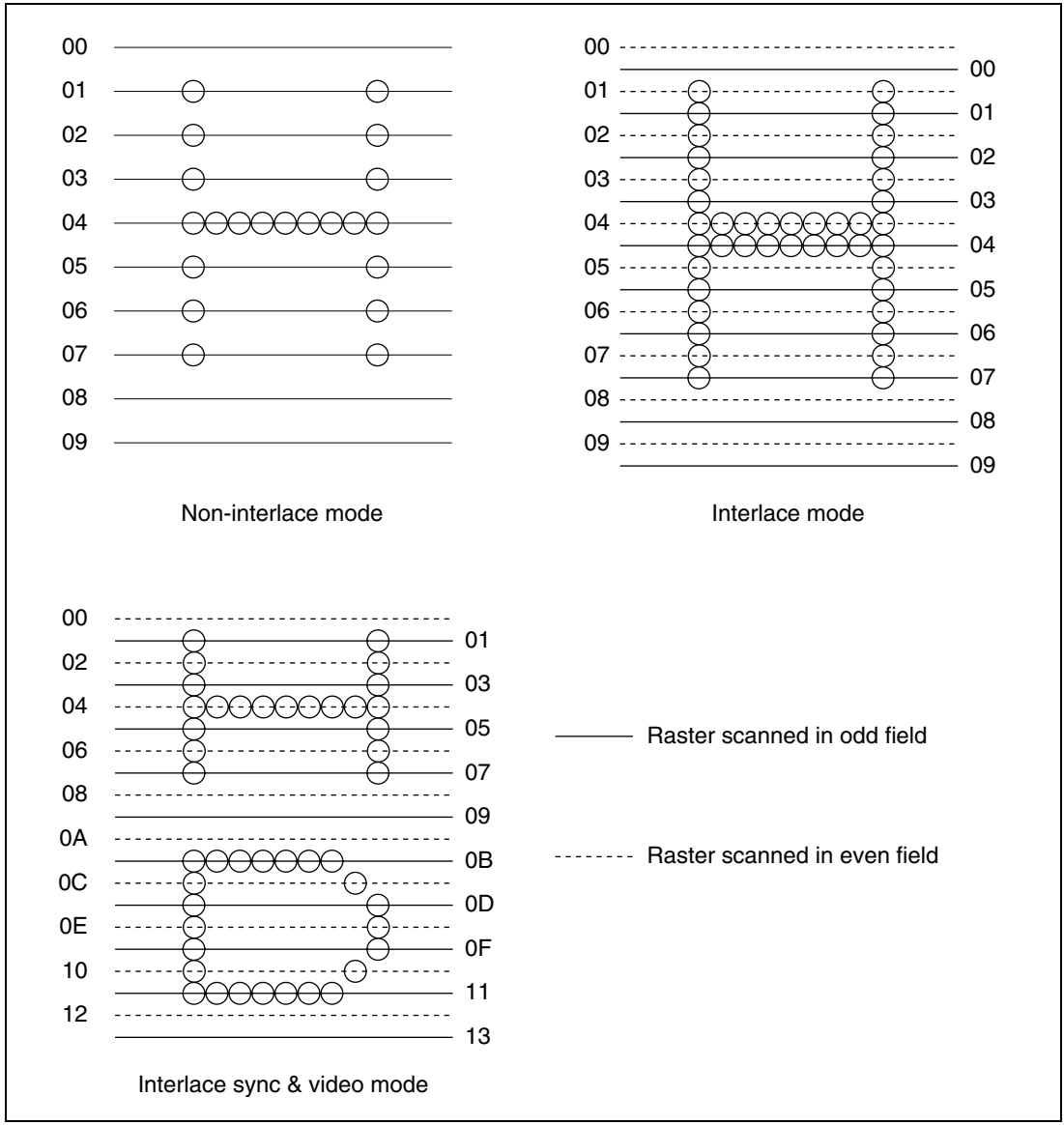


Figure 3.29 Examples of Raster Scan Control Display

(2) Relationship with Monitor Display Method

The methods for display monitor devices are largely divided into two types.

- Interlace sync method

  In this method, the input image data for an odd and an even lines is switched at every scanning cycle VC. One image (a single frame) is thus composed for 2 VC (the first 1-VC data is persistence of vision). This method is common for TVs and VCRs.

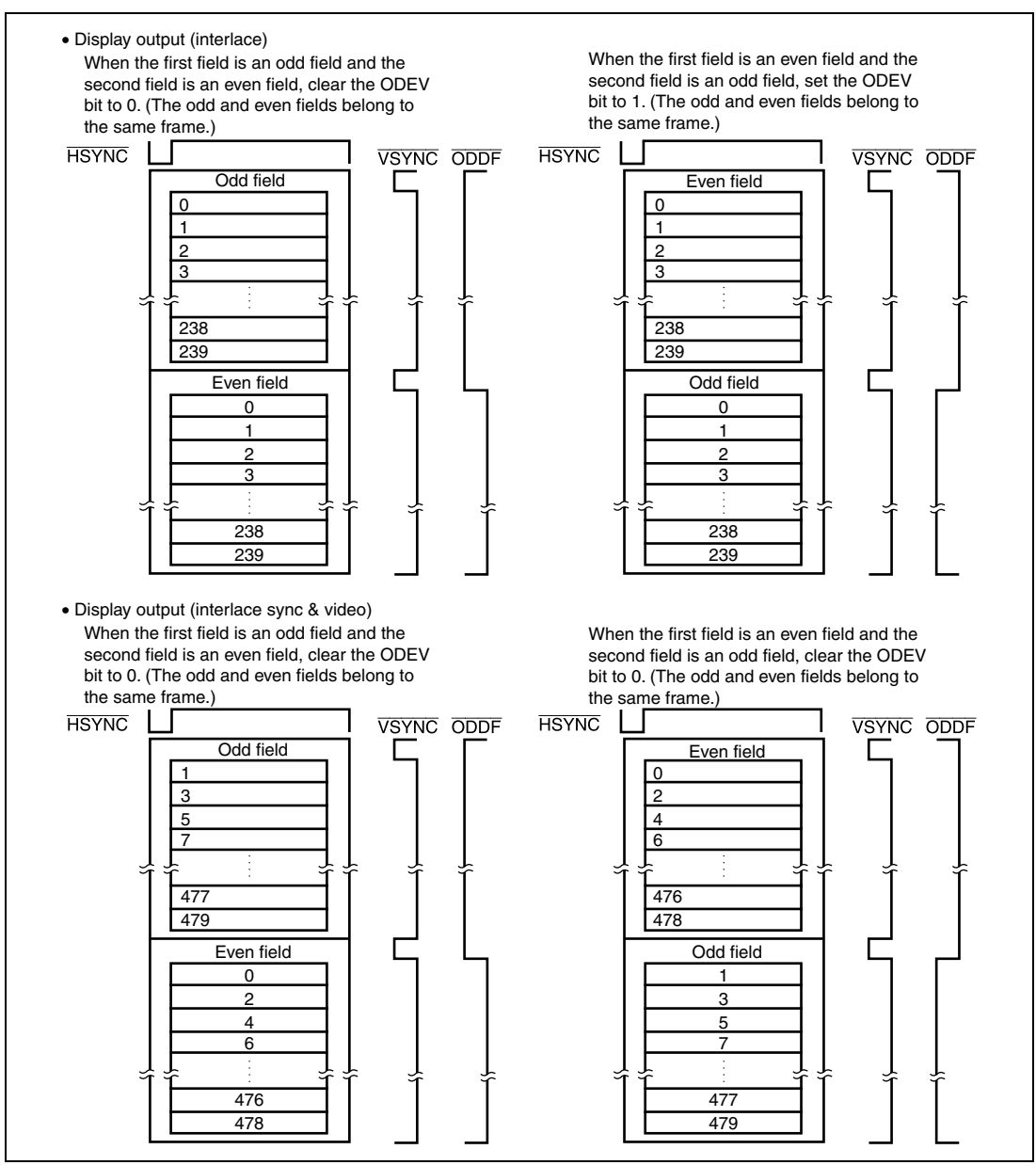


Figure 3.30 Display by Interlace Sync Method

- Non-interlace method

  In this method, the input image data is displayed at a time without any intervals. Some high-resolution monitors use this method.

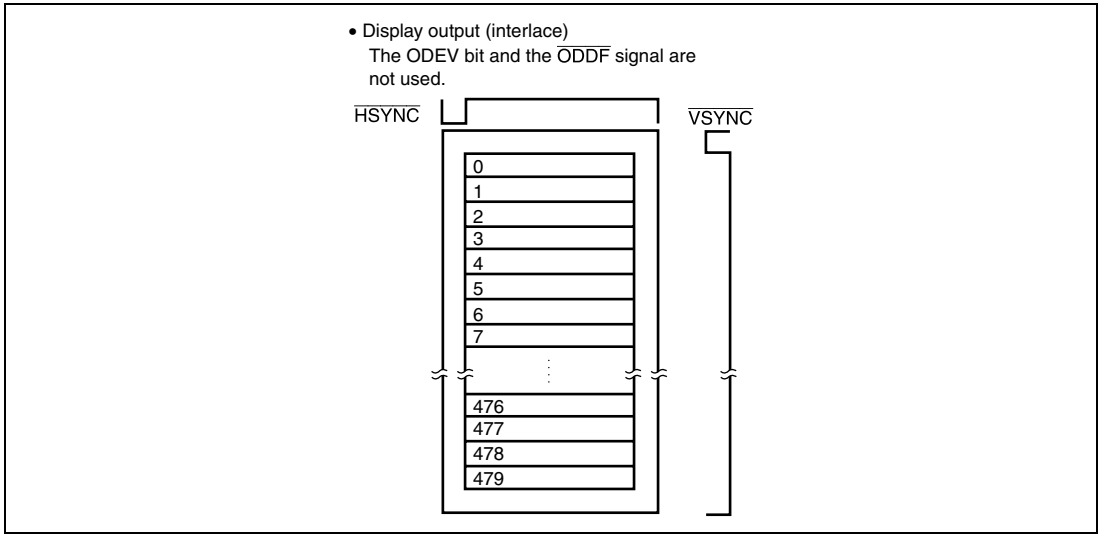


Figure 3.31 Display by Non-Interlace Method

Some display devices receive data in the interlace sync method and display the data in the non-interlace method (progressive conversion function). In this case, the first-half data stored in memory in the display device and the second half data are displayed at one time. Since the display is changed one time for 2 VC, clearness is increased, however, resolution is the same.

Since a multi-scan monitor has a function for selecting the vertical scanning frequency of 55 to 160 Hz and the horizontal scanning frequency of 31 to 96 Hz, improvement of resolution can be achieved.

Select an appropriate method of the Q2SD output to match the input method of the monitor used. Table 3.8 shows the possible combinations.

Table 3.8 Combinations of Q2SD Output and Monitor Input Methods

Monitor Input Method	Q2SD Non-Interlace Mode	Q2SD Interlace Sync Mode	Q2SD Interlace Sync & Video Mode
Interlace sync	Blurring	Blurring	Available
Non-interlace	Available	Available	Display size halved. Blurring

(1) Non-Interlace Mode Display

The non-interlace mode is selected by setting the scan-mode bits in the display mode register (bits SCM1 and SCM0 in DSMR) to B′00. In a non-interlace display, the display on the screen is updated at 59.94 frames/sec. This mode allows the display of high-quality images, since the speed of switching is high. The non-interlace mode is used to output images for non-interlace monitors.

The data read from the UGM as data for display includes the FG, BG, VW, cursor 1, and cursor 2, according to the settings in DSMR and DSMR2. The value of VID for the VW screen is checked on each field.

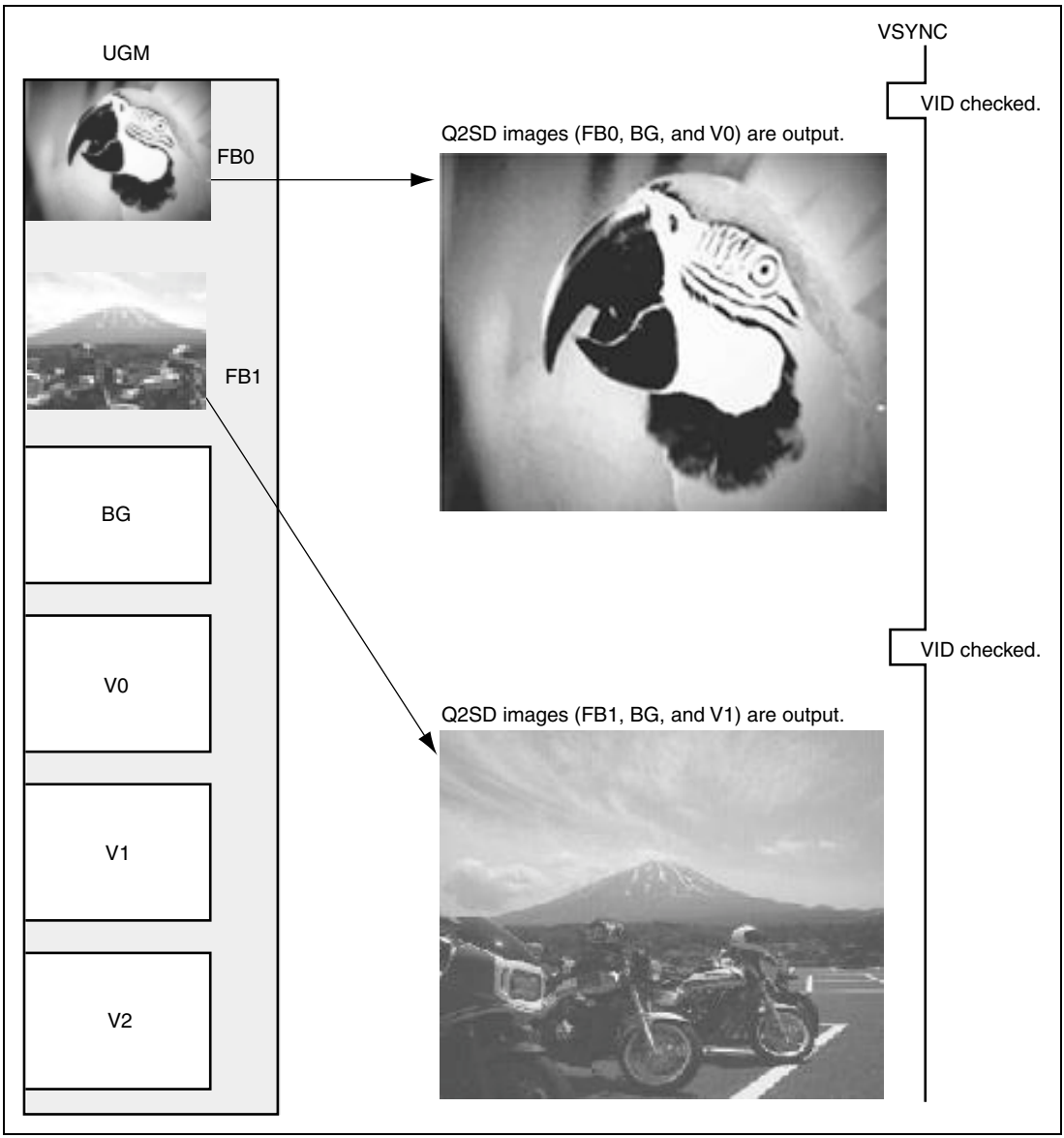


Figure 3.32 Non-Interlace Mode Display Output

(4) Interlace Mode

Interlace mode is entered by setting the scan-mode bits in the display mode register (bits SCM1 and SCM0 in DSMR) to B′10. In interlace display driven by the Q2SD, the data output in each pair of an even and odd field is for the same frame.

The display is at 29.97 frames/sec. and the screen switching speed is reduced.

Since interlace mode is used to output to the interlaced display, the data read from the UGM includes the data for display as FG, BG, VW, cursor 1, and cursor 2, according to the settings in DSMR and DSMR2. VID of the VW screen is checked for each frame.

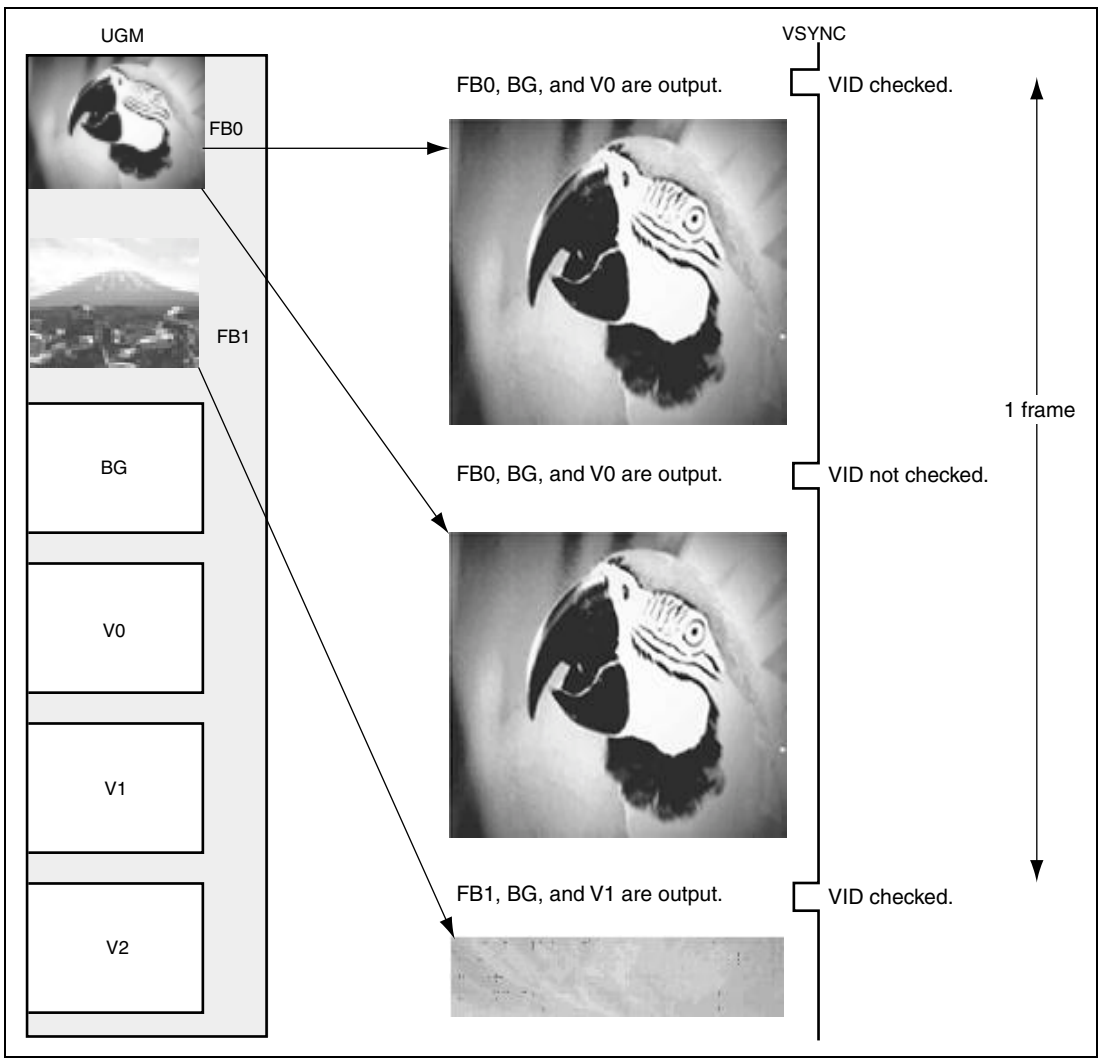


Figure 3.33 Interlace Mode Display Output

(5) Interlace Sync & Video Mode

Interlace sync & video mode is entered by setting the scan-mode bits in the display mode register (bits SCM1 and SCM0 in DSMR) to B′11. This mode is for output to an interlaced display.

In the case for a television tuner, the data of a single frame is divided into an even and odd field while the Q2SD in interlace sync & video mode changes frames for every field. To achieve the correct composition of the window, select FB0 and FB1 which belong to one frame. Since the VID is updated every field, completely different fields may be composed. It is not a problem for still images, however, moving images are not displayed correctly.

The display data in the Y direction only takes up half of the size set in DSY. VID on the VW screen is checked for each field.

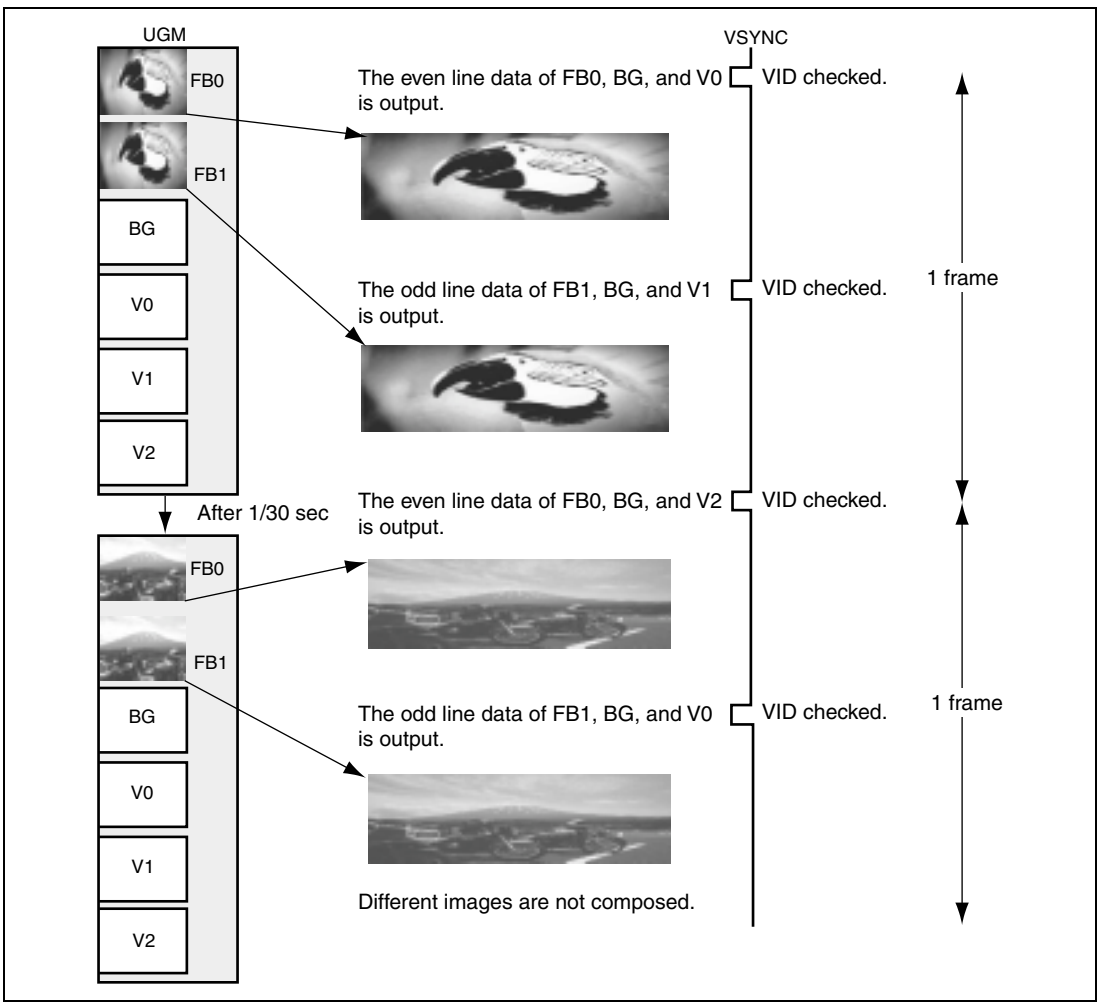


Figure 3.34 (1) Interlace Sync & Video Mode Output

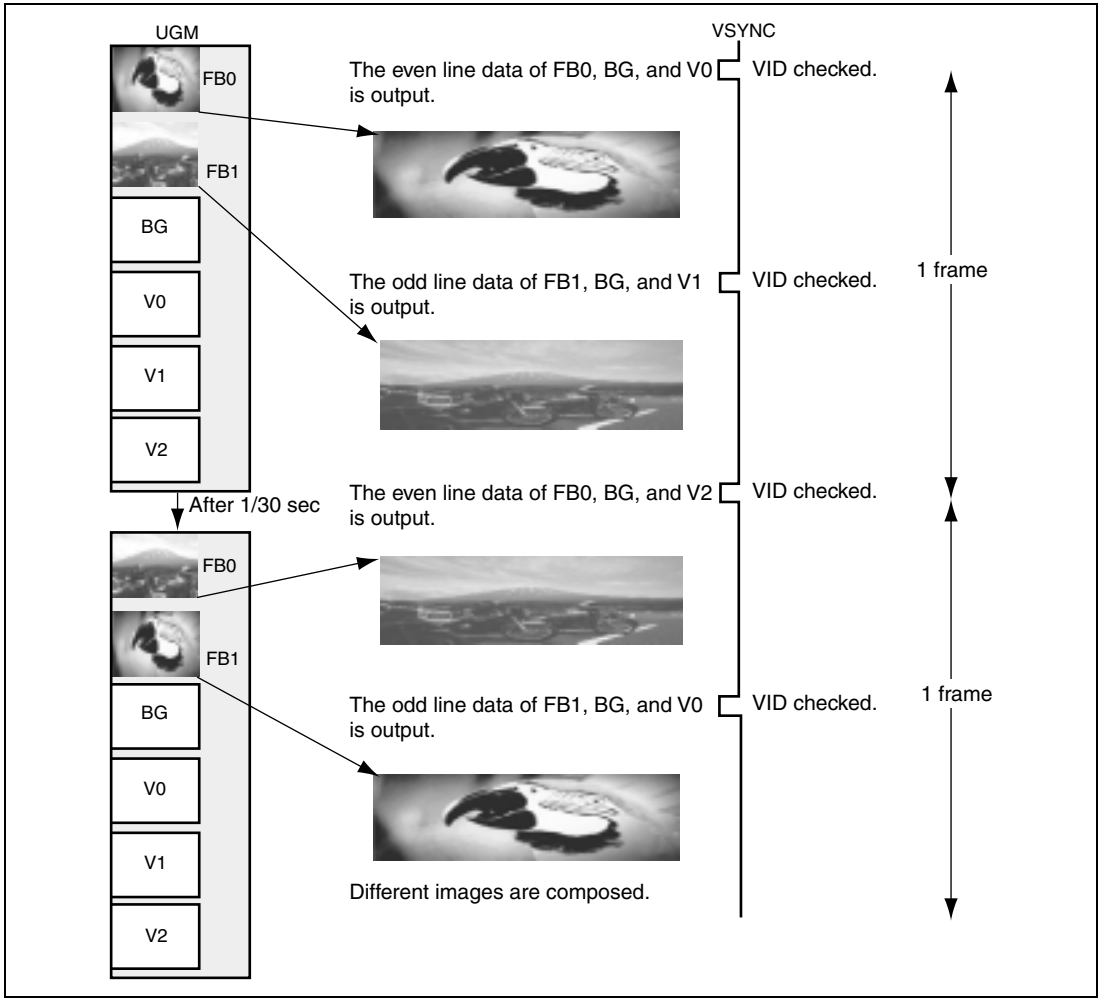


Figure 3.34 (2) Interlace Sync & Video Mode Output

3.4.4 Synchronization Systems

The Q2SD is provided with a TV sync function in addition to master mode to simplify synchronization with an external device. The TVM (TV sync mode) bits in the display register (DSMR) are used to select master mode or TV sync mode.

The frame and vertical blanking flags in the status register (the FRM and VBK flags in SR) are changed at detection of the vertical sync signal start position which is specified by the VSP bits in the vertical start position register (VSPR) regardless of sync mode.

(1) Internal Synchronization Mode (Master Mode)

Setting the horizontal and vertical sync signal ($\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$) cycles and pulse widths in the display control register outputs the corresponding waveforms, and display data is output in synchronization with these signals.

In interlace mode and interlace sync & video mode, a signal indicating odd field or even field is output at the $\overline{\text{ODDF}}$ pin.

The UGM refreshing is performed on the basis of the $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signals.

(2) External Synchronization Mode (TV Sync Mode)

In TV sync mode, the Q2SD is synchronized and operated using the horizontal and vertical sync signals of a TV, VCR, or other external system

In this mode, the TV, video, or other system is treated as the master, and the Q2SD as the slave.

Synchronization is performed every horizontal scan with the $\overline{\text{EXHSYNC}}$ input signal, and every vertical scan with the $\overline{\text{EXVSYNC}}$ input signal.

The Q2SD outputs display data on the basis of the falling edge of the $\overline{\text{EXHSYNC}}$ signal and the rising edge of the $\overline{\text{EXVSYNC}}$ signal.

In this mode, the horizontal sync signal, vertical sync signal, and clock from the sync signal generator should be input at the $\overline{\text{EXHSYNC}}$, $\overline{\text{EXVSYNC}}$, and CLK1 pins, respectively. The $\overline{\text{CYSINC}}$ pin outputs a high-level signal. Signals without equalizing pulses should be used for $\overline{\text{EXHSYNC}}$ and $\overline{\text{EXVSYNC}}$.

In interlace mode and interlace sync & video mode, a signal indicating odd field or even field should be input at the $\overline{\text{ODDF}}$ pin.

When the Q2SD is operated in TV sync mode, display control register HSWR, HCR, VSPR, and VCR settings are essential.

In non-interlace mode, the $\overline{\text{ODDF}}$ pin should be fixed high or low to prevent an unstable input level at this pin.

The Q2SD performs UGM refreshing based on $\overline{\text{EXHSYNC}}$ and $\overline{\text{EXVSYNC}}$. Therefore, $\overline{\text{EXHSYNC}}$ and $\overline{\text{EXVSYNC}}$ must be input to enable UGM refreshing to be carried out.

The signal flow in TV sync mode is shown in figure 3.35.

In this mode, the CDE pin can be controlled by the Q2SD by comparing the colors displayed by the Q2SD with the colors set in color detection registers H and L (CDERH, CDERL), and master R/G/B output and slave R/G/B output can be switched in pixel units by external circuitry.

No matter whether display for the specified size in the Q2SD is completed or not, assertion of the $\overline{\text{EXVSYNC}}$ signal makes the Q2SD process the vertical display completion operation and start the next screen display. When the $\overline{\text{EXVSYNC}}$ signal is not asserted, the assertion of the signal is waited in the vertical blanking interval state (this is not automatically controlled). Similarly, assertion of the $\overline{\text{EXHSYNC}}$ signal makes the Q2SD process the horizontal display completion operation and start the next line display. When the $\overline{\text{EXHSYNC}}$ signal is not asserted, the assertion of the signal is waited in the horizontal blanking interval state (this is not automatically controlled).

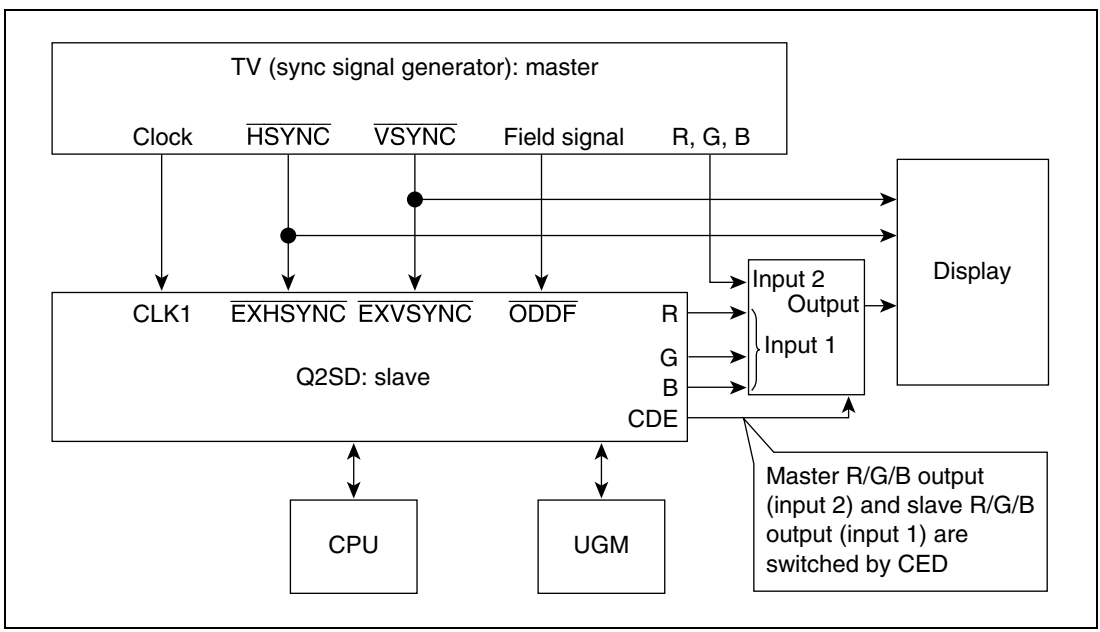


Figure 3.35 Signal Flow in TV Sync Mode

(3) TV Sync Mode Change Procedure

When B'01 is set in the TV sync mode (TVM) bits in the display mode register (DSMR) and a transition is made to synchronization system switching mode, set the display reset bit (DRES) to 1 and clear the display enable bit (DEN) to 0 in the system control register before making the transition to synchronization system switching mode.

This procedure provides for the Q2SD to perform UGM refreshing in synchronization system switching mode. This procedure must only be carried out when the Q2SD is not performing drawing.

The procedure is shown below. Steps 1 to 3 must be carried out in that order.

1. Set BG = 0, VWE = 0, CE1 = 0, and CE2 = 0.
2. Set DRES = 1 and DEN = 0.
3. Set TVM1 = 0 and TVM0 = 1.
   At this time, display reset is executed and the display buffer and the DBF flag is initialized to FB0 and 0, respectively.

The procedure for switching from synchronization system switching mode to TV sync mode is shown in 4 to 7 below.

4. Input the clock to CLK1. When TVM1 = 1 and TVM0 = 0, also input signals to the $\overline{\text{EXHSYNC}}$, $\overline{\text{EXVSYNC}}$, and $\overline{\text{ODDF}}$ pins.
5. If the display size is to be changed, set values in the Q2SD's address-mapped registers.
6. Set TVM1 = 0 and TVM0 = 0, or TVM1 = 1 and TVM0 = 0, to enable clock input from the CLK1 pin. If necessary, also set BG = 1, VWE = 1, CE1 = 1, and CE2 = 1.
7. Set DRES = 0 and DEN = 1. When an internal update is performed, the Q2SD begins display.

The relationship between the display control register settings and the display signals is shown in figure 3.36.

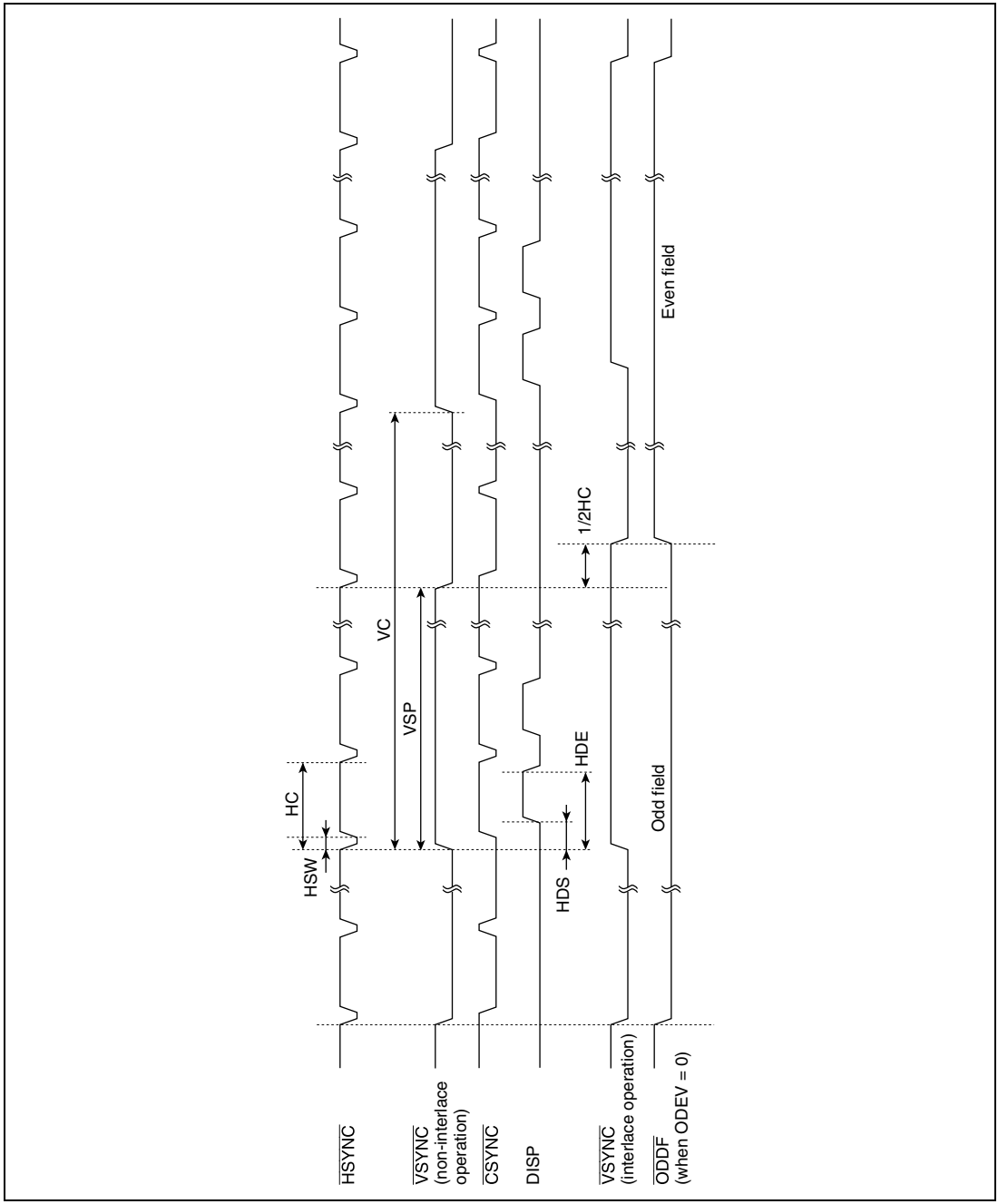


Figure 3.36 Display Timing

When performing display is master mode, the Q2SD outputs a composite sync signal. The signal waveform is based on the falling edge of $\overline{\text{VSYNC}}$. The low-level width of equalizing pulses and separation pulses can be set in the equalizing pulse width register (EQWR) and the separation pulse width register (SPWR), respectively.

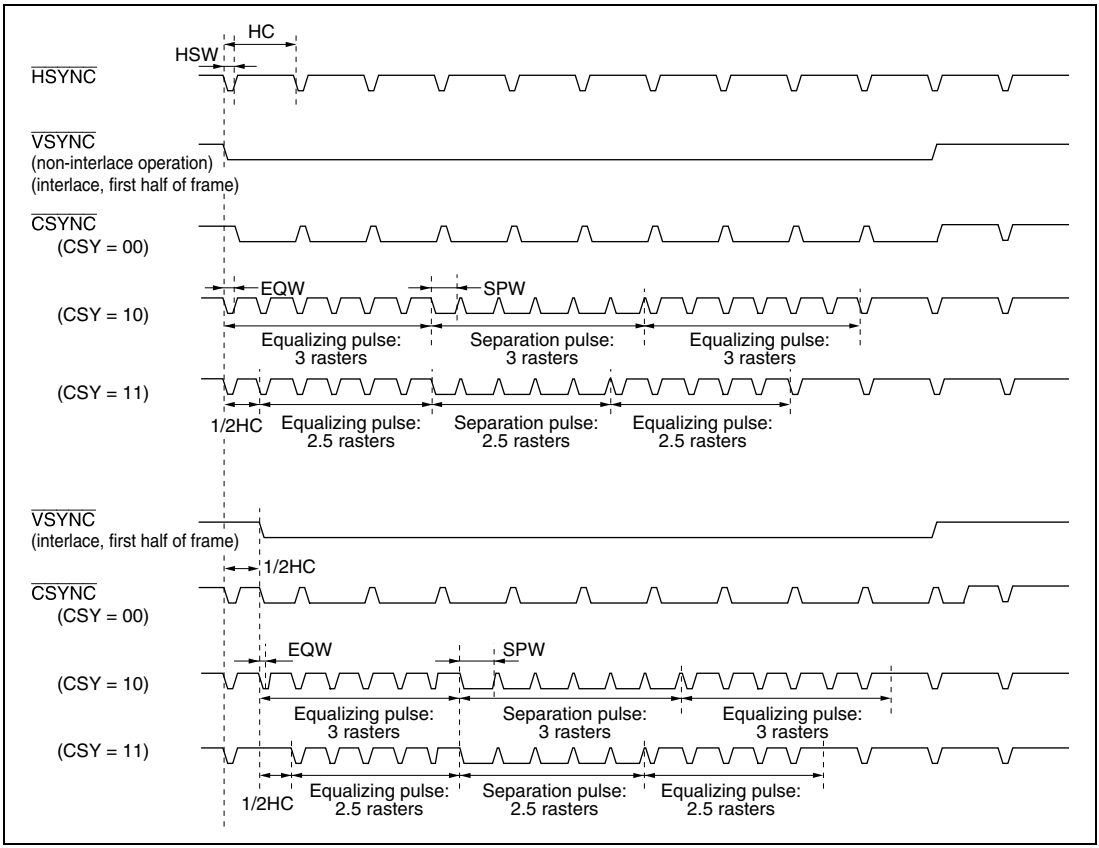


Figure 3.37 $\overline{\text{CSYNC}}$ Output Waveform

3.4.5 Color Expansion of Display Screen

(1) Color Expansion of Display Screen

The Q2SD incorporates the color palette function which can display 256 colors among 260,000 colors simultaneously. The R, G, and B have 6-bit configuration respectively, and are mapped to the Q2SD register space. The color palette function performs expansion of R, G, and B, which are six bits (260,000 colors), respectively, to the specified screen among foreground, background, or cursor screen in 8 bits/pixel. The color palette is shared among these screens.

(2) Color Expansion of Video Screen

When the video screen is in the YCbCr format, the Q2SD performs expansion of the R, G, and B, each of 6 bits, (256,000 colors).

3.5 Rendering

3.5.1 Commands

The Q2SD performs drawing on the basis of a group of drawing commands located in the UGM. This group of drawing commands is called a display list. Drawing commands comprise four-vertex screen drawing and line drawing commands which draw at rendering coordinates, and work screen drawing and work line drawing commands which draw at work coordinates. As for drawing parameter setting commands, there are register setting command and sequence control commands which control the display list such as drawing end control.

Line drawing, trapezoid fill, and current pointer setting commands include absolute coordinate and relative coordinate specification commands.

Table 3.9 lists the drawing commands.

Table 3.9 Drawing Commands

Type	Command Name	Function
Four-vertex screen drawing	POLYGON4 Quadrilateral paint	Draws quadrilateral with four coordinates as vertices. Painting can be performed with source tiling and specified color.
	POLYGON4A	Four-vertex screen drawing with multi-valued source as transfer source
	POLYGON4B	Four-vertex screen drawing with binary source as transfer source
	POLYGON4C	Four-vertex screen drawing using specified color
Line drawing	LINE Polygonal line	Draws solid polygonal line from start coordinates through nodal coordinates.
	LINE	Polygonal line drawing (absolute coordinate specification)
	RLINE	Polygonal line drawing (relative coordinate specification)
	PLINE Polygonal line with line-type specification	Draws polygonal line with line type (pattern) from start coordinates through nodal coordinates.
	PLINE	Pattern-reference polygonal line drawing (absolute coordinate specification)
	RPLINE	Pattern-reference polygonal line drawing (relative coordinate specification)

Table 3.9 Drawing Commands (cont)

Type	Command Name	Function
Work screen drawing	FTRAP Trapezoid paint	Performs binary EOR painting of trapezoid with left side parallel to Y-axis.
	FTRAP	Binary EOR trapezoid fill (absolute coordinate specification)
	RFTRAP	Binary EOR trapezoid fill (relative coordinate specification)
	CLRW Rectangle zero-clear	Performs zero-painting of rectangle with diagonal designated by two coordinate points.
Work line drawing	LINEW Polygonal line	Draws solid polygonal line from start coordinates through nodal coordinates.
	LINEW	Binary polygonal line drawing (absolute coordinate specification)
	RLINEW	Binary polygonal line drawing (relative coordinate specification)
Register setting	MOVE	Current pointer setting (absolute coordinate specification)
	RMOVE	Current pointer setting (relative coordinate specification)
	LCOFS	Local offset value setting (absolute coordinate specification)
	RLCOFS	Local offset value setting (relative coordinate specification)
	SCLIP	Sets rectangle with diagonal designated by origin and specified coordinate point as clipping area.
	UCLIP	Sets rectangle with diagonal designated by two coordinate points as clipping area.
	WPR	Sets a specific address-mapped register.
Sequence control	JUMP	Command sequence jump (branch)
	GOSUB	Subroutine call (branch). Nesting depth is one.
	RET	Subroutine return
	NOP3	No operation: no processing executed.
	VBKEM	Waits until the next vertical blanking interval.
Drawing end	TRAP	Ends drawing processing and generates CPU interrupt.

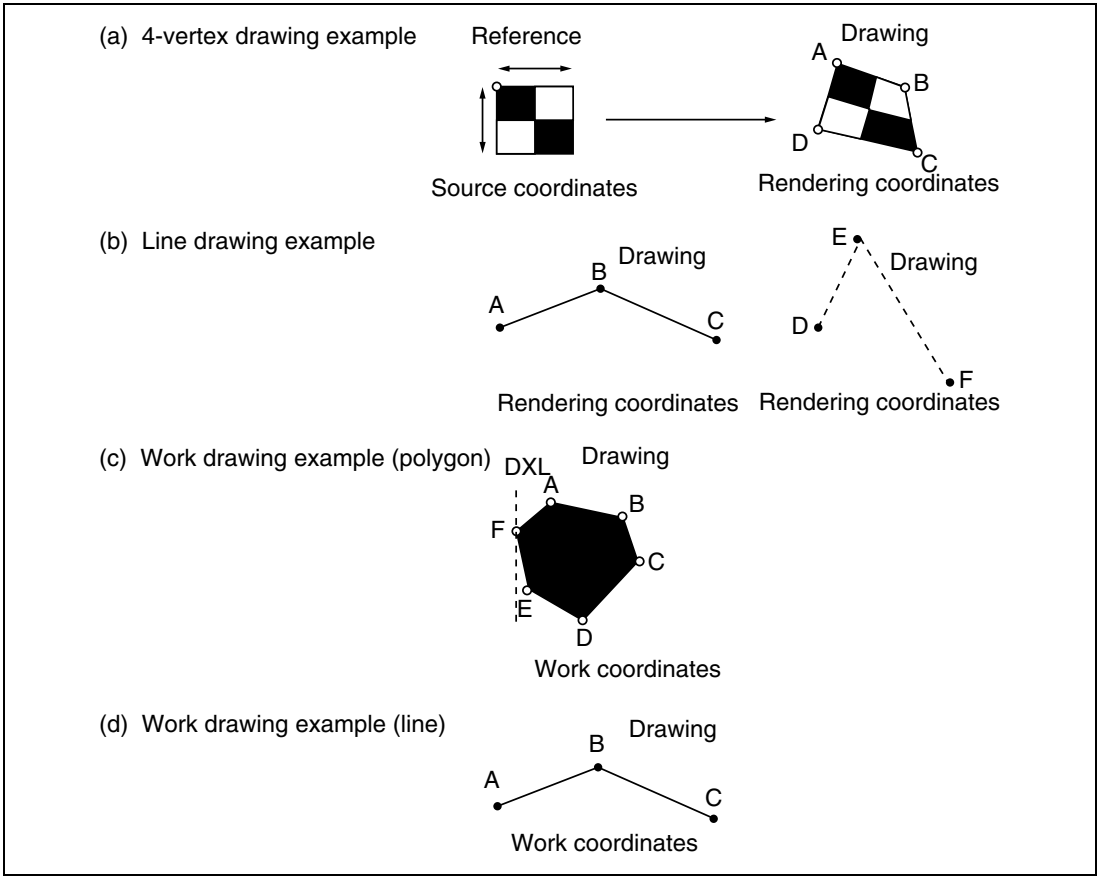


Figure 3.38 Drawing Functions

3.5.2 Image Data Reference

The Q2SD can perform color-drawing while referring to the source data, or cutting-out drawing while referring to the work data. Among the Q2SD commands, the commands that refer to the source data are POLYGON4A, POLYGON4B, PLINE, and RPLINE. The commands that refer to the color data that is included in the command parameter are POLYGON4C, LINE, RLINE, LINEW, and RLINEW. Commands that refer to the binary-value work data are POLYGON4A, POLYGON4B, and POLYGON4C. The commands that create the binary work data are FTRAP, RFTRAP, LINEW, RLINEW, and CLRW. The reference to the binary work data can be performed simultaneously with the reference to the source data or the color data.

There are two types of source data: multi-valued source data or binary source data.

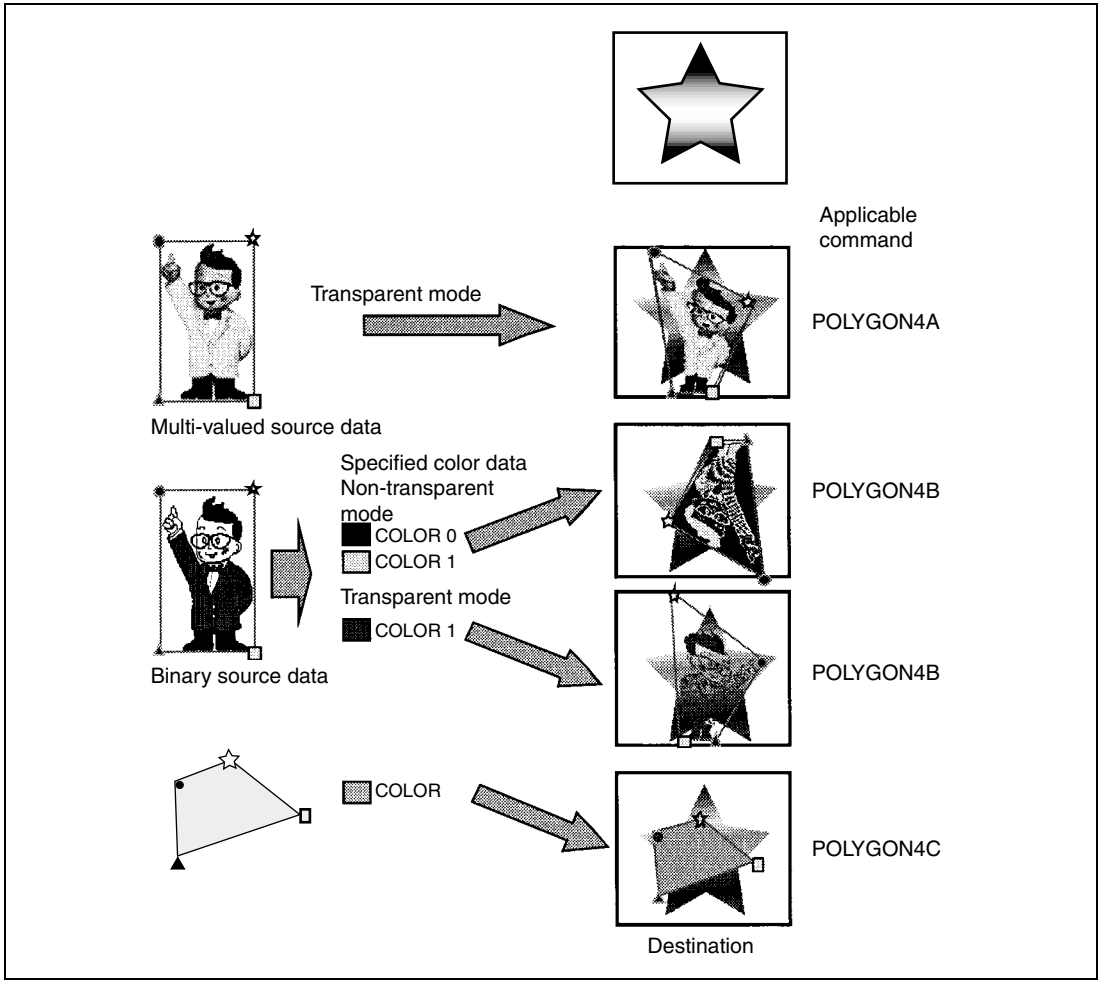


Figure 3.39 Example of POLYGON4 Transfer Data Combinations

(1) Multi-Valued Source Data

Multi-valued source data is defined as multi-valued source coordinates (2-dimensional coordinates). However, the horizontal width (TDX) is specified as a value of 8 pixels or more. The configuration of multi-valued source data is shown in figure 3.40.

In a linear arrangement (LNi = 1), a multiple of 8 pixels should be set as the TDX value.

For the multi-valued source data, either 8 bits/pixel or 16 bits/pixel can be selected. When 8 bits/pixel is used, the lower bytes are the smaller side of the source coordinate x, and the higher bytes are the larger side of the source coordinate x.

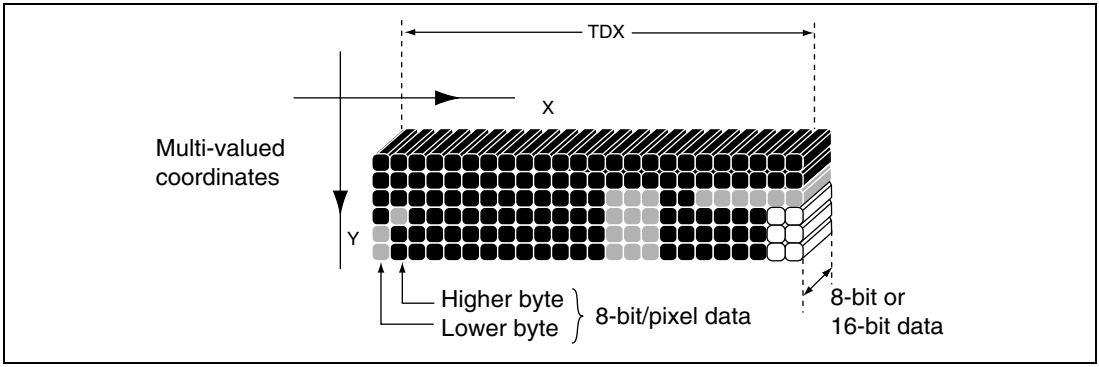


Figure 3.40 Multi-Valued Source Data Configuration

(2) Binary Source Data

Binary source data is arranged in linear fashion in the binary source area in the UGM, and is managed as 2-dimensional coordinates (binary source coordinates) by TDX and TDY in the POLYGON4B command. The left-hand screen pixel must be located at the LSB of the binary source data when the binary source data area is viewed from the Q2SD.

However, the horizontal width (TDX) is specified as a multiple of 8 pixels. An example of binary source data is shown in figure 3.41.

A binary source is used for the definition of character data and line-type data. When drawing, 0s are converted to COLOR0 data, and 1s to COLOR1 data (in transparent mode, only 1s are converted to COLOR1 data for drawing).

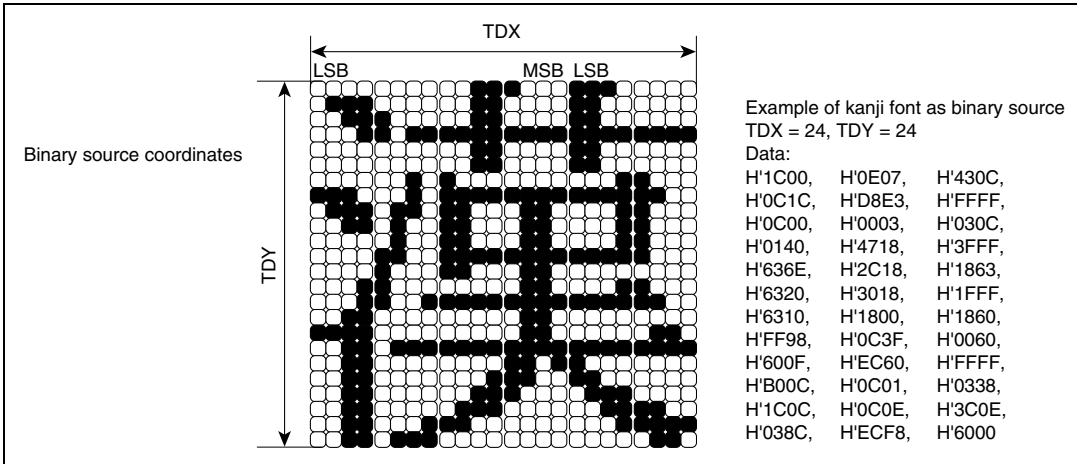


Figure 3.41 Example of Kanji Font as Binary Source (TDX = 24, TDY = 24)

(3) Specified Color Data

Specified color data is defined directly by drawing parameter color specifications (COLOR, COLOR0, COLOR1, LINE COLOR0, and LINE COLOR1). When the Q2SD is used for 8-bit/pixel operation, the same color palette number is defined in the upper 8 bits and lower 8 bits in the drawing parameter color specification. When the Q2SD is used for 16-bit/pixel operation, the R, G, and B values are defined directly by the drawing parameter color specification.

However, with LINEW and RLINEW, the value to be drawn at work coordinates is defined by the rendering attribute EOS bit.

(4) Binary Work Data

Binary work data is defined as binary work coordinates (2-dimensional coordinates). Work data is used to implement polygon painting. Polygon outline data is created with the FTRAP command, etc., and the created figure data is used to delineate the rendering figure. If, for example, the POLYGON4C command is used jointly for work, the work area polygon can be drawn in the rendering area with the specified color value. The configuration of binary work data is shown in figure 3.42.

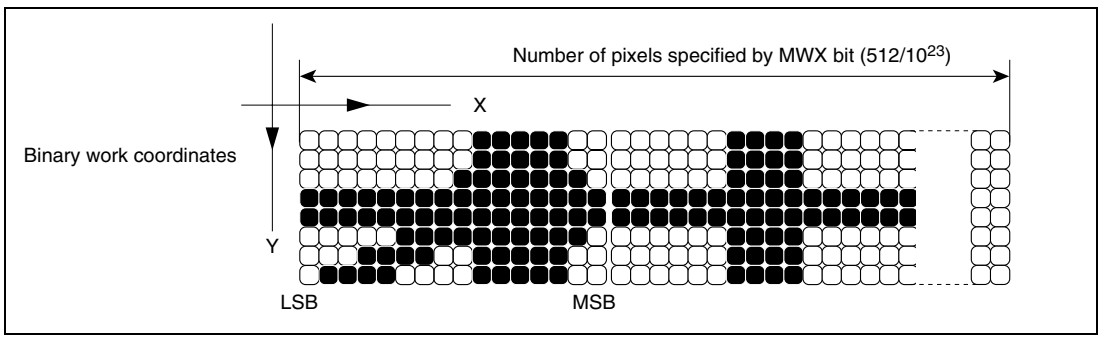
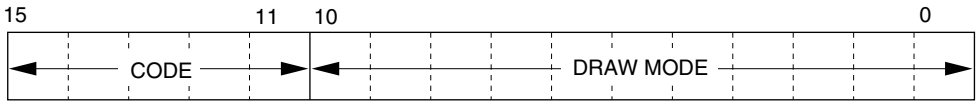


Figure 3.42 Binary Work Data Configuration

3.5.3 Rendering Attributes

Thirteen kinds of attribute specifications can be made: work (WORK), clipping (CLIP), transparent (TRNS), source style (STYL), net drawing (NET), source half (HALF), even/odd select (EOS), bold line drawing (FWUL, W2UL, FWDR, W2DR), source linear address (LNi), 4-pixel-unit processing (FST), source coordinate relative address (REL), edge (EDG), and color offset (COOF). The attributes that can be specified depend on the command. The rendering attributes are embedded in the commands, and can be specified on an individual command basis. Figure 3.43 shows the bit arrangement for rendering attributes.



POLYGON4A		TRNS	STYL	CLIP	0	NET	EOS	FST	LNi	COOF	WORK
POLYGON4A		TRNS	STYL	CLIP	REL	NET	EOS	0	1	COOF	WORK
POLYGON4B		TRNS	STYL	CLIP	REL	NET	EOS			0	WORK
POLYGON4B		TRNS	0	CLIP	REL	NET	EOS			HALF	WORK
POLYGON4C				CLIP		NET	EOS	FST			WORK
FTRAP, RFTRAP				CLIP			EOS	EDG			
LINEW, RLINEW				CLIP			EOS				
LINE, RLINE				CLIP		NET	EOS	FWUL	W2UL	FWDR	W2DR
PLINE, RPLINE		TRNS	1	CLIP		NET	EOS	EDG2		EDG1	1
JUMP, GOSUB					REL						
CLRW				CLIP							
(Commands other than the above)											

Note: Shaded areas should be cleared to 0.
FWUL, W2UL, FWDR, W2DR: Bold line drawing bits
REL: Relative address specification
EDG: Edge drawing bit

Figure 3.43 Rendering Attribute Bit Arrangement

(1) Transparency Specification (TRNS)

When color expansion of binary source data is performed, transparency or non-transparency can be selected on an individual drawing command basis with the TRNS bit. When transparency is selected, a 0 in the binary source data is transparent and a 1 has the value of the COLOR1 parameter. When non-transparency is selected, a binary data 0 has the value of the COLOR0 parameter, and a 1 has the value of the COLOR1 parameter. With multi-valued source data, all-0 data becomes a transparent color, and those pixels are not drawn. The transparency specification can be used with the POLYGON4A, POLYGON4B, PLINE, and RPLINE commands; in other commands, the TRNS bit should be cleared to 0.

(2) Source Style Specification (STYL)

When drawing a rectangle, the STYL bit can be used to select, on an individual drawing command basis, whether the source data is to be enlarged or reduced, or referenced repeatedly. If no style specification is made, the source data is enlarged or reduced in proportion to the size of the rendering area. When a style specification is made, the source data is referenced repeatedly in proportion to the size of the rendering area. This attribute is therefore used when drawing repeated patterns such as hatch patterns. The source style specification can be used with the POLYGON4A, POLYGON4B, PLINE, and RPLINE commands; in other commands, the STYL bit should be cleared to 0. When a source style specification is used, do not make a source half specification.

An example of a source style specification is shown in figure 3.44.

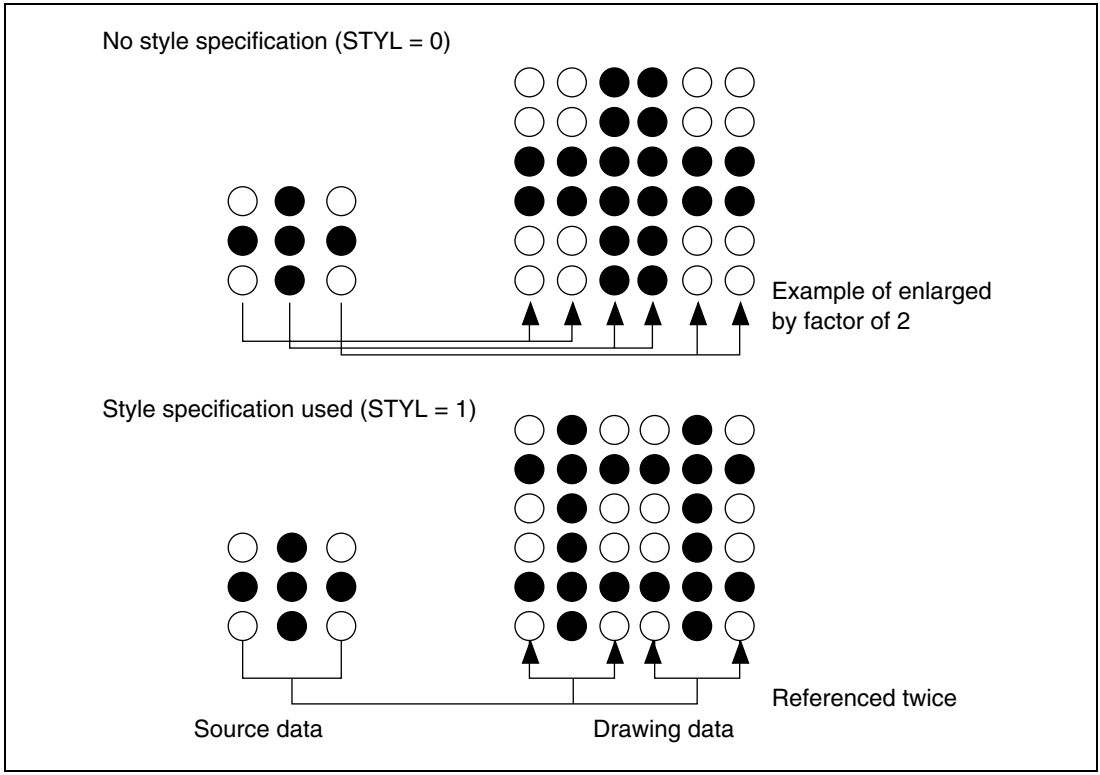


Figure 3.44 Example of Source Style Specification

(3) Clipping Specification (CLIP)

The Q2SD can perform clipping area management. In the clipping area, drawing is performed. Outside the clipping area, only operations are performed although the results are not written to memory. There are two kinds of clipping area: a system clipping area designated by the SCLIP command, and a user clipping area designated by the UCLIP command.

The system clipping area has a fixed drawing range. The system clipping area is always valid, regardless of attribute specifications.

A user clipping area can be designated as desired within the system clipping area. Whether or not clipping is performed in that area can be selected on an individual command basis with the rendering attribute CLIP bit. The boundary is drawn.

Clipping is set in the screen coordinates without offset.

Figure 3.45 shows an example of the clipping specification.

An example of a clipping specification is shown in figure 3.42.

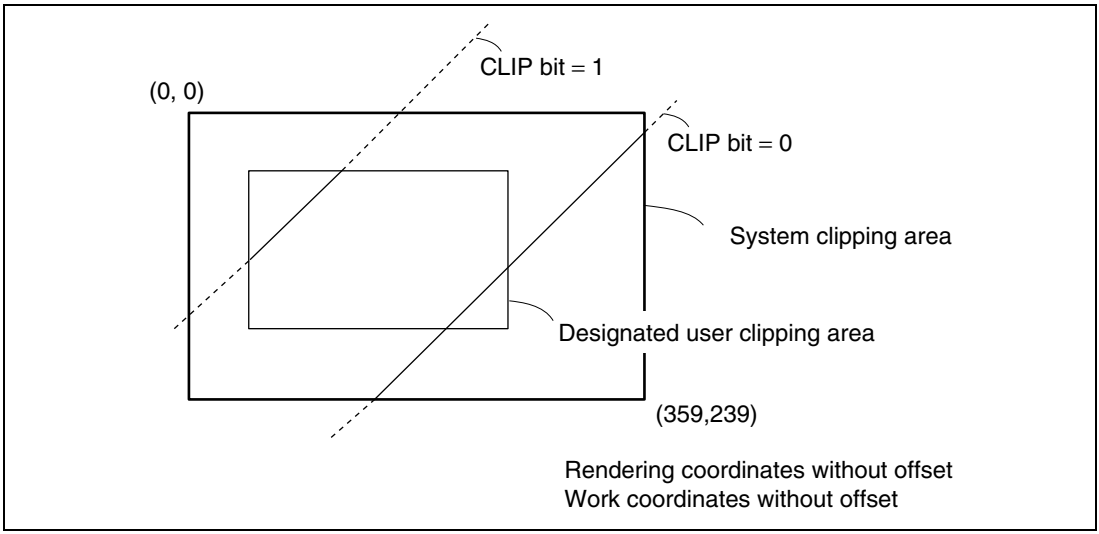


Figure 3.45 Example of Clipping Specification

(4) Net Drawing Specification (NET)

The NET bit can be used to select, on an individual drawing command basis, whether or not net drawing is to be performed. Net drawing is a function for drawing only pixels at coordinates for which the condition “rendering coordinates X + Y = EOS (0: even number, 1: odd number)” is true. For example, if EOS = 0, drawing will only be performed at coordinates Y = 0, X = 0, 2, 4, 6, 8, ..., Y = 1, X = 1, 3, 5, 7, 9, ...

This function enables the drawn figure and ground to be mutually semi-composed.

The net drawing specification can be used with the POLYGON4 commands, and the LINE, RLINE, PLINE, and RPLINE commands; in other commands, the NET bit should be cleared to 0.

(5) Even/Odd Select Specification (EOS)

Even pixels are selected when EOS = 0, and odd pixels when EOS = 1.

The even/odd select specification is used together with the net specification or source half specification.

With the LINEW and RLINEW commands, drawing is performed at the work coordinates with 0 when EOS = 0, and with 1 when EOS = 1.

Examples of even/odd select specifications are shown in figure 3.46.

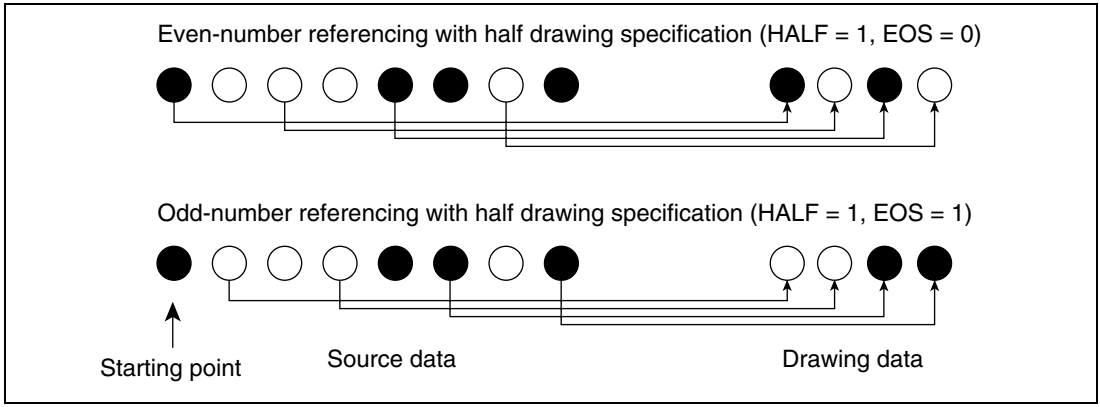


Figure 3.46 Examples of Even/Odd Select Specifications

(6) Source Half Drawing Specification (HALF)

The HALF bit can be used to select whether all or only half of the source data is to be referenced. When the source half drawing specification is selected, only EOS (0: even number, 1: odd number) data is referenced from the source starting point. Thus only half of the source data in the horizontal direction is referenced.

The source half drawing specification can only be used with the POLYGON4B (binary source) command; in other commands, the HALF bit should be cleared to 0. When a source half specification is used, do not make a source style specification. Do not use this specification when the x coordinate of the drawing coordinates is within a negative range since the drawing image may be distorted.

(7) Work Specification (WORK)

When drawing is performed at rendering coordinates with POLYGON4 commands, the WORK bit can be used to select, on an individual drawing command basis, whether or not binary work data is to be referenced.

When binary work data referencing is selected, drawing is performed if the work data for the pixel corresponding to the rendering coordinates is 1, but not if the work data is 0. The same shape as that drawn at work coordinates can thus be drawn at rendering coordinates. Drawing at work coordinates can be performed either by means of the FTRAP command or else by the SuperH. Ensure that UGM drawing access by command and UGM drawing access by the SuperH are not performed simultaneously. The work specification can be used with the POLYGON4A, POLYGON4B, and POLYGON4C commands; in other commands, the WORK bit should be cleared to 0.

With the PLINE and RPLINE commands, this attribute is specified but work references are not performed.

(8) Bold Line Drawing Specification

Taking individual line segments of a polygonal line specified by parameters as reference lines, this specification makes the reference lines bold lines in the upper-left direction and lower-right direction, independently. Whether or not this attribute is enabled is specified by the FWUL bit and FWDR bit, while the width of a bold lines can be selected from line widths 1 to 5 by a combination of bits W2UL and W2DR. The FWUL bit enables bold-line implementation in the upper-left direction, while the FWDR bit enables bold-line implementation in the lower-right direction. The W2UL bit is valid when FWUL = 1, and the W2DR bit when FWDR = 1.

This function is valid for each segment of a polygonal line. Using the segment line main scanning axes, lines with the same slope in the up (left) and down (right) directions, and of the same length, are drawn repeatedly. Therefore, the shape of the segment linkage parts is not considered. This function can be used with the LINE and RLINE commands; in other commands, the FWUL, W2UL, FWDR, and W2DR bits should all be cleared to 0.

When performing bold line drawing, set the vertex coordinates so that the entire bold line area does not extend beyond the drawing area (both x and y in the range –2045 to 2044).

Table 3.10 Bold Line Drawing Settings

FWUL	W2UL	FWDR	W2DR	Line Width (Direction, Magnification)
0	0	0	0	1 (no magnification)
			1	1 (no magnification)
		1	0	2 (lower right 1)
			1	3 (lower right 2)
	1	0	0	1 (no magnification)
			1	1 (no magnification)
		1	0	2 (lower right 1)
			1	3 (lower right 2)
1	0	0	0	2 (upper left 1)
			1	2 (upper left 1)
		1	0	3 (upper left 1, lower right 1)
			1	4 (upper left 1, lower right 2)
	1	0	0	3 (upper left 2)
			1	3 (upper left 2)
		1	0	4 (upper left 2, lower right 1)
			1	5 (upper left 2, lower right 2)

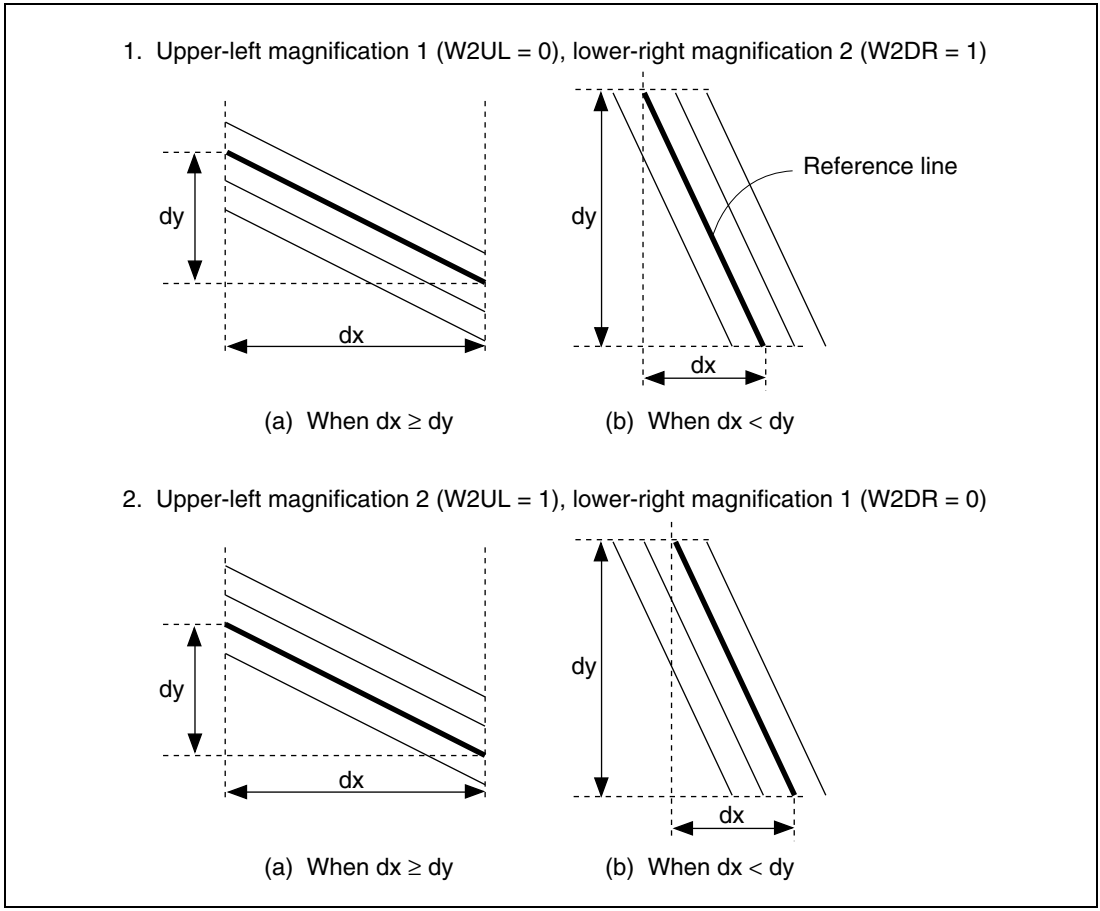


Figure 3.47 Examples of Bold Line Drawing

(9) Source Address Linear Specification (LNi)

Use of a 2-dimensional virtual address or a linear address as the source address can be selected, on an individual drawing command basis, by means of the LNi bit. To use a linear address, set this bit to 1.

This function can be used with the POLYGON4A command; in other commands, the LNi bit should be cleared to 0. For details of command operation, see section 4.1.1, POLYGON4A.

(10) 4-Pixel-Unit Processing (FST)

Whether or not 4-pixel unit processing is performed can be specified for individual drawing commands by means of the FST bit. To perform 4-pixel unit processing, set the FST bit to 1. In this case, no other rendering attributes except CLIP can be used. This function can be used with the POLYGON4A and POLYGON4C commands; in other commands, the FST bit should be cleared to 0.

When using this attribute, set the command parameters as indicated in the individual command descriptions.

(11) Source Coordinate Relative Address Specification (REL)

Setting the REL bit to 1 in POLYGON4A, POLYGON4B, JUMP, and GOSUB commands enables source referencing and branching to be performed at an address relative to (before or after) the command code. The source address must be a linear address. Also, for reasons relating to referencing of a multi-valued source arranged in linear fashion, the LNi bit must be set to 1 when using POLYGON4A; operation cannot be guaranteed if the LNi bit is 0.

The command code address is the relative address origin.

(12) Edge Drawing (EDG)

With the FTRAP and RFTRAP commands, setting the EDG bit to 1 enables edge lines to be drawn after completion of trapezoid painting. Whether edge line drawing is performed with 0 or with 1 is specified by the EOS bit.

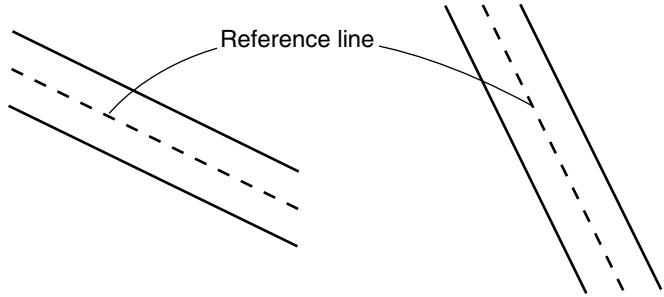
(13) Line Drawing Edge Specification (EDG1, EDG2)

Whether or not edge drawing is performed for a polygonal line with line type can be specified for individual drawing commands by means of the EDG1 bit.

This function is valid for each segment of a polygonal line. Using the segment line main scanning axes, solid lines with the same slope and of the same length, are drawn either vertically or horizontally. Therefore, the shape of the polygonal line linkage parts is not considered. The solid edge lines have the value of COLOR1.

This function can be used with the PLINE and RPLINE commands; in other commands, the EDG1 bit should be cleared to 0. A source size of 8 or 16 can be used. Set 8 or 16 for source size parameter TDX.

Edge drawing 1 specification (EDG1 = 1)

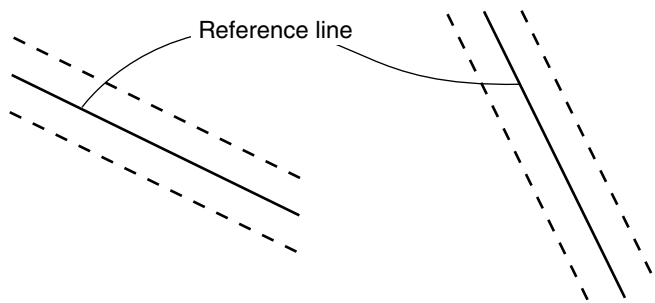


Whether or not edge drawing is performed for a polygonal line with line type can be specified for individual drawing commands by means of the EDG2 bit.

This function is valid for each segment of a polygonal line. Here, each segment of the polygonal line specified by the parameter is considered as a reference line. This function is implemented for each segment of a polygonal line, using the following procedure. First, the reference line is drawn as a line with line type. Next, using the segment line main scanning axes, solid lines with the same slope and of the same length, are drawn either vertically or horizontally. Finally, the reference line is drawn as a solid line. Therefore, the shape of the polygonal line linkage parts is not considered. The solid line drawn last has the value of COLOR1.

This function can be used with the PLINE and RPLINE commands; in other commands, the EDG2 bit should be cleared to 0.

Edge drawing 2 specification (EDG2 = 1)



Both the EDG1 and EDG2 bits should not be set to 1 at the same time.

(14) Color Offset (COOF)

This function can be used with the POLYGON4A command. In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in the COLOR register to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit must be cleared to 0. Use 100% or enlarged drawing since miniaturized drawing of the source may distort the image.

3.5.4 Command Fetching

(1) Command Fetch Operation

When the rendering start bit RS in the system control register SYSR is set to 1, the Q2SD fetches the display list in the UGM to carry out drawing operations. The display list and the source data to be used by the display list should be stored in the UGM before the Q2SD starts to fetch the display list by the rendering start bit.

The Q2SD performs sequential fetches in low-to-high address order, starting at the address set in the display list start address register (DLSAR). The fetch address can be changed midway, using a JUMP or GOSUB command. Q2SD fetching can be terminated by placing a TRAP command at the end of the display list.

The Q2SD has a dedicated command buffer, and an equivalent area of the UGM is accessed at one time. When processing of the commands in this buffer is completed, another command fetch is performed.

If the commands include a JUMP, GOSUB, or other command that changes the flow, the Q2SD starts fetching again from the new address indicated by that command.

Figure 3.48 shows an example of the display list.

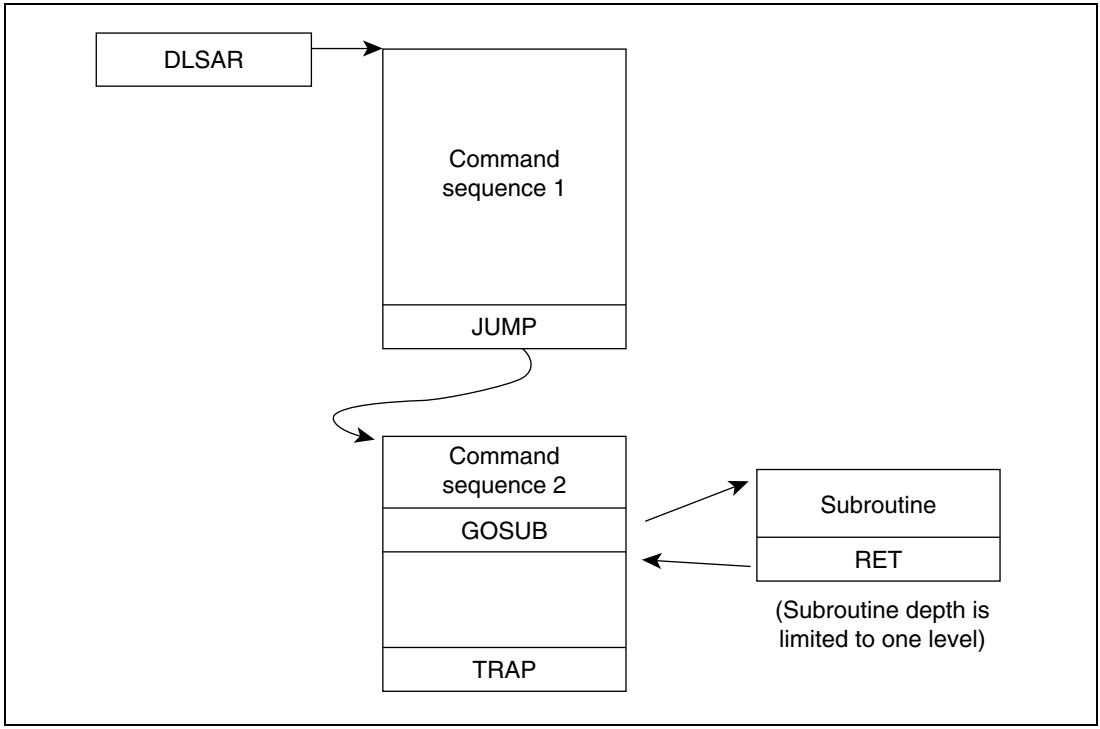


Figure 3.48 Example of Display List

(2) Drawing Suspension and Resumption

The Q2SD supports a drawing suspend/resume function, synchronized with the $\overline{\text{VSYNC}}$ signal between the CPU and Q2SD. This enables multiple drawing processing to be performed in parallel with priority order. This function is mainly used when alternately using frame buffers and the background screen to execute drawing.

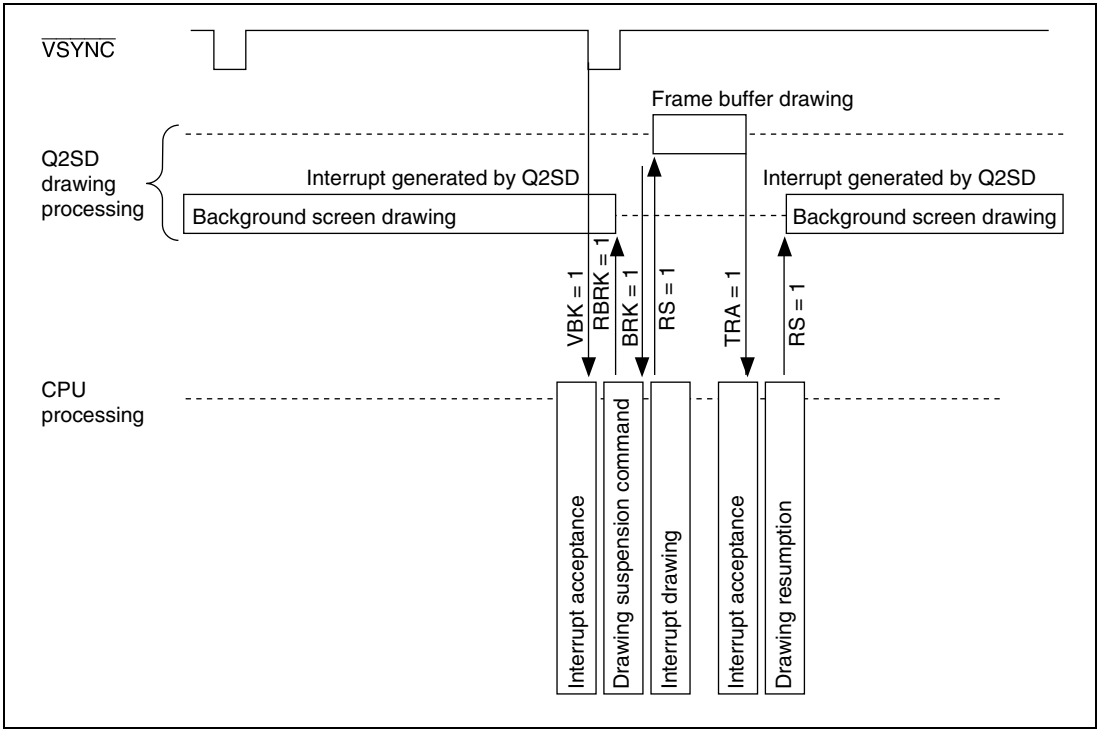


Figure 3.49 Example of Timing for Suspending and Resuming Background Screen Drawing

(3) Suspension Processing

1. Set BRCL to 1 in the status clear register (SRCR), clear the BRK bit to 0 in the status register (SR), and set the drawing suspension directive bit (Rendering Break: RBRK) to 1 in the system control register (SYSR).
2. Next, monitor the BRK bit and TRA bit.
3. When BRK is observed to be set to 1, this means that the currently executing drawing command processing has ended and the drawing unit has halted (drawing has been suspended) at the point at which the next drawing command was fetched. Information required for software processing in anticipation of resumption processing should be read from the address-mapped registers and saved in memory. At this time, the RBRK bit is cleared to 0.
4. When TRA is observed to be set to 1, this means that a TRAP command has been executed and Q2SD drawing processing has ended. Therefore, ensure that no subsequent resumption processing is carried out. If drawing is to be performed after suspension processing, wait until the TRA flag is observed to be set to 1.

(4) Resumption Processing

1. The parameters saved immediately after suspension are restored. Some are written directly to the registers, and some are set by command. The former include the subroutine return address (which can also be set with the WPR command), and the latter, clip area, local offset, current pointer, and execution restart addresses. Of the latter, the execution restart address is restored by setting the command status register value at the time of the suspension as the jump destination of a JUMP command. For the other parameters in the latter group, settings should be made to provide for recovery by means of the appropriate command before execution of this JUMP command.
2. After performing a write for the purpose of subroutine return address restoration, and creating a command list to restore the other parameters, drawing can be resumed by setting the address of this command list in DLSAR and implementing a rendering start.

3.5.5 Internal Buffer

The Q2SD has three internal buffers—a command buffer, source buffer, and work buffer—as shown in figure 3.50.

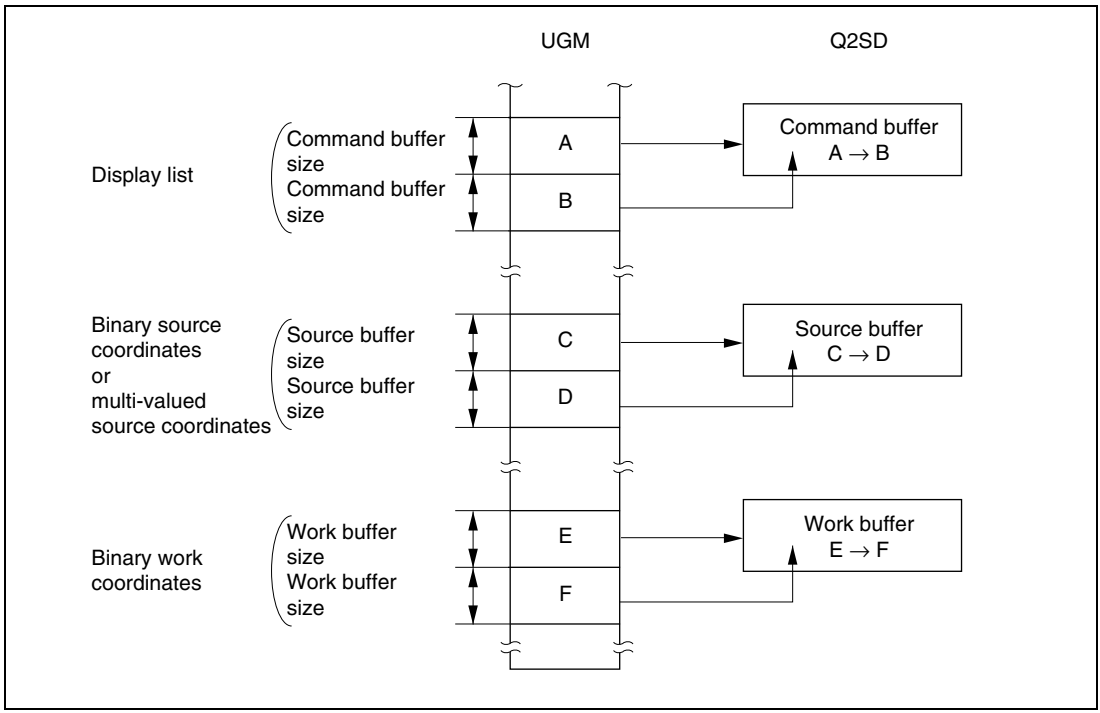


Figure 3.50 Updating of Q2SD's Internal Buffers

These buffers are used by the Q2SD to temporarily store data held in the UGM. The Q2SD uses the data stored in these buffers when executing drawing. The functions of these buffers are as follows:

1. Command buffer (32 bytes × 2)

   Used by the Q2SD to store a display list held in the UGM. The buffer size is 64 bytes.
2. Source buffer (64 bytes)

   Used by the Q2SD to store a binary source or multi-valued source held in the UGM. The buffer size is 64 bytes.
3. Work buffer (16 bytes)

   Used by the Q2SD when performing drawing at binary work coordinates in the UGM. The buffer size is 16 bytes.

When buffer contents are not updated, (when the same address is referenced by data of or below the capacity of the buffer, or a reference ends at a location at or below the capacity of the buffer from the previous reference start location), the previous buffer contents will be used even though the data in the UGM is rewritten. To intentionally update buffer contents, the address of a location exceeding the buffer capacity should be referenced.

3.6 Video Capture

The Q2SD can incorporate a YUV 4:2:2 8-bit data stream obtained by digital encoding of NTSC signals. The captured data is displayed on the video screens.

3.6.1 Configuring Circuit for Video Capture

(1) Video Capture Operation

Video capture is performed at the rising edge of the VQCLK signal. The 8-bit data stream corresponding to the number of pixels set in the VSIZEX field in the video window size register (VSIZER) is captured for each VHS signal and transferred to one of three video storage areas determined by video area start address registers (VSAR). These areas are used sequentially in frame units. The video window status bits (VID0, VID1) are valid when 0 is set in the video incorporation enable bit (VIE) and indicate the most recent video area in which video capture has been completed. The size of the video storage areas is determined by VSIZEX and VSIZEY. Use a frequency not exceeding 1/2 the system operating clock frequency for VQCLK (the system operating clock should be in the range 64 to 66 MHz). A number of VQCLK cycles equal to twice the number of luminous pixels are necessary per VHS. $\overline{\text{VVS}}$, $\overline{\text{VHS}}$, $\overline{\text{VODD}}$ and VQCLK are accepted following hardware reset release, and video capture is started by setting VIE to 1, having the first VVS signal sync signal input, then having the first VHS signal sync signal input.

As the video storage area capture line number is incremented each time a VHS signal sync signal is input, VQCLK must not be input during the VHS signal sync signal period. The VQCLK pin

should be low level except when a valid data is output. For video capture, select a UGM bus width of 32 bits by setting MES1 and MES0 in the memory mode register (MEMR).

The relationship between video input signals is shown in figures 3.51 and 3.52.

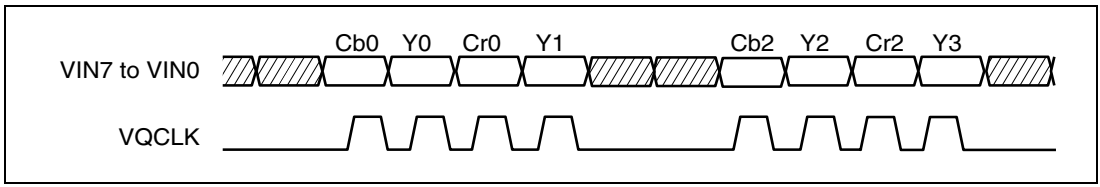


Figure 3.51 Video Incorporation Signals

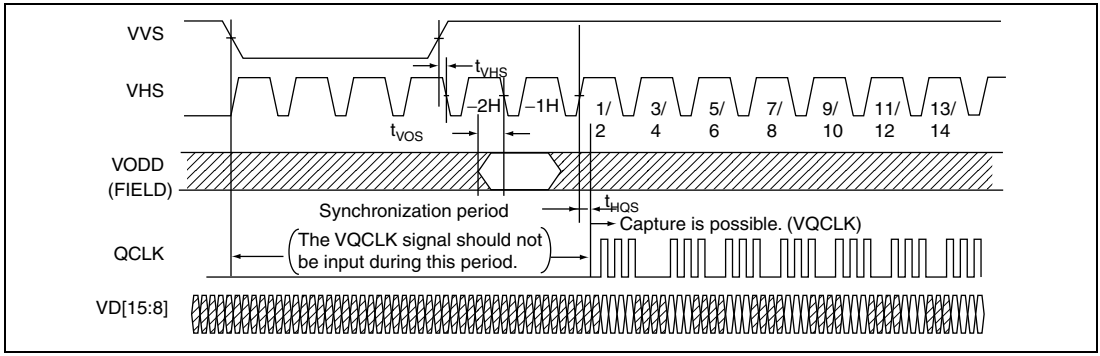


Figure 3.52 Video Capture Timing

(2) Video Capture and Display Operation

As the data (which supports to the 8-bit YCbCr (2:2:1) format specified in ITU-601) arrives from the video decoder, the video-capture function writes it to the video-capture area in the UGM.

Three areas, V0, V1, and V2, are captured in the order and video display from an area may commence once the operation of writing to that area has been completed.

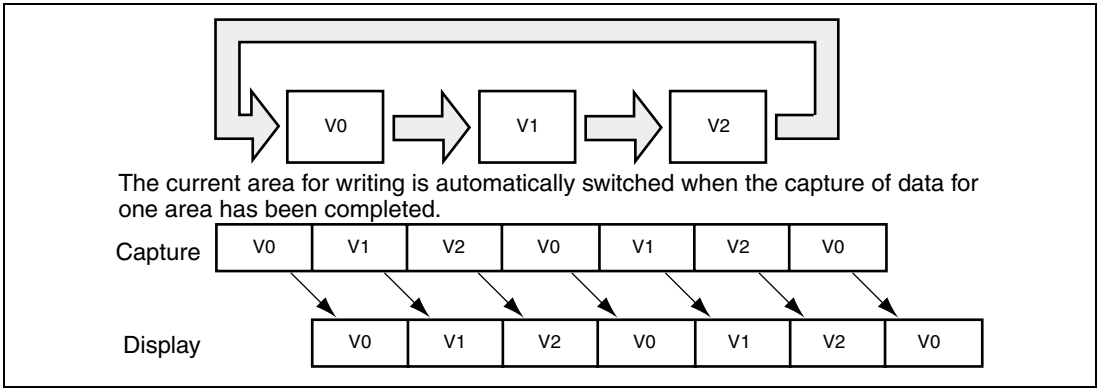


Figure 3.53 Capture State

The functions of displaying and capturing video data are each capable of independent operation since the Q2SD is able to capture video data whether the display is on or off; that is,.

Using the three areas makes it possible to deal with the situation where the times at which capture and display start are not synchronized and thus do not necessarily match.

While video capture is in progress (VIE = 1), display of the area specified by the immediately prior value of the VID bits commences. When a capture operation stops while it is in progress, the current screen continues to be displayed, as is shown in figure 3.54.

When the capture operation is resumed, the current screen will continue to be displayed until the VID bits are updated on completion of the capture of one screen. Setting the VIE bit to 1 resets the video capture area to V0.

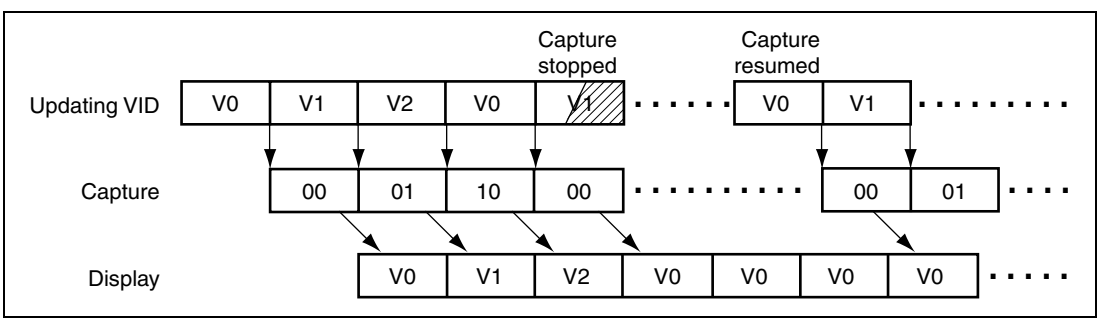


Figure 3.54 Display State

3.6.2 Video Capture Mode

The mode of capture by the Q2SD is selectable from among four modes. The appropriate mode is selected by such factors as the resolution of the video screen, the output format of the video decoder, and the destination device (CRT, LCD, TV, etc.) for the output signal.

When ODEN1, ODEN0 = 0, 1, a one-frame screen is created by combining even and odd fields. Motion interpolation is not performed. In the case of moving pictures with violent motion, the screen may be difficult to see as a still picture. This mode is suitable for interlace display under conditions in which the frame rate and the number of scanning lines in the vertical direction are both the same as for the input video. Line 1 is line 0 of the UGM to support the case that the original signal has no line 0. Note that even and odd lines are reversed between the original signal and the UGM. Therefore, capture begins with an odd field (VINM = 0) when an even field is displayed first within a frame (ODEV = 1), and with an even field (VINM = 1) when an odd field is displayed first within a frame (ODEV = 0).

When ODEN1, ODEN0 = 1, 0, or 1, 1, a one-field image is treated as a one-field image. At this time, the number of vertical scanning lines is halved. Original-size display is not possible. To preserve the vertical/horizontal ratio, the horizontal multiplication factor should be adjusted. This mode is used for non-interlace (SCM1, 0 = 0:0) display.

Set the value of VACTIVE according to the setting of ODEN1 and ODEN0 in the video incorporation mode register (VIMR).

When performing video capture, input the video stream data to the VIN pin, without having scaling processing (thinning-out processing) performed by the video stream decoder.

1. When ODEN1 = 0 and ODEN0 = 1

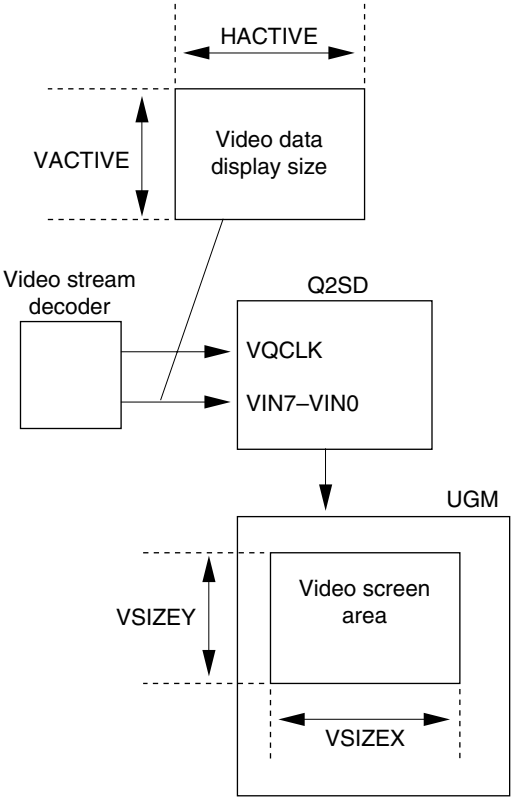
   Make the value of VACTIVE the total number of effective display lines in the vertical direction in two 2 $\overline{\text{VVS}}$ intervals.

   For example, with 240 effective display lines in the vertical direction in one 1 $\overline{\text{VVS}}$ interval, the setting should be:

   VACTIVE = 240 × 2 = 480

2. For settings other than ODEN1 = 0, ODEN0 = 1

   Make the value of VACTIVE the number of effective display lines in the vertical direction in one 1 $\overline{\text{VVS}}$ interval.



VSIZEX: Horizontal reduction (thinning-out) ratio set by video incorporation reduction ratio (1/1, 1/2, 1/3, 1/4, or 1/6)
VSIZEY: Vertical reduction (thinning-out) ratio set by video incorporation reduction ratio (1/1, 1/2, 1/3, or 1/4)

HACTIVE (pixels) ≥ VSIZEX
VACTIVE (pixels) ≥ VSIZEY

$$\text{VQCLK high-level width (sec.)} \geq \frac{2}{\text{MCLK}}$$

MCLK = CLK0 × N (Hz)
CLK0: Frequency (Hz) of clock input to CLK0 pin
N: Multiplication factor determined by pins MODE2 to MODE0

Figure 3.55 Video Screen Area

(3) Non-Interlace Mode Capture (ODEN1 = 0, ODEN0 = 0)

This is the appropriate mode when the video decoder is in non-interlace mode. All video data for each VSYNC signal is stored in a single capture area. When the output of the video decoder is in interlace sync mode, take care with regard to the size of the capture area taken up by the captured data, since the data consists of only half of the lines for the screen.

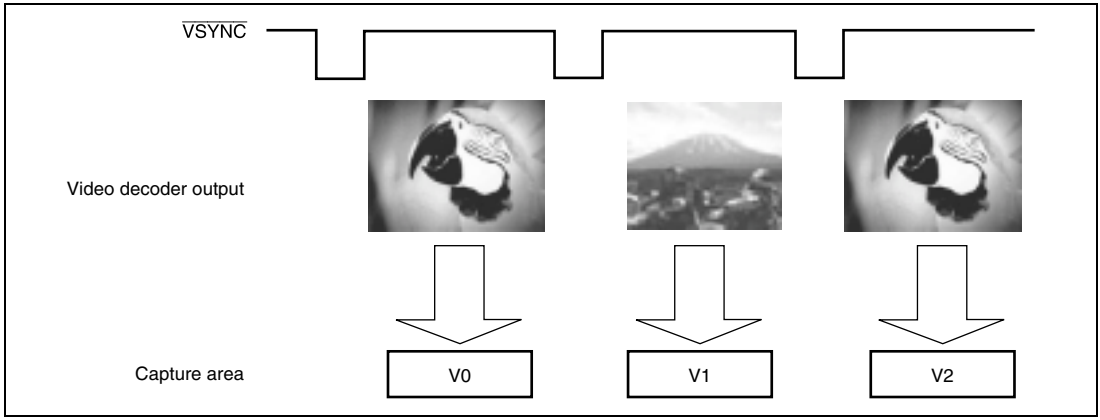


Figure 3.56 Interlace Capture

(4) Interlace Composite Capture (ODEN1 = 0, ODEN0 = 0)

This mode is applicable to video data for an interlaced display. Data for the odd and even fields are composed and stored in a single capture area. When the signal output by the video decoder is not for an interlaced display, correct operation is not guaranteed.

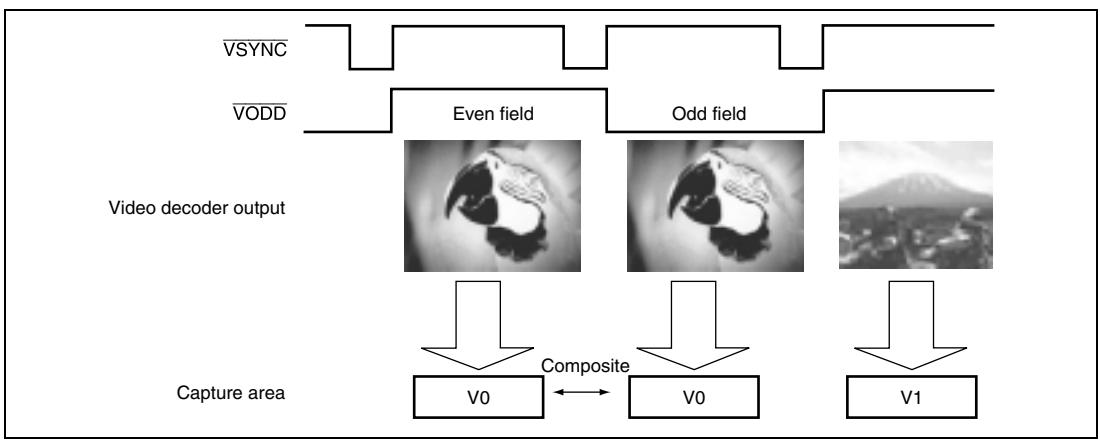


Figure 3.57 Interlace Composite Capture

(5) Interlace Capture (Odd Field Only: ODEN1 = 1, ODEN0 = 0)

This stores the odd fields of data for an interlaced mode display (the VODD signal is at its low level) in a single capture area. Take care with regard to the size of the capture area taken up by the captured data, since the data consists of only half of the lines for the screen.

When the output of the video decoder is in non-interlace sync mode, every second field of data will not be stored. The data size for capture, however, are the same.

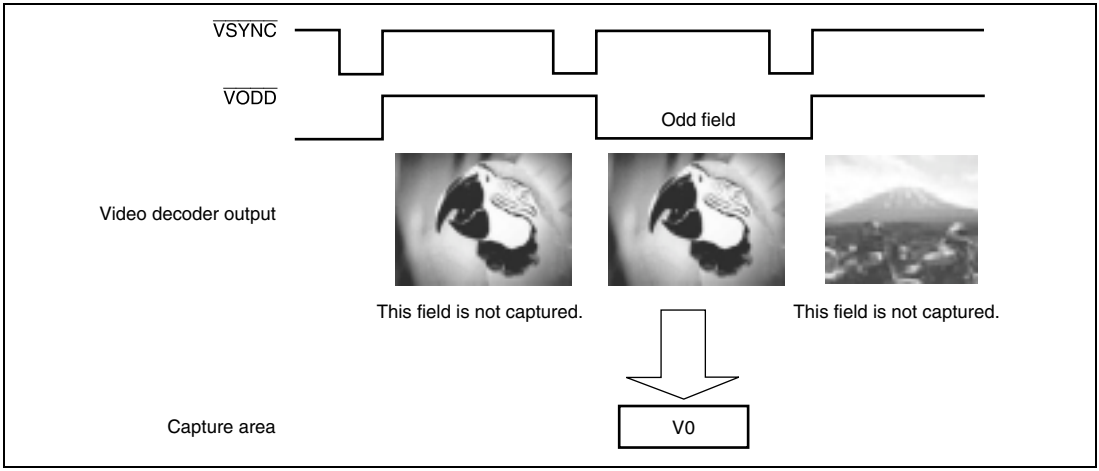


Figure 3.58 Interlace Capture (Odd Field)

(6) Interlace Capture (Even Field Only: ODEN1 = 1, ODEN = 1)

This stores the even fields of data for an interlaced mode display (the VODD signal is at high low level) in the capture area. Take care with regard to the size of the capture area taken up by the captured data, since the data consists of only half of the lines for the screen.

When the output of the video decoder is in non-interlace sync mode, every second field of data will not be stored. The data size for capture, however, are the same.

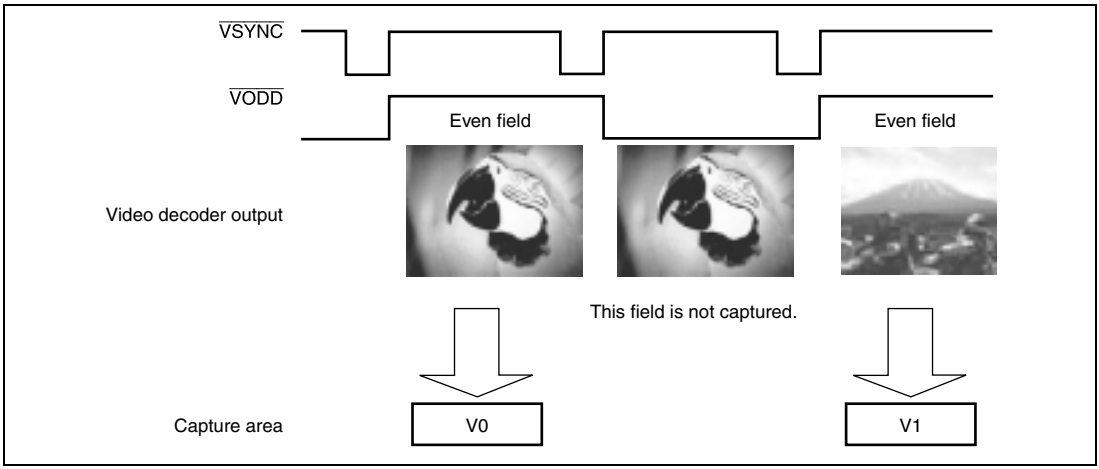


Figure 3.59 Interlace Capture (Even Field)

(7) Field Order for Video Capture

The field order for video capture is specifiable by the video incorporation mode bit (VINM) in the video incorporation mode register (VIMR). This enables to assign the first field to either the upper

or lower line. Motion interpolation is not performed. In the case of moving pictures with violent motion, the screen may be difficult to see as a still picture.

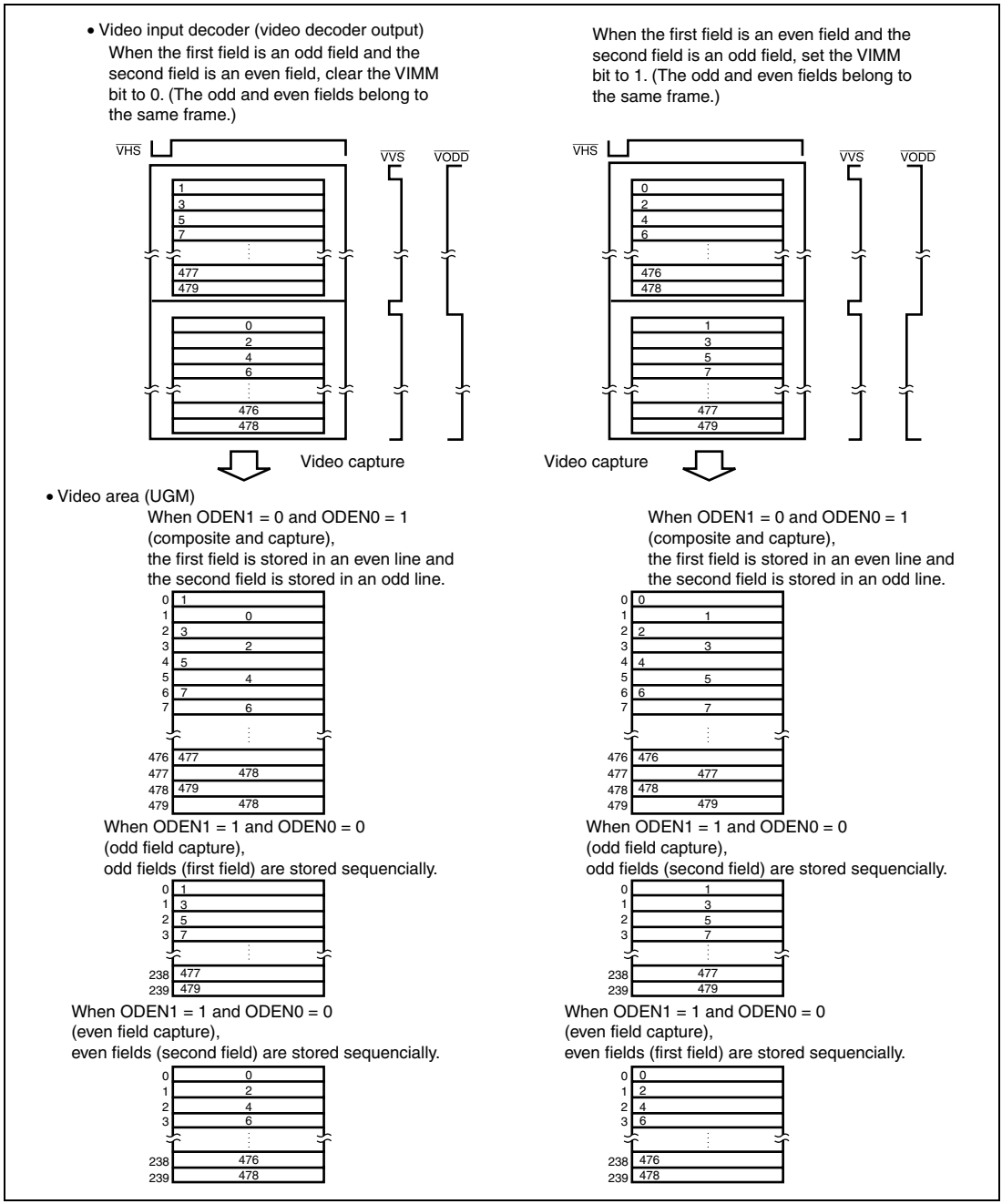


Figure 3.60 Interlace Video Input Field Handling Specification

3.6.3 Reduction of Video Capture Images

The size of the captured image may be reduced by setting bits VSIZ0 to VSIZ4 in the video capture mode register (VIMR), where vertical and horizontal reduction ratios are independently specifiable.

The selectable reduction ratios in the horizontal direction are 1/2, 1/3, and 1/4 and the ratios in the vertical direction are 1/2, 1/3, and 1/4. The VSIZEX and VSIZEY bits should be set to the value obtained that the number of horizontal/vertical valid pixels is multiplied by the video incorporation reduction ratio (VSIZ4 to VSIZ0) and the result is rounded down to 0.

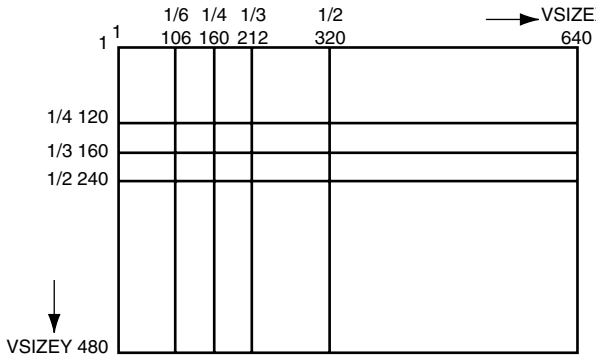


Figure 3.61 Reducing the Size of the Captured Image

As an example, when the setting of the VSIZEX bits is 480 and the setting for the reduction ratios is as above, each current frame of data in the memory is displayed on a video-screen area which is wider than 320 pixels since video data is not sent for the horizontal pixel range from 321 to 480. On the other hand, when the setting of the VSIZEX bits is 240, which is smaller than the captured image, the data which is displayed will be cut off since there is no screen area for the horizontal pixel range from 241 to 320.

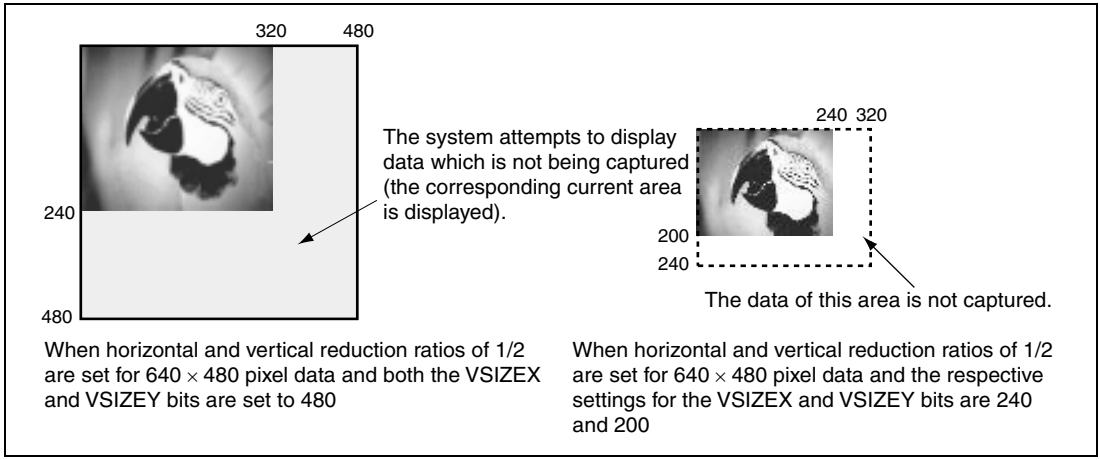


Figure 3.62 Incorrect Settings for the Reduction Ratios

These failures will occur with incorrect setting of the VSIZEY bits. When the result of a reduction calculation is non-integer or odd, the result is rounded off to obtain an even number.

Example: Size of data to be sent by video decoder × reduction ratio = video window size

X: $640 \times 1/3 = 213.3333 \rightarrow 212$

Y: $480 \times 1/3 = 160$

3.6.4 Setting Video Capture Position

The method of address calculation is shown below.

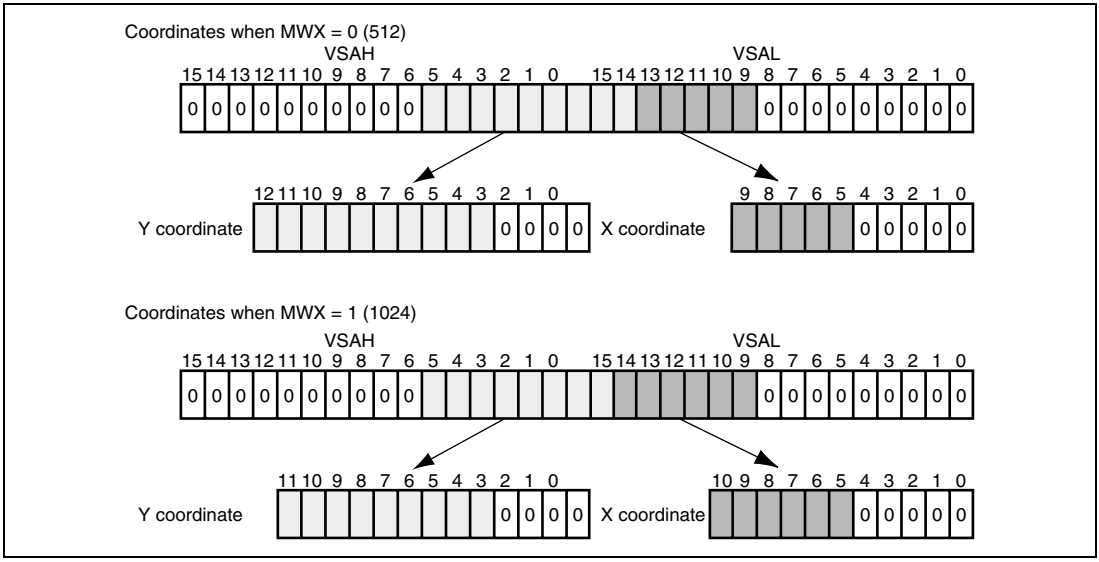


Figure 3.63 Setting up the Capture Area

Within the range of the UGM, any multiple of 16 is specifiable as the Y coordinate and any multiple of 64 is specifiable as the X coordinate. Note that the specified area is accessed as 16-bit/pixel data. Therefore, when the video screen overlaps with the foreground or background screen, the area of overlap is also accessed as 16-bit/pixel data. When the MWX bit is specified as 0 to select the 512-pixel mode, the values for the Y coordinate are from 0 to 8176 (pay attention to the setting for memory) and values for the X coordinate are from 0 to 960 (actually, the values which exceeds 511 should not be specified); Y coordinates are specified as integer multiples of 16 and X coordinates are specified as integer multiples of 64.

When the MWX bit is specified as 1 to select the 1024-pixel mode, the values for the Y coordinate are from 0 to 4080 and the values for the X coordinate are from 0 to 1984 (actually, values which exceed 1023 should not be specified); Y coordinates are specified as integer multiples of 16 and X coordinates are specified as integer multiples of 64. The value of the video window size in the X direction (VSIZEX) is up to 640.

An example of the calculation of the video area is given below.

When the MWX bit specifies 512-pixel mode and three video screens are allocated, as is shown in figure 3.64, the settings of each of VSAH and VSAL registers are as given below.

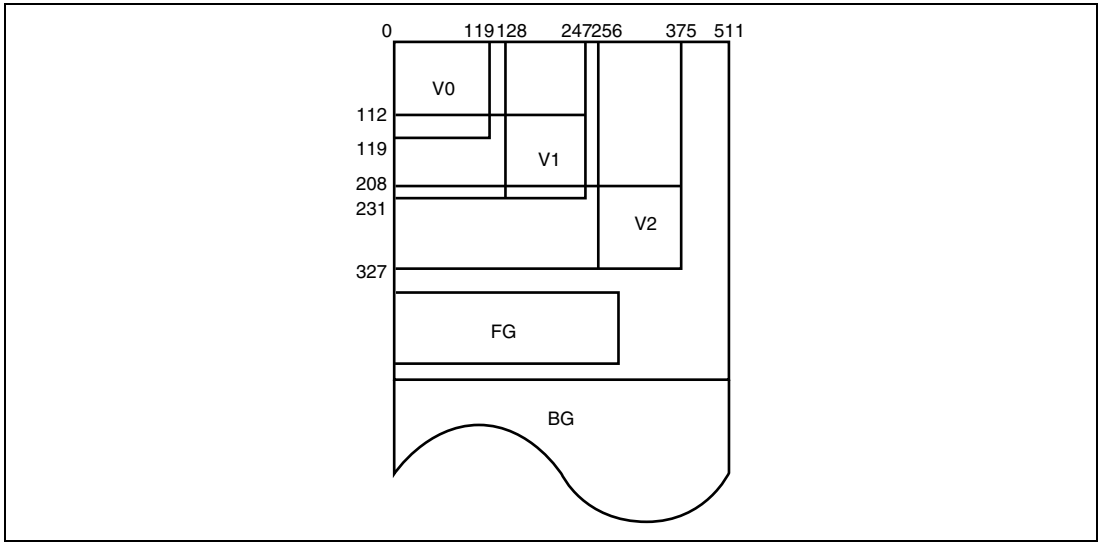


Figure 3.64 Example of the Settings for Capture Areas

V0: X = 0, Y = 0
Y coordinate: 0000000000000, X coordinate: 00000000000
VSA: 0000000000000000, 0000000000000000
VSAH0: H′0000, VSAL0: H′0000

V0: X = 128, Y = 112
Y coordinate: 0000001110000, X coordinate: 00010000000
VSA: 0000000000000001, 1100010000000000
VSAH0: H′0001, VSAL0: H′C400

V0: X = 256, Y = 208
Y coordinate: 0000011010000, X coordinate: 00100000000
VSA: 0000000000000011, 0100100000000000
VSAH0: H′0003, VSAL0: H′4100

3.6.5 Format of Captured Data

The Q2SD video input interface supports the 8-bit YCrCb pixel-stream format. Table 3.11 shows the configuration of the Q2SD's pins and the correspondence between the Q2SD pins and the bits of Y, Cr, and Cb data. Figure 3.65 shows the flow of data from a video decoder.

A video signal according to the NTSC specification consists of the Y, or luminance, signal (monochrome signal) and the C, or chrominance, signal (color signal)—this was chosen to retain compatibility with monochrome broadcasting. The result of the sampling of these signals by a video decoder is the quantized data.

Since the NTSC specification is based on the nature of the human eye, which is less sensitive to chrominance than to luminance, chrominance is only represented by half as many bits as luminance. Only half as many bits are thus sampled from the C signal as from the Y signal, and the same proportion applies to the data. Furthermore, the C data is also divided into red and blue components, i.e., Cr (red − Y) and Cb (blue − Y). The final result is thus YCbCr data.

Figure 3.66 depicts the data for one pixel.

Table 3.11 8-Bit Pixel Interface

Q2SD	VIN7	VIN6	VIN5	VIN4	VIN3	VIN2	VIN1	VIN0
Y data	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
C data	Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0
	Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0

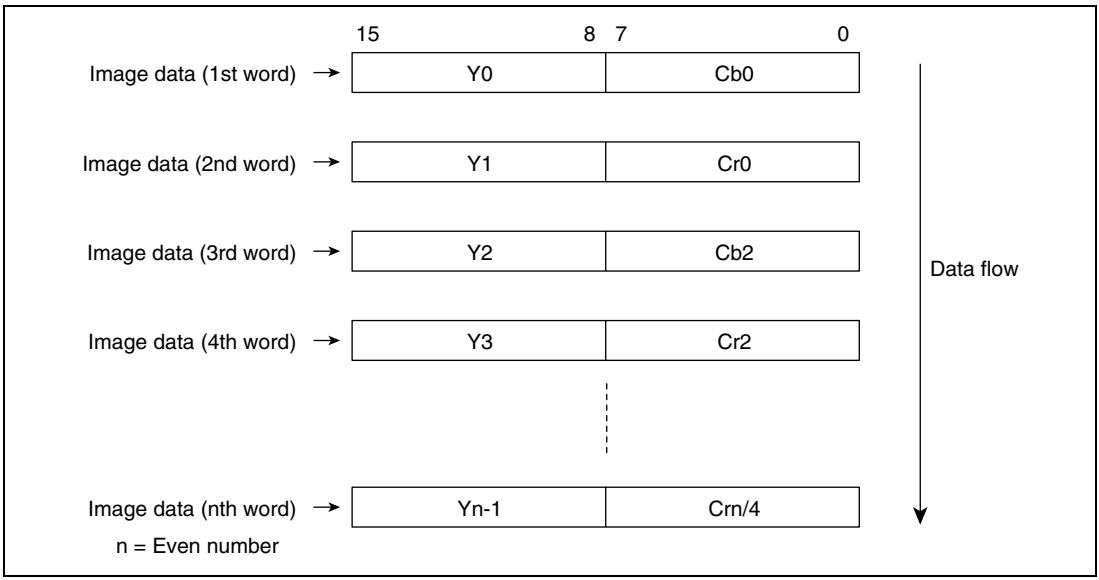
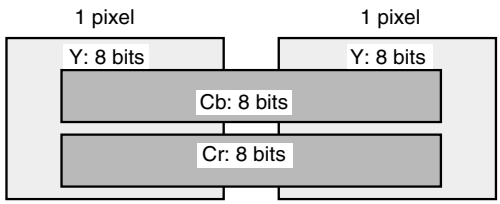


Figure 3.65 The Flow of YCbCr (4:2:2) Data



Two pixels of data are processed as a single item of information in the YCbCr format. One pixel of data consists of the components shown below.

1 pixel = Y (8 bits) + Cb (4 bits) + Cr (4 bits) = 16 bits

The ration of the respective amounts of data is thus 2:1:1. Since two pixels of data are sent in each transmission as described above, the ratio is in fact 4:2:2.

Figure 3.66 YCbCr (4:2:2) Data Format

Although YUV and YC data differ in terms of the range used to represent the data (notation), the same formula, which conforms with CCIR-601, is applied in converting both into RGB format. YUV data is represented by values in the range from 0 to 1 while YC data is represented as 8-bit data.

- When YUV format:

  Luminance: Y: 0 to 1,

  Chrominance: U: –0.5 to +0.5, V: –0.5 to +0.5

  RBG: R: 0 to 1, G: 0 to 1, B: 0 to 1

- When YC format:

Luminance:	Y: 16 to 235	U: 16 to 240	V: 16 to 240
Chrominance:	Cb: –112 to 112*	Cr: –112 to 112*	
RBG:	R: 16 to 235	G: 16 to 235	B: 16 to 235

Note: * When data is input to the Q2SD video capture input, the value ranges from 16 to 240 because offset of 128 is added.

- YCbCr – RGM conversion formula

  $R = Y + (Cr - 128) \times 1.37$

  $G = Y - 0.698 \times (Cr - 128) - 0.036 \times (Cb - 128)$

  $B = Y + (Cb - 128) \times 1.73$

  Where Y ranges from 16 to 235, Cr ranges from 16 to 240, and Cb ranges from 16 to 240.

3.6.6 YCbCr and RGB Data

The Q2SD has two circuits which convert YCbCr data into 16-bit RGB data as shown in figure 3.67. Use either of them. When RGB = 1, select VWRY = 0. When RGB = 0, select VWRY = 1.

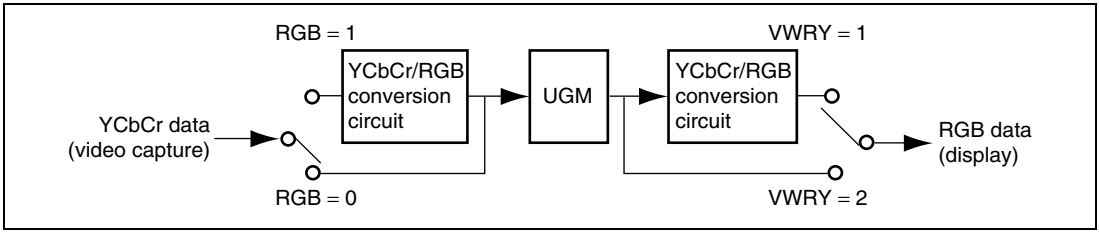


Figure 3.67 Conversion of YCbCr Data into RGB Format

When the first-stage conversion circuit is selected by setting the RGB bit in VIMR to 1, the YCbCr data sent from the video decoder is converted into RGB data for storage in the UGM. When the second-stage conversion circuit is selected by setting the VWRY bit in DSMR2 to 1, the YCbCr data sent from the video decoder is converted into RGB data when the video screen is displayed. This makes it possible to store data in either the YUV or RGB format.

When the first-stage circuit is applied to store RGB data in the UGM, the stored data can provide multi-valued source data for use in drawing. When the foreground or background screen is specified as being in the 16-bit/pixel mode, the RGB video data in a given screen area can be directly captured for display other than on the video screen. When the second-stage conversion circuit is used, the YCbCr data in the video capture area may be captured by the CPU for display elsewhere.

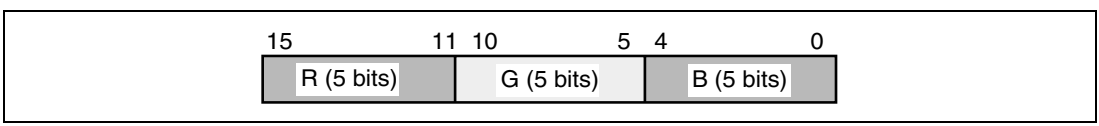


Figure 3.68 The RGB Data Format (16 Bits/Pixel)

3.7 Video Display Function

3.7.1 Video Screen Display

Setting the VWE bit of display mode register 2 (DSMR2) places the data from the video-capture area (VSA0 to 2) indicated by VID of the video-capture mode register (VIMR) on the video screen in 16-bit/pixel mode. When the video-capture function is in operation, the area read for display as the current screen is automatically switched according to the specification in VID.

The position at which the video screen is displayed is specified by the video display start position register. Before the VWE bit is set to 1, the initial value should be set to the video display start position register. The display size is specified by the VSIZEX and VSIZEY bits. The data is displayed on an independent window (video screen).

Set a display position within the display area specified by DSX/DSY. The size of video screen is the same as that of a captured area. In the non-interlace display mode, the video image can be

displayed at any desired position. In interlace sync & video and interlace mode, the Y position must be an even number (the lowest available setting is 0). The following conditions apply to the settings in the VPR:

Video horizontal-display start-position register (HVPR) DSX VSIZEX
Video vertical-display start-position register (VVPR) = DSY > VSIZEY

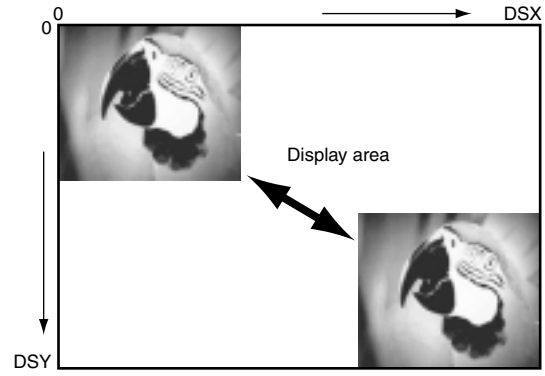


Figure 3.69 Position of the Video Image

3.7.2 Relationship between the Display Mode and Video-Capture Mode

The Q2SD is able to display images in any of three modes according to the setting of the SCM10 bit of the display-mode register (DSMR): the respective modes produce a non-interlace display, interlace display, and interlace sync & video display. Four video-capture modes are available, and the way in which the video data is captured in the UGM varies according to the mode of capture. Select the appropriate display mode for the correct display of the captured video data.

(1) Display of Data Captured in Non-Interlace Mode

The non-interlace capture mode is used when the video decoder outputs in non-interlace mode. The display of video data is completed for every VC. Capture in this mode is compatible with non-interlace mode. In an interlace sync display, one field is dropped out (missing of field occurs). In interlace sync & video mode, a frame may be composed of even and odd data in reverse order from that in the original frame of video data.

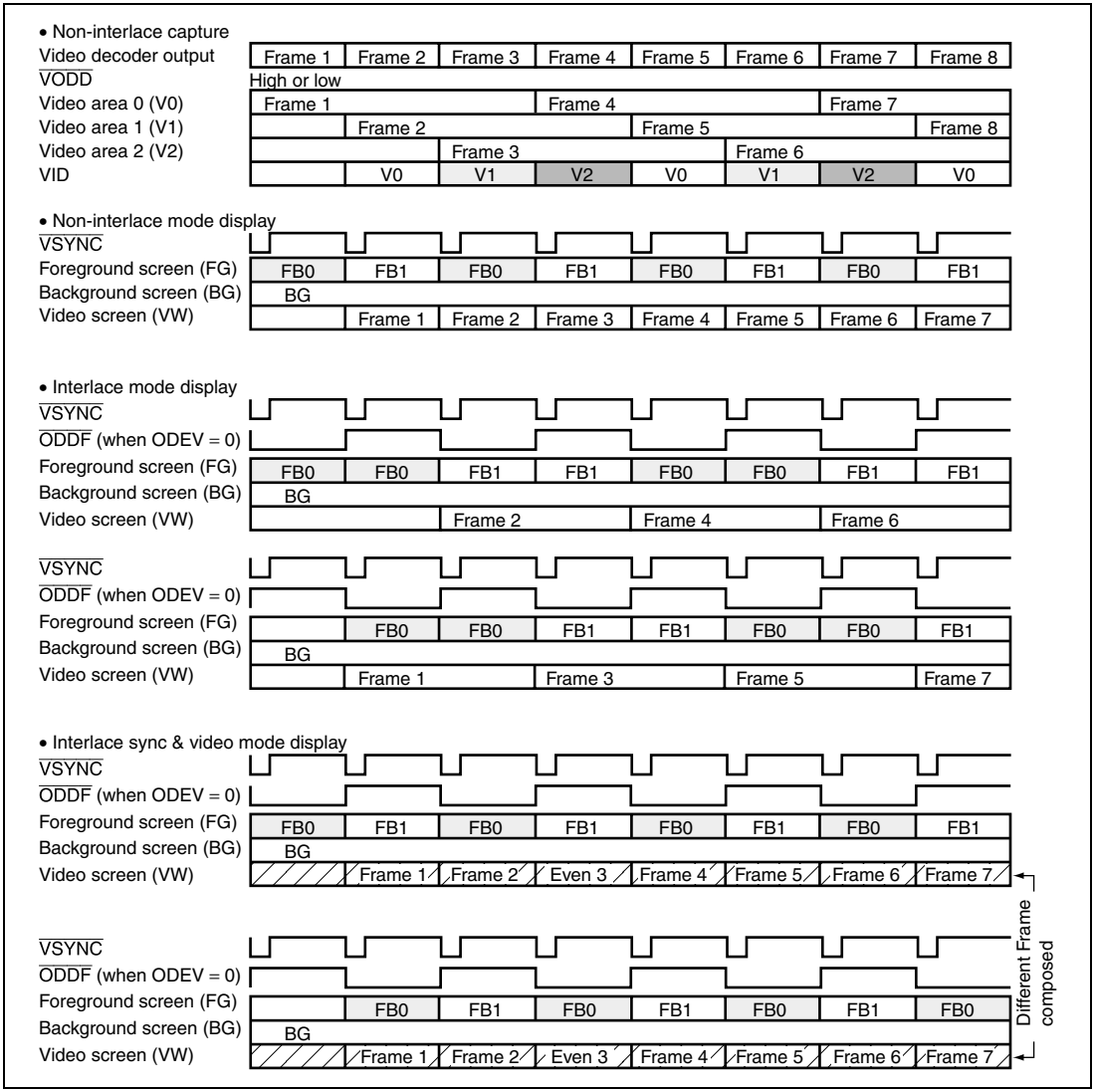


Figure 3.70 The Display of Data Captured in Interlace Mode and Display

(2) Display of Data Captured in Interlace Composite Mode

Interlace composite mode is used when the video decoder outputs in interlace 2 format. In this capture mode, a frame of video data is displayed every 2 VC, and the data is composed at the UGM area. Capture in this mode is compatible with non-interlace and interlace mode. However, in interlace sync & video display mode, a frame may be incorrectly composed (e.g., the ODD data for V0 is combined with the EVEN data of V1) if the start of the capture operation does not match the start of the frame. If synchronization of the display of data with the timing of the data being captured is left to chance, there will be a 50% probability of the incorrect composition of the displayed frames.

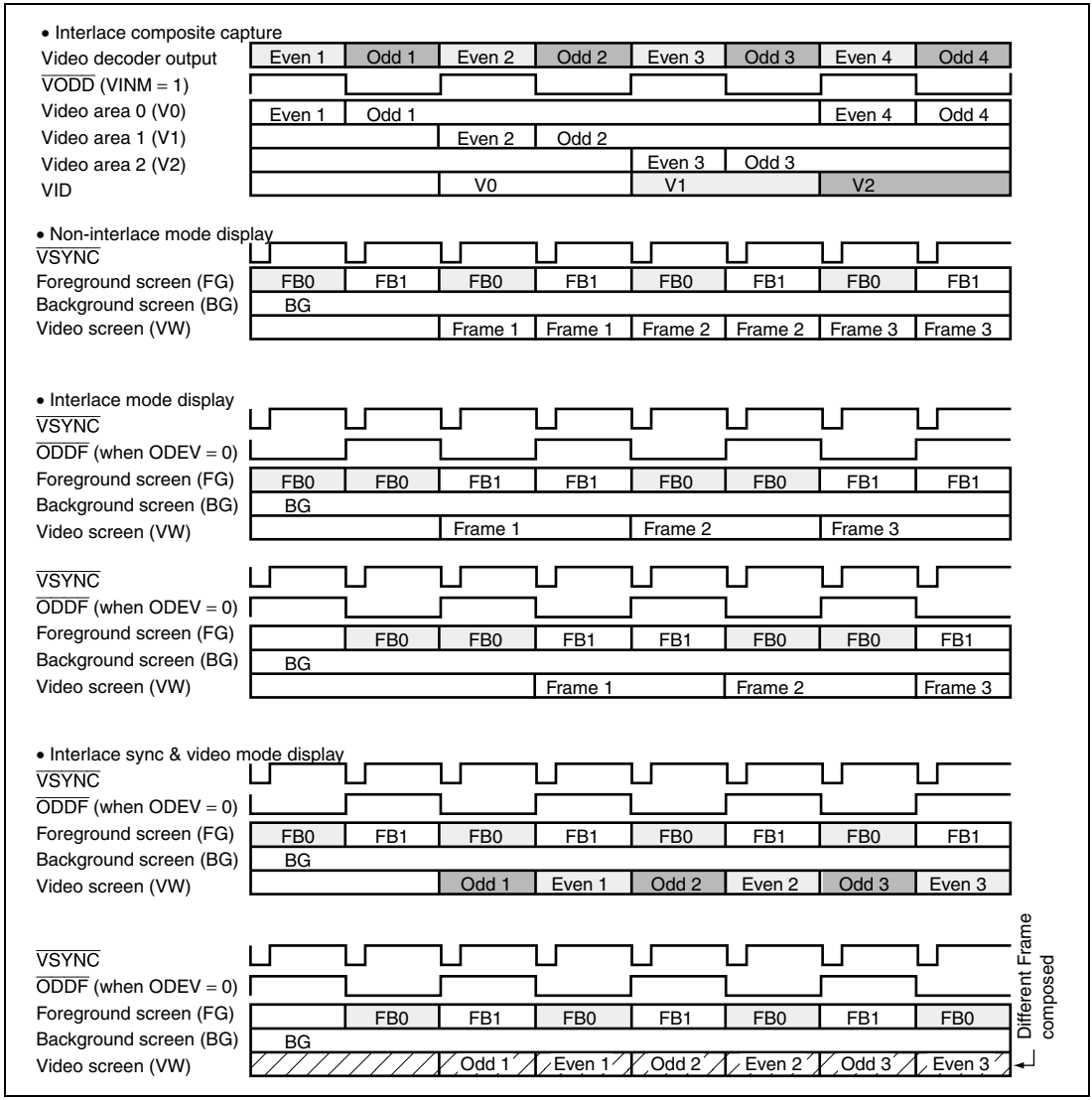


Figure 3.71 The Display of Data Captured in the Interlace Composite Mode

(3) Display of Data Captured in Interlace Odd-Only Mode

Interlace odd-only mode is used when the video decoder output in interlace format. In this capture mode, only the odd-field video data is captured for display. This mode is compatible with the non-interlace and interlace modes. However, in the interlace sync & video display mode, a frame may be incorrectly composed (e.g., the ODD data for V0 is combined with the EVEN data of V1) if the start of the capture operation does not match the start of the frame. If synchronization of the display of data with the timing of the data being captured is left to chance, there will be a 50% probability of the incorrect composition of the displayed frames.

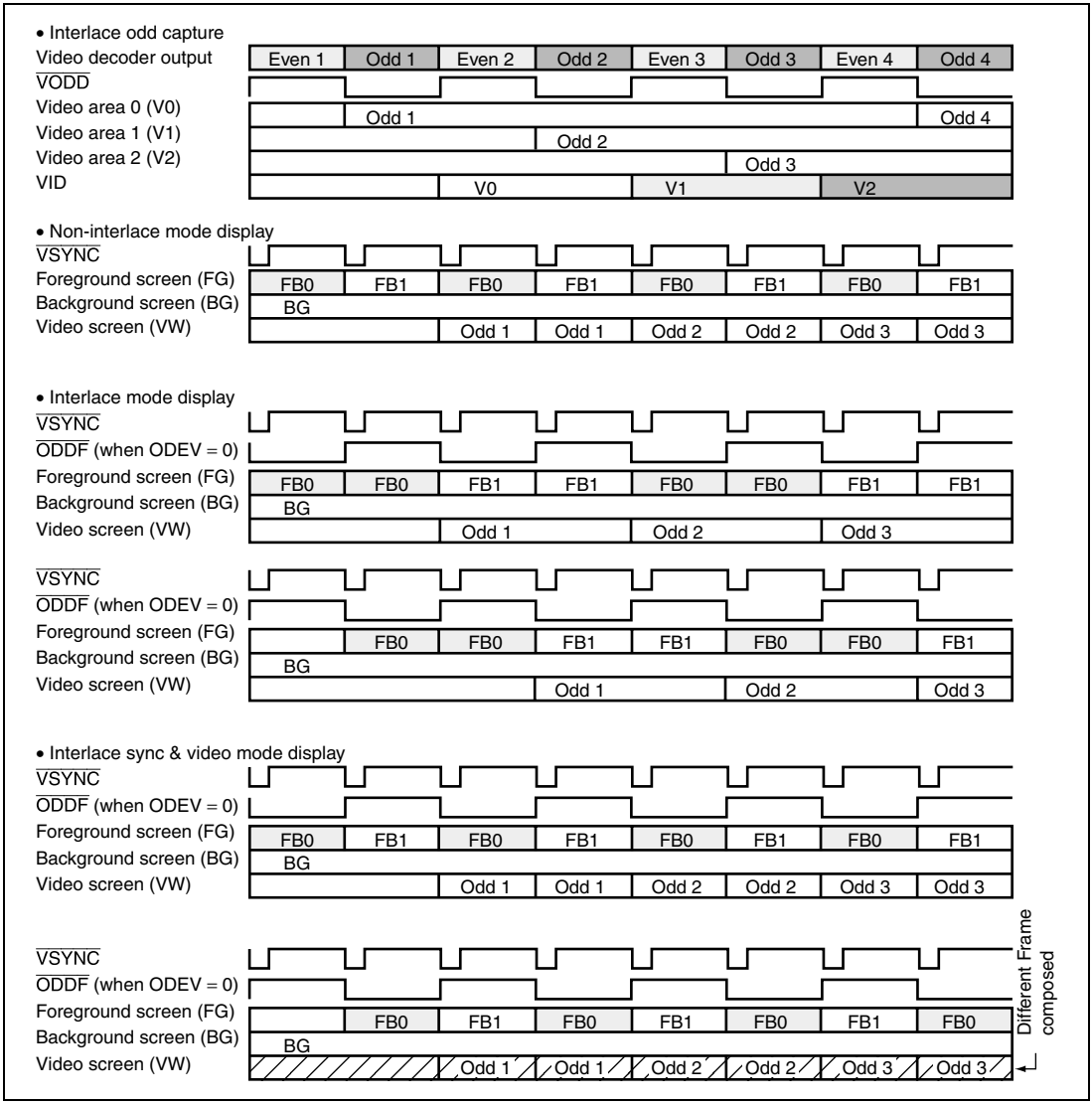


Figure 3.72 The Display of Data Captured in the Interlace Odd-Only Mode

(4) Display of Data Captured in Interlace Even-Only Mode

Interlace even-only mode is used when the video decoder output in interlace format. In this capture mode, display of video data is completed only by the data of the even field. This mode is compatible with the non-interlace and interlace mode. However, in the interlace sync & video display mode, a frame may be incorrectly composed (e.g., the ODD data for V0 is combined with the EVEN data of V1) if the start of the capture operation does not match the start of the frame. If synchronization of the display of data with the timing of the data being captured is left to chance, there will be a 50% probability of the incorrect composition of the displayed frames.

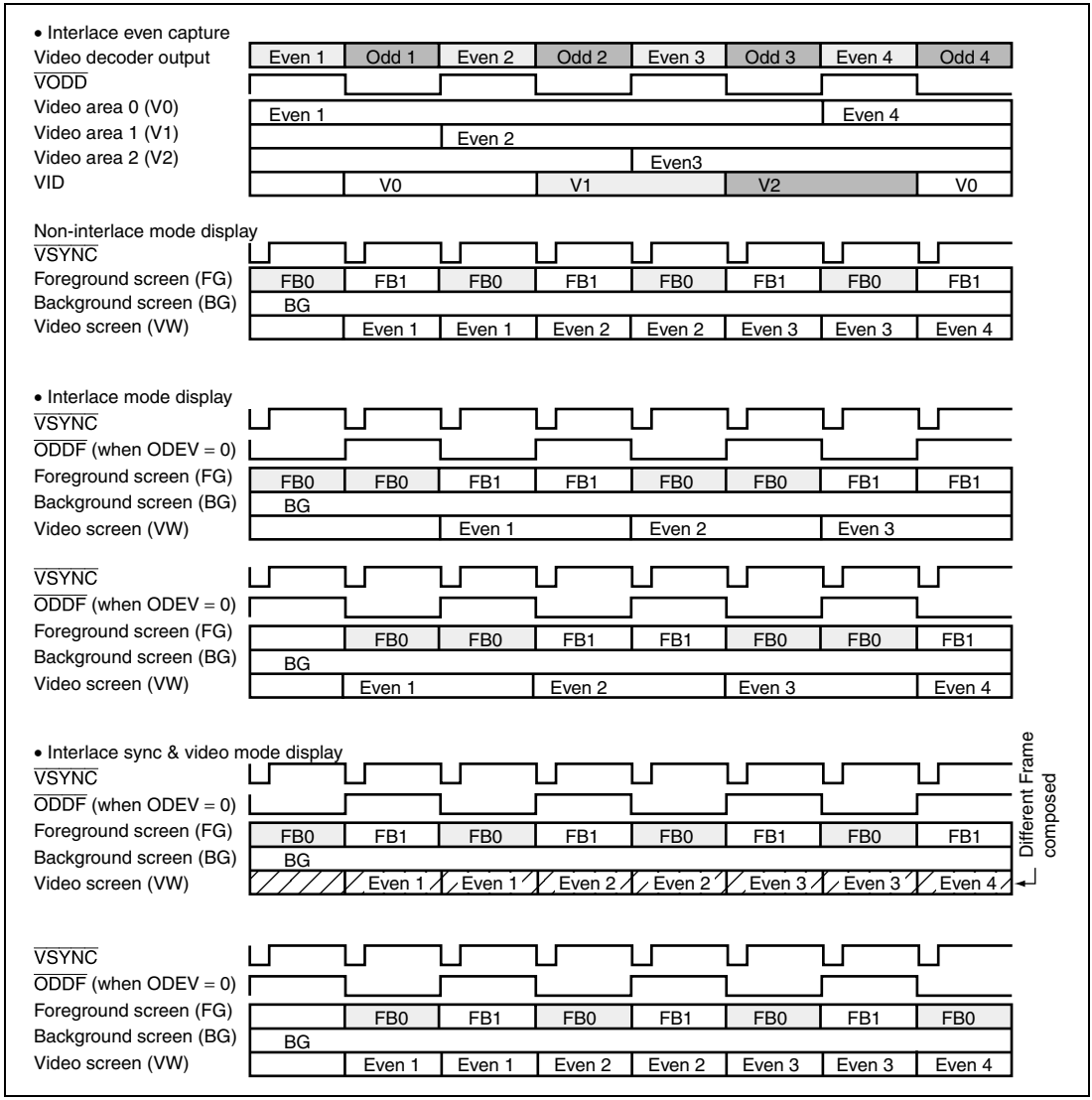


Figure 3.73 The Display of Data Captured in the Interlace Even-Only Mode

(5) Selecting the Display Mode

The result of analysis of compatibility between the video capture mode and Q2SD display mode are given in table 3.13. The entries A in the table indicate combinations that are recommended without reservation. The entries B in the table indicate that a sufficient resolution may be obtained by setting the output of the video decoder to non-interlace mode. However, if this mode is used in interlace mode, the vertical size of the captured image is ½ that of the original (i.e., the resolution of the image is halved).

The entries C in the table indicate that the smoothness of the sequence of images will be disrupted (frames will be missing), or different frame composition (blurring or overlap when the shot changes frame to frame) occurs.

Table 3.12 Selecting Modes of Video Capture and Display for the Q2SD

	Non-interlace Display Mode		Interlace Sync Display Mode		Interlace Sync & Video Display Mode*[2]	
Non-interlace capture	B	When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size).	C	Missing frame occurs. When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size).	D	Different frames are composed. When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size).
Interlace composite capture	A	No problem (the display is the same as with interlace mode)	A	No problem	C	Different frames are composed.
Interlace odd capture	B	When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size).*[1]	B	When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size). *[1]	C	Different frames are composed. When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size).
Interlace even capture	B	When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size). *[1]	B	When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size). *[1]	C	Different frames are composed. When the output of the video decoder is set to interlace sync mode, pay attention to the display size (the display size is reduced to 1/2 that of the source size).

Notes: 1. When the video decoder is placed in the non-interlace mode, the corresponding mode cannot be used if the FIELD signal is output.

2. The frame is changed field by field (1/60 sec) in Q2SD interlace sync & video display mode since the VID of the video screen is checked for each field. The data which belongs to a single screen when captured is not divided into odd and even fields when displayed. After only a half of captured data has been displayed, the next captured data starts to be displayed.

   Therefore, the data in the Y direction are halved when the data is captured in interlace, interlace odd-only, or interlace even-only mode in which a frame consists of two-field. If the data captured in this way is displayed on a monitor in non-interlace mode, the screen is halved in the Y direction, and if the data captured is displayed on a TV in interlace mode, the screen on which an even field and an odd field for different frames are composed is displayed.

   When the video data for one frame is captured over 1/30 s in the interlaced-composite capture mode but the first field to be captured is the second in the pair of fields, the timing of the captured data will be incorrect when it is displayed. This may lead to the composite display of data for different frames. To avoid this, enter the external synchronization mode and the video capture signals (the vertical sync input (VVS), horizontal sync input (VHS), and field (VODD) signals) are input to the EXVSYNC, EXHSYNC, and ODDF pins for synchronization.

Table 4.1 Command List

Type	Command Name	Function
Four-vertex screen drawing	POLYGON4A	Performs any four-vertex drawing at rendering coordinates while referencing a multi-valued (8- or 16-bit/pixel) source.
	POLYGON4B	Performs any four-vertex drawing at rendering coordinates while referencing a binary (1-bit/pixel) source.
	POLYGON4C	Performs any four-vertex drawing at rendering coordinates with a monochrome specification.
Line drawing	LINE	Draws a solid line 1 to 5 bits in width at rendering coordinates.
	RLINE	Draws a solid line 1 to 5 bits in width at rendering coordinates.
	PLINE	Draws a polygonal line at rendering coordinates while referencing a binary source.
	RPLINE	Draws a polygonal line at rendering coordinates while referencing a binary source.
Work screen drawing command	FTRAP	Draws a polygon at work coordinates.
	RFTRAP	Draws a polygon at work coordinates.
	CLRW	Zeroizes the work coordinates.
Work line drawing	LINEW	Draws a 1-bit-wide solid line at work coordinates.
	RLINEW	Draws a 1-bit-wide solid line at work coordinates.
Register setting commands	MOVE	Sets the current pointer.
	RMOVE	Sets the current pointer.
	LCOFS	Sets the local offset.
	RLCOFS	Sets the local offset.
	SCLIP	Sets the system clipping area.
	UCLIP	Sets the user clipping area.
	WPR	Sets a value in a specific address-mapped register.
Sequence control commands	JUMP	Changes the display list fetch destination.
	GOSUB	Makes a subroutine call for the display list.
	RET	Returns from a subroutine call made by the GOSUB command.
	NOP3	Executes no operation.
	VBKEM	Performs synchronization with the frame change timing.
	TRAP	Informs the Q2SD of the end of the display list.

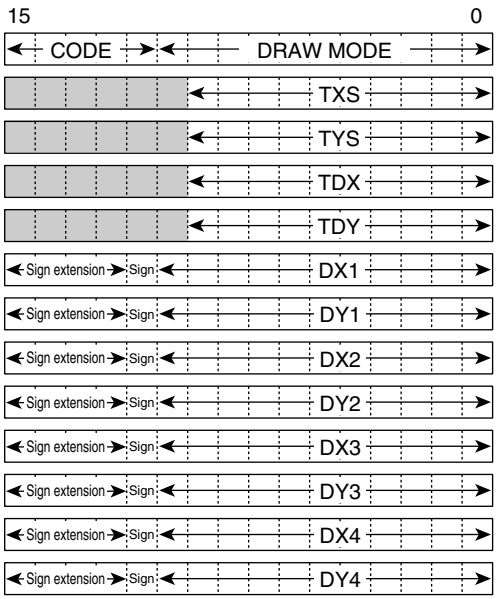
4.1 Four-Vertex Screen Drawing

4.1.1 POLYGON4A

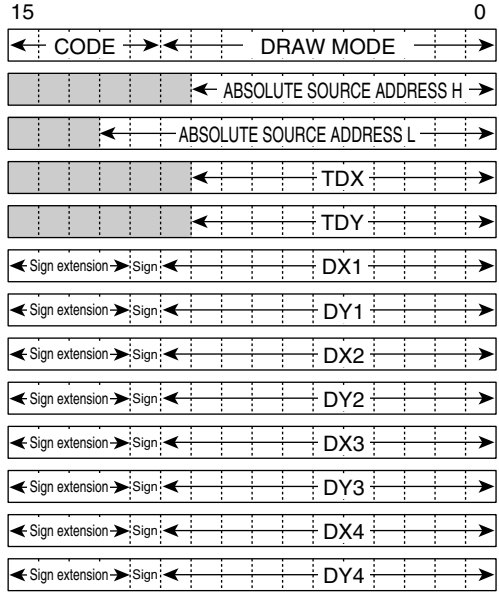
Function

Performs any four-vertex drawing at rendering coordinates while referencing a multi-valued (8- or 16-bit/pixel) source.

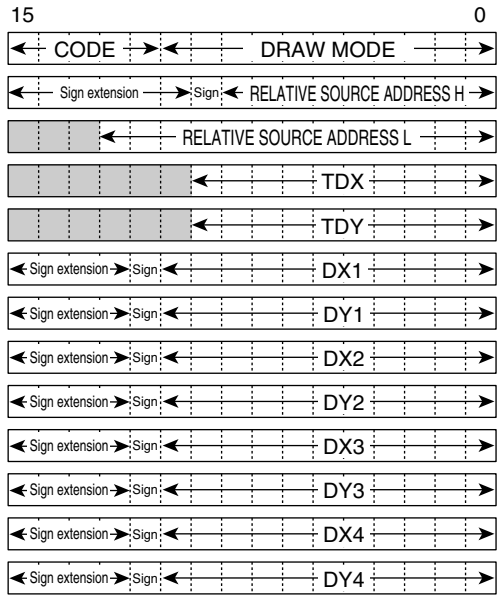
Command Format LNi = 0



LNi = 1, REL = 0



LNi = 1, REL = 1



1. Code

   B'00000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
O		A		O	

DRAW MODE										
Reserved	TRNS	STYL	CLIP	REL	NET	EOS	FST	LNi	COOF	WORK
Fixed at 0	*	*	O	Z	*	*	O	*	O	*

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   TXS, TYS: Source starting point

   ABSOLUTE/RELATIVE SOURCE ADDRESS H: Source start upper address (byte address)

   ABSOLUTE/RELATIVE SOURCE ADDRESS L: Source start lower address (byte address)

   TDX, TDY: Source size

   DXn, DYn (n = 1 to 4): Absolute values, rendering coordinates, negative numbers expressed as two's complement

Description

Transfers multi-valued (8- or 16-bit/pixel) source data to any quadrilateral rendering coordinates. The source is always scanned horizontally, but diagonal scanning may be used in the drawing, depending on the shape. In diagonally-scanned drawing, double-writing occurs to fill in gaps.

When LNi = 1, set a multiple of 8 pixels as the TDX value.

When LNi = 0, set 8 pixels or more as the TDX value.

If the TDX setting is less than 8 pixels, multi-valued source references will not be performed normally.

1. When repeated source referencing is selected as a rendering attribute (STYL = 1), the source is not enlarged or reduced, but is referenced repeatedly.
2. When work referencing is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
3. When LNi = 0, make TXS and TYS settings in pixel units.
4. When LNi = 1, the linear address space in the UGM can be used for multi-valued source coordinates. See section 3.3.3 (4) multi-valued source coordinates.

   When LNi = 1, set the upper bits of the source address in SOURCE ADDRESS H, and the lower bits in SOURCE ADDRESS L. When REL = 0, the source address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the UGM address at which the POLYGON4A command code is located. Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

   In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in the COLOR register to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit must be cleared to 0.

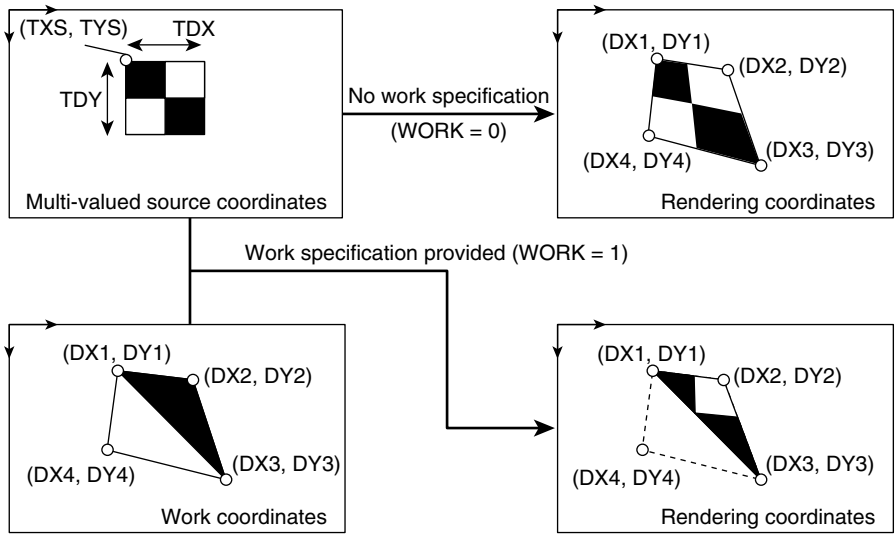
Note on FST Mode

When the register attribute FST bit is set to 1, processing is carried out in 4-pixel units. However, operation will be executed normally only if all the following conditions are satisfied; in other cases, operation cannot be guaranteed. Evaluation of these conditions is not performed internally.

- Make settings so that the source and destination are rectangles of the same size, with DX1 = DX4 = 4j – 4, DX2 = DX3 = 4k – 1, DY1 = DY2, DY3 = DY4, DX2 – DX1 = 32n – 1 (where j, k, and n are natural numbers).
- When FST = 1, no other rendering attributes except CLIP can be used.

- When this command is used with FST = 1, first use the MOVE, RMOVE, LCOFS, or RLCOFS command to change the clipping range and local offset values to the values given in the descriptions of the individual commands.
- Set a multiple of 4 for TXS and TYS.
- Operation is valid in 8-bit/pixel and 16-bit/pixel modes.
- The local offset values set by the LCOFS and RLCOFS commands must be non-negative.

Example

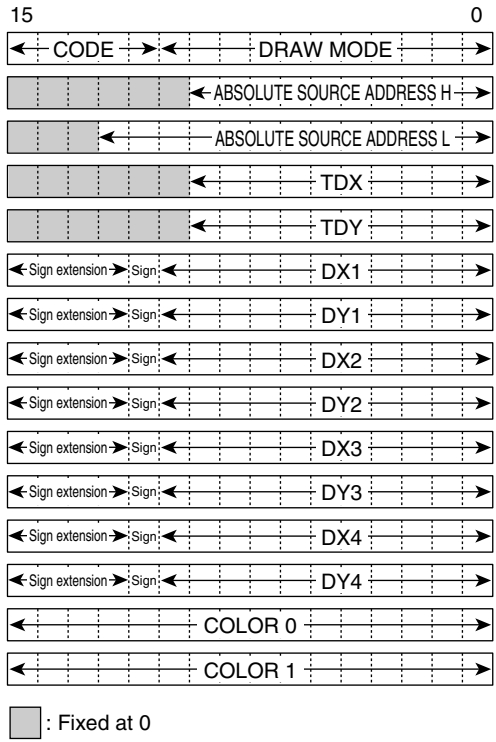


4.1.2 POLYGON4B

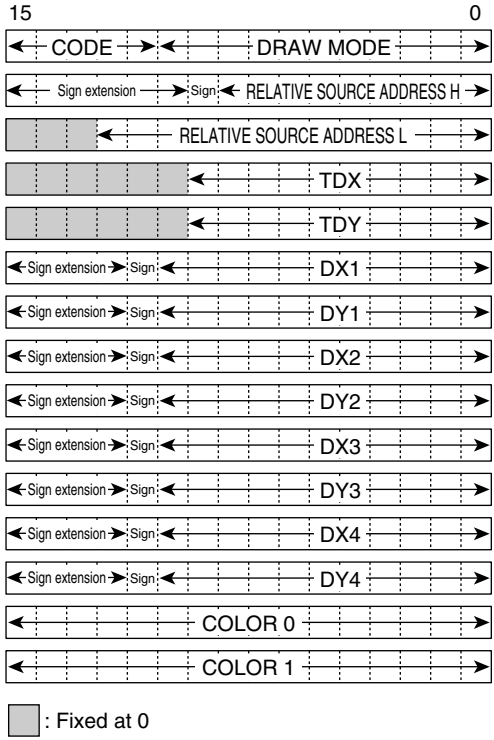
Function

Performs any four-vertex drawing at rendering coordinates while referencing a binary (1-bit/pixel) source.

Command Format REL = 0



REL = 1


15
0
CODE
DRAW MODE
Sign extension
Sign
RELATIVE SOURCE ADDRESS H
RELATIVE SOURCE ADDRESS L
TDX
TDY
Sign extension
Sign
DX1
DY1
DX2
DY2
DX3
DY3
DX4
DY4
COLOR 0
COLOR 1
: Fixed at 0

1. Code

   B'00001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
	O	A		O	

DRAW MODE										
Reserved	TRNS	STYL	CLIP	REL	NET	EOS	Reserved	Reserved	HALF	WORK
Fixed at 0	O	O*	O	O	O	O	Fixed at 0	Fixed at 0	O*	O

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

Note: * The STYL bit and HALF bit cannot both be set to 1 at the same time.

3. Command Parameters

   ABSOLUTE/RELATIVE SOURCE ADDRESS H: 1-bit/pixel source start upper address (byte address)

   ABSOLUTE/RELATIVE SOURCE ADDRESS L: 1-bit/pixel source start lower address (byte address)

   TDX, TDY: Source size

   DXn, DYn (n = 1 to 4): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   COLOR0, COLOR1: 8- or 16-bit/pixel color specifications

Description

Draws binary (1-bit/pixel) source data in any quadrilateral rendering area, using the colors specified by parameters COLOR0 and COLOR1. For the COLOR0 and COLOR1 data formats, see section 3.2.9, Input Color Data Configuration. The source is always scanned horizontally, but diagonal scanning may be used in the drawing, depending on the shape. In diagonally-scanned drawing, double-writing occurs to fill in gaps.

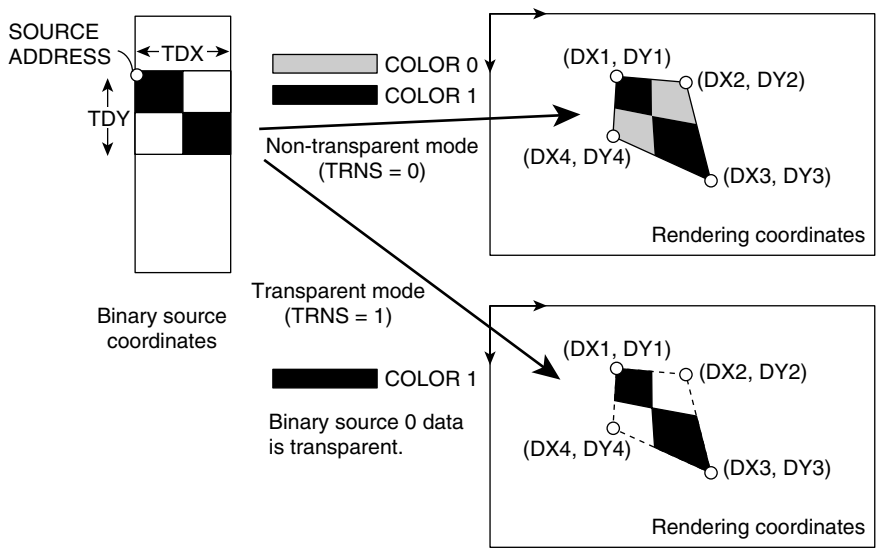
A multiple of 8 pixels must be set as the TDX value.

1. When repeated source referencing is selected as a rendering attribute (STYL = 1), the source is not enlarged or reduced, but is referenced repeatedly.
2. When work referencing is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.

Binary source data is located in an area in the UGM. When REL = 0, the source address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the UGM address at which the POLYGON4B command code is located.

Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

Example

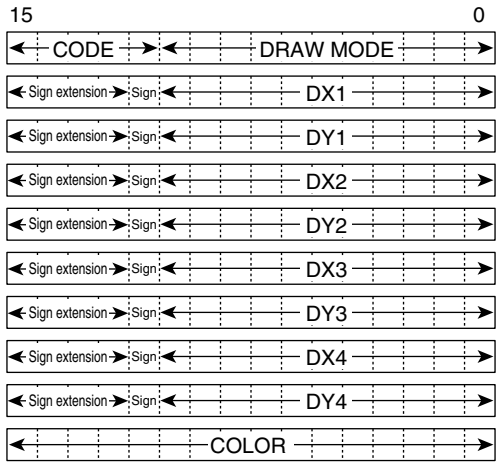


4.1.3 POLYGON4C

Function

Performs any four-vertex drawing at rendering coordinates with a monochrome specification.

Command Format



1. Code

   B'00010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
		A	O	O	

DRAW MODE										
Reserved			CLIP	Reserved	NET	EOS	FST	Reserved		WORK
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	*	*	O	Fixed at 0	Fixed at 0	*

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   DXn, DYn (n = 1 to 4): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   COLOR: 8- or 16-bit/pixel color specification

Description

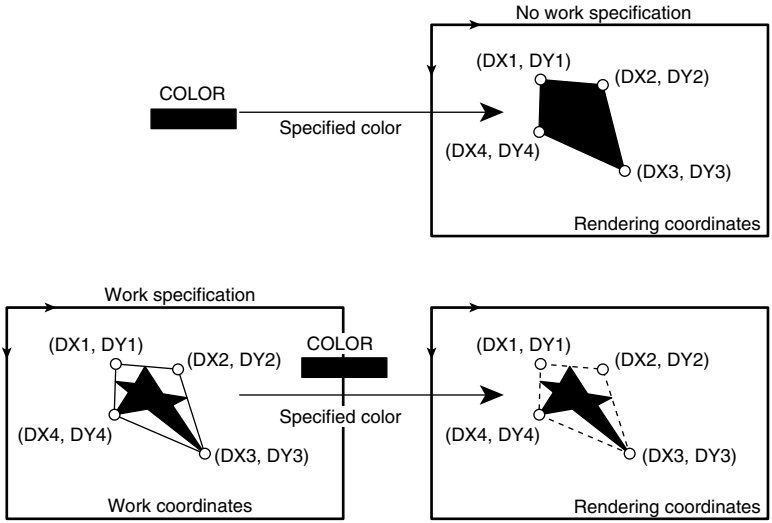
Draws any quadrilateral in the rendering area in the single color specified by the COLOR parameter. For the COLOR data format, see section 3.2.9, Input Color Data Format Configuration.

When work referencing is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.

When the register attribute FST bit is set to 1, processing is carried out in 4-pixel units. However, operation will be executed normally only if all the following conditions are satisfied; in other cases, operation cannot be guaranteed. Evaluation of these conditions is not performed internally.

- Make settings so that the source and destination are rectangles of the same size, with DX1 = DX4 = 4j – 4, DX2 = DX3 = 4k – 1, DY1 = DY2, DY3 = DY4, DX2 – DX1 = 32n – 1 (where j, k, and n are natural numbers).
- When FST = 1, no other rendering attributes except CLIP can be used.
- When this command is used with FST = 1, first use the MOVE, RMOVE, LCOFS, or RLCOFS command to change the clipping range and local offset values to the values given in the descriptions of the individual commands.
- Operation is valid in 8-bit/pixel and 16-bit/pixel modes. In 8-bit/pixel mode, set the same 8-bit data for the upper and lower color attribute values.
- The local offset values set by the LCOFS and RLCOFS commands must be non-negative.

Example


No work specification
(DX1, DY1)
(DX2, DY2)
COLOR
Specified color
(DX4, DY4)
(DX3, DY3)
Rendering coordinates
Work specification
(DX1, DY1)
(DX2, DY2)
COLOR
Specified color
(DX4, DY4)
(DX3, DY3)
Work coordinates
(DX1, DY1)
(DX2, DY2)
(DX4, DY4)
(DX3, DY3)
Rendering coordinates

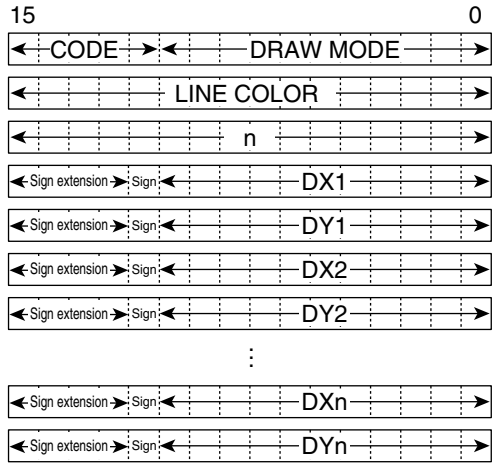
4.2 Line Drawing

4.2.1 LINE

Function

Draws a solid line 1 to 5 bits in width at rendering coordinates.

Command Format



1. Code
   B'01100

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			O	O	

DRAW MODE									
Reserved			CLIP	Reserved	NET	EOS	FWUL	W2UL	FWDR	W2DR
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	O	O	0000 to 1111			

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters

   LINE COLOR: 8- or 16-bit/pixel color specification

   n (n = 2 to 65,535): Number of vertices

   DXn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   DYn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

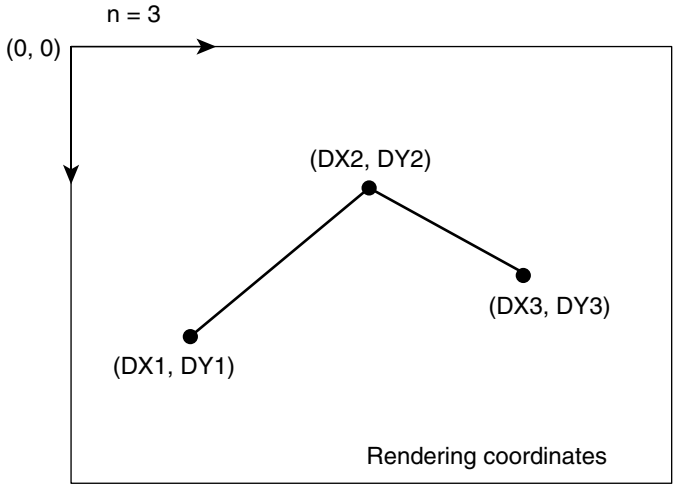
Description

Draws a polygonal line at rendering coordinates from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n – 1 (DXn – 1, DYn – 1), to vertex n (DXn, DYn), using the single color specified by parameter LINE COLOR.

For the LINE COLOR data format, see section 3.2.9, Input Color Data Configuration.

Note: 8-point drawing is used.

Example

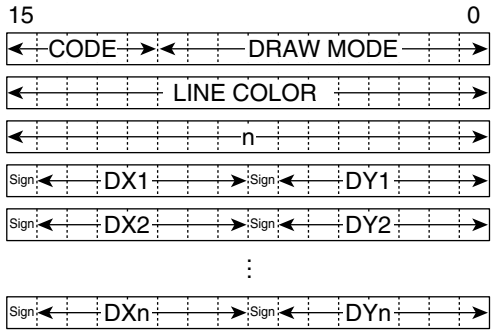


4.2.2 RLINE

Function

Draws a solid line 1 to 5 bits in width at rendering coordinates.

Command Format



1. Code
   B'01101

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			O	O	

DRAW MODE									
Reserved			CLIP	Reserved	NET	EOS	FWUL	W2UL	FWDR	W2DR
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	O	O	0000 to 1111			

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   LINE COLOR: 8- or 16-bit/pixel color specification

n (n = 1 to 65,535): Number of vertices

DXn, DYn (n = 1 to 65,535): Relative values, rendering coordinates, negative numbers expressed as two's complement

Description

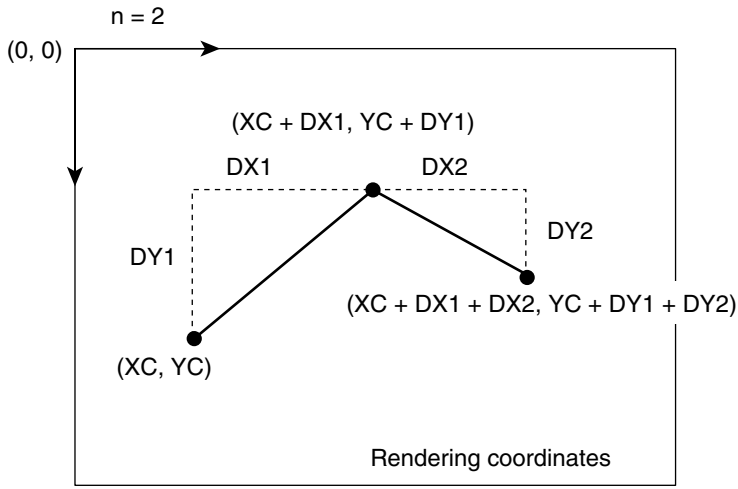
Draws, at rendering coordinates, a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn – 1 + DXn, YC + ... + DYn – 1 + DYn) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC), using the single color specified by parameter LINE COLOR.

For the LINE COLOR data format, see section 3.2.9, Input Color Data Format Configuration.

The final coordinate point is stored as the current pointer values (XC, YC).

Note: 8-point drawing is used.

Example

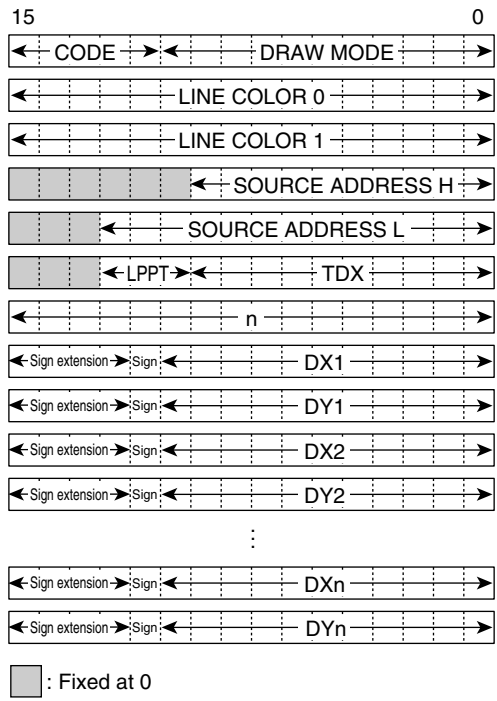


4.2.3 PLINE

Function

Draws a polygonal line at rendering coordinates while referencing a binary source.

Command Format



1. Code

   B'01110

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
	O			O	

DRAW MODE										
Reserved	TRNS	Reserved	CLIP	Reserved	NET	EOS	EDG2	Reserved	EDG1	Reserved
Fixed at 0	O	Fixed at 1	O	Fixed at 0	O	O	O	Fixed at 0	O	Fixed at 1

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   LINE COLOR0: 8- or 16-bit/pixel color specification

   LINE COLOR1: 8- or 16-bit/pixel color specification

   SOURCE ADDRESS H: 1-bit/pixel source start upper address (byte address)

   SOURCE ADDRESS L: 1-bit/pixel source start lower address (byte address)

   TDX: Source size

   LPPT: Line pattern pointer

   n (n = 2 to 65,535): Number of vertices

   DXn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   DYn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

Description

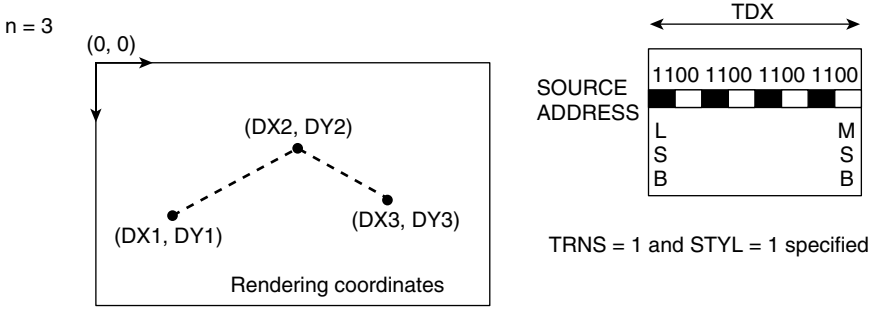
Draws a polygonal line from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n – 1 (DXn – 1, DYn – 1), to vertex n (DXn, DYn).

A multiple of 8 pixels must be set for the TDX value.

The reference start position of the binary source data can be adjusted by setting a value between 0 and 7 in the line pattern pointer. For example, if 0 is set, referencing starts at the beginning of the source data, while if 5 is set, referencing starts 5 pixels from the beginning of the source data. When STYL = 1, pattern repetition starts at the pixel after [source start position + TDX + LPPT – 1]. The source start address must be an even number.

Note: 4-point drawing is used.

Example

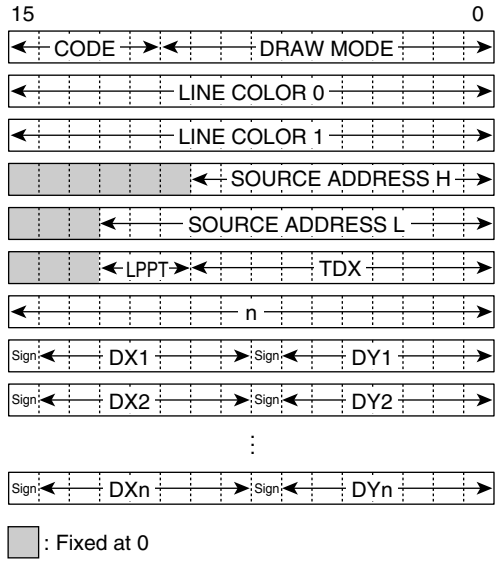


4.2.4 RPLINE

Function

Draws a polygonal line at rendering coordinates while referencing a binary source.

Command Format



1. Code

   B'01111

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
	O			O	

DRAW MODE										
Reserved	TRNS	Reserved	CLIP	Reserved	NET	EOS	EDG2	Reserved	EDG1	Reserved
Fixed at 0	O	Fixed at 1	O	Fixed at 0	O	O	O	Fixed at 0	O	Fixed at 1

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   LINE COLOR0: 8- or 16-bit/pixel color specification

   LINE COLOR1: 8- or 16-bit/pixel color specification

   SOURCE ADDRESS H: 1-bit/pixel source start upper address (byte address)

   SOURCE ADDRESS L: 1-bit/pixel source start lower address (byte address)

   LPPT: Line pattern pointer

   TDX: Source size

   n (n = 1 to 65,535): Number of vertices

   DXn, DYn (n = 1 to 65,535): Relative values, rendering coordinates, negative numbers expressed as two's complement

Description

Draws a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn –1 + DXn, YC + ... + DYn – 1 + DYn) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC).

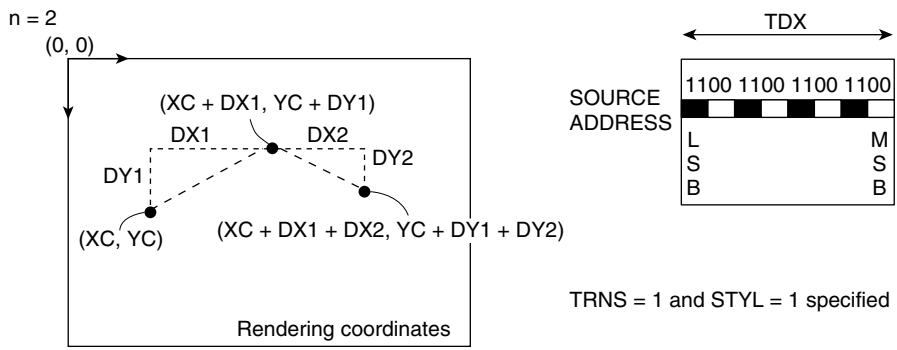
The final coordinate point is stored as the current pointer values (XC, YC).

A multiple of 8 pixels must be set for the TDX value.

The reference start position of the binary source data can be adjusted by setting a value between 0 and 7 in the line pattern pointer. For example, if 0 is set, referencing starts at the beginning of the source data, while if 5 is set, referencing starts 5 pixels from the beginning of the source data. When STYL = 1, pattern repetition starts at the pixel after [source start position + TDX + LPPT – 1]. The source start address must be an even number.

Note: 4-point drawing is used.

Example



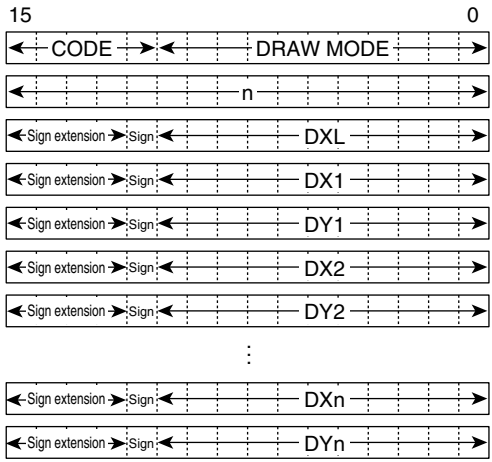
4.3 Work Screen Drawing Command

4.3.1 FTRAP

Function

Draws a polygon at work coordinates.

Command Format



1. Code
   B'01000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
					O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	EDG	Reserved		
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	B	O	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

B: Referenced depending on mode (valid when EDG = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   n (n = 2 to 65,535): Number of vertices

   DXL: Left-hand side coordinate

   DXn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

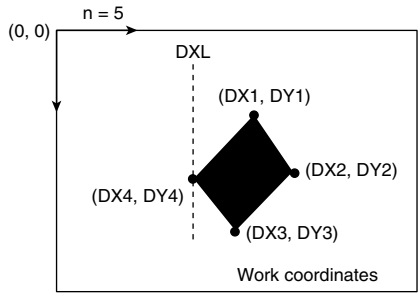
   DYn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

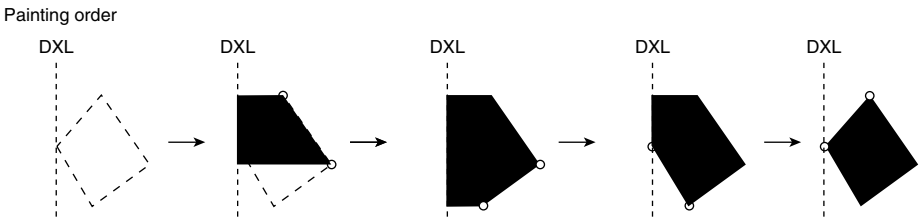
Description

Draws a polygon with n-1 vertices at work coordinates. Paints n-1 trapezoids at work coordinates using binary EOR, with X = DXL as the left-hand side, and line segments (DX1, DY1) – (DX2, DY2), (DX2, DY2) – (DX3, DY3), ..., (DXn-1, DYn-1) – (DXn, DYn) as the right-hand sides, and with top and bottom bases parallel to the X-axis. Bottom base drawing is not performed. Set the minimum value of DX1 to DXn as DXL.

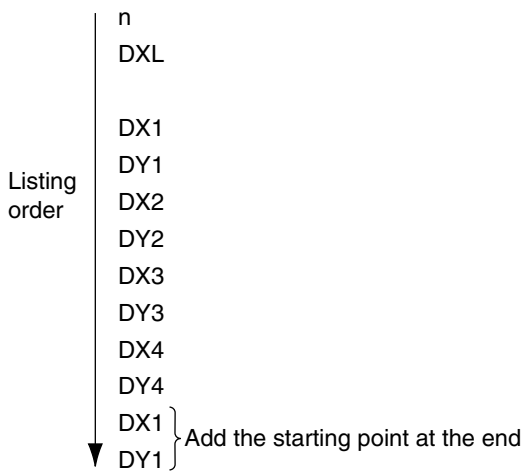
If the draw mode EDG bit is set to 1, an edge line is drawn after the paint operation. The line drawing data is selected with the EOS bit. When setting the EDG bit to 1, set (DXN, DYN) = (DX1, DY1) to give a closed figure.

Example





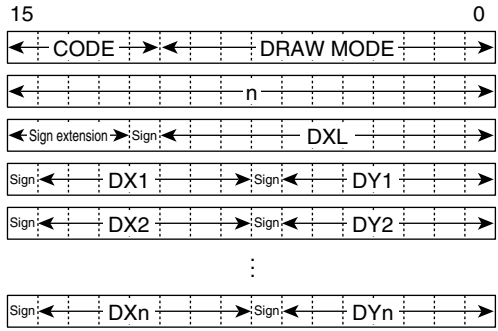
Order of Listing FTRAP Parameters



4.3.2 RFTRAP

Draws a polygon at work coordinates.

Command Format



1. Code
   B'01001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
					O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	EDG	Reserved		
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	B	O	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
B: Referenced depending on mode (valid when EDG = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   n (n = 1 to 65,535): Number of vertices

DXL: Left-hand side coordinate, work coordinate, negative number expressed as two's complement

DXn, DYn (n = 1 to 65,535): Relative values, work coordinates, negative numbers expressed as two's complement

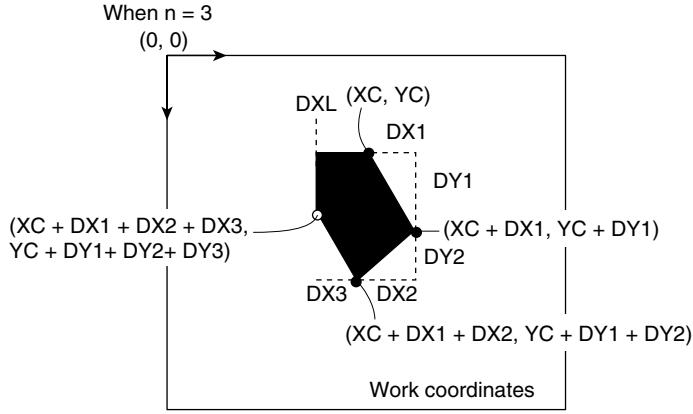
Description

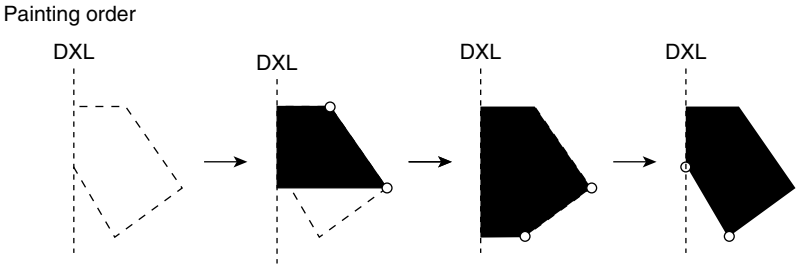
Paints n trapezoids at work coordinates using binary EOR, with X = DXL as the left-hand side, and line segments specified by the relative shift (DX, DY) from the current pointer values (XC, YC) ((XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn –1 + DXn, YC + ... + DYn – 1 + DYn)) as the right-hand sides, and with top and bottom bases parallel to the X-axis. Bottom base drawing is not performed.

The final coordinate point is stored as the current pointer values (XC, YC).

If the draw mode EDG bit is set to 1, an edge line is drawn after the paint operation. The line drawing data is selected with the EOS bit. When setting the EDG bit to 1, set (DX1 + DX2 + ... + DXn = 0, DY1 + DY2 + ... + DYn = 0) to give a closed figure.

Example


When n = 3
(0, 0)
DXL
(XC, YC)
DX1
DY1
(XC + DX1 + DX2 + DX3,
YC + DY1+ DY2+ DY3)
(XC + DX1, YC + DY1)
DY2
DX3
DX2
(XC + DX1 + DX2, YC + DY1 + DY2)
Work coordinates

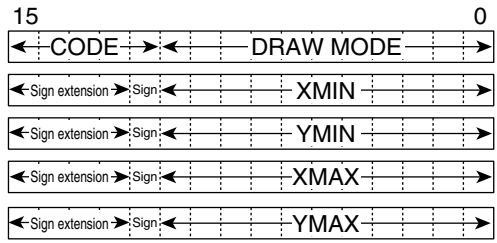

Painting order
DXL
DXL
DXL
DXL

4.3.3 CLRW

Function

Zeroizes the work coordinates.

Command Format



1. Code
   B'10100

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
					O

DRAW MODE										
Reserved			CLIP	Reserved						
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters

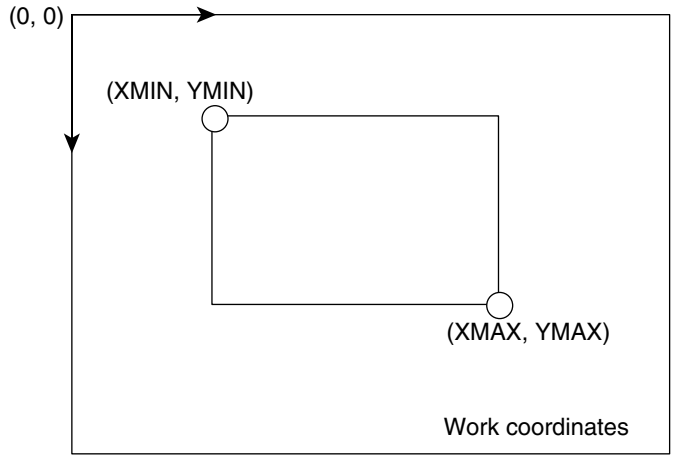
   XMIN, XMAX: Left and right X coordinate values, work coordinates, negative numbers expressed as two's complement

   YMIN, YMAX: Upper and lower Y coordinate values, work coordinates, negative numbers expressed as two's complement

Description

Zero-clears the area specified by upper-left coordinates (XMIN, YMIN) and lower-right coordinates (XMAX, YMAX) in the work coordinate system.

Example



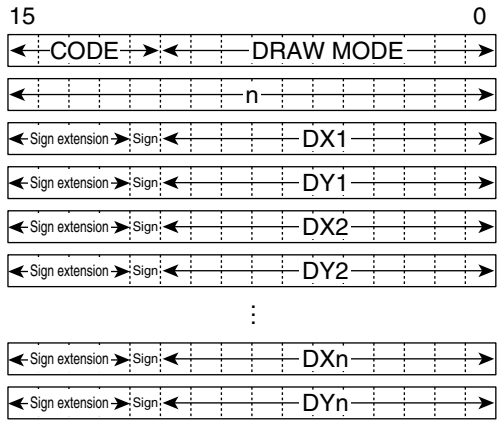
4.4 Work Line Drawing

4.4.1 LINEW

Function

Draws a 1-bit-wide solid line at work coordinates.

Command Format



1. Code
   B'01010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			V		O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	Reserved			
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   n (n = 2 to 65,535): Number of vertices

   DXn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

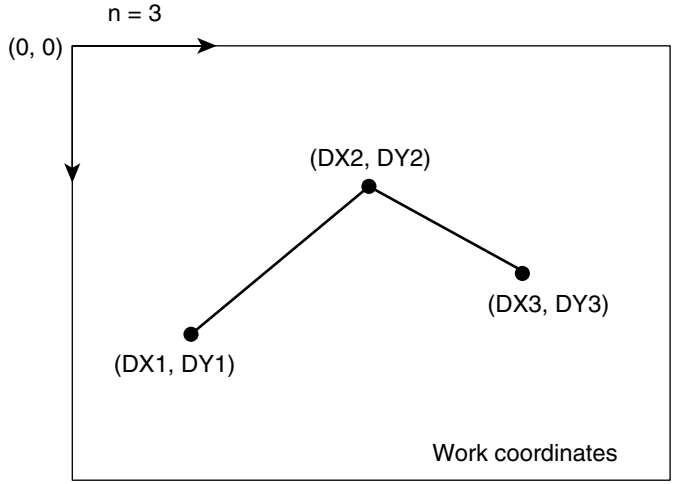
   DYn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

Description

Performs binary drawing at work coordinates of a polygonal line from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n – 1 (DXn – 1, DYn – 1), to vertex n (DXn, DYn). 0 drawing or 1 drawing is selected with the drawing mode EOS bit. Drawing is performed at work coordinates with 0 when EOS = 0, and at work coordinates with 1 when EOS = 1. (Used for border drawing at work coordinates for a polygonal painted figure.)

Note: 8-point drawing is used.

Example

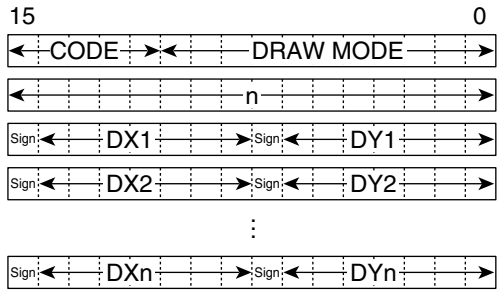

n = 3
(0, 0)
(DX2, DY2)
(DX3, DY3)
(DX1, DY1)
Work coordinates

4.4.2 RLINEW

Function

Draws a 1-bit-wide solid line at work coordinates.

Command Format



1. Code
   B'01011

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			V		O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	Reserved			
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   n (n = 1 to 65,535): Number of vertices

DXn, DYn (n = 1 to 65,535): Relative values, work coordinates, negative numbers expressed as two's complement

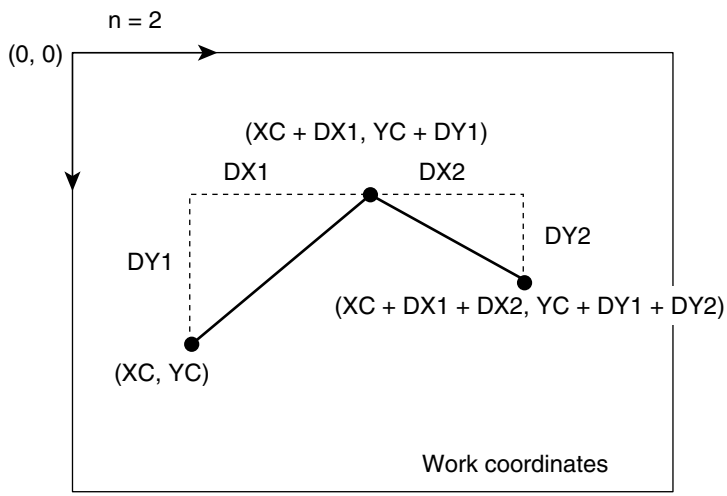
Description

Performs binary drawing at work coordinates of a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn –1 + DXn, YC + ... + DYn – 1 + DYn) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC). 0 drawing or 1 drawing is selected with the drawing mode EOS bit. Drawing is performed at work coordinates with 0 when EOS = 0, and at work coordinates with 1 when EOS = 1.

The final coordinate point is stored as the current pointer values (XC, YC). (Used for border drawing at work coordinates for a polygonal painted figure.)

Note: 8-point drawing is used.

Example



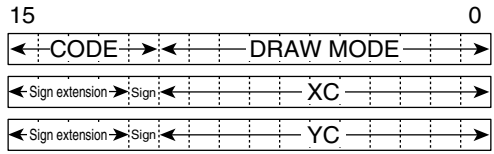
4.5 Register Setting Commands

4.5.1 MOVE

Function

Sets the current pointer.

Command Format



1. Code
   B'10000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

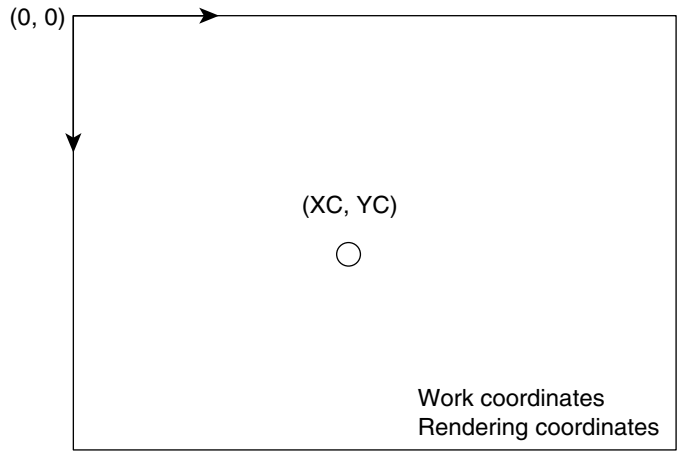
3. Command Parameters
   XC: Absolute value, rendering coordinate, work coordinate, negative number expressed as two's complement
   YC: Absolute value, rendering coordinate, work coordinate, negative number expressed as two's complement

Description

Sets the values obtained by adding the local offset values to XC and YC in the current pointers. XC and YC are set as absolute coordinates. The current pointers are used by relative drawing commands only.

After issuing a MOVE command, use relative drawing commands in succession. If an absolute drawing command is used during this sequence, the current pointers will be used as registers for internal computation, and the current pointer values will be lost. A MOVE command must be therefore be issued before using relative drawing commands again.

Example

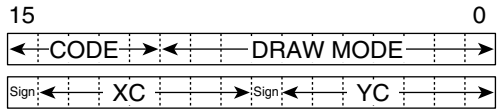


4.5.2 RMOVE

Function

Sets the current pointer.

Command Format



1. Code
   B'10001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

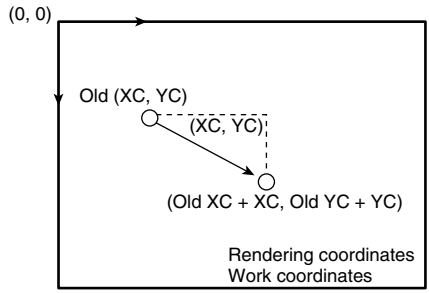
O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XC, YC: Relative values, rendering coordinates, work coordinates, negative numbers expressed as two's complement

Description

Adds XC and YC to the current pointers.

Example

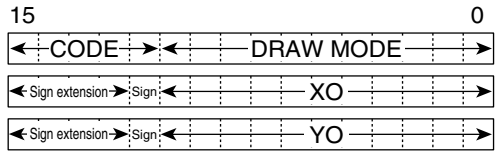


4.5.3 LCOFS

Function

Sets the local offset.

Command Format



1. Code
   B'10010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XO, YO: Local offset value absolute specifications, rendering coordinates, work coordinates, negative numbers expressed as two's complement

Description

Sets the local offset with absolute coordinates. After these settings are made, these offset values are added in all subsequent coordinate specifications.

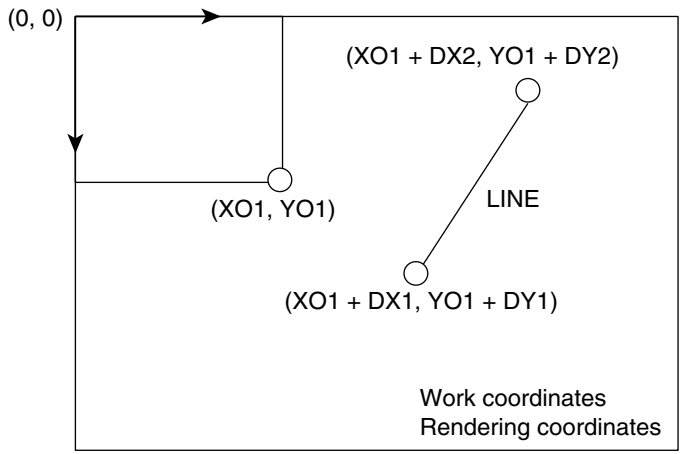
These settings must be made at the start of the display list (the initial values are undefined).

To reflect the local offset values in the current pointers, issue a MOVE command after the LCOFS command.

When using a command that employs the FST specification, a multiple of 4 must be set for the XO value.

Use non-negative values for both XO and YO.

Example

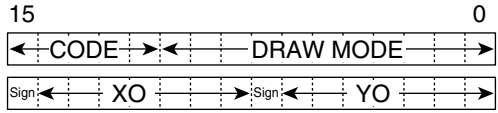


4.5.4 RLCOFS

Function

Sets the local offset.

Command Format



1. Code
   B'10011

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XO, YO: Local offset value relative specifications, rendering coordinates, work coordinates, negative numbers expressed as two's complement

Description

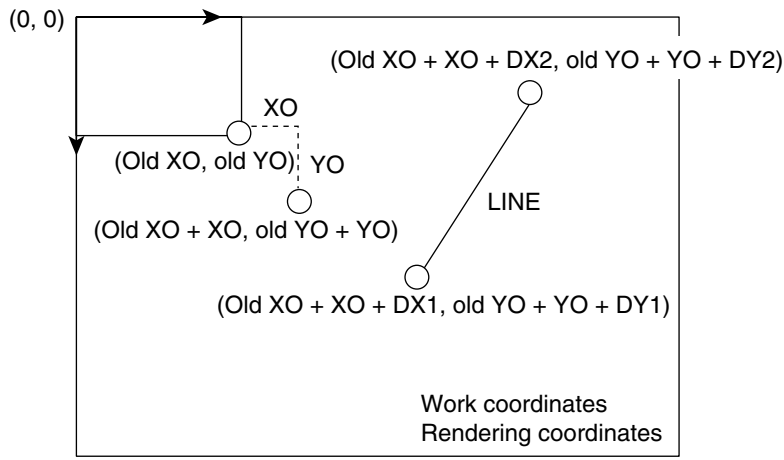
Adds XO and YO to the local offset. After these settings are made, these offset values are added in all subsequent coordinate specifications.

To reflect the local offset values in the current pointers, issue a MOVE command after setting the local offset with the LCOFS or RLCOFS command.

When using a command that employs the FST specification, the value obtained by adding XO to the local offset must be a multiple of 4.

The local offset values set by XO and YO must be non-negative.

Example

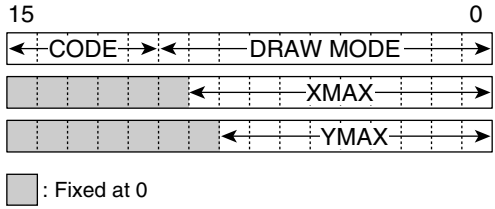


4.5.5 SCLIP

Function

Sets the system clipping area.

Command Format



1. Code
   B'10111

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XMAX: Left and right X coordinate values, rendering coordinates, work coordinates
   YMAX: Upper and lower Y coordinate values, rendering coordinates, work coordinates

Description

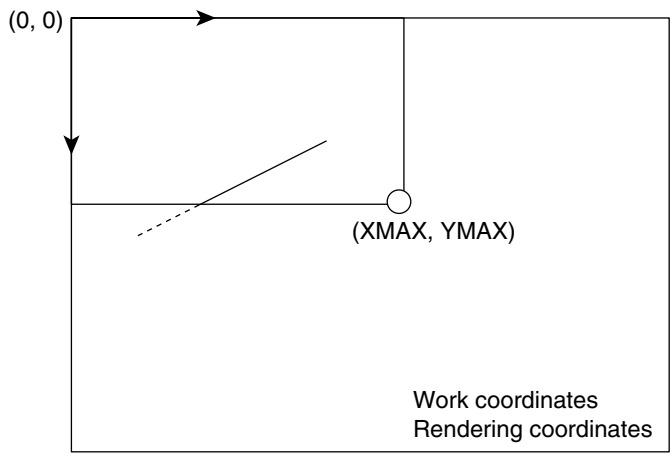
Designates the area specified by upper-left coordinates (0, 0) and lower-right coordinates (XMAX, YMAX) in the rendering coordinate and work coordinate systems as the system clipping area. The local offset values specified by the LCOFS or RLCOFS command are not added to the coordinates set by this command.

Set the maximum drawing range values for XMAX and YMAX. After powering on, the initial values of the clipping range are undefined. The clipping range must therefore be set with the SCLIP command at the start of the first display list executed.

For the set values given by this command, screen coordinates must be set as reference coordinates.

When using a command that employs the FST specification, set a multiple of 4 – 1 as the XMAX value.

Example

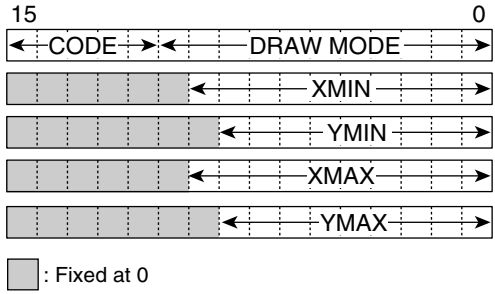


4.5.6 UCLIP

Function

Sets the user clipping area.

Command Format



1. Code
   B'10101

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XMIN, XMAX: Left and right X coordinate values, rendering coordinates, work coordinates

YMIN, YMAX: Upper and lower Y coordinate values, rendering coordinates, work coordinates

Description

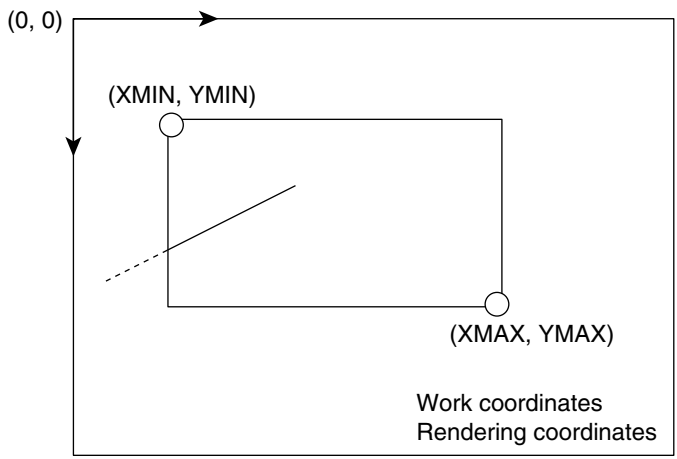
Designates the area specified by upper-left coordinates (XMIN, YMIN) and lower-right coordinates (XMAX, YMAX) in the rendering coordinate and work coordinate systems as a user clipping area. The local offset values specified by the LCOFS or RLCOFS command are not added to the coordinates set by this command.

When making these settings, ensure that XMIN < XMAX and YMIN < YMAX, and that the system clipping area is not exceeded.

This setting is valid when CLIP = 1.

When using a command that employs the FST specification, set a multiple of 4 as the XMIN value, and a multiple of 4 – 1 as the XMAX value.

Example

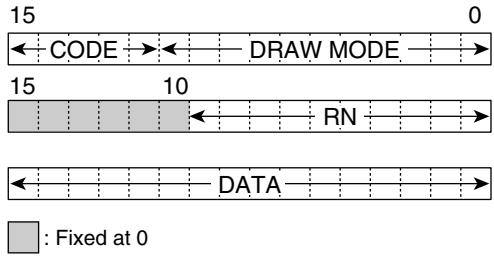


4.5.7 WPR

Function

Sets a value in a specific address-mapped register.

Command Format



1. Code
   B'10110

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   RN: Register number
   DATA: Data

Description

Writes data to the Q2SD's address-mapped registers. The register number is set in RN, and the write data in DATA.

When a write is performed to an address-mapped register with this command, select the location to ensure that the currently executing drawing processing is not adversely affected.

Also ensure that there is no conflict with access by the SuperH.

This command is intended primarily for performing the operations shown in (a) to (e).

(a) Change of display start address or drawing start address (RN = 00A, 00B, 04C)
(b) Change of multi-valued source or work start address (RN = 00E, 00F)
(c) Change of graphic bit mode (RN = 006)
(d) Return address setting when performing resumption processing after drawing suspension (RN = 04A, 04B)
(e) Change of drawing color offset value when performing drawing processing (RN = 04D)

The registers that can be written to are limited to those listed below. If a write is performed to another register, subsequent operation cannot be guaranteed.

Register No.	Register Address	Name
00A:	H′014	DSA0
00B:	H′016	DSA1
00E:	H′01C	SSAR
00F:	H′01E	WSAR
04C:	H′098	RSAR
006:	H′00C	REMR
04A:	H′094	RTNH
04B:	H′096	RTNL
04D:	H′09A	COLOR

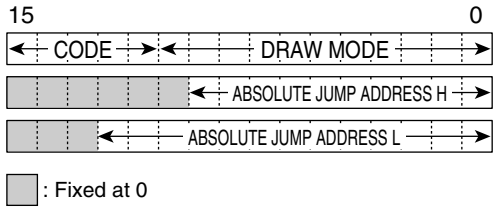
4.6 Sequence Control Commands

4.6.1 JUMP

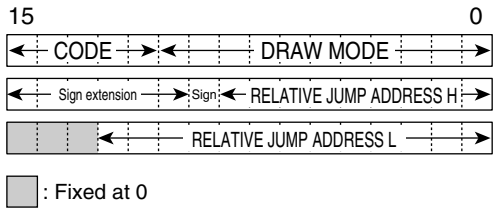
Function

Changes the display list fetch destination.

Command Format REL = 0



REL = 1



1. Code
   B'11000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved				REL	Reserved					
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters

   ABSOLUTE/RELATIVE JUMP ADDRESS H: Absolute/relative jump destination upper address (byte address)

   ABSOLUTE/RELATIVE JUMP ADDRESS L: Absolute/relative jump destination lower address (byte address)

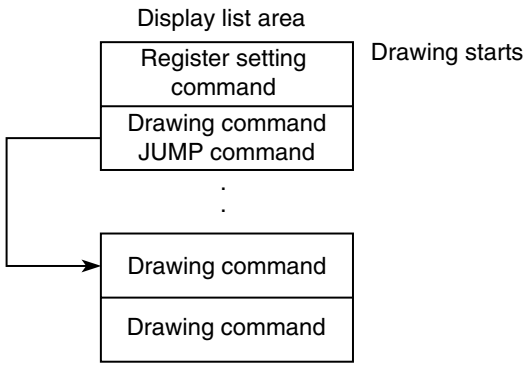
Description

Changes the display list fetch destination to the specified address.

When REL = 0, the jump destination address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the UGM address at which the command code is located.

Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

Example

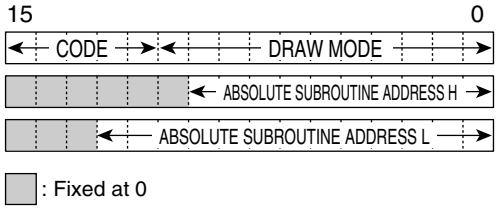


4.6.2 GOSUB

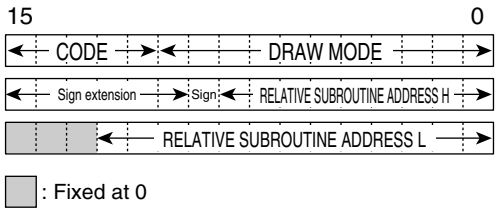
Function

Makes a subroutine call for the display list.

Command Format REL = 0



REL = 1



1. Code
   B'11001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved				REL	Reserved					
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters

   ABSOLUTE/RELATIVE SUBROUTINE ADDRESS H: Absolute/relative subroutine upper address (byte address)

   ABSOLUTE/RELATIVE SUBROUTINE ADDRESS L: Absolute/relative subroutine lower address (byte address)

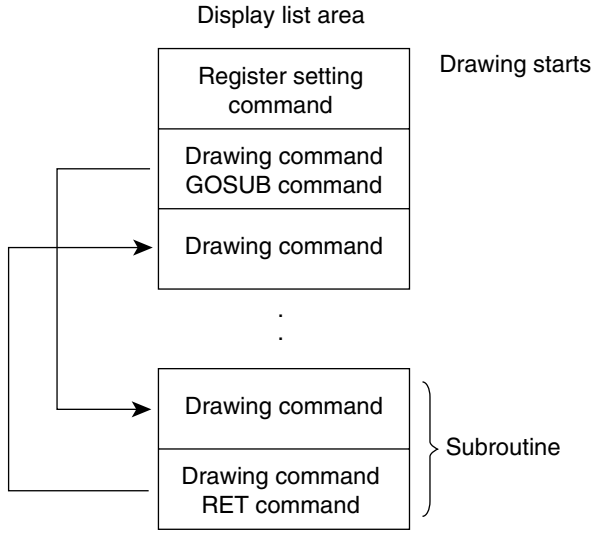
Description

Changes the display list fetch destination to the specified subroutine address. The fetch address is restored by an RET instruction. As only one level of nesting is permitted, it will not be possible to return if a subroutine call is issued within the subroutine.

When REL = 0, the subroutine destination address can be specified as an absolute address. When REL = 1, the address can be specified as a relative address with respect to the UGM address at which the command code is located.

Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

Example

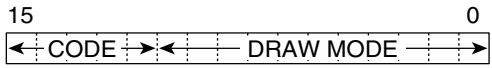

Display list area
Register setting command
Drawing starts
Drawing command GOSUB command
Drawing command
Drawing command
Drawing command RET command
Subroutine

4.6.3 RET

Function

Returns from a subroutine call made by the GOSUB command.

Command Format



1. Code
   B'11011

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

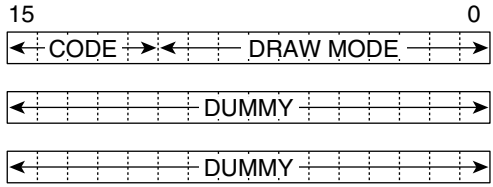
Restores the display list fetch destination to the address following the source of the subroutine call.

4.6.4 NOP3

Function

Executes no operation.

Command Format



1. Code
   B'11110

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

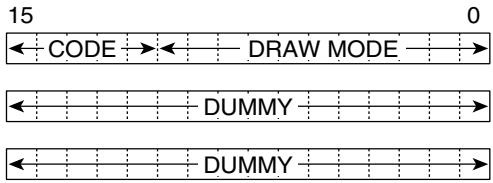
The NOP3 command does not perform any operation. This command, which consists of three words including the command code, simply fetches the next instruction without executing any processing.

4.6.5 VBKEM

Function

Performs synchronization with the frame change timing.

Command Format



1. Code
   B'11010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

When this command is executed, the drawing operation is kept waiting until the timing for a frame change. As soon as the frame change timing has elapsed, control passes to the next command. The frame change timing is every VBK in non-interlace and interlace & video modes, and every FRM in interlace mode.

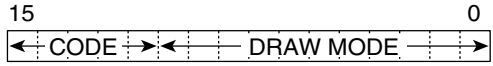
Do not use this command in auto display charge mode.

4.6.6 TRAP

Function

Informs the Q2SD of the end of the display list.

Command Format



1. Code
   B'11111

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

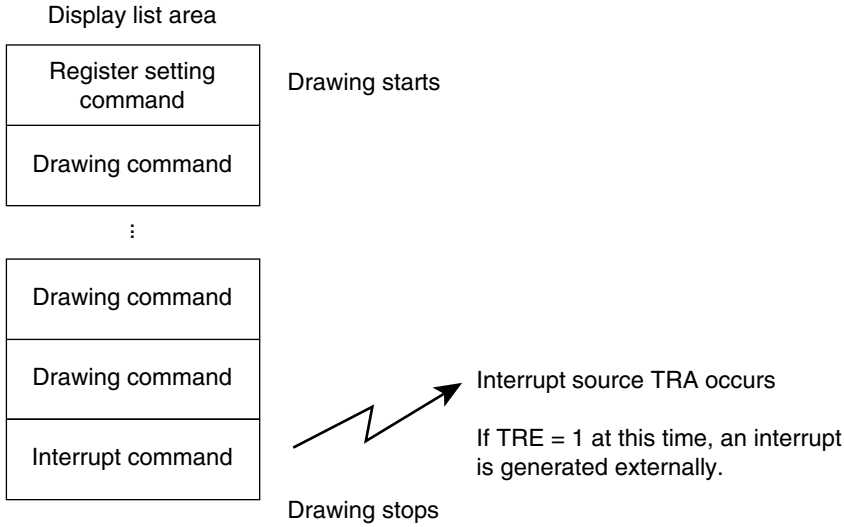
O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

Halts the drawing operation and sets TRA to 1 in the status register (SR). If TRE is set to 1 in the interrupt enable register (IER), an interrupt is sent to the SuperH.

This command must be placed at the end of the display list.

Example


Display list area
Register setting command
Drawing command
Drawing command
Drawing command
Interrupt command
Drawing starts
Interrupt source TRA occurs
If TRE = 1 at this time, an interrupt is generated externally.
Drawing stops

5.1 Register Map

Table 5.1 Registers

Register Address		R/W	Register Name		Abbre-viation	Data															
$\overline{CS1}$	A [10:0]					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	—	—	—		—	—															
0	000	R/W	System control		SYSR	SRES	DRES	DEN			RBRK	DC	RS	DBM1	DBM0	DMA1	DMA0	DAA1	DAA0		
	002	R	Status		SR	TVR	FRM	DMF	CER	VBK	TRA	CSF	DBF	BRK	FEMP			Q3	Q2	Q1	Q0
	004	W	Status register clear		SRCR	TVCL	FRCL	DMCL	CECL	VBCL	TRCL	CSCL		BRCL							
	006	R/W	Interrupt enable		IER	TVE	FRE	DME	CEE	VBE	TRE	CSE		BRE							
	008	R/W	Memory mode		MEMR											MES1	MES0				MAT
	00A	R/W	Display mode		DSMR	FLT				WRAP	BG		TVM1	TVM0	SCM1	SCM0	REF3	REF2	REF1	REF0	
	00C	R/W	Rendering mode		REMR	RSAE								MWX				GBM2	GBM1	GBM0	
	00E	R/W	Input data conversion mode		IEMR											YUV	MDTP	DTP	YUV1	YUV0	
	010	R/W	Display size	X	DSR	DSX															
	012	R/W		Y		DSY															
	014	R/W	Display start address	0	DSAR	DSA0															
	016	R/W		1		DSA1															
	018	R/W	Display list start address	H	DLSAR	DLSAH															
	01A	R/W		L		DLSAL															
	01C	R/W	Multi-valued source area start address		SSAR	SSAL												SSAH			
	01E	R/W	Work area start address		WSAR	WSAL												WSAH			
	020	R/W	DMA transfer start address	H	DMASR	DMASH															
	022	R/W		L		DMASL															
	024	R/W	DMA transfer word count	L	DMAWR	DMAWL															
	026	R/W	Display window	Horizontal display start position	DSWR	HDS															
	028	R/W		Horizontal display end position		HDE															
	02A	R/W		Vertical display start position		VDS															
	02C	R/W		Vertical display end position		VDE															
	02E	R/W	Horizontal sync pulse width		HSWR	HSW															
	030	R/W	Horizontal scan cycle		HCR	HC															
	032	R/W	Vertical sync position		VSPR	VSP															
	034	R/W	Vertical scan cycle		VCR	VC															
	036	R/W	Display off output	H	DOOR	DOR															
	038	R/W		L		DOG												DOB			
	03A	R/W	Color detection	H	CDER	CDR															
	03C	R/W		L		CDG												CDB			
	03E	R	Command status	H	CSTR	CSTH															
	040	R		L		CSTL															

Table 5.1 Registers (cont)

Register Address		R/W	Register Name		Abbre-viation	Data															
CS1	A [10:0]					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	042	R/W	Image data transfer start address	H	ISAR										ISAH						
	044	R/W		L		ISAL															
	046	R/W	Image data size	X	IDSR						IDSX										
	048	R/W		Y								IDSY									
	04A	W	Image data entry		IDER	IDE															
	04C	R/W	Background start coordinate	X	BGSR							BGSX									
	04E	R/W		Y				BGSY													
	050	R/W	DMA transfer word count	H	DMAWR														DMAWH		
	052	R/W	Equalizing pulse width		EQWR										EQW						
	054	R/W	Separation width		SPWR							SPW									
	056	R/W	Display mode 2		DSMR2				CDED	PRI2	VWRY	HDIS	ODEV	CSY1	CSY0	PRI		FBD	CE2	CE1	VWE
	058	R/W	Video display start position		VPR							HVP									
	05A	R/W											VVP								
0	05C to 060	R/W	Reserved																		
	062	R/W	Video area start address		VSAR										VSAH0						
	064	R/W				VSAL0															
	066	R/W													VSAH1						
	068	R/W				VSAL1															
	06A	R/W													VSAH2						
	06C	R/W				VSAL2															
	06E	R/W	Video window size		VSIZER								VSIZEX								
	070	R/W											VSIZEY								
	072	R/W	Video incorporation mode		VIMR	VID1	VID0					VSIZ4	VSIZ3	VSIZ2	VSIZ1	VSIZ0	VINM	ODEN1	ODEN0	RGB	VIE
	074	R/W	Cursor display start position		CSR	BLINKA							HCS1								
	076	R/W				BLINKB								VCS1							
	078	R/W											HCS2								
	07A	R/W												VCS2							
	07C	R/W	Cursor area start address		CSAR	CSARL1									CSARH1						
	07E	R/W				CSARL2									CSARH2						

Table 5.1 Registers (cont)

Register Address		R/W	Register Name		Abbre-viation	Data															
CS1	A [10:0]					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	080	R	Current pointer	X	CURR									XC							
	082	R		Y										YC							
	084	R	Local offset	X	LCOR									XO							
	086	R		Y										YO							
	088	R	User clipping area	XMIN	UCLR									UXMIN							
	08A	R		YMIN										UYMIN							
	08C	R		XMAX										UXMAX							
	08E	R		YMAX										UYMAX							
	090	R	System clipping area	XMAX	SCLR									SXMAX							
	092	R		YMAX										SYMAX							
	094	R/W	Return address	H	RTNR	RTNH															
	096	R/W		L		RTNL															
	098	R/W	Rendering start address		RSAR	RSA															
	09A	R/W	Color offset		COLOR	COOFR						COOFG					COOFB				
	09C to 1FE					Reserved															
	200	R/W	Color palette	000H	CP000R	G000								R000							
	202	R/W		000L										B000							
	204	R/W		001H	CP001R	G001								R001							
	206	R/W		001L										B001							
	208	R/W		002H	CP002R	G002								R002							
	20A	R/W		002L										B002							
	—	—	—	—	—	—								—							
	5EC	R/W		255H	CP255R	G255								R255							
	5FE	R/W		255L										B255							
	600to 7FE					Reserved															

5.2 Interface Control Registers

The interface control registers are registers related to overall Q2SD control, mapped onto addresses (A10 to A1) H'000 to H'00E, H’056, and H’072.

- System control register (SYSR)
- Status register (SR)
- Status register clear register (SRCR)
- Interrupt enable register (IER)
- Memory mode register (MEMR)
- Display mode register (DSMR)
- Display mode 2 register (DSMR2)
- Rendering mode register (REMR)
- Input data conversion mode register (IEMR)
- Video incorporation mode register (VIMR)

5.2.1 System Control Register (SYSR)

The system control register (SYSR) specifies Q2SD system operation.

The SYSR is initialized as follows in a reset:

- Bits SRES and DRES are set to 1.
- Bits DEN, RBRK, DC, RS, DMA1, DMA0, DAA1, and DAA0 are cleared to 0.
- Bits DBM1 and DBM0 retain their values.

Register Address: H'000

Bit	Bit Name	Initial Value	R/W	Description
15	SRES	1	R/W	Software Reset (SRES) Controls execution and suspension of command processing. 0: Command processing execution is enabled. 1: SRES is set to 1 when a hardware reset is performed. Clear to 0 in initialization. When this bit is set to 1 by software, a reset is performed for drawing operations only. In this case, the bit must be set to 1 for at least 16 system operating clock cycles. When SRES is set to 1, the command error flag (CER), trap flag (TRA), command suspend flag (CSF), rendering break bit (RBRK), and drawing break flag (BRK) are cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
14	DRES	1	R/W	Display Reset (DRES)
13	DEN	0	R/W	Display Enable (DEN) These bits control starting and stopping of display synchronous operation. 00: Display operation is started. The DRES bit cannot be cleared to 0 while the $\overline{\text{RESET}}$ pin is low. When using the Q2SD from the initial state, make all control register settings before clearing the DRES bit to 0. When the DEN bit is 0, display data has the value set in the display off output register. 01: Display operation is started. The DRES bit cannot be cleared to 0 while the $\overline{\text{RESET}}$ pin is low. When using the Q2SD from the initial state, make all control register settings, clear the DRES bit to 0, and then set the DEN bit to 1. Display data has the value stored in the UGM from the next frame. 10: Display synchronous operation is started. The Q2SD only performs UGM refresh operations, regardless of the setting of TVM1 and TVM0 in the display mode register. With these settings, the Q2SD operates as shown below. When switching from DRES, DEN = 01 to DRES, DEN = 10, the setting DRES, DEN = 11 occurs temporarily for reasons relating to internal updating, but this does not affect operation. 1. Drawing is not performed even if the RS bit is set to 1 in SYSR. 2. Display data is all-0 output. 3. The VBK flag is cleared to 0 in SR. 4. Except during video incorporation (VIE = 1), waits are output continuously when UGM access is performed by the CPU or DMA controller. 11: Setting prohibited
12, 11	—	—	—	Reserved Only 0 should be written to these bits.

Bit	Bit Name	Initial Value	R/W	Description
10	RBRK	0	R/W	Rendering Break (RBRK) Controls rendering (drawing) breaks. This bit should only be set when the BRK bit is cleared to 0. 0: The TRA bit in the status register (SR) is set to 1 by TRAP command execution, and drawing is terminated. 1: The currently executing command ends while the Q2SD is performing drawing, and when the next command is fetched the BRK bit in the status register (SR) is set to 1 and drawing enters the terminated state. The BRK bit does not change if this bit is set to 1 while the Q2SD is not performing drawing. After the break, the start address of the next command is placed in the command status register (CSTR). This bit is cleared to 0 only when a drawing break is effected.
9	DC	0	R/W	Display Area Change (DC) Controls frame buffer switching in manual display change mode. 0: Switching of the frame buffer for display is not performed in manual display change mode. When the DC bit is 0, it can be set to 1. 1: Switching of the frame buffer for display is performed in manual display change mode. This bit can be set to 1 set only when it is 0. Switching is performed in frame units in non-interlace and interlace modes, and in field units in interlace sync & video mode. This bit is cleared to 0 after frame buffer switching, and so should not be cleared to 0 by the SuperH.

Bit	Bit Name	Initial Value	R/W	Description
8	RS	0	R/W	Rendering Start (RS) Specifies the start of rendering. 0: Rendering is not started. 1: Rendering is started. This bit is cleared to 0 after rendering starts. When this bit is set to 1, all the data held in the FIFO in the CPU interface unit is stored in the UGM. All the data held in the FIFO is also stored in the UGM when the SuperH does not access the UGM for 32 tcyc0 or longer, and when the SuperH reads the UGM.
7	DBM1	*	R/W	Double-Buffer Mode 1 and 0 (DBM1, DBM0)
6	DBM0	*	R/W	These bits select double-buffer control. 00: Auto display change mode is set. 01: Auto rendering mode is set. 10: Manual display change mode is set. 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
5	DMA1	0	R/W	DMA Mode (DMA1, DMA0) These bits specify DMA transfer. Use the DMA flag (DMF) in the status register (SR) to check for the beginning and end of DMA mode. 00: Normal mode is set. If DMA transfer is in progress at this time, the transfer data is not guaranteed. 01: The mode for DMA transfer to memory (UGM) corresponding to $\overline{CS0}$ is set. When the remaining DMA transfer count reaches 0, this bit is automatically cleared and normal mode is entered. The initial value of the remaining DMA transfer count is determined by the setting in the DMA transfer word count register (DMAWR). The remaining DMA transfer count is an internal value in the LSI, and is decremented by 1 each time a word is processed. Do not perform UGM access by the CPU in this mode. If normal mode (DMA1 = 0, DMA0 = 0) is set by the SuperH in this mode, DMA transfer will be aborted. As the value of the transfer data at the time of the abort is undefined, if an abort is performed, DMA transfer must be started over again from the beginning. 10: Setting prohibited 11: The mode for DMA transfer to the register [image data entry register (IDER)] corresponding to $\overline{CS1}$ is set. In this mode, register address incrementing is not performed and all writes are to IDER. When the remaining DMA transfer count reaches 0, this bit is automatically cleared and normal mode is entered. The initial value of the remaining DMA transfer count is determined by the setting in the DMA transfer word count register (DMAWR). The remaining DMA transfer count is an LSI internal value, and is decremented by 1 each time a word is processed. Do not perform UGM access by the CPU in this mode. If normal mode (DMA1 = 0, DMA0 =0) is set by the SuperH in this mode, DMA transfer will be aborted. As the value of the transfer data at the time of the abort is undefined, if an abort is performed, DMA transfer must be started over again from the beginning.
4	DMA0	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
3	DAA1	0	R/W	DMA Address Mode (DAA1, DAA0)
2	DAA0	0	R/W	Sets the address mode for DMA transfer. 00: Single address mode, data is latched at the rising edge of the $\overline{RD}$ signal or the $\overline{DACK}$ signal, whichever comes first. 01: Single address mode, with data latched at the rise of the $\overline{DACK}$ signal. The $\overline{RD}$ signal is ignored. 10: Dual address mode 11: Setting prohibited
1, 0	—	—	—	Reserved The write value should always be 0.

Note: * Value is retained.

5.2.2 Status Register (SR)

The status register (SR) is used to read the internal status of the Q2SD from outside.

The SR is initialized as follows in a reset:

- The DBF flag retains its value.
- The Q flags are set to 0100.
- The FEMP flag is set to 1.
- All other flags are cleared to 0.

Register Address: H'002

Bit	Bit Name	Initial Value	R/W	Description
15	TVR	0	R	TV Sync Signal Error Flag (TVR) Flag that indicates that $\overline{\text{EXVSYNC}}$ has been detected within the vertical cycle. 0: The rise of $\overline{\text{EXVSYNC}}$ has been detected each time within the vertical cycle determined by the vertical scan cycle register (VCR) setting after the TVR flag has been cleared by the DRES bit in SYSR or the TVCL bit in SRCR. 1: In TV sync mode (bits TVM1 and TVM0 = 10 in DSMR), a rise of $\overline{\text{EXVSYNC}}$ has not been detected within the vertical cycle determined by the VCR set value. The TVR flag retains its state until cleared by a reset or by software.
14	FRM	0	R	Frame Flag (FRM) Flag that indicates the vertical blanking interval after frame display. 0: Indicates the interval from FRM flag clearing by the DRES bit in SYSR or the FRCL bit in SRCR until the end of the next display in non-interlace mode, or until the end of the next even field display in interlace mode or interlace sync & video mode. 1: Indicates the interval from the first even field vertical blanking interval after FRM flag clearing by the DRES bit in SYSR or the FRCL bit in SRCR until the FRM flag is cleared again (switched in frame units).

Bit	Bit Name	Initial Value	R/W	Description
13	DMF	0	R	DMA Flag (DMF) Flag that indicates that DMA transfer mode has been initiated and transfer has been completed. 0: DMA transfer mode has not been initiated at all since DMF flag clearing by the DMCL bit in SRCR, or the next DMA transfer mode (bits DMA1 and DMA0 = 01 or 11 in SYSR) has been initiated and the remaining transfer count has not yet reached 0. 1: DMA transfer mode has been initiated and the transfer word count has reached 0. The DMF flag retains its state until cleared by a reset or by software.
12	CER	0	R	Command Error Flag (CER) Flag that indicates that an illegal command has been fetched. 0: Normal state. An illegal command has not been fetched since CER flag clearing by the SRES bit in SYSR or the CECL bit in SRCR. An illegal command is one in which the upper 5 bits of the command code are undefined. The Q2SD does not check the legality of the rendering attributes in the lower 11 bits. 1: Drawing operation halt state. Drawing operation remains halted because an illegal command was fetched after CER flag clearing by the SRES bit in SYSR or the CECL bit in SRCR. The CER flag retains its state until cleared by a reset or by software.
11	VBK	0	R	Vertical Blanking Flag (VBK) Flag that indicates the vertical blanking interval. 0: Indicates the interval from VBK flag clearing by the DRES bit in SYSR or the VBCL bit in SRCR until the end of the next display. 1: Indicates the interval from the first vertical blanking interval after VBK flag clearing by the DRES bit in SYSR or the VBCL bit in SRCR until the VBK flag is cleared again (switched in field units).

Bit	Bit Name	Initial Value	R/W	Description
10	TRA	0	R	Trap Flag (TRA) Flag that indicates the end of command execution. 0: Indicates the interval from TRA flag clearing by the SRES bit in SYSR or the TRCL bit in SRCR until the end of execution of the next command. 1: Command execution has ended, or the current command is not being executed. The TRA flag retains its state until cleared by a reset or by software.
9	CSF	0	R	Command Suspend Flag (CSF) Flag that indicates that command execution has been suspended due to a frame change in auto display change mode or manual display change mode. 0: Normal operation 1: A rendering end interrupt has not been generated in the interval from CSF flag clearing by the SRES bit in SYSR or the CSCL bit in SRCR until the next frame change. The CSF flag retains its state until cleared by a reset or by software.
8	DBF	*	R	Display Buffer Frame (DBF) Flag that indicates the display start address register used as the display start address by the Q2SD. 0: Address indicated by DSAR0 is being used as display start address. 1: Address indicated by DSAR1 is being used as display start address.
7	BRK	0	R	Drawing Break Flag (BRK) Flag that indicates a drawing break. 0: Indicates the interval until the next drawing break occurs after the BRK flag is cleared by the SRES bit in SYSR or the BRCL bit in SRCR. 1: Indicates that a command is not currently being executed due to a drawing break directive. The BRK flag retains its state until cleared by a reset or by software.

Bit	Bit Name	Initial Value	R/W	Description
6	FEMP	1	R	FIFO Empty Flag (FEMP) Transfer data from the CPU to the UGM is temporarily stored in a FIFO. These transfers include UGM writes and data transfers via IDR. This flag indicates whether there is UGM storage data in the FIFO. 0: There is UGM storage data in the FIFO. 1: There is no UGM storage data in the FIFO.
5, 4	—	—	—	Reserved These bits always read 0.
3	Q3	0	R	Q Flags (Q3 to Q0)
2	Q2	1	R	Flags used for Q2SD Series product identification. In the Q2SD, these flags read 0100.
1	Q1	0	R	
0	Q0	0	R	0010: HD64411 (Q2) 0011: HD64412 (Q2i) 0100: HD64413A (Q2SD)

Note: * Value is retained.

5.2.3 Status Register Clear Register (SRCR)

The status register clear register (SRCR) clears the corresponding flags in the status register (SR). Writing 1 to one of bits 15 to 9 or 7 in the SRCR register will clear the corresponding flag in SR to 0. When SR clearing is completed, the value of the SRCR register is cleared to all-0 internally (a read will return 0).

Register Address: H'004

Bit	Bit Name	Abbreviation	Description
15	TV sync signal error flag clear	TVCL	Writing 1 to the TCVL bit clears the TVR flag to 0 in SR.
14	Frame buffer clear	FRCL	Writing 1 to the FRCL bit clears the FRM flag to 0 in SR.
13	DMA flag clear	DMCL	Writing 1 to the DMCL bit clears the DMF flag to 0 in SR.
12	Command error flag clear	CECL	Writing 1 to the CECL bit clears the CER flag to 0 in SR.
11	Vertical blanking flag clear	VBCL	Writing 1 to the VBCL bit clears the VBK flag to 0 in SR.
10	Trap flag clear	TRCL	Writing 1 to the TRCL bit clears the TRA flag to 0 in SR.
9	Command suspend flag clear	CSCL	Writing 1 to the CSCL bit clears the CSF flag to 0 in SR.
8	Reserved	—	Only 0 should be written to this bit.
7	Drawing break flag clear	BRCL	Writing 1 to the BRCL bit clears the BRK flag to 0 in SR.
6 to 0	Reserved	—	Only 0 should be written to these bits.

Note: * Value is retained.

5.2.4 Interrupt Enable Register (IER)

The interrupt enable register (IER) enables or disables interrupts by the corresponding flags in the status register (SR). When a bit in SR is set to 1 and the bit at the corresponding bit position in the IER register is also 1, $\overline{IRL}$ is driven low and an interrupt request is sent to the CPU.

The interrupt generation condition is as follows.

Interrupt generation condition = $\overline{\overline{IRL}} = \overline{a+b+c+d+e+f+g}$

a = TVR·TVE
b = FRM·FRE
c = DMF·DME
d = CER·CEE
e = VBK·VBE
f = TRA·TRE
g = CSF·CSE
h = BRK·BRE

Register Address: H'006

Bit	Bit Name	Initial Value	R/W	Description
15	TVE	0	R/W	TV Sync Signal Error Flag Enable (TVE) Enables or disables interrupts initiated by the TVR flag in SR. 0: Interrupts initiated by the TVR flag in SR are disabled. 1: Interrupts initiated by the TVR flag in SR are enabled. When TVR·TVE = 1, an $\overline{IRL}$ interrupt request is sent to the CPU.
14	FRE	0	R/W	Frame Flag Enable (FRE) Enables or disables interrupts initiated by the FRM flag in SR. 0: Interrupts initiated by the FRM flag in SR are disabled. 1: Interrupts initiated by the FRM flag in SR are enabled. When FRM·FRE = 1, an $\overline{IRL}$ interrupt request is sent to the CPU.

Bit	Bit Name	Initial Value	R/W	Description
13	DME	0	R/W	DMA Flag Enable (DME) Enables or disables interrupts initiated by the DMF flag in SR. 0: Interrupts initiated by the DMF flag in SR are disabled. 1: Interrupts initiated by the DMF flag in SR are enabled. When DMF·DME = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.
12	CEE	0	R/W	Command Error Flag Enable (CEE) Enables or disables interrupts initiated by the CER flag in SR. 0: Interrupts initiated by the CER flag in SR are disabled. 1: Interrupts initiated by the CER flag in SR are enabled. When CER·CEE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.
11	VBE	0	R/W	Vertical Blanking Flag Enable (VBE) Enables or disables interrupts initiated by the VBK flag in SR. 0: Interrupts initiated by the VBK flag in SR are disabled. 1: Interrupts initiated by the VBK flag in SR are enabled. When VBK·VBE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.
10	TRE	0	R/W	Trap Flag Enable (TRE) Enables or disables interrupts initiated by the TRA flag in SR. 0: Interrupts initiated by the TRA flag in SR are disabled. 1: Interrupts initiated by the TRA flag in SR are enabled. When TRA·TRE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.
9	CSE	0	R/W	Command Suspend Flag Enable (CSE) Enables or disables interrupts initiated by the CSF flag in SR. 0: Interrupts initiated by the CSF flag in SR are disabled. 1: Interrupts initiated by the CSF flag in SR are enabled. When CSF·CSE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.

Bit	Bit Name	Initial Value	R/W	Description
8	—	—	—	Reserved Only 0 should be written to this bit.
7	BRE	0	R/W	Drawing Break Flag Enable (BRE) Enables or disables interrupts initiated by the BRK flag in SR. 0: Interrupts initiated by the BRK flag in SR are disabled. 1: Interrupts initiated by the BRK flag in SR are enabled. When BRK·BRE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.
6 to 0	—	—	—	Reserved Only 0 should be written to these bits.

5.2.5 Memory Mode Register (MEMR)

The memory mode register (MEMR) specifies the size of UGM used and the memory access timing.

If the value of this register is modified during a memory access, operation will be temporarily unstable.

The MEMR bits MES1, MES0, and MAT are initialized to 0 by a reset.

Register Address: H'008

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	—	—	Reserved Only 0 should be written to these bits.
5	MES1	0	R/W	Memory Size (MES1, MES0)
4	MES0	0	R/W	These bits select the size and quantity of memories used for the UGM. 00: One 16-Mbit (×16) memory, 16-bit bus 01: Two 16-Mbit (×16) memories, 32-bit bus 10: One 64-Mbit (×16) memory, 16-bit bus 11: One 64-Mbit (×32) memory, 32-bit bus

Bit	Bit Name	Initial Value	R/W	Description
3 to 1	—	—	—	Reserved Only 0 should be written to these bits.
0	MAT	0	R/W	Memory Access Timing (MAT) Sets the UGM access timing. APL (Active Precharge Latency) 0: 5 1: 5 PI (Precharge Latency) 0: 3 1: 2 PCL (RAS-CAS Latency) 0: 3 1: 2 WPL (Write Precharge Latency) 0: 2 1: 2

5.2.6 Display Mode Register (DSMR)

The display mode register (DSMR) specifies Q2SD display operations.

If the value of this register is modified during a display operation, operation will be temporarily unstable.

The DSMR is initialized as follows in a reset:

Bits WRAP and BG are initialized to 0, bits TVM1 and TVM0 to 10, and bits REF3 to REF0 to 1000.

The SCM1 and SCM0 bits retain their values.

Register Address: H'005

Bit	Bit Name	Initial Value	R/W	Description
15	FLT	0	R/W	Filter Mode (FLT) 0: FG and BG pixel data is output for display as the respective screens. 1: FG and BG pixel data is averaged and output for display as the FG screen. Set GBM = 001/101, VWE = 0, PRI = 00, FBD = 0, SCM = 11. FG transparent color determination is not performed. Transparent color determination (CDE) is performed on the result. Set the BG start position one line below the FG start position. The average is found by right-shifting the result of addition of each part in 16-bit format (5:6:5). A fraction of a shift is ignored.
14 to 12	—	—	—	Reserved Only 0 should be written to these bits.

Bit	Bit Name	Initial Value	R/W	Description
11	WARP	0	R/W	Background Screen Wraparound Mode Configuration (WRAP) 0: Background screen wraparound is not performed. Display contents are not guaranteed if the display area extends beyond the memory installation space. 1: Background screen wraparound is performed. The wraparound units are the number of pixels specified by the MWX bit in the rendering mode register (REMR) in the X direction, and 512 pixels in the Y direction. The start coordinates of this area are indicated by bits 13 to 9 of the background start coordinate register (BGSR).
10	BG	0	R/W	Background Screen Combination (BG) 0: Background screen combination is not performed. 1: Background screen combination is performed.
9, 8	—	—	—	Reserved Only 0 should be written to these bits.

Bit	Bit Name	Initial Value	R/W	Description
7	TVM1	1	R/W	TV Sync Mode (TVM1, TVM0)
6	TVM0	0	R/W	These bits specify TV sync mode, in which synchronous operation is performed by means of $\overline{\text{EXHSYNC}}$ and $\overline{\text{EXVSYNC}}$ input from an external source, or master mode, in which $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output. 00: Master mode is set. The Q2SD outputs $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{ODDF}}$ signals. In this mode, when CSY1 = 1 in display mode register 2 (DSMR2), set initial values in the equalizing pulse width register (EQWR) and separation width register (SPWR). 01: Synchronization system switching mode is set. Switching is performed from TV sync mode to master mode, or vice versa, via this mode. In this mode, display operations are forcibly halted and the DISP pin output goes low. The clock supply to the CLK1 pin can also be stopped (input invalidated) (fixed high within the chip). The $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{ODDF}}$ pins are inputs. 10: TV sync mode is set. $\overline{\text{EXHSYNC}}$, $\overline{\text{EXVSYNC}}$, and $\overline{\text{ODDF}}$ signals are input to the Q2SD. CSYNC output is fixed high. In this mode, clear both CSY1 and CSY0 to 0 in display mode register 2 (DSMR2). 11: Setting prohibited
5	SCM1	*	R/W	Scan Mode (SCM1, SCM0)
4	SCM0	*	R/W	These bits specify the display output scan mode and the unit of display switching. 00: Non-interlace mode: Frame buffer switching can be performed in 1-VC units. 01: Setting prohibited 10: Interlace mode: Frame buffer switching can be performed in 2-VC units. 11: Interlace sync & video mode: Frame buffer switching can be performed in 1-VC units.

Bit	Bit Name	Initial Value	R/W	Description
3	REF3	1	R/W	Refresh Cycles (REF3 to REF0)
2	REF2	0	R/W	These bits specify the number of cycles for which refreshing is performed within one raster in the display screen area.
1	REF1	0	R/W	
0	REF0	0	R/W	0000: Refresh timing is not output
				0001: Number of refresh cycles = 1
				0010: Number of refresh cycles = 2
				0011: Number of refresh cycles = 3
				0100: Number of refresh cycles = 4
				0101: Number of refresh cycles = 5
				0110: Number of refresh cycles = 6
				0111: Number of refresh cycles = 7
				1000: Number of refresh cycles = 8
				1001: Number of refresh cycles = 9
				1010: Number of refresh cycles = 10
				1011: Number of refresh cycles = 11
				1100: Number of refresh cycles = 12
				1101: Number of refresh cycles = 13
				1110: Number of refresh cycles = 14
				1111: Number of refresh cycles = 15

Note: * Value is retained.

5.2.7 Display Mode 2 Register (DSMR2)

The display mode 2 register (DSMR2) specifies Q2SD display operations. If the value of this register is modified during a display operation, operation will be temporarily unstable.

In a reset, bits CSY1 and CYS0 retain their values, and the other bits are cleared to 0.

Register Address: H'056

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	—	—	Reserved Only 0 should be written to these bits.
12	CDED	0	R/W	CDE Disable (CDED) Controls CDE pin output. In TV sync mode (TVM1 = 1, TVM0 = 0), the CDE pin is used to switch between external sync signal generation circuit video output and Q2SD analog R/G/B output. 0: CDE pin output is enabled. 1: CDE pin output is disabled.
11	PRI2	0	R/W	Window Priority (PRI2, PRI) These bits set the screen display priority.
10	VWRY	0	R/W	Video Window RGB/YC Mode (VWRY) Selects whether the data displayed in the video window is stored in the UGM in RGB format or YC format. 0: Video window displays RGB data in the UGM as RGB data. 1: Video window displays YC data in the UGM as RGB data.
9	HDIS	0	R/W	[Mode in which Foreground Screen 1 Starts at x = 512 in Case of 1024-Pixel Memory Width] (HDIS) When HDIS = 1, use is possible when GBM = 000 or 001 and RSAE = 0. 0: Foreground screen 1 starts at x = 0. 1: Foreground screen 1 starts at x = 512.

Bit	Bit Name	Initial Value	R/W	Description
8	ODEV	0	R/W	$\overline{\text{ODDF}}$ Signal Polarity Select (ODEV): Selects the polarity of the $\overline{\text{ODDF}}$ signal. 0: $\overline{\text{ODDF}}$ goes low in first-half field in same frame of interlace display. 1: $\overline{\text{ODDF}}$ goes high in first-half field in same frame of interlace display.
7	CSY1	*	R/W	$\overline{\text{CSYNC}}$ Mode (CSY1, CSY0)
6	CSY0	*	R/W	These bits select the $\overline{\text{CSYNC}}$ signal output mode in master mode (TVM1 = 0, TVM0 = 0). When CSY1 = 1, values must be set in the equalizing pulse width register (EQWR) and separation width register (SPWR). 00: Waveform determined by exclusive logical OR of $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ is output as $\overline{\text{CSYNC}}$. In TV sync mode (TVM1 = 1, TVM0 = 0), this mode should be selected. 01: Setting prohibited 10: Equalizing pulses are output in 3-raster period from fall of $\overline{\text{VSYNC}}$, separation in next 3-raster period, equalizing pulses in next 3-raster period, and $\overline{\text{HSYNC}}$ waveform in other periods. 11: Equalizing pulses are output in 2.5-raster period starting 0.5 raster after fall of $\overline{\text{VSYNC}}$, separation in next 2.5-raster period, equalizing pulses in next 2.5-raster period, and $\overline{\text{HSYNC}}$ waveform in other periods.
5	PRI	0	R/W	Window Priority (PRI2, PRI) These bits set the screen display priority. 00: Screen priority order is: cursor 1, cursor 2, foreground, video, background. 01: Setting prohibited 10: Screen priority order is: cursor 1, foreground, video, cursor 2, background. 11: Screen priority order is: foreground, video, cursor 1, cursor 2, background.
4	—	—	—	Reserved The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	FBD	0	R/W	Foreground Disable (FBD) Selects display or non-display of the foreground screen. 0: Foreground screen is displayed. 1: Foreground screen is not displayed.
2	CE2	0	R/W	Cursor 2 Enable (CE2) Selects display or non-display of cursor 2. 0: Cursor 2 is not displayed. 1: Cursor 2 is displayed. Cursor blinking is always performed. To give the appearance of a non-blinking cursor, make the same setting for cursor blink shapes A and B stored in the cursor area. In Q2SD cursor blinking, cursor blink shapes A and B are displayed alternately. To provide a period in which the cursor is not displayed, make one entire waveform a transparent color.
1	CE1	0	R/W	Cursor 1 Enable (CE1) Selects display or non-display of cursor 1. 0: Cursor 1 is not displayed. 1: Cursor 1 is displayed. Cursor blinking is always performed. To give the appearance of a non-blinking cursor, make the same setting for cursor blink shapes A and B stored in the cursor area. In Q2SD cursor blinking, cursor blink shapes A and B are displayed alternately. To provide a period in which the cursor is not displayed, make one entire waveform a transparent color.
0	VWE	0	R/W	Video Window Enable (VWE) Selects display or non-display of the video window. 0: Video window is not displayed. 1: Video window is displayed. The display contents are not guaranteed if this bit is set before VID changes after VIE is set to 1.

Note: * Value is retained.

5.2.8 Rendering Mode Register (REMR)

The rendering mode register (REMR) specifies Q2SD rendering operations.

If the value of this register is modified during a drawing operation, operation will be temporarily unstable. The exception is modification by a WPR command from the display list, in which case the following conditions must be satisfied:

- Changing the MWX setting is prohibited.
- For the GBM bits, only the drawing bit configuration can be changed; changing the display bits is prohibited.
- RSAE can be changed, on condition that the change agrees with the GBM setting.

In a reset, the RSAE bit in the REMR register is cleared to 0, while the MWX and GBM bits retain their values.

Register Address: H'00C

Bit	Bit Name	Initial Value	R/W	Description
15	RSAE	0	R/W	Drawing Start Address Enable (RSAE) Allows the drawing area to be set separately from the display area. The start address of a drawing area separate from the display area is set in the drawing start address register (RSAR). 0: Value in display start address register (DSAR) is used for drawing area. When this setting is made, the GBM setting must be 000 or 001. 1: Value in rendering start address register (RSAR) is used for drawing area.
14 to 7	—	—	—	Reserved Only 0 should be written to these bits.
6	MWX	*	R/W	Memory Width (MWX) Specifies the X-direction logical coordinate space of the UGM connected to the Q2SD. 0: X-direction logical coordinate space is 512 pixels 1: X-direction logical coordinate space is 1024 pixels

Bit	Bit Name	Initial Value	R/W	Description
5 to 3	—	—	—	Reserved Only 0 should be written to these bits.
2	GBM2	*	R/W	Graphic Bit Mode 2 to 0 (GBM2 to GBM0)
1	GBM1	*	R/W	These bits specify the bit configuration of the rendering data and display data handled by the Q2SD.
0	GBM0	*	R/W	Note that the setting of these bits may be linked to the RSAE bit setting.

Note: * Value is retained.

Table 5.2 Bit Configuration

			Description			
Bit 2: GBM2	**Bit 1: GBM1**	**Bit 0: GBM0**	**FG Bit Configuration**	**BG Bit Configuration**	**Rendering Bit Configuration**	**RSAE Bit Setting**
0	0	0	8 bits/pixel	8 bits/pixel	8 bits/pixel	0 or 1
		1	16 bits/pixel	16 bits/pixel	16 bits/pixel	0 or 1
	1	0	8 bits/pixel	16 bits/pixel	8 bits/pixel	0 or 1
		1	16 bits/pixel	8 bits/pixel	16 bits/pixel	0 or 1
1	0	0	8 bits/pixel	8 bits/pixel	16 bits/pixel	Must be 1
		1	16 bits/pixel	16 bits/pixel	8 bits/pixel	Must be 1
	1	0	8 bits/pixel	16 bits/pixel	16 bits/pixel	Must be 1
		1	16 bits/pixel	8 bits/pixel	8 bits/pixel	Must be 1

5.2.9 Input Data Conversion Mode Register (IEMR)

The input data conversion mode register (IEMR) specifies the conversion format for input data from the SuperH.

If the value of this register is modified during a data conversion, operation will be temporarily unstable.

In a reset, all IEMR bits are cleared to 0.

Register Address: H'00E

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	—	—	Reserved Only 0 should be written to these bits.
4	YUV2	0	R/W	YUV Mode: This bit specify whether data input in YUV or ΔYUV format is to be converted to RGB format before being stored in the UGM.
3	MDTP	0	R/W	Memory Data Type Mode (MDTP) Specifies whether byte-unit swapping is to be performed in a word access UGM memory write transfer from the SuperH. This bit is valid when bits YUV2 to YUV0 are set to 000, and bits DMA1 and DMA0 are set to either 00 or 01. This bit is invalid for register writes from the SuperH, and also for UGM memory read operations by the SuperH. 0: Byte-unit swapping is not performed in a word access UGM memory write transfer from the SuperH. 1: In a word access UGM memory write transfer from the SuperH, the upper and lower bytes are swapped within the same word (16 bits).

Bit	Bit Name	Initial Value	R/W	Description
2	DTP	0	R/W	Data Type Mode (DTP) Specifies whether byte-unit swapping is to be performed in a transfer. This bit is valid for data transfers via the image data entry register (IDER). This bit is valid when bits YUV2 to YUV0 are set to 001, 010, 011, or 111, and bits DMA1 and DMA0 are set to either 00 or 11. 0: Byte-unit swapping is not performed in a transfer via IDER. 1: In a transfer via IDER, the upper and lower bytes are swapped within the same word (16 bits).
1	YUV1	0	R/W	YUV Mode:
0	YUV0	0	R/W	These bits specify whether data input in YUV or ΔYUV format is to be converted to RGB format before being stored in the UGM.

Table 5.3 YUV Mode Setting

Bit 4	Bit 1	Bit 0	
YUV2	**YUV1**	**YUV0**	**Description**
0	0	0	Normal mode is set. Data transfer via IDER is not performed. Also used when setting YUV2, 1, 0 to (0, 1, 1).
0	0	1	YUV-RGB conversion is performed. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.
0	1	0	ΔYUV-RGB conversion is performed. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.
0	1	1	16-bit/pixel data is simply transferred, without conversion. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.
1	0	0	Used when setting YUV2, 1, 0 to (1, 1, 1).
1	0	1	Setting prohibited
1	1	0	Setting prohibited
1	1	1	8-bit/pixel data is simply transferred, without conversion. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). Set the number of transfer words (1/2 the number of pixels) as the IDSX value. The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.

5.2.10 Video Incorporation Mode Register (VIMR)

The video incorporation mode register (VIMR) is used to make various video capture settings.

Register Address: H'072

Bit	Bit Name	Initial Value	R/W	Description
15	VID1	1	R	Video Window Status (VID1, VID0)
14	VID0	1	R	These bits are status flags that indicate the video area storing the most recent image incorporated from the video input. Note that these bits are different in nature from the other bits in this register. The value of these bits is significant only when the VIE bit is cleared to 0. Note that the meaning of these bits is not guaranteed if video capture proceeds while the VIE bit is set to 1. Only 00 should be written to these bits (although the write value is ignored). The meaning of the values read from these bits is shown below. 00: Most recent image is in video area 0. When video window enable (VWE) is 1, video area 0 is displayed. 01: Most recent image is in video area 1. When video window enable (VWE) is 1, video area 1 is displayed. 10: Most recent image is in video area 2. When video window enable (VWE) is 1, video area 2 is displayed. 11: Indicates initial state after a reset. When video window enable (VWE) is 1, video area 0 is displayed. To save or fetch an image as a still picture, video capture must be halted. The sequence of operations is: halt video capture, read the video window status, and fetch the still picture from the relevant area.

Bit	Bit Name	Initial Value	R/W	Description
13 to 10	—	—	—	Reserved Only 0 should be written to these bits (a read will return an undefined value).
9	VSIZ4	0	R/W	Video Incorporation Reduction (Thinning-Out) Ratio (VSIZ4 to VSIZ0) These bits set the reduction ratio when performing video capture. See table 5.4.
8	VSIZ3	0	R/W	
7	VSIZ2	0	R/W	
6	VSIZ1	0	R/W	
5	VSIZ0	0	R/W	
4	VINM	0	R/W	Video Incorporation Mode (VINM) Specifies the field order in video capture. 0: Field for which $\overline{\text{VODD}}$ input is low (lines 1, 3, 5, ...) is incorporated first, followed by field for which $\overline{\text{VODD}}$ input is high (lines 2, 4, 6, ...). 1: Field for which $\overline{\text{VODD}}$ input is high (lines 2, 4, 6, ...) is incorporated first, followed by field for which $\overline{\text{VODD}}$ input is low (lines 1, 3, 5, ...).

Bit	Bit Name	Initial Value	R/W	Description
3	ODEN1	0	R/W	Incorporated Field Select (ODEN1, ODEN0)
2	ODEN0	0	R/W	These bits select the field for which video input scanning method specification and capture are to be performed in video capture. 00: Input video is non-interlace. Do not input interlace signal. 01: Input video is interlace, and frame screens are incorporated with combination of even and odd fields. Supplementing is not performed for operation when fields are combined. 10: Input video is interlace, and only fields for which $\overline{\text{VODD}}$ signal is low (odd fields) are incorporated. Number of scanning lines of incorporated image is 1/2 number of frame screen scanning lines. 11: Input video is interlace, and only fields for which $\overline{\text{VODD}}$ signal is high (even fields) are incorporated. Number of scanning lines of incorporated image is 1/2 number of frame screen scanning lines. The vertical size of video storage area (VSIZEY) depends on the setting values of ODEN1 and ODEN0. ODEN1 and ODEN0 are described and the calculation formula of VSIZEY is shown below: • ODEN1 = 0, ODEN0 = 0 The timing of specifying the start address of video storage area is in VVS unit, and data is taken in VVS units. VSIZEY = (number of effective lines existing in 1VVS signals) × (video capture thinning rate) • ODEN1 = 0, ODEN0 = 1 The timing of specifying the start address of video storage area is in 2VVS units, and data of both even and odd-number fields are taken. VSIZEY = (number of effective lines existing in 2VVS signals) × (video capture thinning rate) • ODEN1 = 1 The timing of specifying the start address of video storage area is in 2VVS units, and data of either even or odd-number field is taken. VSIZEY = (number of effective lines existing in 1VVS signals) × (video capture thinning rate)

Bit	Bit Name	Initial Value	R/W	Description
1	RGB	0	R/W	RGB Conversion Mode (RGB) Selects whether RGB conversion is to be performed in video capture. 0: YUV4:2:2 data is stored directly in UGM, without conversion to RGB. This data cannot be used for any purpose except display in the video window. 1: Data undergoes RGB conversion and is stored in UGM as RGB data. This data can be used as multi-valued source data.
0	VIE	0	R/W	Video Incorporation Enable (VIE) Enables or disables video capture. 0: Video capture is not performed. 1: Video capture is performed.

Table 5.4 Video Incorporation Reduction Ratio

Bit 9	Bit 8	Bit 7	Bit 6	Vertical Reduction Ratio	Horizontal Reduction Ratio	
VSIZ4	VSIZ3	VSIZ2	VSIZ1		VSIZ0 = 0	VSIZ0 = 1
0	0	0	0	1	1	1/2
			1	1	1/3	Setting prohibited
		1	0	1	Setting prohibited	Setting prohibited
			1	1	Setting prohibited	Setting prohibited
	1	0	0	1/2	Setting prohibited	1/2
			1	1/2	1/3	1/6
		1	0	1/2	1/4	Setting prohibited
			1	1/2	Setting prohibited	Setting prohibited
1	0	0	0	1/3	Setting prohibited	Setting prohibited
			1	1/3	1/3	1/6
		1	0	1/3	Setting prohibited	Setting prohibited
			1	1/3	Setting prohibited	Setting prohibited
	1	0	0	1/4	Setting prohibited	Setting prohibited
			1	1/4	Setting prohibited	1/6
		1	0	1/4	1/4	Setting prohibited
			1	1/4	Setting prohibited	Setting prohibited

5.3 Memory Control Registers

The memory control registers are registers related to the unified graphics memory (UGM) configuration, mapped onto addresses (A10 to A1) H'010 to H'01E, H'04C, H’04E, H’062 to H’070, H’07C to H’07E, and H’098.

- Display size registers (DSR)
- Display address registers (DSAR)
- Display list start address registers (DLSAR)
- Multi-valued source area start address register (SSAR)
- Work area start address register (WSAR)
- Background start coordinate registers (BGSR)
- Video area start address registers (VSAR)
- Video window size registers (VSIZER)
- Cursor area start address register (CSAR)
- Rendering start address register (RSAR)

5.3.1 Display Size Registers (DSR)

The display size registers (DSR) specify the size of the display screen. The number of dots in the horizontal direction is set in DSX, and the number of dots in the vertical direction in DSY.

Write 0 to bits that are not used for the DSX and DSY fields (a read will return an undefined value).

The DSX and DSY fields in the DSR registers retain their values in a reset.

Register Address: H'010

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 0	—	*	R/W	DSX

Register Address: H'012

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	—	—	
8 to 0	—	*	R/W	DSY

Note: * Value is retained.

5.3.2 Display Address Registers (DSAR)

The display address registers (DSAR) specify the memory areas to be used as UGM frame buffers.

Only the upper 7 bits (A22 to A16) of the start physical address of frame buffer 0 (FB0) are set in the DSA0 field in DSAR, and only the upper 7 bits (A22 to A16) of the start physical address of frame buffer 1 (FB1) are set in the DSA1 field in DSAR.

The display address register whose contents are actually valid as the display start address is the register indicated by the DBF bit in the status register (SR). The display address register whose contents are not valid as the display start address indicates the rendering coordinate origin when RASE = 0 in the rendering mode register (REMR). When these registers are modified, the new set value becomes valid when an internal update is performed in the case of the display address register whose contents are valid as the display start address, and when an external update (rewrite) is performed in the case of the display address register that indicates the rendering coordinate origin.

Write 0 to bits that are not used for the DSA0 and DSA1 fields.

The DSA0 and DSA1 fields in the DSAR registers retain their values in a reset.

Register Address: H'014

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	DSA0 (address A22 to A16 setting)

Register Address: H'016

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	DSA1 (address A22 to A16 setting)

Note: * Value is retained.

5.3.3 Display List Start Address Registers (DLSAR)

The display list start address registers (DLSAR) specify the memory area to be used as the display list.

The DLSAH and DLSAL fields in DLSAR contain a total of 18 bits, and only the upper bits (A22 to A5) of the start physical address of the display list are set in these fields.

Write 0 to bits that are not used for the DLSAH and DLSAL fields (a read will return an undefined value).

The DLSAH and DLSA fields in the DLSAR registers retain their values in a reset.

Register Address: H'018

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	DLSAH (address A22 to A16 setting)

Register Address: H'01A

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	*	R/W	DLSAL (address A15 to A5 setting)
4 to 0	—	—	—	

Note: * Value is retained.

5.3.4 Multi-Valued Source Area Start Address Register (SSAR)

The multi-valued source area start address register (SSAR) specifies the memory area to be used as the multi-valued source area. The physical address set in this register will be the origin physical address of the multi-valued coordinate. The upper bits (A22 to A16) of the start physical address of the source area are set in the SSAH field, and the lower bits (A15 to A13) in the SSAL field.

The settable bit range depends on the highest color representation mode and maximum memory width used in each of the display, drawing, and video areas. In 8-bit/pixel mode with a 512-pixel memory width, all bits can be set. In 8-bit/pixel mode with a 1024-pixel memory width, or 16-bit/pixel mode with a 512-pixel memory width, bit 13 should be cleared to 0. In 16-bit/pixel mode with a 1024-pixel memory width, bits 14 and 13 should be cleared to 0.

The SSAH and SSAL fields in the SSAR register retain their values in a reset.

Register Address: H'01C

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	*	R/W	SSAL (address A15 to A13 setting)
12 to 7	—	—	—	Reserved Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	SSAH (address A22 to A16 setting)

Note: * Value is retained.

5.3.5 Work Area Start Address Register (WSAR)

The work area start address register (WSAR) specifies the memory area to be used as the work area. The physical address set in this register will be the origin physical address of the work coordinate. The upper bits (A22 to A16) of the start physical address of the work area are set in the WSAH field, and the lower bits (A15 to A13) in the WSAL field.

The settable bit range depends on the highest color representation mode and maximum memory width used in each of the display, drawing, and video areas. In 8-bit/pixel mode with a 512-pixel memory width, all bits can be set. In 8-bit/pixel mode with a 1024-pixel memory width, or 16-bit/pixel mode with a 512-pixel memory width, bit 13 should be cleared to 0. In 16-bit/pixel mode with a 1024-pixel memory width, bits 14 and 13 should be cleared to 0.

The WSAH and WSAL fields in the WSAR register retain their values in a reset.

Register Address: H'01E

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	*	R/W	WSAL (address A15 to A13 setting)
12 to 7	—	—	—	Reserved Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	WSAH (address A22 to A16 setting)

Note: * Value is retained.

5.3.6 Background Start Coordinate Registers (BGSR)

The background start coordinate registers (BGSR) specify the background start coordinates in the background screen. The settings should be made so that the background screen does not overlap the frame buffers. Write 0 to bits that are not used for the BGSX and BGSY fields (a read will return an undefined value).

The BGSX and BGSY bits in the BGSR registers retain their values in a reset.

Register Address: H'04C

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 0	—	*	R/W	BGSX

Register Address: H'04E

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13 to 0	—	*	R/W	BGSY

Note: * Value is retained.

5.3.7 Video Area Start Address Registers (VSAR)

The video area start address registers (VSAR) specify the memory areas used as UGM video areas. Only the upper 13 bits (A22 to A10) of the start physical addresses are specified by the video area start address fields (VSAH, VSAL).

Three video storage areas are used, of the size specified by VSIZEX and VSIZEY. Each area has a memory-unit address layout.

VSAH0 and VSAL0 are bits that specify the start address of video area 0 (V0).
VSAH1 and VSAL1 are bits that specify the start address of video area 1 (V1).
VSAH2 and VSAL2 are bits that specify the start address of video area 2 (V2).

When the VIE bit in the video incorporation mode register (VIMR) is 1, the area in which the most recent image captured by video capture was stored is automatically selected as the area used for display. When the VIE bit is 0, the video area holding the most recent image is displayed.

New values set when these registers are modified become effective when the display is updated internally in the case of display output, or when the next image is incorporated (at the rising edge of the $\overline{\text{VVS}}$ input) in the case of image capture.

Write 0 to bits that are not used for VSAH0 to VSAH2 and VSAL0 to VSAL2. (a read will return an undefined value).

The VSAR retains the values in a reset.

- VSAR0

Register Address: H'062

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	VSAH0

Register Address: H'064

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	VSAL0
9 to 0	—	—	—	

- VSAR1

Register Address: H'066

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	VSAH1

Register Address: H'068

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	VSAL1
9 to 0	—	—	—	

- VSAR2

Register Address: H'06A

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	VSAH2

Register Address: H'06C

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	VSAL2
9 to 0	—	—	—	

Note: * Value is retained.

5.3.8 Video Window Size Registers (VSIZER)

The video window size registers (VSIZER) specify the video window display size. Set the value obtained by multiplying the number of effective pixels input from off-chip by the reduction (thinning-out) ratio, VSIZ, at the time of capture. Set 0 for the least significant bits of X and Y as shown in the register diagram. This makes the set values of VSIZEX and VSIZEY even numbers.

Write 0 to bits that are not used for the VSIZEX and VSIZEY fields (a read will return an undefined value).

The VSIZER retain their values in a reset.

Register Address: H'06E

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 1	—	*	R/W	VSIZEX
0	—	—	—	

Register Address: H'070

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	*	R/W	
8 to 1	—	—	—	VSIZEY
0	—	—	—	

Note: * Value is retained.

5.3.9 Cursor Area Start Address Register (CSAR)

The cursor area start address registers (CSAR) specify the memory areas used as cursor areas in the UGM. The upper bits (A22 to A16) of the start physical address of the cursor area are set in the cursor area start address high (CSAH) field, and the lower bits (A15 to A11) in the cursor area start address low (CSAL) field.

Set the cursor A shape in the 1024 bytes from the set address, and the cursor B shape in the next 1024 bytes.

The new values set when these registers are modified become effective when internal updating is performed.

Cursor display data should be set in linear address data format.

The CSAL1, CSAL2, CSAH1, and CSAH2 fields in the CSAR registers retain their values in a reset.

The cursor 1 area start addresses are set in CSAH1 and CSAL1. The cursor 2 area start addresses are set in CASH2 and CSAL2.

- CSAR1

Register Address: H'07C

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	*	R/W	CSAL1 (address A15 to A11 setting)
10 to 7	—	—	—	Reserved Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	CSAH1 (address A22 to A11 setting)

- CSAR2

Register Address: H'07E

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	*	R/W	CSAL2 (address A15 to A11 setting)
10 to 7	—	—	—	Reserved Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	CSAH2 (address A22 to A16 setting)

Note: * Value is retained.

5.3.10 Rendering Start Address Register (RSAR)

The rendering start address register (RSAR) specifies the start address of the rendering area that is valid when the RSAE bit is set to 1 in the rendering mode register (REMR).

Only the upper 7 bits (A22 to A16) of the start physical address of the rendering area are set in the RSA field.

The RSA field in the RSAR register retains its value in a reset.

Register Address: H'098

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	Reserved Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	RSA (address A22 to A16 setting)

Note: * Value is retained.

5.4 Display Control Registers

The display control registers are used to set the display timing, and are mapped onto addresses (A10 to A1) H'026 to H'03C, H’052 to H’054, H’058 to H’05A, H’074 to H’07A, and H’200 to H’5FE.

- Display window registers (DSWR)
- Horizontal sync pulse width register (HSWR)
- Horizontal scan cycle register (HCR)

- Vertical start position register (VSPR)
- Vertical scan cycle register (VCR)
- Display off output registers (DOOR)
- Color detection registers (CDER)
- Equalizing pulse width register (EQWR)
- Separation width register (SPWR)
- Video display start position registers (VPR)
- Cursor display start position registers (CSR)
- Color palette registers (CP000R to CP255R)

5.4.1 Display Window Registers (DSWR)

The display window registers (DSWR) specify the horizontal and vertical output timing for the display screen.

1. Horizontal Display Start Position (HDS Fields)
   Field that specifies the horizontal display start position in dot-clock units.
2. Horizontal Display End Position (HDE Fields)
   Field that specifies the horizontal display end position in dot-clock units.
3. Vertical Display Start Position (VDS Fields)
   Field that specifies the vertical display start position in raster-line units.
4. Vertical Display End Position (VDE Fields)
   Field that specifies the vertical display end position in raster-line units.

Write 0 to bits that are not used for the HDS, HDE, VDS, and VDE fields (a read will return an undefined value).

The HDS, HDE, VDS, and VDE fields in the DSWR registers retain their values in a reset.

Register Address: H'026

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	—	—	
8 to 0	—	*	R/W	HDS

Register Address: H'028

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 0	—	*	R/W	HDE

Register Address: H'02A

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	—	—	
8 to 0	—	*	R/W	VDS

Register Address: H'02C

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 0	—	*	R/W	VDE

Note: * Value is retained.

5.4.2 Horizontal Sync Pulse Width Register (HSWR)

The horizontal sync pulse width register (HSWR) specifies the horizontal signal low-level pulse width in dot-clock units.

The HSW bits in the HSWR register retain their values in a reset.

Register Address: H'02E

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	Reserved. Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	HSW

Note: * Value is retained.

5.4.3 Horizontal Scan Cycle Register (HCR)

The horizontal scan cycle register (HCR) specifies the horizontal scan cycle in dot-clock units. In TV sync mode (bits TVM1 and TVM0 set to 10 in DSMR), this register setting must be made so that the $\overline{\text{HSYNC}}$ cycle specified by this register is the same as or greater than the $\overline{\text{EXHSYNC}}$ cycle.

The HC bits in the HCR register retain their values in a reset.

Register Address: H'030

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	—	—	Reserved. Only 0 should be written to these bits (a read will return an undefined value).
10 to 0	—	*	R/W	HC

Note: * Value is retained.

5.4.4 Vertical Start Position Register (VSPR)

The vertical start position register (VSPR) specifies the vertical sync signal start position in raster-line units. In TV sync mode (TVM1 = 1, TVM0 = 0 in DSMR), this register setting must be made so that the $\overline{\text{VSYNC}}$ fall setting position specified by this register is the same as or later than the fall of $\overline{\text{EXVSYNC}}$.

The VSP bits in the VSPR register retain their values in a reset.

Register Address: H'032

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	Reserved. Only 0 should be written to these bits (a read will return an undefined value).
9 to 0	—	*	R/W	VSP

Note: * Value is retained.

5.4.5 Vertical Scan Cycle Register (VCR)

The vertical scan cycle register (VCR) specifies the vertical scan interval, including the vertical retrace line interval, in raster-line units. In TV sync mode (TVM1 = 1, TVM0 = 0 in DSMR), set this register so that the $\overline{\text{VSYNC}}$ rise position set with this register is the same as, or later than, the rise of $\overline{\text{EXVSYNC}}$. If a rise of $\overline{\text{EXVSYNC}}$ is not detected within the vertical scan interval set in this register, the TVR flag in the status register (SR) will be set to 1.

The VC bits in the VCR register retain their values in a reset.

Register Address: H'034

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	Reserved. Only 0 should be written to these bits (a read will return an undefined value).
9 to 0	—	*	R/W	VC

Note: * Value is retained.

5.4.6 Display Off Output Registers (DOOR)

The display off output registers (DOOR) specify the display data to be output when display is off. A 6-bit setting is made for each of the RGB components, in the DOR fields, DOG fields, and DOB fields.

Write 0 to bits that are not used for the DOR, DOG, and DOB fields.

The DOR, DOG, and DOB fields in the DOOR registers retain their values in a reset.

Register Address: H'036

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	—	—	
7 to 2	—	*	R/W	DOR
1, 0	—	—	—	

Register Address: H'038

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	DOG
9, 8	—	—	—	
7 to 2	—	*	R/W	DOB
1, 0	—	—	—	

Note: * Value is retained.

5.4.7 Color Detection Registers (CDER)

The color detection registers (CDER) output 1 from the CDE pin, when the output color data (DD17 to DD0) matches the values set in these registers. For details of the output color data format, see section 3.2.11, Q2SD Internal Data Format. The CDR fields in these registers is compared with DD17 to DD12, the CDG field with DD11 to DD6, and the CDB field with DD5 to DD0. As the display data is all-0 outside the display interval, if an all-0 setting is made in CDER, 1 will be output from the CDE pin outside the display interval.

Write 0 to bits that are not used for the CDR, CDB, and CDG fields.

The CDR, CDG, and CDB fields in the CDER registers retain their values in a reset.

Register Address: H'03A

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	—	—	
7 to 2	—	*	R/W	CDR
1, 0	—	—	—	

Register Address: H'03C

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	CDG
9, 8	—	—	—	
7 to 2	—	*	R/W	CDB
1, 0	—	—	—	

Note: * Value is retained.

5.4.8 Equalizing Pulse Width Register (EQWR)

The equalizing pulse width register (EQWR) specifies the low-level pulse width of $\overline{\text{CSYNC}}$ signal equalizing pulses in dot-clock units. Equalizing pulses are generated at the start and in the middle of each raster.

This register is valid when CYS1 is set to 1 in display mode 2 register (DSMR2).

The EQW bits in the EQWR register retain their values in a reset.

For example, in the case of the NTSC specification, the low-level pulse width is approximately 2.4 µs. If the display operating clock frequency is 14.31818 MHz, a value of 2.4 µs × 14.31818 MHz = 35 should be set in this register.

Register Address: H'052

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	Reserved. Only 0 should be written to these bits (a read will return an undefined value).
6 to 0	—	*	R/W	EQW

Note: * Value is retained.

5.4.9 Separation Width Register (SPWR)

The separation width register (SPWR) specifies the low-level pulse width of $\overline{\text{CSYNC}}$ signal separation pulses in dot-clock units. Separation pulses are generated at the start and in the middle of each raster. Set an SPW value of less than 1/2 the horizontal scan interval.

This register is valid when CYS1 is set to 1 in display mode 2 register (DSMR2).

The SPW bits in the SPWR register retain their values in a reset.

If HC is the horizontal scan interval, in the case of the NTSC specification, for example, the separation pulse low width is approximately HC/2 – 4.7 µs. If HC is 63.555 µs and the display operating clock frequency is 14.31818 MHz, a value of (63.555 µs/2 – 4.7µs) × 14.31818 MHz = 357 should be set in this register.

Register Address: H'054

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	Reserved. Only 0 should be written to these bits (a read will return an undefined value).
9 to 0	—	*	R/W	SPW

Note: * Value is retained.

5.4.10 Video Display Start Position Registers (VPR)

The video display start position registers (VPR) specify the video horizontal and vertical output timing.

1. Video Horizontal Display Start Position (HVP Fields)
   This field sets the video horizontal start position in dot-clock units.
2. Video Vertical Display Start Position (VVP Fields)
   This field sets the video vertical start position in raster-line units.

When the SCM1 and SCM0 bits in the display mode register (DSMR) are set to 11 or 10 (interlace sync & video mode or interlace mode), bit 0 in VVP fields should be cleared to 0.

Set the start position so that the video display area does not extend beyond the frame buffer display screen. Unlike the HDS and VDS fields in the display window registers (DSWR), the screen coordinate upper-left reference values should be set in the HVP and VVP fields. In the horizontal direction the upper-left point is 0, and the right direction is positive, with changes made one by one in dot units. In the vertical direction the upper-left point is 0, and the downward direction is positive, with changes made one by one in line units.

Write 0 to bits that are not used for the HVP and VVP fields (a read will return an undefined value).

The HVP and VVP bits in the VPR (HVP/VVP) registers retain their values in a reset.

Register Address: H'058

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 0	—	*	R/W	HVP

Register Address: H'05A

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	—	—	
8 to 0	—	*	R/W	VVP

Note: * Value is retained.

5.4.11 Cursor Display Start Position Registers (CSR)

The cursor display start position registers (CSR) specify the cursor 1 and 2 horizontal and vertical output timing and the length of the cursor blink shape A and B display intervals.

1. Cursor 1 Horizontal Display Start Position (HCS1)
   These bits set the cursor 1 horizontal display start position in dot-clock units.
2. Cursor 1 Vertical Display Start Position (VCS1)
   These bits set the cursor 1 vertical display start position in raster-line units.
3. Cursor 2 Horizontal Display Start Position (HCS2)
   These bits set the cursor 2 horizontal display start position in dot-clock units.
4. Cursor 2 Vertical Display Start Position (VCS2)
   These bits set the cursor 2 vertical display start position in raster-line units.
5. Cursor Blink Shape A Display Interval Length (BLNKA)
   These bits set, in field units, the length of the interval during which cursor shape A (stored in the cursor area) is displayed. These bits should not be cleared to 0. This field is used for both cursor 1 and cursor 2. Display shape switching is performed simultaneously for both cursors.
6. Cursor Blink Shape B Display Interval Length (BLNKB)
   These bits set, in field units, the length of the interval during which cursor shape B (stored in the cursor area) is displayed. These bits should not be cleared to 0. This field is used for both cursor 1 and cursor 2. Display shape switching is performed simultaneously for both cursors.

The cursor is 32×32 pixels in size, and is displayed in the color assigned in the color palette register. Set the start positions so that the upper-left coordinates of the cursor display area do not extend outside the frame buffer display screen. Also set the start positions so that cursors 1 and 2 do not overlap, as cursor 1 will have priority and cursor 2 will be lost in this case.

Unlike the HDS and VDS fields in the display window registers (DSWR), the screen coordinate upper-left reference values should be set in the HCS and VCS fields. In the horizontal direction the upper-left point is 0, and the right direction is positive, with changes made one by one in dot units. In the vertical direction the upper-left point is 0, and the downward direction is positive, with changes made one by one in line units.

In cursor blinking, in the cursor display A interval, the 1024 bytes of data from the address specified by the cursor area start address register are used for display. In the cursor display B interval, the 1024 bytes of data from the location obtained by adding 1024 bytes to the address specified by the cursor area start address register are used for display.

Write 0 to bits that are not used for the HCS1, VCS1, HCS2, VCS2, BLINKA, and BLINKB fields (a read will return an undefined value).

The HCS1, VCS1, HCS2, VCS2, BLINKA, and BLINKB bits in the CSR registers retain their values in a reset.

Register Address: H'074

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	BLNKA
9 to 0	—	*	R/W	HCS1

Register Address: H'076

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	R/W	BLNKB
9	—	—	—	
8 to 0	—	*	R/W	VCS1

Register Address: H'078

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	—	R/W	
8 to 0	—	*	R/W	HCS2

Register Address: H'07A

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	—	R/W	
8 to 0	—	*	R/W	VCS2

Note: * Value is retained.

5.4.12 Color Palette Registers (CP000R to CP255R)

The color palette is mapped onto addresses (A10 to A1) H'200 to H'5FE. Settings can be made for 256 colors, with 6 bits each for R, G, and B. The color palette can only be used in 8-bit/pixel mode.

When the color palette is accessed by the CPU, bits GBM2 to GBM0 in the rendering mode register (REMR) should be set to 000, 010, 100, or 110.

In the Q2SD, the color palette set values are retained regardless of the GBM values.

- CP000R

Register Address: H'200

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	—	—	
7 to 2	—	*	R/W	R000 (Red: 6 bits)
1, 0	—	—	—	

Register Address: H'202

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	G000 (Green: 6 bits)
9, 8	—	—	—	
7 to 2	—	*	R/W	B000 (Blue: 6 bits)
1, 0	—	—	—	

- CP001R

Register Address: H'204

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	—	—	
7 to 2	—	*	R/W	R001 (Red: 6 bits)
1, 0	—	—	—	

Register Address: H'206

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	G001 (Green: 6 bits)
9, 8	—	—	—	
7 to 2	—	*	R/W	B001 (Blue: 6 bits)
1, 0	—	—	—	

- CP002R

  :

- CP255R

Register Address: H'5FC

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	—	—	
7 to 2	—	*	R/W	R255 (Red: 6 bits)
1, 0	—	—	—	

Register Address: H'5FE

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	*	R/W	G255 (Green: 6 bits)
9, 8	—	—	—	
7 to 2	—	*	R/W	B255 (Blue: 6 bits)
1, 0	—	—	—	

Note: * Value is retained.

5.5 Rendering Control Registers

The rendering control registers are 16-bit registers, mapped onto addresses (A10 to A1) H'03E to H'040, H’080 to H’096, and H’09A. Before the current pointer register (CURR), local offset register (LCOR), user clipping area register (ULCR), system clipping area register (SCLR), or return address register (RTNR) is read, the RBRK of the system control register (SYSR) must be set to 1, and BRK must be 1. When these values are read when BRK is not 1, an invalid value may be read.

- Command status registers (CSTR)
- Current pointer registers (CURR)
- Local offset registers (LCOR)
- User clipping area registers (UCLR)
- System clipping area registers (SCLR)
- Return address registers (RTNR)

5.5.1 Command Status Registers (CSTR)

The command status registers (CSTR) store the address of the command word (op code word) being executed when a frame change is performed.

The upper bits (A22 to A16) of the command word address are indicated by the CSTH field, and the lower bits (A15 to A1) by the CSTL field. The address indicated by the CSTH and CSTL fields is a word address.

Bits that are not used for the CSTH and CSTL fields are always read as 0.

The CSTH and CSTL fields in the CSTR registers retain their values in a reset.

Register Address: H'03E

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
9 to 0	—	*	R	CSTH (address A22 to A16 setting)

Register Address: H'040

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	*	R	CSTL (address A15 to A1 setting)
0	—	—	—	

Note: * Value is retained.

5.5.2 Current Pointer Registers (CURR)

The current pointer registers (CURR) indicate the current pointer coordinates.

When these registers are read, bits that are not used for the XC and YC fields are always read as 0.

The XC and YC bits in the CURR registers retain their values in a reset.

Register Address: H'080

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	XC

Register Address: H'082

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	YC

Note: * Value is retained.

5.5.3 Local Offset Registers (LCOR)

The local offset registers (LCOR) indicate the offset coordinates.

When these registers are read, bits that are not used for the XO and YO fields are always read as 0.

The XO and YO bits in the LCOR registers retain their values in a reset.

Register Address: H'084

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	XO

Register Address: H'086

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	YO

Note: * Value is retained.

5.5.4 User Clipping Area Registers (UCLR)

The user clipping area registers (UCLR) indicate the user clipping area.

When these registers are read, bits that are not used for the UXMIN, UYMIN, UXMAX, and UYMAX fields are always read as 0.

The UXMIN, UYMIN, UXMAX, and UYMAX bits in the UCLR registers retain their values in a reset.

Register Address: H'088

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	UXMIN (upper-left X)

Register Address: H'08A

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	UYMIN (upper-left Y)

Register Address: H'08C

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	UXMAX (upper-left X)

Register Address: H'08E

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	UYMAX (upper-left Y)

Note: * Value is retained.

5.5.5 System Clipping Area Registers (SCLR)

The system clipping area registers (SCL) indicate the system clipping area.

When these registers are read, bits that are not used for the SXMAX, and SYMAX fields are always read as 0.

The SXMAX and SYMAX bits in the SCLR registers retain their values in a reset.

Register Address: H'090

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	SXMAX (upper-right X)

Register Address: H'092

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	—	—	
13	—	*	R	Sign
12 to 0	—	*	R	SYMAX (upper-right Y)

Note: * Value is retained.

5.5.6 Return Address Registers (RTNR)

The return address registers (RTNR) specify the return address.

The upper bits (A22 to A16) of the start address are set in the RTNH field, and the lower bits (A15 to A1) in the RTNL field.

The address (bits A22 to A1) indicated by the RTNH and RTNL fields is a word address.

Write 0 to bits that are not used for the RTNH and RTNL fields (a read will return an undefined value).

The RTNH and RTNL fields in the RTNR registers retain their values in a reset.

Register Address: H'094

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	*	R/W	RTNH (address A22 to A16 setting)

Register Address: H'096

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	*	R	RTNL (address A15 to A1 setting)
0	—	—	—	

Note: * Value is retained.

5.5.7 Color Offset Register (COLOR)

The offset components are treated as signed integers.

This register can be used by the POLYGON4A command. In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in the COLOR register to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the rendering attribute COOF bit must be cleared to 0.

Register Address: H'09A

Bit	Bit Name	Initial Value	R/W	Description
15	—	*	R/W	Sign
14 to 11	—	*	R/W	COOFR (Color offset R) Color offset red component
10	—	*	R/W	Sign
9 to 5	—	*	R/W	COOFG (Color offset G) Color offset green component
4	—	*	R/W	Sign
3 to 0	—	*	R/W	COOFB (Color offset B) Color offset blue component

Note: * Value is retained.

5.6 Data Transfer Control Registers

The data transfer control registers are related to the control of input data transfer and conversion, mapped onto addresses (A10 to A1) H'020 to H'024 and H'042 to H'04A.

5.6.1 DMA Transfer Start Address Registers (DMASR)

The DMA transfer start address registers (DMASR) specify the start address of the transfer destination UGM in a DMA transfer.

The upper bits (A22 to A16) of the start address are set in the DMASH field in DMASR, and the lower bits (A15 to A1) in the DMASL field in DMASR.

If the value of these registers is modified during a series of DMA operations from the time bits DMA1 and DMA0 in the system control register (SYSR) are set to 01 by the CPU until they are cleared automatically by the Q2SD, operation will be unstable.

When bits DMA1 and DMA0 are set to 11, the value in these registers is not referenced. Transfer data passes via the image data entry register (IDER), is converted, and stored sequentially starting at the data transfer start address indicated by the image data transfer start address register (ISAR).

The address (A22 to A1) indicated by the DMASH and DMASL fields is a word address.

Write 0 to bits that are not used for the DMASH and DMASL fields (a read will return an undefined value).

The values of the DMASH and DMASL fields in the DMASR registers are initialized to all-0 by a reset.

These registers are not incremented when DMA transfer is performed.

Register Address: H'020

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	All 0	R/W	DMASH (address A22 to A16 setting)

Register Address: H'022

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R/W	DMASH (address A15 to A1 setting)
0	—	—	—	

5.6.2 DMA Transfer Word Count Registers (DMAWR)

The DMA transfer word count registers (DMAWR) specify the number of words (1 word = 16 bits) to be transferred in DMA transfer.

If the value of these registers is modified during a series of DMA operations from the time bits DMA1 and DMA0 in the system control register (SYSR) are set to 01 or 11 by the CPU until they are cleared automatically by the Q2SD, operation will be unstable.

When bits DMA1 and DMA0 are set to 11, the value in these registers is not referenced. Transfer data passes via the image data entry register (IDER), is converted, and stored sequentially starting at the data transfer start address indicated by the image data transfer start address register (ISAR).

Write 0 to bits that are not used for the DMAWH and DMAWL fields (a read will return an undefined value).

The values of the DMAWH and DMAWL fields in the DMAWR registers are initialized to all-0 by a reset.

These registers are not decremented when DMA transfer is performed.

Register Address: H'050

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	—	—	
2 to 0	—	All 0	R/W	DMAWH

Register Address: H'054

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R/W	DMAWL

5.6.3 Image Data Transfer Start Address Registers (ISAR)

The image data transfer start address registers (ISAR) specify the image data transfer destination as a physical address when the setting of bits YUV2, YUV1, and YUV0 is 001, 010, 011, or 111. The upper bits (A22 to A16) of the start address are set in the ISAH field, and the lower bits (A15 to A1) in the ISAL field. The address indicated by the ISAH and ISAL fields is a word address.

If the value of these registers is modified during a series of data conversion operations from the time bits YUV2, YUV1, and YUV0 are set to 001, 010, 011, or 111 by the CPU until YUV mode is cleared automatically by the Q2SD, operation will be unstable.

Write 0 to bits that are not used for the ISAH and ISAL fields.

The values of the ISAH and ISAL fields in the ISAR registers are initialized to all-0 by a reset.

These registers are not incremented when image data is transferred.

Register Address: H'042

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	—	—	
6 to 0	—	All 0	R/W	ISAH (address A22 to A16 setting)

Register Address: H'044

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R/W	ISAL (address A15 to A1 setting)
0	—	—	—	

5.6.4 Image Data Size Registers (IDSR)

The image data size registers (IDSR) specify the image data X size and Y size when the setting of bits YUV2, YUV1, and YUV0 is 001, 010, 011, or 111. For the image data X size, set the number of pixels when bits YUV2, YUV1, and YUV0 = 001, 010, or 011, and set 1/2 the number of pixels when bits YUV2, YUV1, and YUV0 = 111. An even number should be set for the X size (IDSX0 bit = 0).

If the value of these registers is modified during a series of data conversion operations from the time bits YUV2, YUV1, and YUV0 are set to 001, 010, 011, or 111 by the CPU until YUV mode is cleared automatically by the Q2SD, operation will be unstable.

Write 0 to bits that are not used for the IDSX and IDSY fields.

The values of the IDSX and IDSY bits in the IDSR registers are initialized to all-0 by a reset.

Register Address: H'046

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	—	—	
10 to 0	—	All 0	R/W	IDSX*

Register Address: H'048

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	—	—	
9 to 0	—	All 0	R/W	IDSY

5.6.5 Image Data Entry Register (IDER)

The image data entry register (IDER) comprises the entry in which image data is input when the setting of bits YUV2, YUV1, and YUV0 is 001, 010, 011, or 111.

The IDER is initialized to H'0000 by a reset.

Register Address: H'048

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	W	IDE

6.1 Power-On Sequence

The timing of the CLK0, CLK1, and RESET signals at power-on is shown in figure 6.1. Set 50 ms or less as the time from the rising edge of VCCn to the rising edge of CLK0/CLK1, and 100 ms or more as the time from the rising edge of VCCn to the rising edge of RESET. If CLK0 and CLK1 are halted for a long time (50 ms or more) after powering on, the device may be permanently damaged.

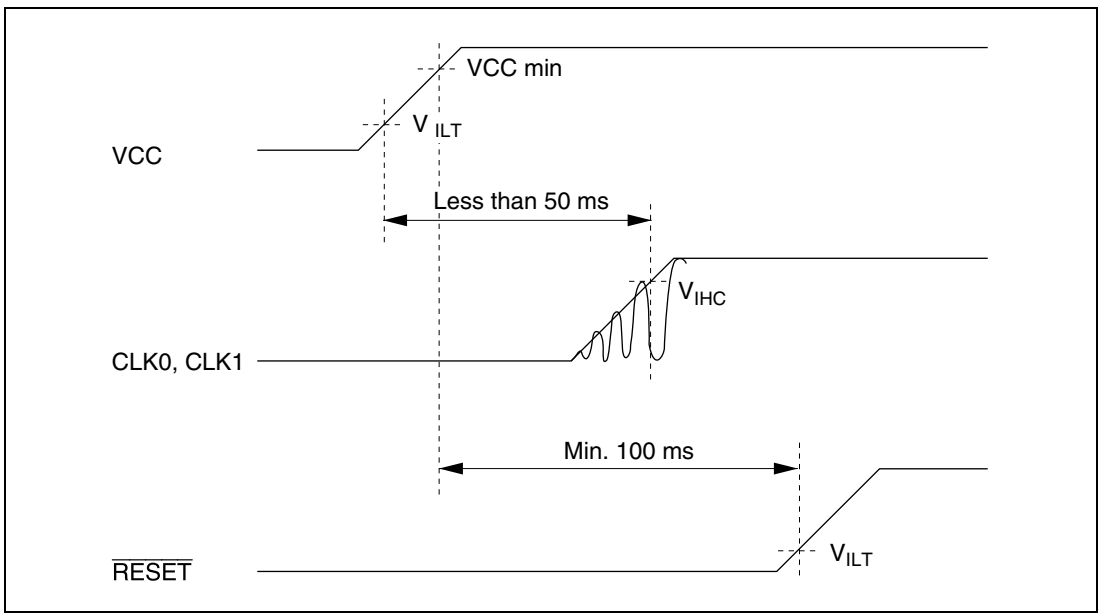


Figure 6.1 Power-On Sequence

6.2 Use of 64-Mbit SDRAM (×16 Type)

The Q2SD references the value of bits MES1 and MES0 in the memory mode register (MMR) following the elapse of 70 tcyc0 after a hardware reset, and makes the UDQM1 pin the MA13 signal output pin if MES1 and MES0 = B′10, or the upper word upper byte input/output mask signal output pin if MES1 and MES0 = B′00. If the setting of MES1 and MES0 has not been carried out by this time, the values of MES1 and MES0 cleared by a hardware reset will be referenced.

Therefore, only when using the MES1 and MES0 = 1, 0 mode (64-Mbit (×16) memory size, one memory used, 16-bit bus), the MES1, MES0 = 1, 0 setting must be made before the elapse of 70 tcyc0 after a hardware reset.

6.3 CPU Interface Unit FIFO

The Q2SD stores the display list which is sent from the CPU to the UGM via a 16-word on-chip FIFO. The CPU gives the rendering start instruction to the Q2SD after the transfer of display list. However, note that when the rendering start address is within the last 16-word data at the end of the display list, the Q2SD may fetch the previous fetch-starting data on the UGM before the completion of flushing the FIFO caused by the start of rendering. To avoid the such previous data from being fetched, CPU must perform UGM dummy read after the display list transfer, and give instruction to start rendering to the Q2SD.

- Rendering start bit (RS)

  When RS is set to 1, starts fetching the data (display list) on the UGM from the address that is shown by the display list start address register (DLASR).
- Display list start address register (DLSAR)

  Register that stores the display list fetching start address.

6.4 Video Fetching Start Timing

Data is captured at the timing of detecting two rising edges of the VHS signal after detecting VVS = 1 and VHS = 1. The VQCLK must be input only for necessary data.

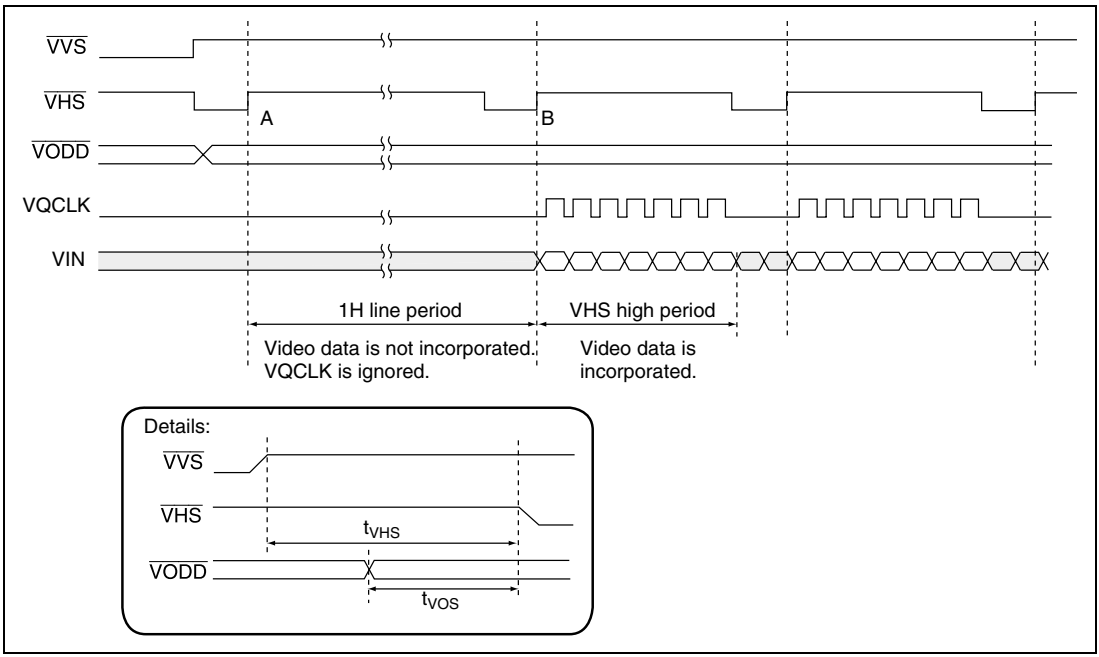


Figure 6.2 Video Interface Timing

6.5 Drawing Using Linear Format Source

When the POLYGON4A, POLYGON4B, PLINE, or RPLINR command is executed with linear format source specified, there is the following restriction regarding the size in the X direction of the linear format source. If a command is executed ignoring the restriction, the error drawing (dot) absence may occur. Use the above commands within the following restrictions.

Product Type	Marking Specifications		Source X Direction Maximum Size					
			1 Bit/Pixel		8 Bits/Pixel		16 Bits/Pixel	
	Marking Type No.	Mask Code	BYTE	TDX (pixel)	BYTE	TDX (pixel)	BYTE	TDX (pixel)
HD64413AF	HD64413AF	None	1 to 32	8 to 256	8 to 32	8 to 32	16 to 32	8 to 16
HD64413AFI	HD64413AFI	None	1 to 32	8 to 256	8 to 32	8 to 32	16 to 32	8 to 16
HD64413ASF	HD64413AF	S	1 to about 128	8 to 1023	8 to 1023	8 to 1023	8 to 1023	8 to 1023
HD64413ASFI	HD64413AFI	S	1 to about 128	8 to 1023	8 to 1023	8 to 1023	8 to 1023	8 to 1023

Note: TDX: Source X direction size (pixel)
Products with restrictions: HD64413AF, HD64413AFI
Products with no restrictions: HD64413ASF, HD64413ASFI

6.6 SDRAM Mode Register Values for UGM Set by Q2SD

Initial sequence is executed in order to set the mode register in the SDRAM which is connected as the UGM that is set by the Q2SD. The SDRAM that is used for the UGM must support the following functions that are set by the Q2SD. The mode register settings in the SDRAM are the following fixed values. Please keep in mind that those values depend on mask version of the Q2SD.

Type No.	Marking No.	Process Code	Mask Code	SDRAM Operating Mode Set by the Q2SD
HD64413AF*[4]	HD64413AF	None	None	Burst read & burst write mode, CAS latency 3, burst type is sequential, burst length 1*[1]
HD64413AF*[4]	HD64413AF	I	None	Burst read & burst write mode, CAS latency 3, burst type is sequential, burst length 1*[1]
HD64413ASF	HD64413AF	None	S	Burst read & single write mode, CAS latency 3, burst type is sequential, burst length 1*[2]*[3]
HD64413ASFI	HD64413AF	I	S	Burst read & single write mode, CAS latency 3, burst type is sequential, burst length 1*[2]*[3]

Notes: 1. SDRAM mode register value set by the Q2SD is H'2030. When a single SRAM with the memory capacity of 64 Mbits and data width of 16 bits is used, select a product which the SRAM mode register bit that corresponds to Q2SD MA13 is "don't care".

2. SDRAM mode register value set by the Q2SD is H'2230. When a single SRAM with the memory capacity of 64 Mbits and data width of 16 bits is used, select a product which the SRAM mode register bit that corresponds to Q2SD MA13 is "don't care".

3. Normal operation can be performed by the following SDRAM even though they do not support the burst read & single write mode: MSM56V16160F (Oki Electric Industry Co., Ltd., 2-bank x 512-kword x 16-bit SDRAM F version)

4. The production of the HD64413AF and the HD64413AFI will be discontinued after the HD64413ASF and the HD64413ASFI start mass production.

Section 7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC} *1	–0.3 to +4.6	V
Input voltage	V_{in} *1	–0.3 to V_{CC} +0.3	V
Permissible output low current	$\lvert I_{oL} \rvert$ *2	2	mA
Total permissible output low current	$\lvert \Sigma I_{oL} \rvert$ *3	172	mA
Permissible output high current	$\lvert -I_{oH} \rvert$ *2	2	mA
Total permissible output high current	$\lvert \Sigma(-I_{oH}) \rvert$ *3	172	mA
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Value based on GND = 0 V. Includes DAV_{CC} and $PLLV_{CC}$.
2. The permissible output current is the maximum value of the current drawn in or flowing out from one output pin and one input/output pin.
3. The total permissible output current is the sum of currents drawn in or flowing out from output pins and input/output pins.

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded. In normal operation, it is advisable to observe the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the chip.

7.2 Recommended Operating Conditions

Table 7.2 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC} *1	3.0	3.3	3.6	V
Input low voltage (except CLK0, CLK1)	V_{ILT} *1	0	—	0.6	V
Input low voltage (CLK0, CLK1)	V_{ILC} *1	0	—	0.6	V
Input high voltage (except CLK0, CLK1)	V_{IHT} *1	2.2	—	V_{CC}	V
Input high voltage (CLK0, CLK1)	V_{IHC} *1	$0.8V_{CC}$	—	V_{CC}	V
Operating temperature	T_{opr} *2	0	25	70	°C

Notes: 1. Value based on GND = 0 V.
2. For details on the product with the operating temperature of -40°C to 85°C, please contact your Hitachi sales agency.

7.3 Electrical Characteristics Test Methods

7.3.1 Timing Testing

The output low voltage for timing testing is 1.5 V. The output high voltage for timing testing is 1.5 V.

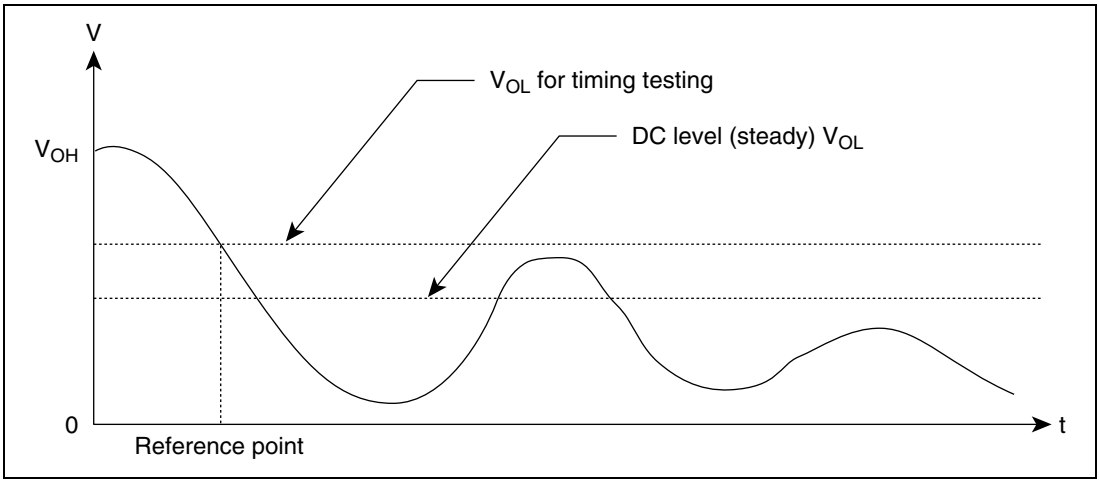


Figure 7.1 Basis of V_{OL} Timing Testing

7.3.2 Test Load Circuit (All Output and Input/Output Pins)

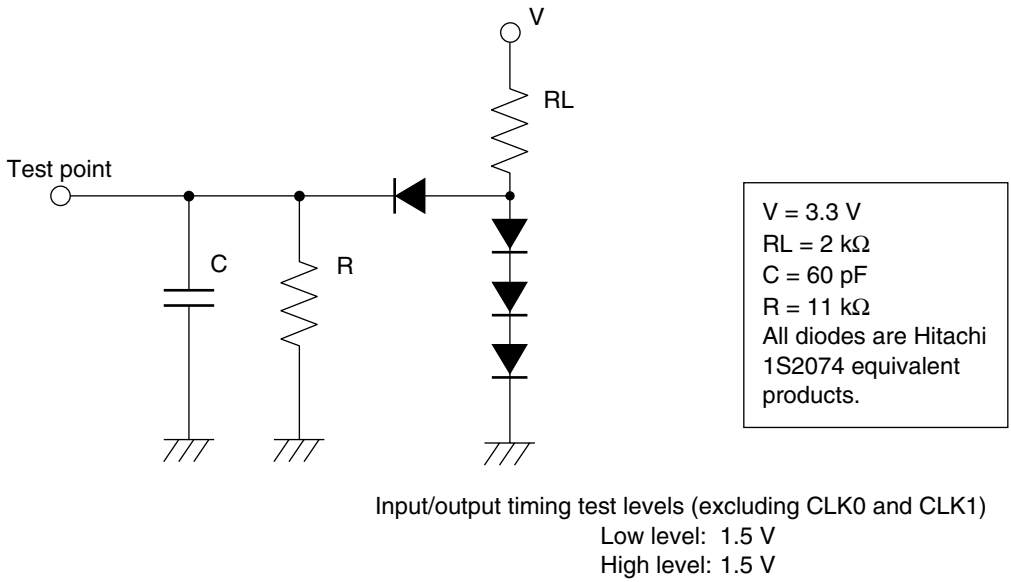


Figure 7.2 Test Load Circuit

7.4 Electrical Characteristics

7.4.1 DC Characteristics

Table 7.3 DC Characteristics

Unless otherwise indicated, V_{CC} = $DACV_{CC}$ = $PLLV_{CC}$ = 3.3 V ±0.3 V, GND = DACGND = PLLGND = 0 V, T_a = 0 to +70°C.

Each value listed below is target one. Some values are reflected the result of the test of sample chips.

Item	Pin Names	Symbol	Min	Max	Unit	Test Conditions
Input high voltage (CMOS level)	I1	V_{IHC}	0.8 × V_{CC}	V_{CC} + 0.3	V	
Input low voltage (CMOS level)		V_{ILC}	–0.3	V_{CC} × 0.2		
Input high voltage (TTL level)	I2, IO	V_{IHT}	2.2	V_{CC} + 0.3	V	
Input low voltage (TTL level)		V_{ILT}	–0.3	V_{CC} × 0.2		
Input leakage current	I1, I2	I_{in}	—	1	µA	V_{in} = 0 – V_{CC}
Three-state leakage current (off state)	IO, O	I_{TSI}	—	1		V_{in} = 0.4 – V_{CC}
Output high voltage	IO, O	V_{OH}	2.2	—	V	I_{OH} = –200 µA
Output low voltage	IO, O	V_{OL}	—	0.6		I_{OL} = 1.6 mA
Input capacitance	IO	C_{in}	—	20	pF	V_{in} = 0 V
	I1, I2		—	20		T_a = 25°C
						f = 1.0 MHz
Current consumption		I_{CC}	—	350	mA	Data bus operating/display operating/ command being executed

Note: The symbols used in table 7.3 are explained below.

Symbol	Input	Output	High-Z	Pull-up	Pin Names
I1	CMOS	—	—	—	CLK0, CLK1
I2	TTL	—	—	—	MOD2 to MOD0, $\overline{\text{RESET}}$, A22 to A1, $\overline{\text{CS1}}$, $\overline{\text{CS0}}$, $\overline{\text{RD}}$, $\overline{\text{WE1}}$, $\overline{\text{WE0}}$, $\overline{\text{DACK}}$, VIN7 to VIN0, $\overline{\text{VHS}}$, $\overline{\text{VVS}}$, $\overline{\text{VODD}}$, VQCLK
IO	TTL	CMOS	Yes	—	D15 to D0, $\overline{\text{HSYNC}}$/$\overline{\text{EXHSYNC}}$, $\overline{\text{VSYNC}}$/$\overline{\text{EXVSYNC}}$, $\overline{\text{ODDF}}$, MD31 to MD0
O	—	CMOS	—	—	$\overline{\text{DREQ}}$, $\overline{\text{WAIT}}$, $\overline{\text{IRL}}$, $\overline{\text{CSYNC}}$, DISP, CDE, MA13 to MA0, $\overline{\text{MCS}}$, $\overline{\text{MWE}}$, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, LDQM1, LDQM0, UDQM1, UDQM0, MCLK

7.4.2 AC Characteristics

Clocks

Table 7.4 Input Clocks (Pins MODE2 to MODE0 = 000, 001, or 010: Multiplication On)

Unless otherwise indicated, V_{CC} = $DACV_{CC}$ = $PLLV_{CC}$ = 3.3 V ±0.3 V, GND = DACGND = PLLGND = 0 V, T_a = 0 to +70°C.

Each value listed below is target one. Some values are reflected the result of the test of sample chips.

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
CLK0 cycle time 1	t_{cyc}	15	25	ns	Figure 7.3	×1
CLK0 cycle time 2	t_{cyc}	30	50	ns		×2
CLK0 cycle time 3	t_{cyc}	60	100	ns		×4
CLK0 high pulse width	t_{CPWH}	5.5	—	ns		
CLK0 low pulse width	t_{CPWL}	5.5	—	ns		
MCLK cycle time	t_{cyc0}	15	25	ns		
MCLK high pulse width	t_{CMPWH}	5.0	—	ns		
MCLK low pulse width	t_{CMPWL}	5.0	—	ns		
CLK1 cycle time	t_{cyc1}	30	200	ns		
CLK1 high pulse width	t_{C1PWH}	10	—	ns		
CLK1 low pulse width	t_{C1PWL}	10	—	ns		
CLK1 duty	t_{C1DT}	$0.5t_{cyc1}$ – $0.07t_{cyc1}$	$0.5t_{cyc1}$ + $0.07t_{cyc1}$	ns		
CLK1 rise time	t_{cr}	—	5.0	ns		
CLK1 fall time	t_{cf}	—	5.0	ns		
MCLK rise time	t_{mcr}	—	4.5	ns		
MCLK fall time	t_{mcf}	—	4.5	ns		

Reset

Table 7.5 Reset

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{\text{RESET}}$ low pulse width	t_{RESW}	40	—	t_{cyc0}	Figure 7.4	

Table 7.6 CPU Read Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
Address setup time	t_{ADS}	0	—	ns	Figure 7.5	
Address hold time	t_{ADH}	0	—	ns		1
$\overline{CSn}$ setup time	t_{CSS}	0	—	ns		2
$\overline{CSn}$ hold time	t_{CSH}	0	—	ns		3
$\overline{WAIT}$ cycle start time 1	t_{WAS1}	—	$3t_{cyc0} + 15$	ns		
$\overline{RD}$ high width	t_{RDHW}	t_{cyc0}	—	ns		
Read data setup time with respect to $\overline{WAIT}$	t_{RDDWS}	0	—	ns		
$\overline{WAIT}$ drive time	t_{WAD}	t_{cyc0}	—	ns		
Read data turn-on time	t_{RDDON}	0	—	ns		
Read data hold time	t_{RDDH}	1.5	—	ns		
Read data turn-off time	t_{RDDOF}	1.5	—	ns		
$\overline{WE}$ high width	t_{WEHW}	t_{cyc0}	—	ns		

Notes: 1. Address signals A22 to A1 must be held at least until the rise of $\overline{WAIT}$.

2. If the fall of $\overline{CSn}$ is later than the fall of $\overline{RD}$, the specifications for t_{ADS}, t_{WAS1}, t_{RDDON}, and t_{WEHW} are from the fall of $\overline{CSn}$. $\overline{CSn}$ = $\overline{CS0}$, $\overline{CS1}$.

3. If the rise of $\overline{CSn}$ is earlier than the rise of $\overline{RD}$, the specifications for t_{ADH}, t_{RDDH}, t_{RDDOF}, and t_{WEHW} are from the rise of $\overline{CSn}$. $\overline{CSn}$ = $\overline{CS0}$, $\overline{CS1}$.

Table 7.7 CPU Write Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
Address setup time	t_{ADS}	0	—	ns	Figure 7.6	
Address hold time	t_{ADH}	2	—	ns		
$\overline{CSn}$ setup time	t_{CSS}	0	—	ns		1
$\overline{CSn}$ hold time	t_{CSH}	0	—	ns		2
$\overline{RD}$ high width	t_{RDHW}	t_{cyc0}	—	ns		
$\overline{WAIT}$ drive time	t_{WAD}	t_{cyc0}	—	ns		
$\overline{WAIT}$ cycle start time 2	t_{WAS2}	—	$3t_{cyc0} + 15$	ns		
$\overline{WE}$ high width	t_{WEHW}	t_{cyc0}	—	ns		3
Write data setup time with respect to $\overline{WE}$	t_{WRDES}	$2t_{cyc0}$	—	ns		3
Write data hold time	t_{WRDH}	2	—	ns		

Notes: 1. If the fall of $\overline{CSn}$ is later than the fall of $\overline{WEn}$, the specifications for t_{ADS}, t_{RDHW}, and t_{WAS2} are from the fall of $\overline{CSn}$. $\overline{CSn}$ = $\overline{CS0}$, $\overline{CS1}$; $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.

2. If the rise of $\overline{CSn}$ is earlier than the rise of $\overline{WEn}$, the specifications for t_{ADH}, t_{RDHW}, t_{WRDES}, t_{WRDH}, and t_{WRDOF} are from the rise of $\overline{CSn}$. $\overline{CSn}$ = $\overline{CS0}$, $\overline{CS1}$; $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.

3. $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.

Table 7.8 DMA Write Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{RD}$ high width	t_{RDHW}	t_{cyc0}	—	ns	Figure 7.7 (1), (2), (3), (4)	
$\overline{RD}$ low width	t_{RDLW}	$3t_{cyc0}$	—	ns		
$\overline{WE}$ high width	t_{WEHW}	t_{cyc0}	—	ns		
Write data hold time	t_{WRDH}	2	—	ns		
Write data setup time with respect to $\overline{RD}$	t_{WRDRS}	$2t_{cyc0}$	—	ns		
$\overline{DREQ}$ negate time with respect to $\overline{RD}$	t_{DARN}	—	$3t_{cyc0}$ + 15	ns		
$\overline{DREQ}$ assert time with respect to $\overline{RD}$	t_{DARA}	$3t_{cyc0}$ + 15	—	ns		
$\overline{DACK}$ setup time with respect to $\overline{RD}$	t_{DARS}	0	—	ns		
$\overline{DACK}$ hold time with respect to $\overline{RD}$	t_{DARH}	0	—	ns		
$\overline{DACK}$ setup time with respect to $\overline{WE}$	t_{DAWS}	0	—	ns		
$\overline{DACK}$ hold time with respect to $\overline{WE}$	t_{DAWH}	0	—	ns		
$\overline{WE}$ low width	t_{WELW}	$3t_{cyc0}$	—	ns		
Write data setup time with respect to $\overline{WE}$	t_{WRDWS}	$2t_{cyc0}$	—	ns		
Write data hold time with respect to $\overline{WE}$	t_{WRDWH}	2	—	ns		
$\overline{DREQ}$ negate time with respect to $\overline{WE}$	t_{DAWN}	—	$3t_{cyc0}$ + 15	ns		
$\overline{DREQ}$ hold time with respect to $\overline{WE}$	t_{DAWA}	$3t_{cyc0}$ + 15	—	ns		

Notes:
1. If the fall of $\overline{DACK}$ is later than the fall of $\overline{RD}$, the specification for t_{RDLW} is from the fall of $\overline{DACK}$.
2. If the rise of $\overline{DACK}$ is earlier than the rise of $\overline{RD}$, the specifications for t_{RDLW}, t_{WRDH}, and t_{WRDRS} are from the rise of $\overline{DACK}$.
3. If the fall of $\overline{DACK}$ is later than the fall of $\overline{WEn}$, the specification for t_{WELW} is from the fall of $\overline{DACK}$. $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.
4. If the rise of $\overline{DACK}$ is earlier than the rise of $\overline{WEn}$, the specifications for t_{WELW}, t_{WRDWS}, and t_{WRDWH} are from the rise of $\overline{DACK}$. $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.

Interrupt Output

Table 7.9 Interrupt Output

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{IRL}$ delay time	t_{IRD}	—	15	ns	Figure 7.8	

UGM Read Cycle

Table 7.10 UGM Read Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
MD input setup time	t_{MDIS}	6	—	ns	Figure 7.9	
MD input hold time	t_{MDIH}	3	—	ns		
MD input turn-on time	t_{MDIN}	0	—	ns		
MD input turn-off time	t_{MDIF}	—	9	ns		
MA delay time	t_{MAD}	—	12	ns		
MA hold time	t_{MAH}	1	—	ns		
MD output turn-off time	t_{MDOF}	—	12	ns		
MD output turn-on time	t_{MDON}	0	—	ns		
MCS delay time	t_{MCSD}	—	12	ns		
MCS hold time	t_{MCSH}	1	—	ns		

UGM Write Cycle

Table 7.11 UGM Write Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
MD output delay time	t_{MDOD}	—	12	ns	Figure 7.10	
MD output hold time	t_{MODH}	1	—	ns		
MA delay time	t_{MAD}	—	12	ns		
MA hold time	t_{MAH}	1	—	ns		
MCS delay time	t_{MCSD}	—	12	ns		
MCS hold time	t_{MCSH}	1	—	ns		

UGM Refresh Cycle/Mode Register Setting Cycle

Table 7.12 UGM Refresh Cycle/Mode Register Setting Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
MA delay time	t_{MAD}	—	12	ns	Figure 7.11 (1), (2)	
MA hold time	t_{MAH}	1	—	ns		
MCS delay time	t_{MCSD}	—	12	ns		
MCS hold time	t_{MCSH}	1	—	ns		

Master Display Mode

Table 7.13 Master Display Mode

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{\text{HSYNC}}$ delay time from CLK1	t_{HSDD}	—	15	ns	Figure 7.12	
$\overline{\text{VSYNC}}$ delay time from CLK1	t_{VSDD}	—	15	ns		
$\overline{\text{ODDF}}$ delay time from CLK1	t_{ODDD}	—	15	ns		
$\overline{\text{CSYNC}}$ delay time from CLK1	t_{SYDD}	—	15	ns		
DISP delay time from CLK1	t_{DIDD}	—	15	ns		
CDE delay time from CLK1	t_{CDEDD}	—	15	ns		

Table 7.14 TV Sync Display Mode

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
DISP delay time from CLK1	t_{DIDD}	—	15	ns	Figure 7.13 (1), (2)	
CDE delay time from CLK1	t_{CDEDD}	—	15	ns		
$\overline{\text{EXHSYNC}}$ low width	t_{EXLLW}	$4t_{cyc1}$	—	ns		
$\overline{\text{EXHSYNC}}$ high width	t_{EXHHW}	$4t_{cyc1}$	—	ns		
$\overline{\text{EXHSYNC}}$ reception undefined time 1	t_{EXH1}	5	—	ns		
$\overline{\text{EXHSYNC}}$ reception undefined time 2	t_{EXH2}	5	—	ns		
DISP start time with respect to $\overline{\text{EXHSYNC}}$	t_{DIEXH}	hds – 1	hds – 1	t_{cyc1}		*
$\overline{\text{EXVSYNC}}$ low width	t_{EXVLW}	3HC	—	t_{cyc1}		
$\overline{\text{EXVSYNC}}$ reception undefined time 1	t_{EXV1}	5	—	ns		
$\overline{\text{EXVSYNC}}$ reception undefined time 2	t_{EXV2}	5	—	ns		
$\overline{\text{ODDF}}$ reception undefined time 1	t_{OD1}	(ys + yw) × HC	—	t_{cyc1}		
$\overline{\text{ODDF}}$ reception undefined time 2	t_{OD2}	$1t_{cyc1}$	—	ns		

Note: * hds = hsw + xs

Video Interface

Table 7.15 Video Interface

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
VQCLK high pulse width	t_{QHW}	15	—	ns	Figure 7.14 (1), (2)	
VQCLK low pulse width	t_{QLW}	15	—	ns		
$\overline{\text{VODD}}$ setup time	t_{VOS}	1	—	t_{cyc0}		
VIN setup time	t_{VNS}	5	—	ns		
VIN hold time	t_{VNH}	11.7	—	ns		
$\overline{\text{VVS}}$ low pulse width	t_{VVL}	2	—	Hline		*
$\overline{\text{VHS}}$ low pulse width	t_{VHL}	64	—	t_{cyc0}		
VQCLK rise—VQCLK rise interval	t_{QQP}	34.5	—	ns		$t_{QQP} > 2 \times t_{cyc0}$
$\overline{\text{VODD}}$ hold time	t_{VOH}	1	—	t_{cyc0}		
$\overline{\text{VVS}}$ setup time	t_{VHS}	5	—	t_{cyc0}		
$\overline{\text{VHS}}$ setup time	T_{HQS}	10	—	t_{cyc0}		
$\overline{\text{VHS}}$ reception undefined time	t_{VHSRU}	2	—	Hline		*

Note: * Hline is the $\overline{\text{VHS}}$ cycle.

Video DAC

Table 7.16 Video DAC

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
Resolution		8	8	Bit	DC test	
Differential linearity error		—	0.5	LSB	DC test	
Conversion speed		—	33	MHz	Data write test	
Maximum output current	I_{out}		3	mA		
Analog full-scale output		0.9	1.1	V	DC test	
Analog zero-scale output		–0.1	0.1	V	DC test	
Full-scale error		–10	10	%	DC test	

7.5 Timing Charts

7.5.1 Clocks

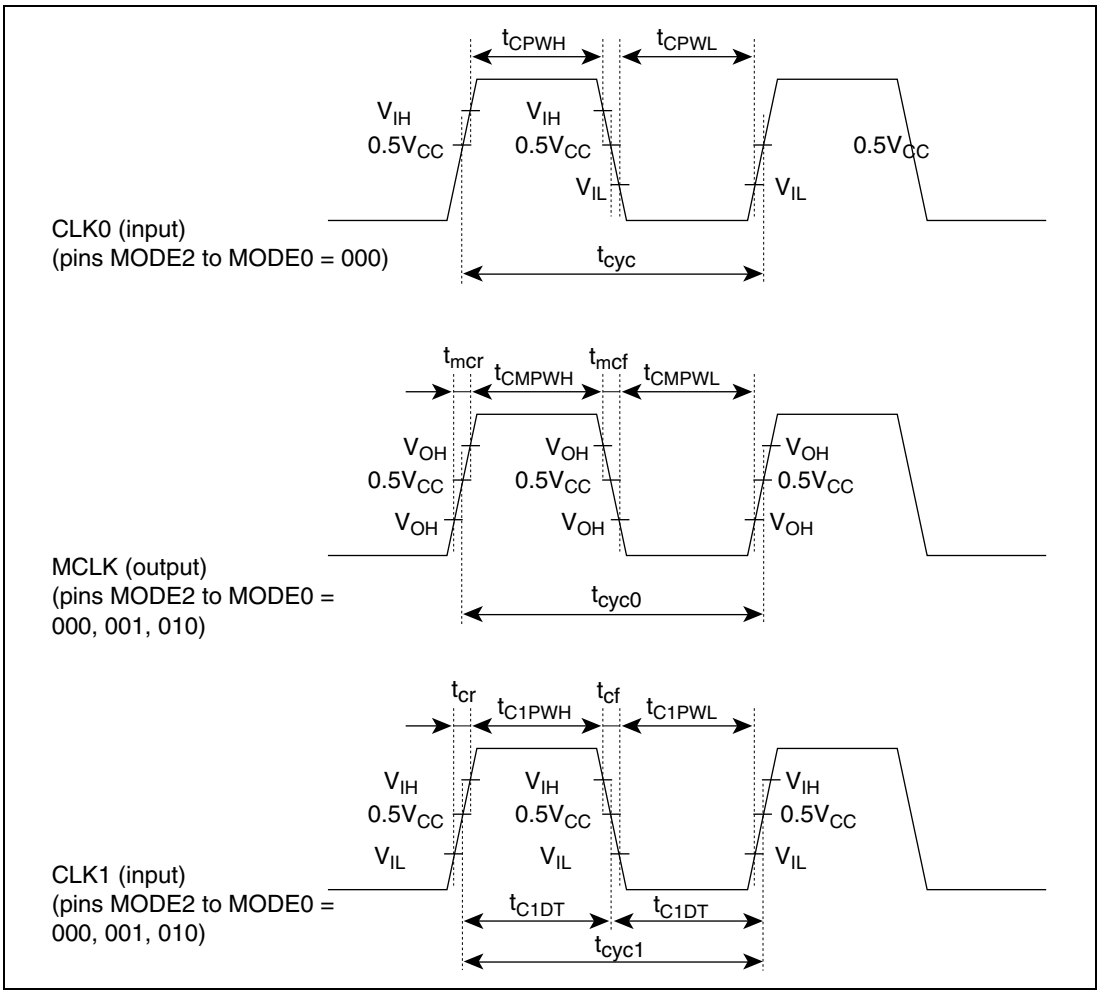


Figure 7.3 Input Clocks

7.5.2 Reset Timing

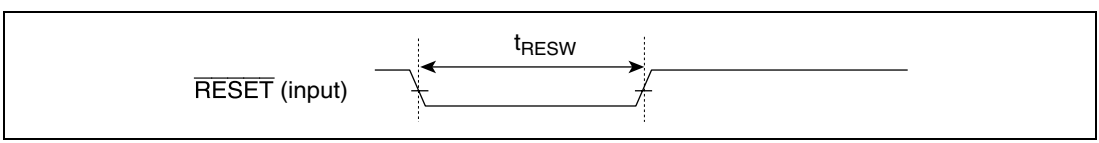


Figure 7.4 Reset Timing

7.5.3 CPU Read Cycle Timing

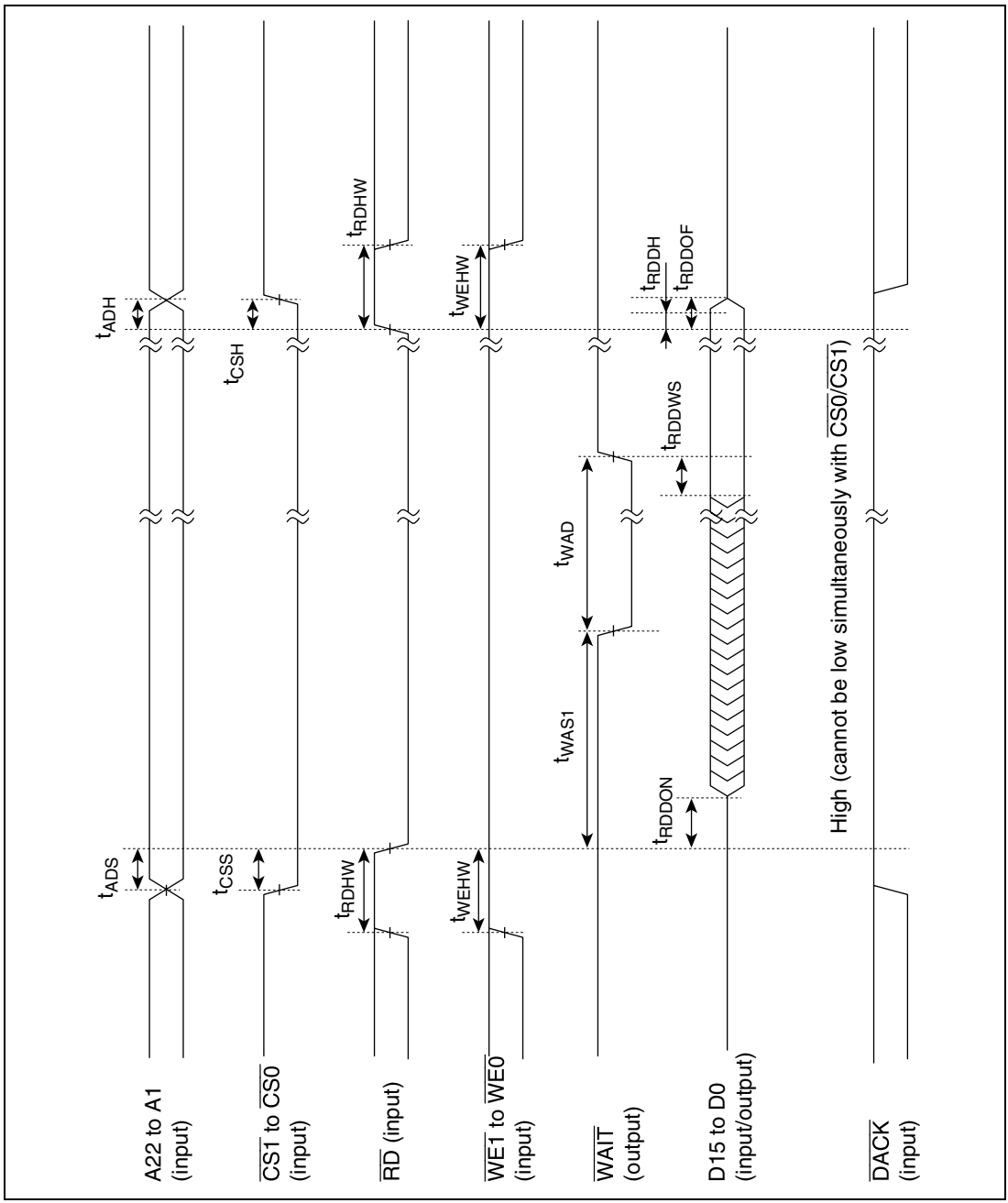


Figure 7.5 CPU Read Cycle Timing (CPU ← Q2SD) with Hardware Wait

7.5.4 CPU Write Cycle Timing

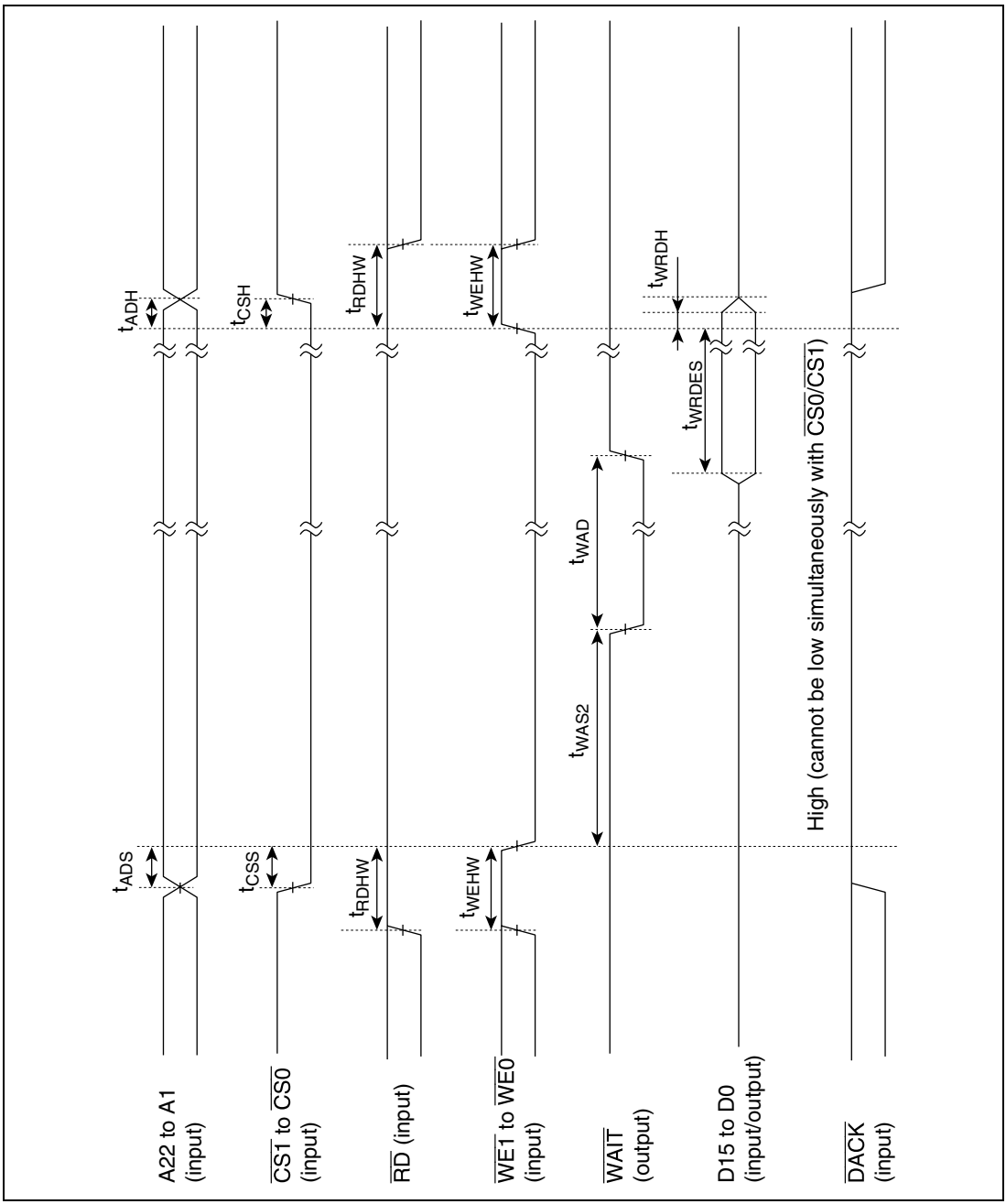


Figure 7.6 CPU Read Cycle Timing (CPU → Q2SD) with Hardware Wait

7.5.5 DMA Write Cycle Timing (DMAC → Q2SD)

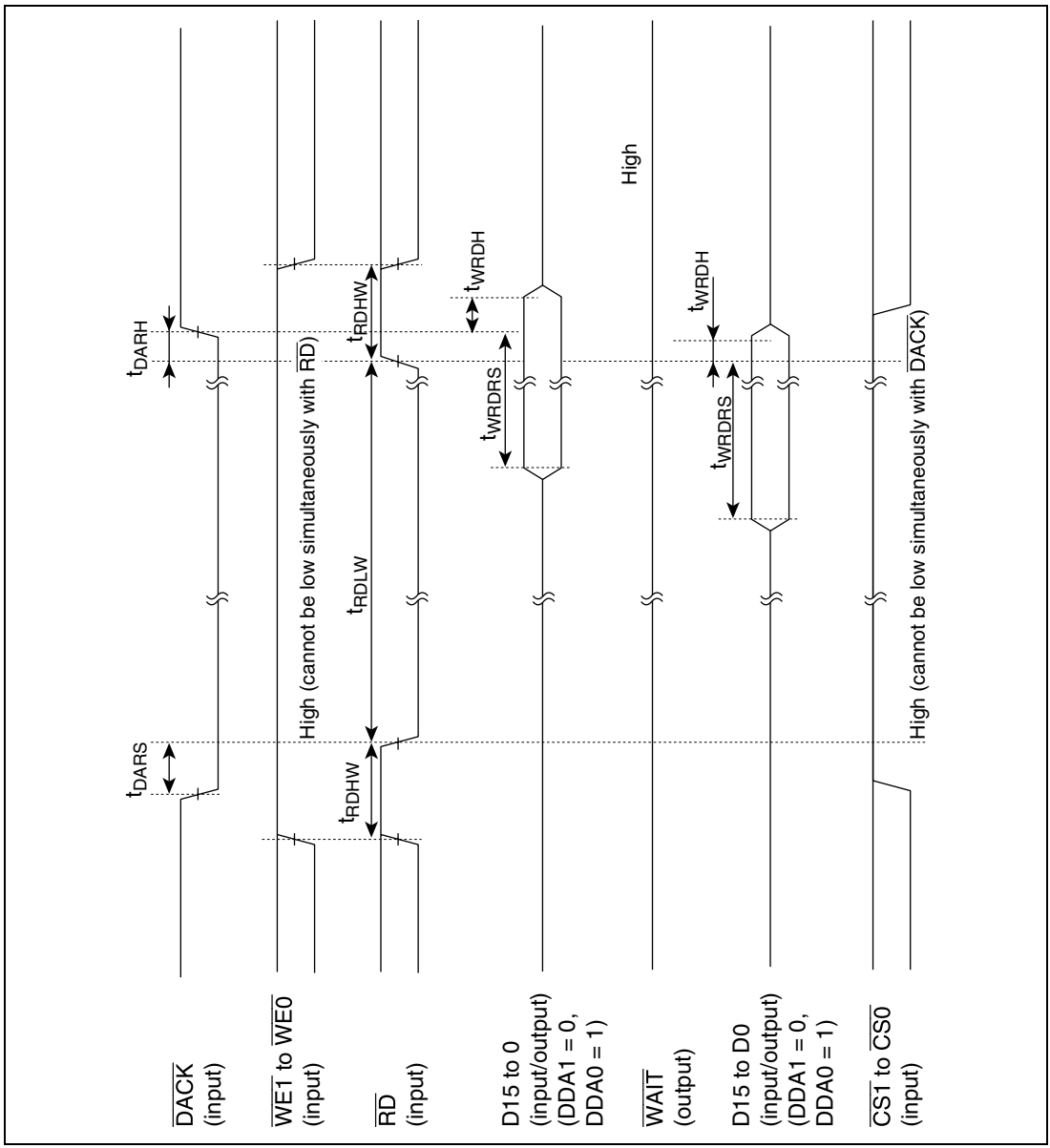


Figure 7.7 (1) DMA Write Cycle Timing (Single Address, DMAC → Q2SD)

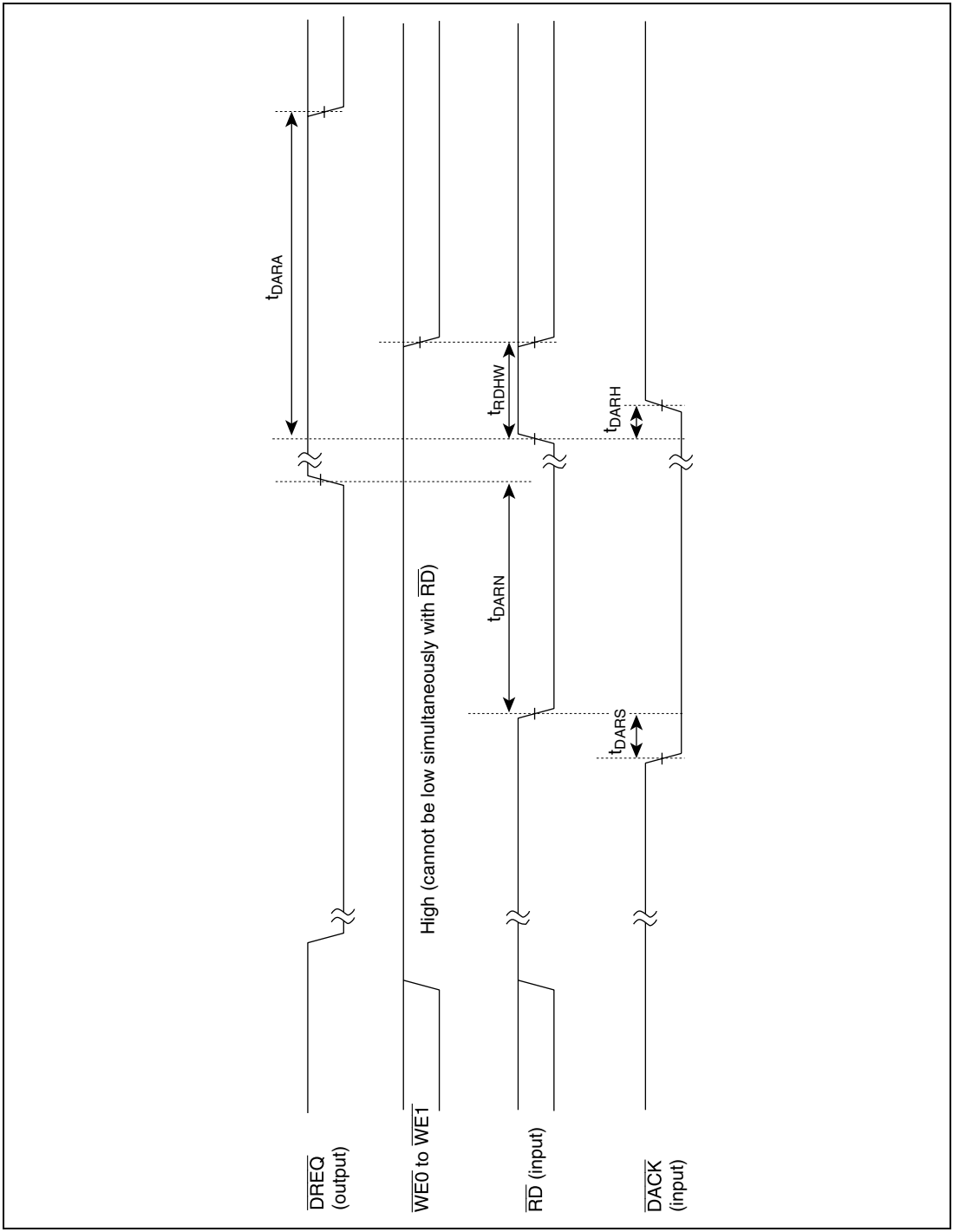


Figure 7.7 (2) DMA Write Cycle Timing (Single Address, DMAC → Q2SD)

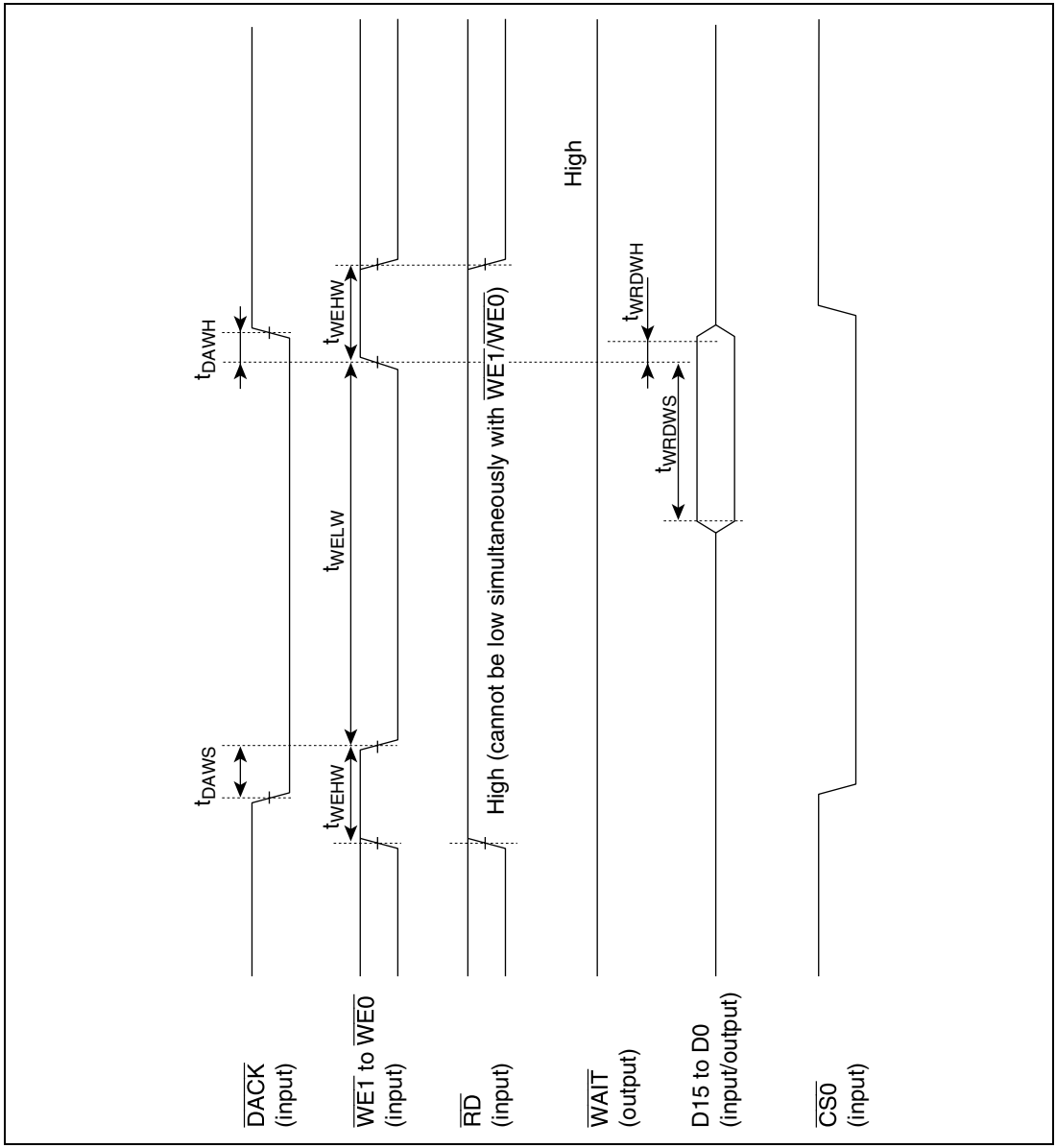


Figure 7.7 (3) DMA Write Cycle Timing (Dual Address, DMAC → Q2SD)

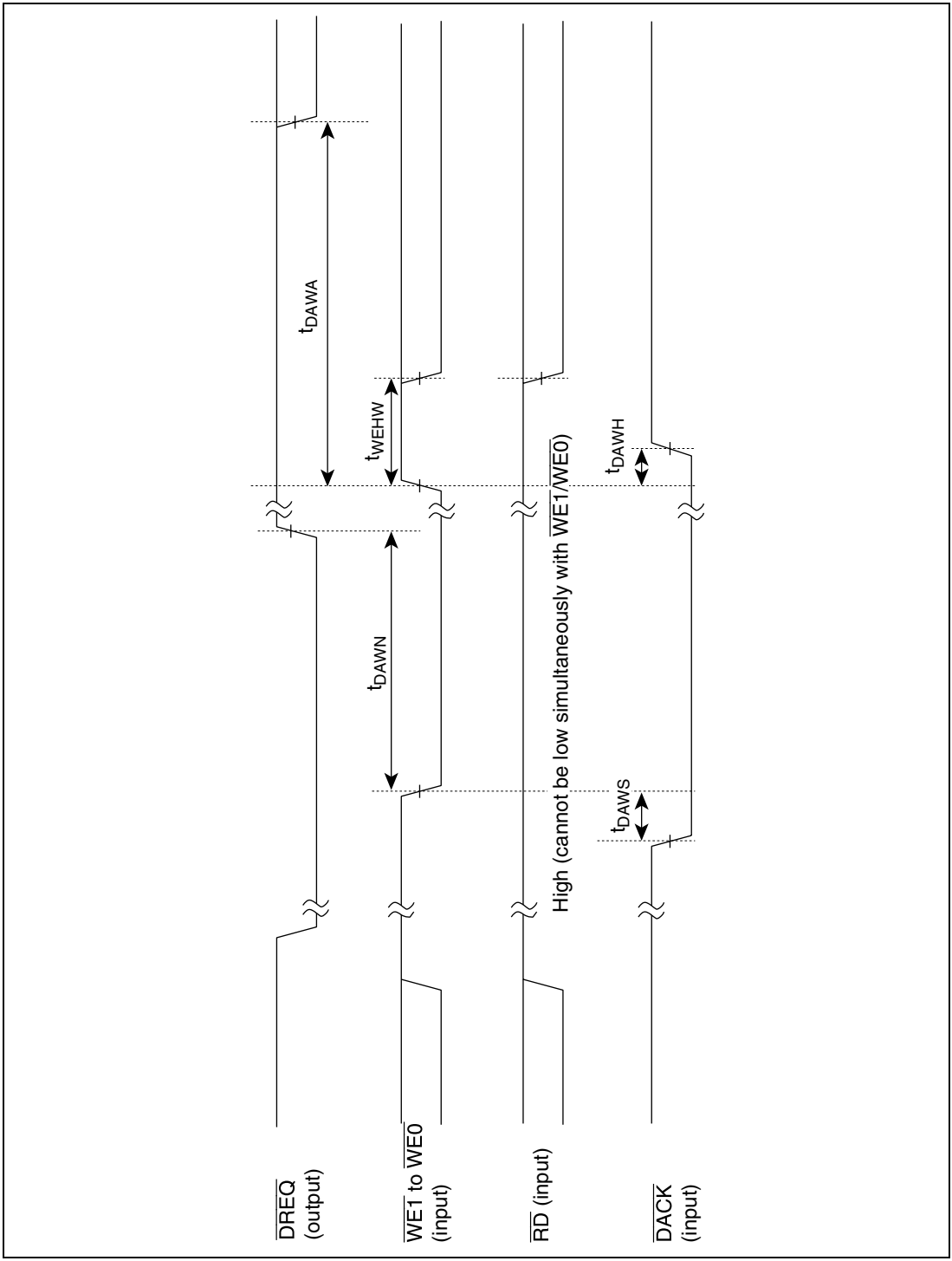


Figure 7.7 (4) DMA Write Cycle Timing (Dual Address, DMAC → Q2SD)

7.5.6 Interrupt Output Timing

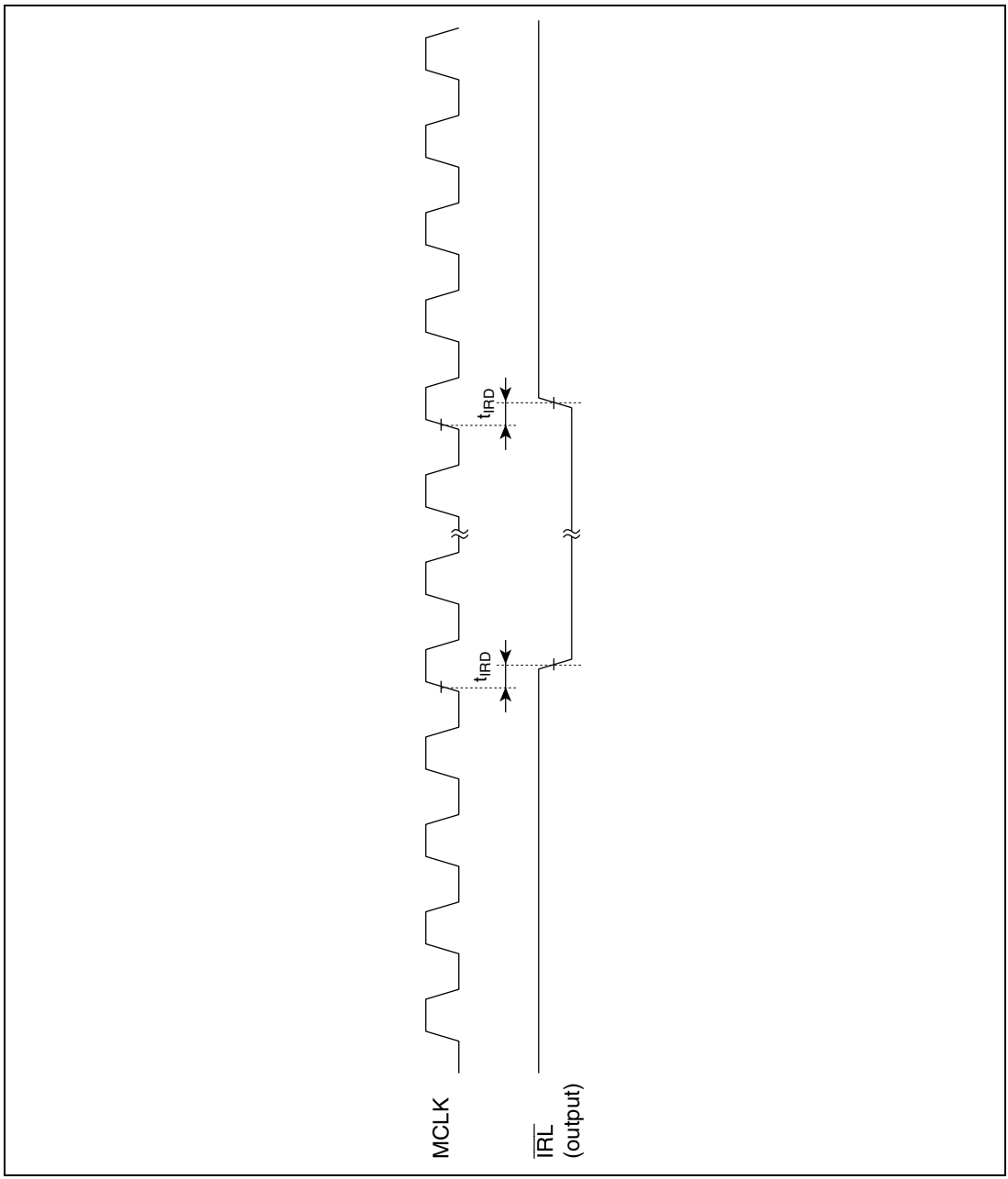


Figure 7.8 Interrupt Output Timing

7.5.7 UGM Read Cycle Timing

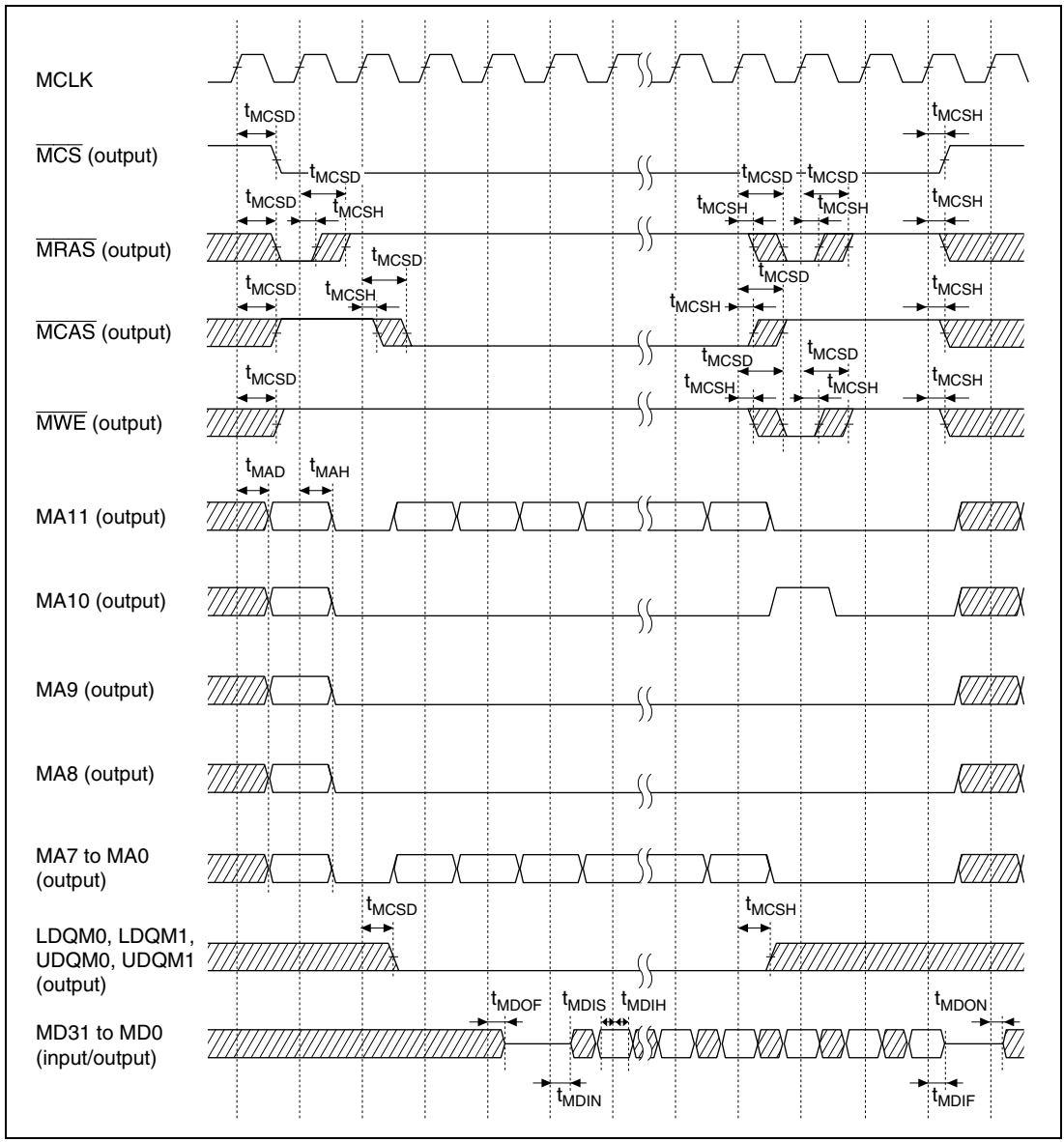


Figure 7.9 UGM Read Cycle Timing

7.5.8 UGM Write Cycle Timing

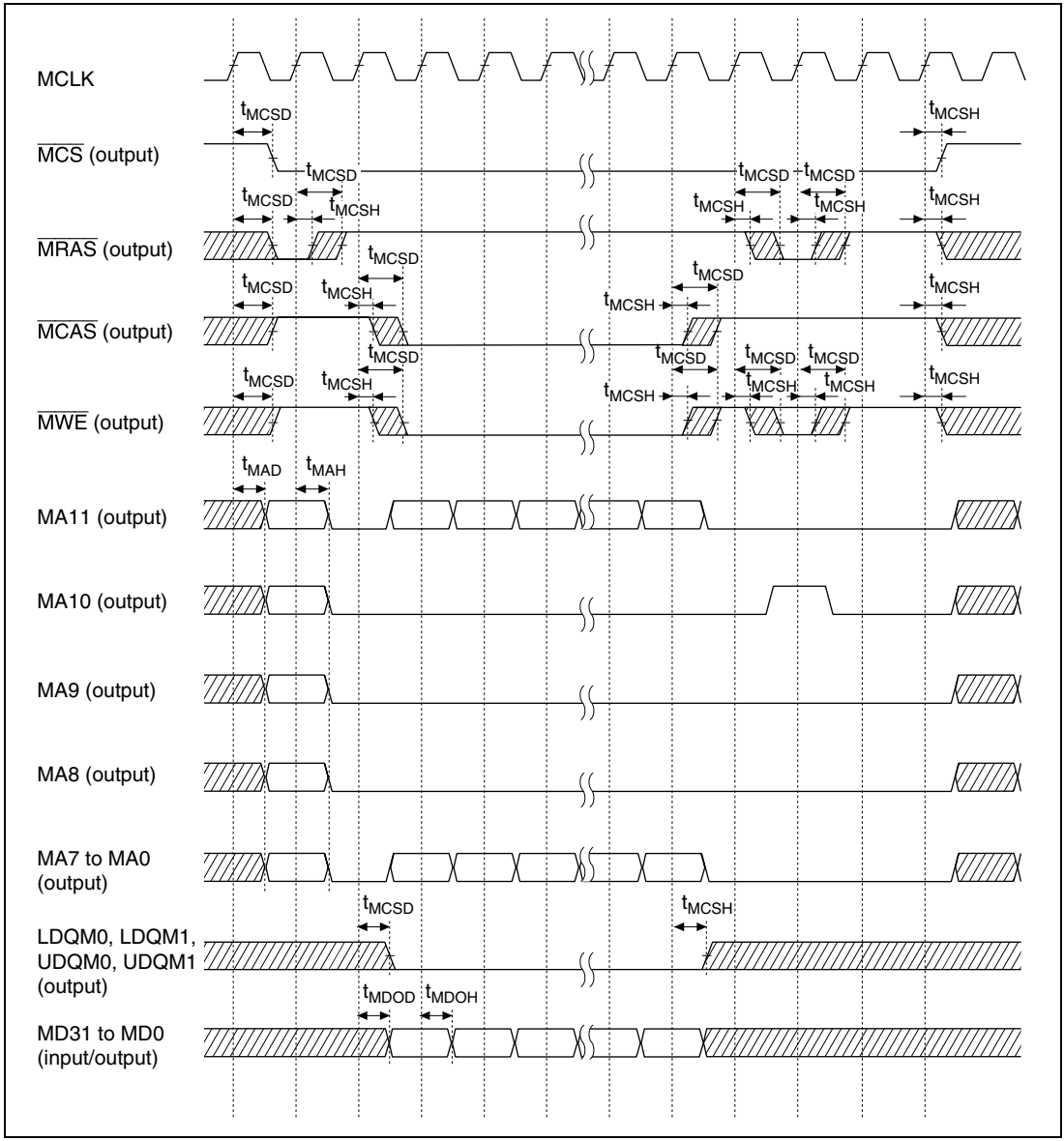


Figure 7.10 UGM Write Cycle Timing

7.5.9 UGM Refresh Cycle Timing and Mode Register Setting Timing

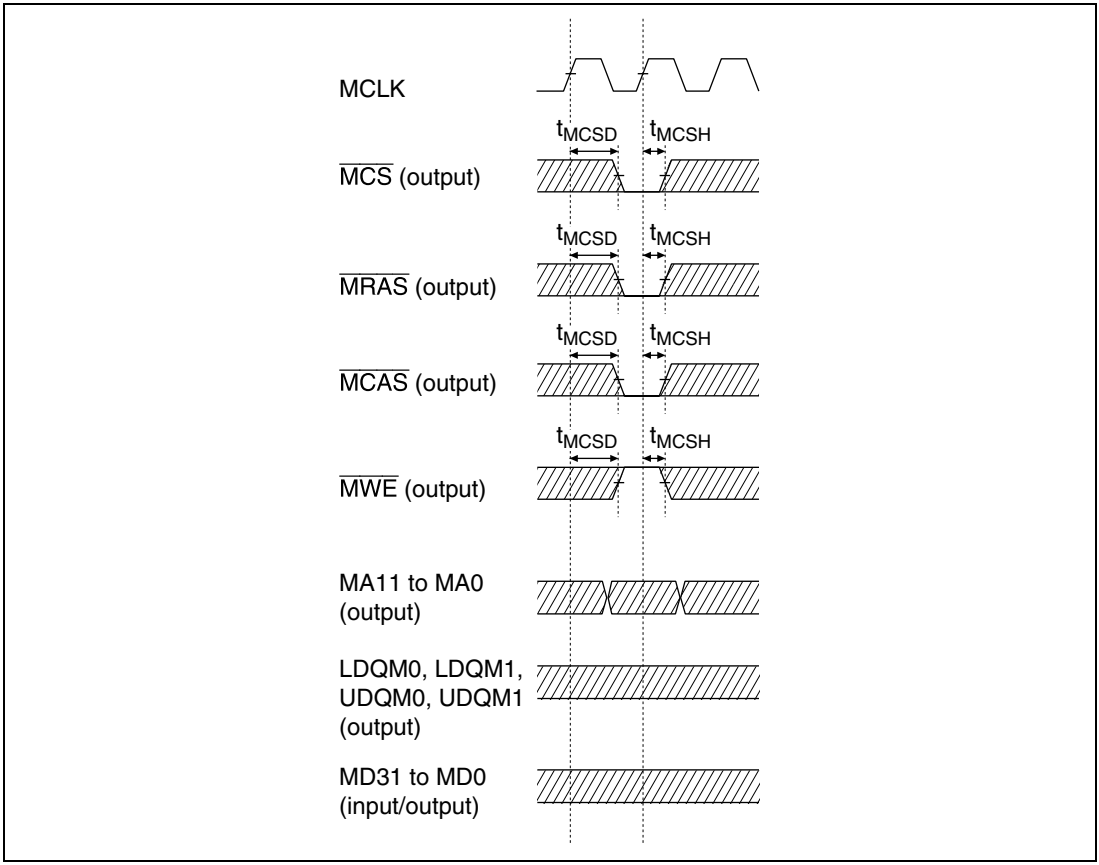


Figure 7.11 (1) UGM Refresh Cycle Timing

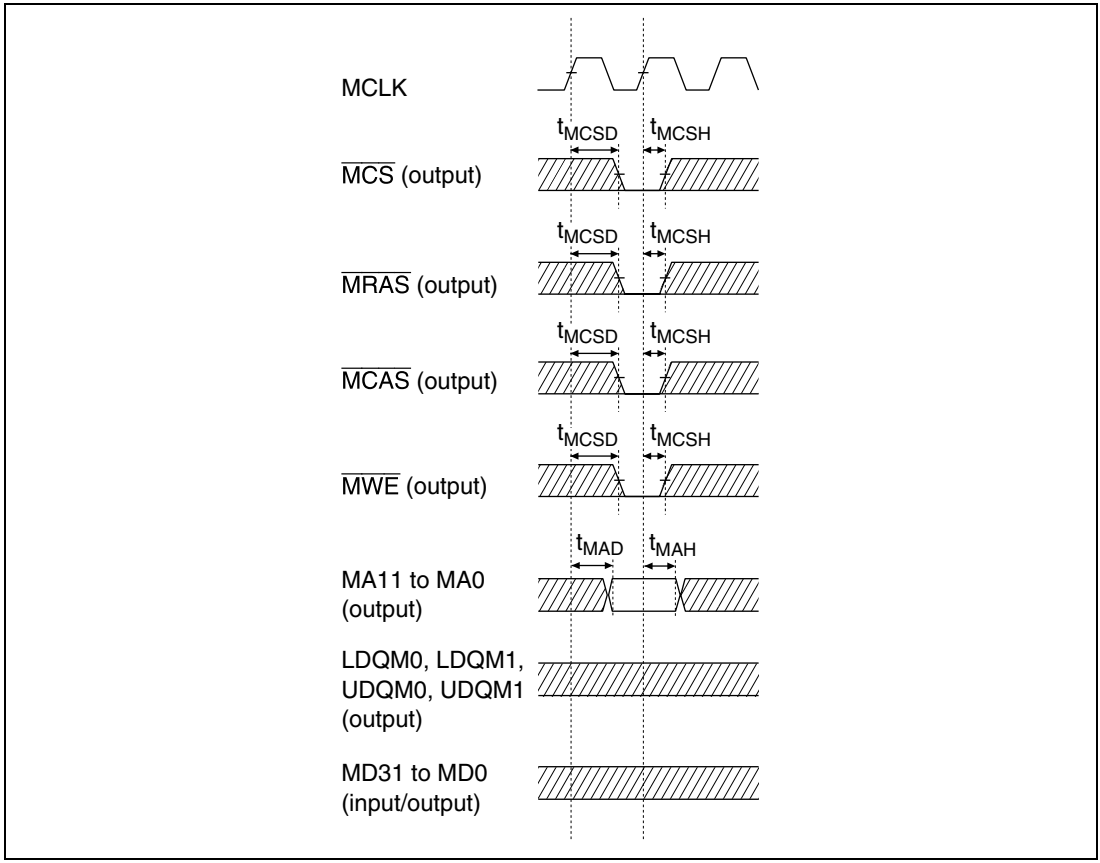


Figure 7.11 (2) UGM Mode Register Setting Cycle Timing

7.5.10 Master Mode Display Timing

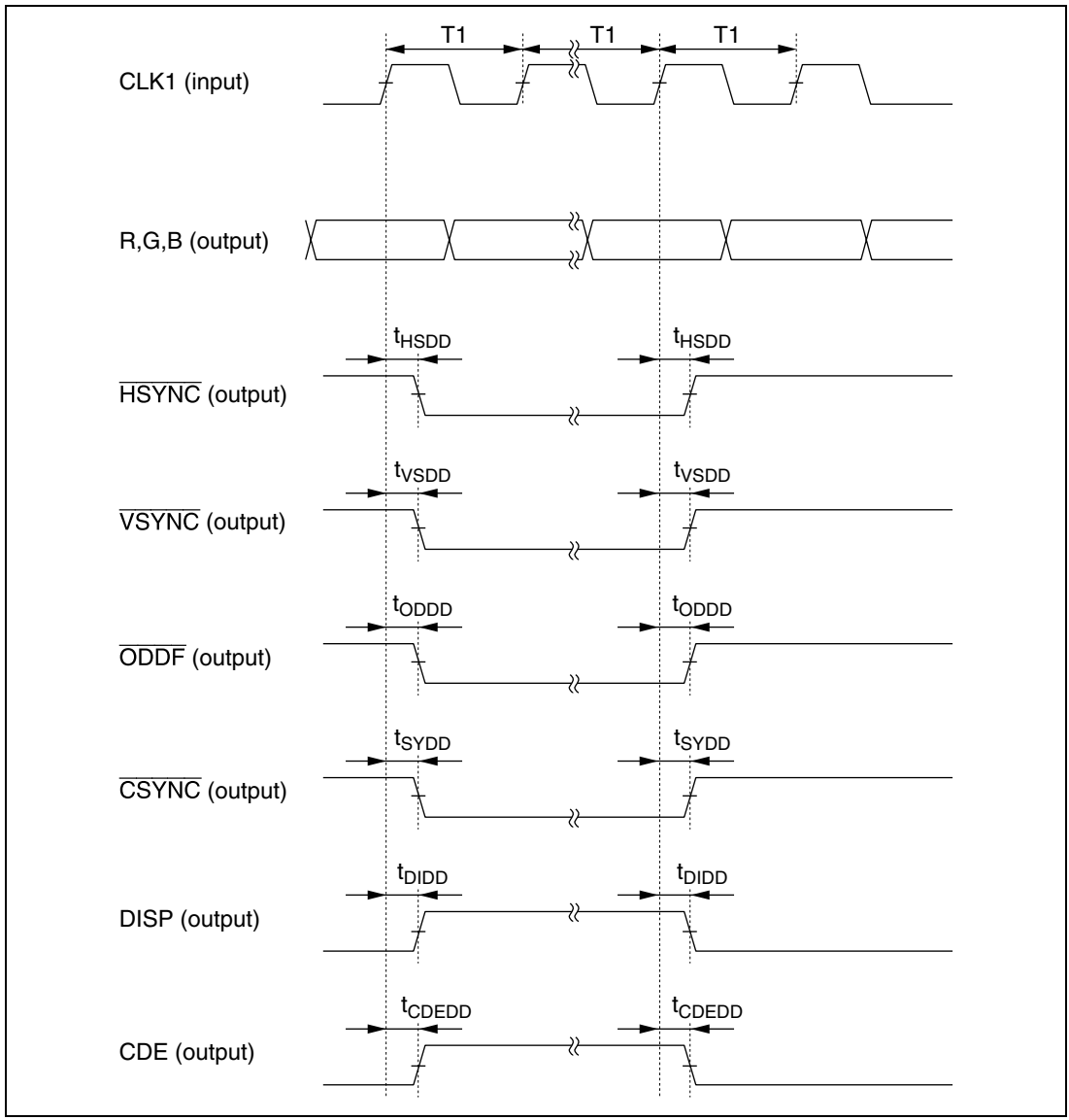


Figure 7.12 Master Mode Display Timing

7.5.11 TV Sync Mode Display Timing

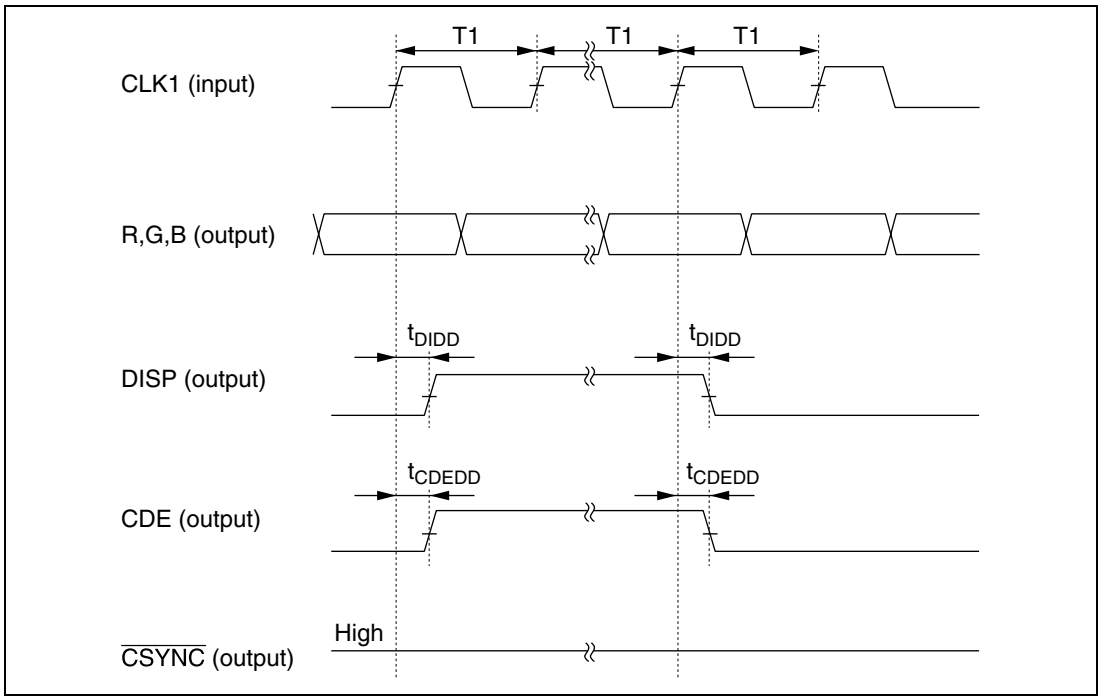


Figure 7.13 (1) TV Sync Mode Display Timing

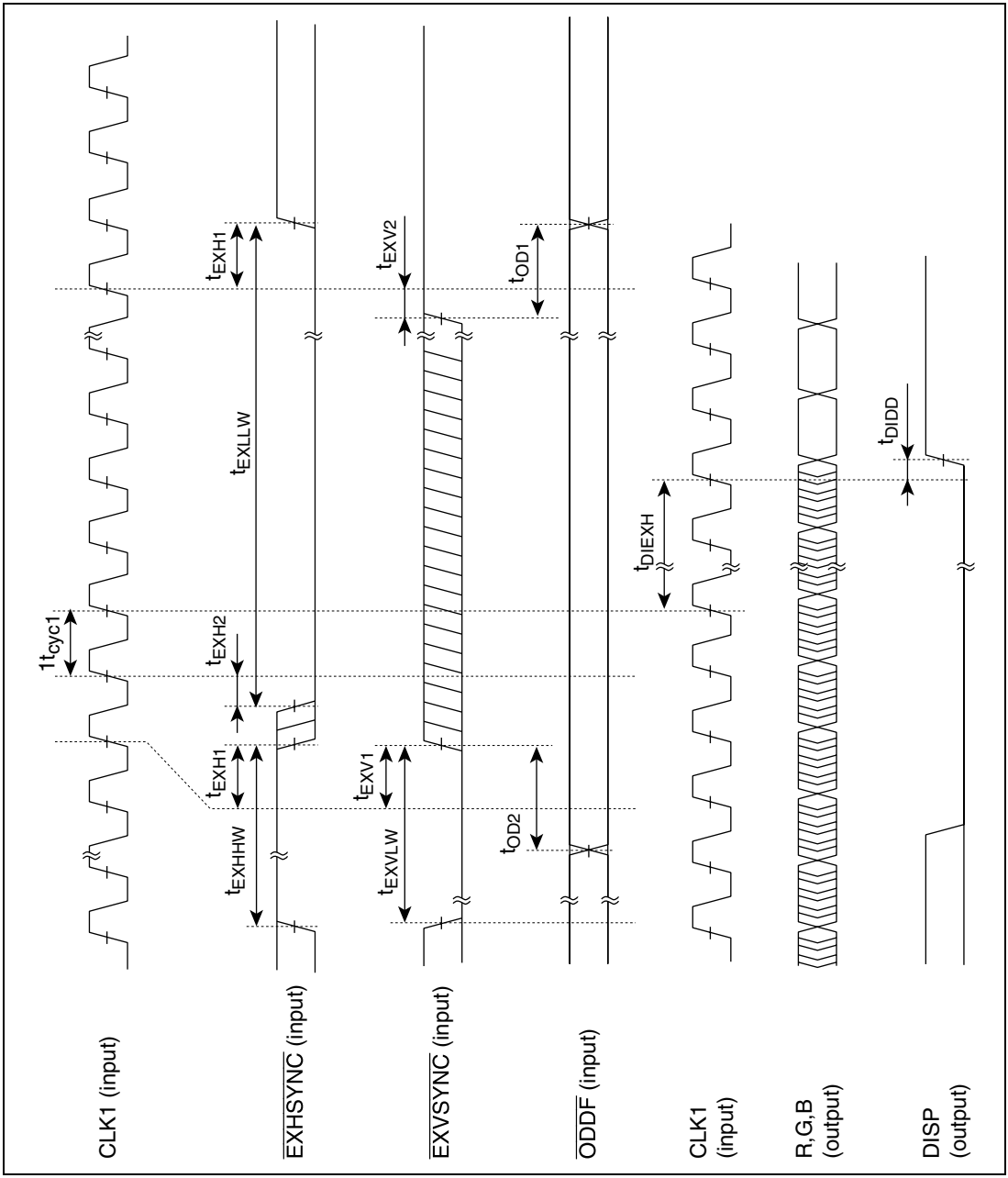


Figure 7.13 (2) TV Sync Mode Display Timing

7.5.12 Video Interface Timing

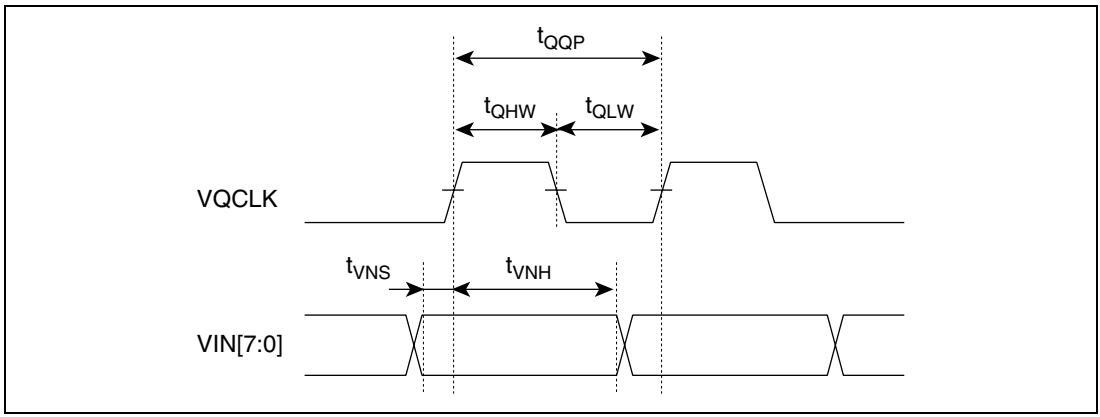


Figure 7.14 (1) Video Interface Timing

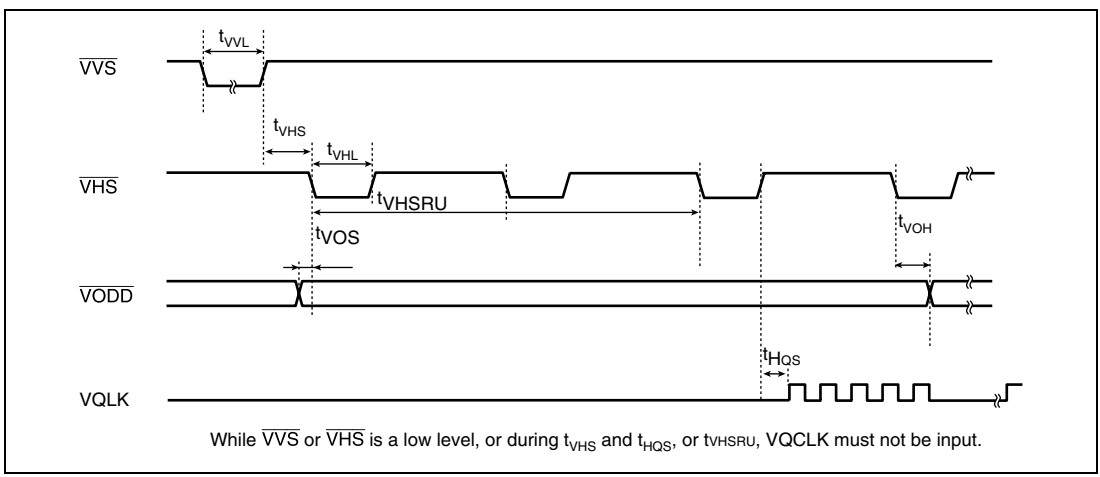


Figure 7.14 (2) Video Interface Timing

Table A.1 Initial Register Values after Hardware Reset

Register Address		R/W	Register Name	Abbreviation	Data															
$\overline{CS1}$	A [10:0]				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	—	—	—	—	—								—							
0	000	R/W	System control	SYSR	1	1	0			0	0	0	DBM1	DBM0	0	0	0	0		
	002	R	Status	SR	0	0	0	0	0	0	0	DBF	0	1			0	1	0	0
	004	W	Status register clear	SRCR	TVCL	FRCL	DMCL	CECL	VBCL	TRCL	CSCL		BRCL							
	006	R/W	Interrupt enable	IER	0	0	0	0	0	0	0		0							
	008	R/W	Memory mode	MEMR											0	0				
	00A	R/W	Display mode	DSMR	0				0	0			1	0	SCM1	SCM0	1	0	0	0
	00C	R/W	Rendering mode	REMR	0									MWX				GBM2	GBM1	GBM0
	00E	R/W	Input data conversion mode	IEMR												0	0	0	0	0
	020	R/W	DMA transfer start address	H DMASR										0	0	0	0	0	0	0
	022	R/W		L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	024	R/W	DMA transfer word count	L DMAWR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	042	R/W	Image data transfer start address	H ISAR									0	0	0	0	0	0	0	0
	044	R/W		L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	046	R/W	Image data size	X IDSR						0	0	0	0	0	0	0	0	0	0	0
	048	R/W		Y							0	0	0	0	0	0	0	0	0	0
	04A	W	Image data entry	IDER	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	050	R/W	DMA transfer word count	H DMAWR														0	0	0
	056	R/W	Display mode 2	DSMR2			0	0	0	0	0	0	CSY1	CSY0	0		0	0	0	0
	072	R/W	Video incorporation mode	VIMR	1	1					0	0	0	0	0	0	0	0	0	0

Only bits marked ☐ are affected by a reset. Registers other than those shown above are not affected by a reset.

B.1 Relationship between Commands and Rendering Attributes

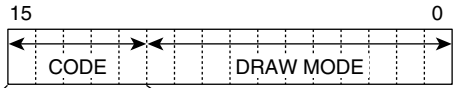
Table B.1 Relationship between Commands and Rendering Attributes

Command	Reference Data				Drawing Destination		Rendering Attributes													
	Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work	TRNS	STYL	CLIP	NET	EOS	HALF	WORK	Bold Line Drawing	FST	LNi	EDG	REL	COOF	Line drawing edge
POLYGON4A	O		A		O		*	*	O	*	*		*		O	*		Z	▲	
POLYGON4B		O	A		O		O	O	O	O	O	▲	O					O		
POLYGON4C			A	O	O				O	*	*		*		O					
LINE				O	O				O	O	O			O						
RLINE				O	O				O	O	O			O						
PLINE		O			O		O	O	O	O	O									O
RPLINE		O			O		O	O	O	O	O									O
FTRAP						O			O		B						O			
RFTRAP						O			O		B						O			
CLRW						O			O											
LINEW				V		O			O		O									
RLINEW				V		O			O		O									
MOVE																				
RMOVE																				
LCOFS																				
RLCOFS																				
CLIP																				
WPR																				
JUMP																		O		
GOSUB																		O		
RET																				
NOP3																				
VBKEM																				
TRAP																				

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
B: Referenced depending on mode (valid when EDG = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)
▲: Can be used with restriction, HALF: x < 0 is prohibited, COOF: miniaturization is prohibited.)

B.2 Command Codes

Table B.2 Command Codes

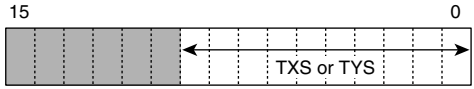


CODE					COMMAND
0	0	0	0	0	POLYGON4A
0	0	0	0	1	POLYGON4B
0	0	0	1	0	POLYGON4C
0	1	0	0	0	FTRAP
0	1	0	0	1	RFTRAP
0	1	0	1	0	LINEW
0	1	0	1	1	RLINEW
0	1	1	0	0	LINE
0	1	1	0	1	RLINE
0	1	1	1	0	PLINE
0	1	1	1	1	RPLINE
1	0	0	0	0	MOVE
1	0	0	0	1	RMOVE
1	0	0	1	0	LCOFS
1	0	0	1	1	RLCOFS
1	0	1	0	0	CLRW
1	0	1	0	1	UCLIP
1	0	1	1	0	WPR
1	0	1	1	1	SCLIP
1	1	0	0	0	JUMP
1	1	0	0	1	GOSUB
1	1	0	1	0	VBKEM
1	1	0	1	1	RET
1	1	1	1	1	TRAP
1	1	1	1	0	NOP3

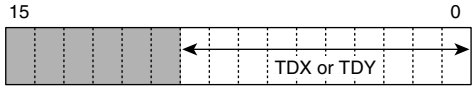
B.3 Command Parameter Specifications

Note that words of the command code are omitted.

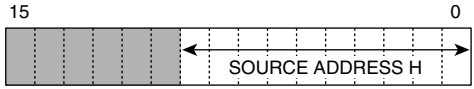
: Fixed at 0



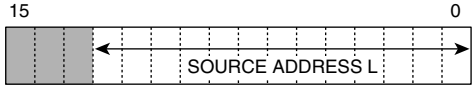
Source starting point TXS or TYS
Given as unsigned max. 10-bit data.
Specify correctly according to source area size.



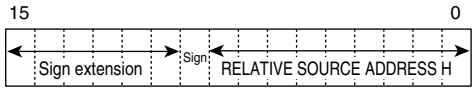
Source size TDX or TDY
Given as unsigned max. 10-bit data.
TDX can only be set in 8-pixel units.



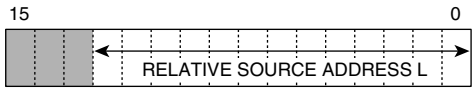
1-bit/pixel source start upper address
Given as upper 10 bits.



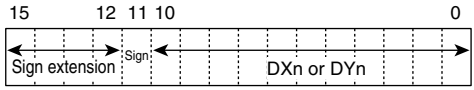
1-bit/pixel source start lower address
Given as lower 13 bits.
Source address is set as a byte address.



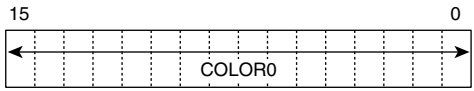
Source start relative upper address
Given as upper 10 bits.
Use sign extension in upper vacant bits.



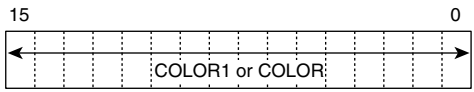
Source start relative lower address
Given as lower 13 bits.



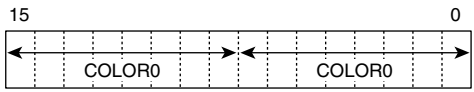
Rendering, work coordinate
Vertex coordinate DXn or DYn ($1 \leq n \leq 4$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



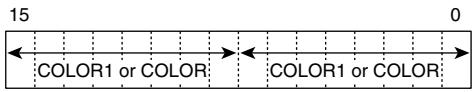
16-bit/pixel color specification
Color data 0 given as 16-bit data.



16-bit/pixel color specification
Color data 1 given as 16-bit data.

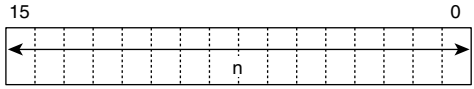


8-bit/pixel color specification
Color data 0 given as repeated 8-bit data.

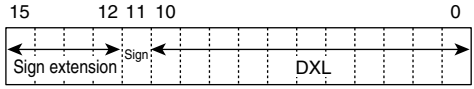


8-bit/pixel color specification
Color data 1 given as repeated 8-bit data.

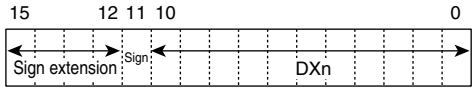
FTRAP, RFTRAP



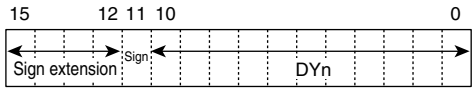
Number of vertices ($2 \le n \le 65,535$), absolute
($1 \le n \le 65,535$), relative
Given as unsigned 16-bit data.



Left-hand side coordinate DXL
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



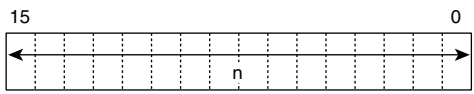
Absolute coordinate
Vertex coordinate DXn ($2 \le n \le 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



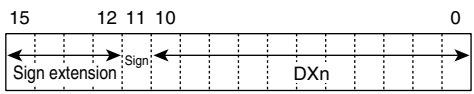
Absolute coordinate
Vertex coordinate DYn ($2 \le n \le 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

Relative coordinates
Vertex coordinates DXn, DYn ($1 \le n \le 65,535$)
Given as signed 8-bit data.

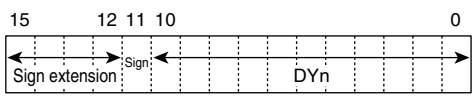
LINEW, RLINEW



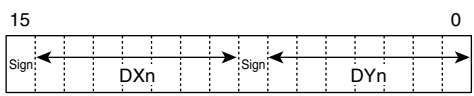
Number of vertices ($2 \le n \le 65,535$), absolute
($1 \le n \le 65,535$), relative
Given as unsigned 16-bit data.



Absolute coordinate
Vertex coordinate DXn ($2 \le n \le 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

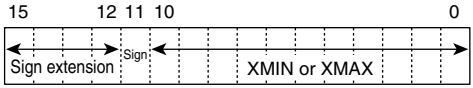


Absolute coordinate
Vertex coordinate DYn ($2 \le n \le 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

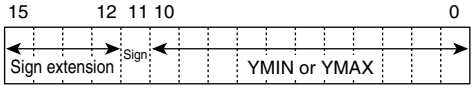


Relative coordinates
Vertex coordinates DXn, DYn ($1 \le n \le 65,535$)
Given as signed 8-bit data.

CLRW

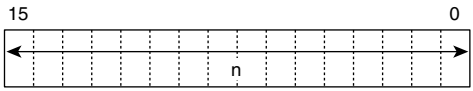


Left and right X coordinates XMIN, XMAX
Given as unsigned 12-bit data.

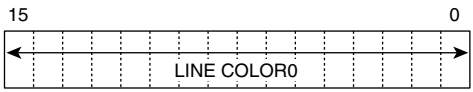


Upper and lower Y coordinates YMIN, YMAX
Given as signed 12-bit data.

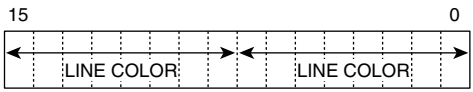
LINE, RLINE



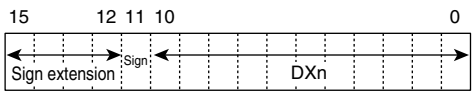
Number of vertices ($2 \leq n \leq 65,535$), absolute
($1 \leq n \leq 65,535$), relative
Given as unsigned 16-bit data.



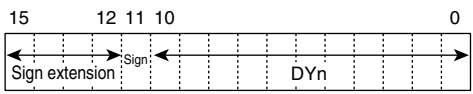
16-bit/pixel color specification
Color data given as 16-bit data.



8-bit/pixel color specification
Color data given as repeated 8-bit data.



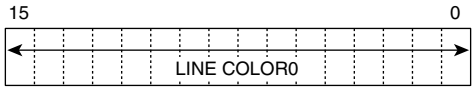
Absolute coordinate
Vertex coordinate DXn ($2 \leq n \leq 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



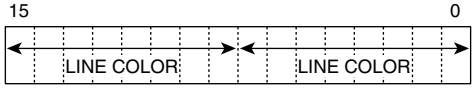
Absolute coordinate
Vertex coordinate DYn ($2 \leq n \leq 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

Relative coordinates
Vertex coordinates DXn, DYn ($1 \leq n \leq 65,535$)
Given as signed 8-bit data.

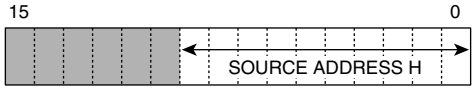
: Fixed at 0



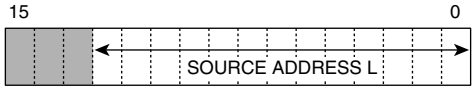
16-bit/pixel color specification
Color data given as 16-bit data.



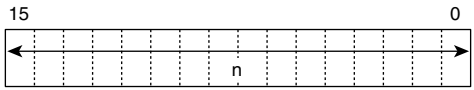
8-bit/pixel color specification
Color data given as repeated 8-bit data.



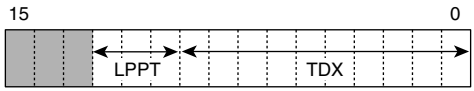
1-bit/pixel source start upper address
Given as upper 10 bits.



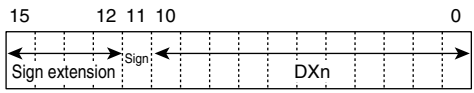
1-bit/pixel source start lower address
Given as lower 13 bits.
Source address is set as a byte address.



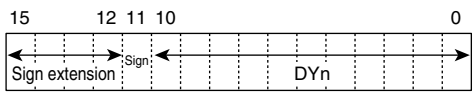
Number of vertices ($2 \leq n \leq 65,535$), absolute
($1 \leq n \leq 65,535$), relative
Given as unsigned 16-bit data.



Source size TDX
Line pattern pointer LPPT
Given as unsigned max. 10-bit data.
TDX can only be set in 8-pixel units.



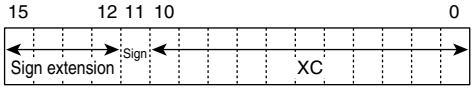
Absolute coordinate
Vertex coordinate DXn ($2 \leq n \leq 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



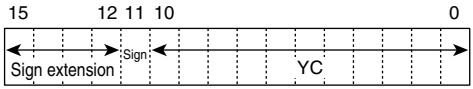
Absolute coordinate
Vertex coordinate DYn ($2 \leq n \leq 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

Relative coordinates
Vertex coordinates DXn, DYn ($1 \leq n \leq 65,535$)
Given as signed 8-bit data.

MOVE, RMOVE



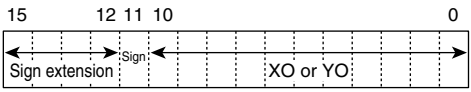
Absolute coordinate
Vertex coordinate XC
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



Absolute coordinate
Vertex coordinate YC
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

Relative coordinates
Vertex coordinates XC, YC
Given as signed 8-bit data.

LCOFS, RLCOFS

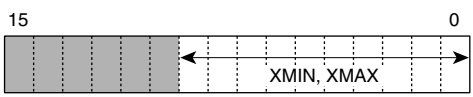


Relative specification
Local offset value XO or YO
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

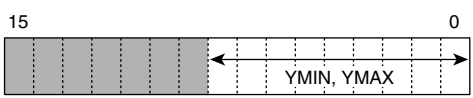
Relative specification
Local offset values XO, YO
Given as signed 8-bit data.

UCLIP, SCLIP

: Fixed at 0



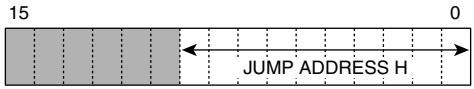
Left and right X coordinates XMIN, XMAX
Given as unsigned 10-bit data.



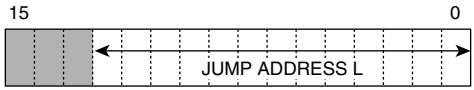
Upper and lower Y coordinates YMIN, YMAX
Given as unsigned 9-bit data.

JUMP

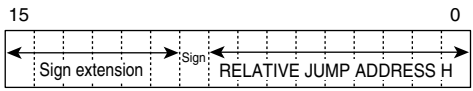
: Fixed at 0



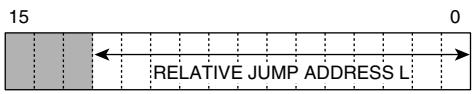
Jump destination upper address
Given as upper 10 bits.



Jump destination lower address
Given as lower 13 bits.
Jump destination address is set as an even byte address.



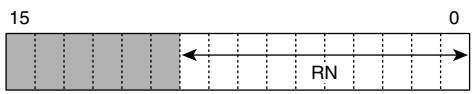
Relative jump destination upper address
Given as upper 10 bits.
Use sign extension in upper vacant bits.



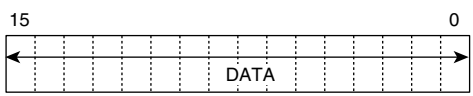
Relative jump destination lower address
Given as lower 13 bits.
Jump destination address is set as an even byte address.

WPR

: Fixed at 0



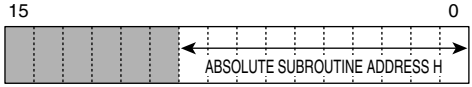
Register number RN
Given as 10-bit data.
Settable registers are limited.



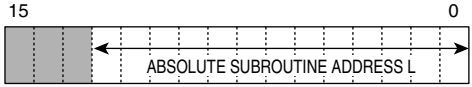
Data
Given as 16-bit data.

GOSUB

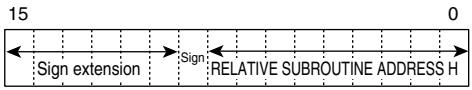
: Fixed at 0



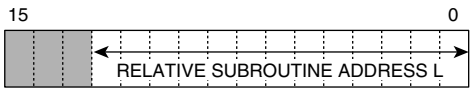
Subroutine upper address
Given as upper 10 bits.



Subroutine lower address
Given as lower 13 bits.
Subroutine destination address is set as an even byte address.

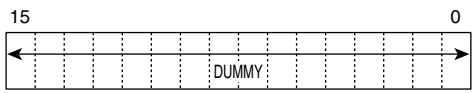


Relative subroutine destination upper address
Given as upper 10 bits.
Use sign extension in upper vacant bits.

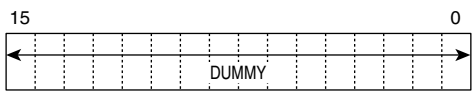


Relative subroutine destination lower address
Given as lower 13 bits.
Subroutine destination address is set as an even byte address.

NOP3, VBKEM



Cannot be referred.



Cannot be referred.

RET, TRAP

Command code words only.
No parameters.

Appendix C Drawing Algorithms

Straight Line Drawing Algorithms: 8-Point Drawing and 4-Point Drawing

Figures C.1 (a) and (b) show examples of straight lines plotted on a bit-mapped display. Circles in the figures represent pixels. Due to the characteristics of a bit-mapped display, a straight line is drawn with the pixels arranged in a path differing slightly from an actual straight line. The same line is drawn in figures C.1 (a) and (b), but the algorithms are different, and so the pixel arrangements are also different. In both figures the line starts at the bottom left of the figure and is drawn dot by dot toward the top right corner. With the method shown in figure C.1 (a), the next dot drawn is to the right, or diagonally to the upper right, of the current dot. With the method shown in figure C.1 (b), on the other hand, the next dot drawn is to the right of, or directly above, the current dot.

For the sake of convenience, the method in figure C.1 (a) is here called 8-point drawing, and that in figure C.1 (b), 4-point drawing.

The difference between 8-point and 4-point drawing is illustrated in figure C.2. With 4-point drawing, the move to draw the next dot can be made in one of only four directions, up, down, left, or right (figure C.2 (b)). With 8-point drawing, moves can also be made in the four diagonal directions (figure C.2 (a)).

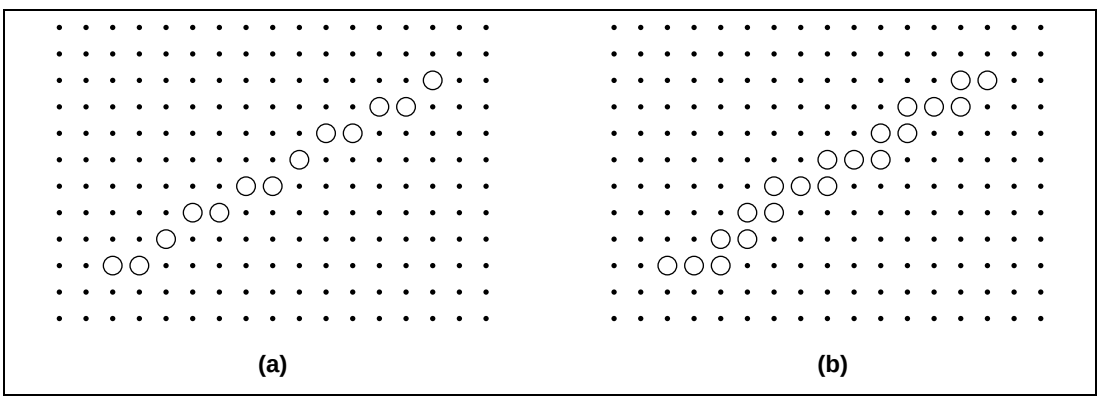


Figure C.1 Two Representations of a Straight Line on a Raster Display

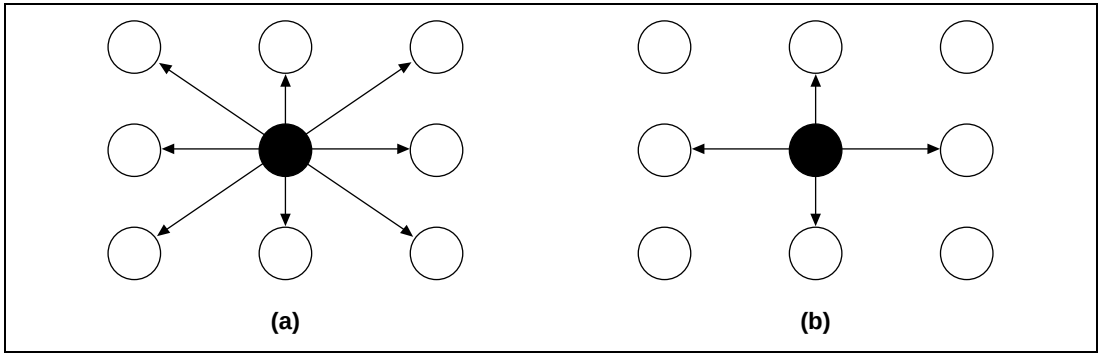


Figure C.2 Comparison of (a) 8-Point Drawing and (b) 4-Point Drawing

Next, 8-point drawing straight line approximation is described, using figure C.3 (a). After pixel A is drawn, either pixel B or pixel C is selected; the basis for selection is proximity to an actual straight line. The same approach is also used in 4-point drawing (figure C.3 (b)).

A comparison between 8-point drawing and 4-point drawing shows that closer approximation to a straight line can be achieved with 8-point drawing. However, the algorithm is correspondingly complex, requiring longer processing time.

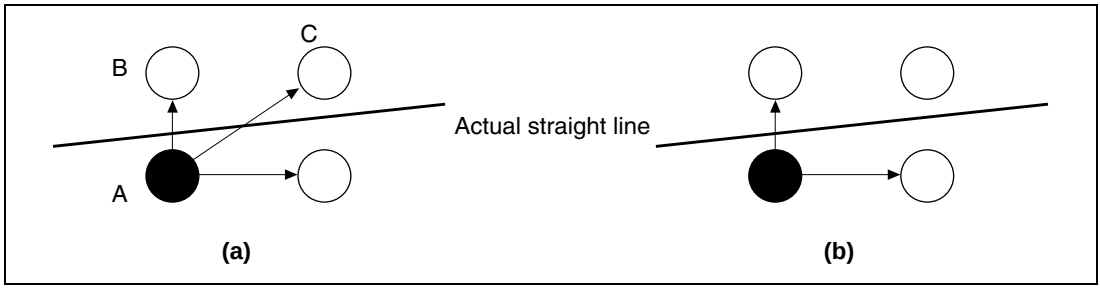
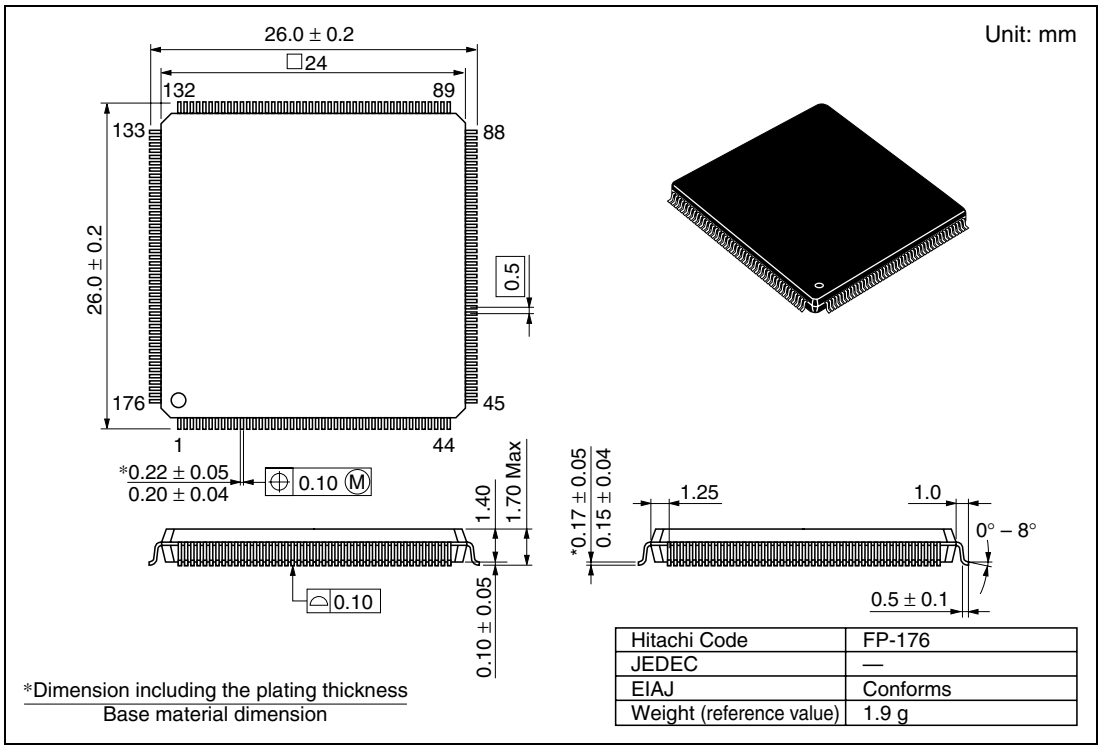


Figure C.3 Drawing Dot Determination Process in (a) 8-Point Drawing and (b) 4-Point Drawing

Readers interested in drawing algorithms can find further information in the sources listed below.

1. Jerry van Aken: “Curve-Drawing Algorithms for Raster Display,” ACM Trams. Graph. Vol. 4, No. 2—(April, 1985), 147–169.
2. J.E.Bresenham: “Algorithm for Computer Control of a Digital Plotter,” IBM Syst. J. Vol. 4, No. 1 (1965), 25–30
3. J.E.Bresenham: “A Liner Algorithm for Incremental Digital Display of Digital Arcs,” Commum. ACM. Vol. 20, No. 2 (February 1977), 100–106
4. P.E.Danielsson “Incremental Curve Generation,” IEEE Trans. Comput. Vol. C-19 (September 1970), 783-793
5. W.J.Jr.Bernard: “An Improved Algorithm for the Generation of Nonparametric Curves,” IEEE Trans. Comput. Vol. C-22, No. 12 (December 1973), 1052–1060
6. Jerry van Aken: “An Efficient Ellipse—Drawing Algorithm,” IEEE Comput. Graph & Appl. Vol. 4, No. 9 (September 1984), 24–35
7. Y.Suenaga: “A High-Speed Algorithm for the Generation of Straight Lines and Circular Arcs,” IEEE Trans. Comput. Vol. C-28, No. 10 (October 1979), 728–736

Appendix D Package Dimensions



Hitachi Code	FP-176
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.9 g

Figure D.1 Package Dimensions (FP-176)

Appendix E Display Operating Clock and Screen Synthesis

The display operating clock (CLK1) and possible FG screen, BG screen, and video screen display synthesis ranges are shown in tables E.1 to E.8.

The following symbols are used in the tables:

Table E.1 32-Bit UGM Bus Width, 66 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility				
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 240 14 MHz	640 × 480 25 MHz	800 × 480 33 MHz
8 bpp	—	—	O	O	O	O	O
16 bpp	—	—	O	O	O	O	O
8 bpp	8 bpp	—	O	O	O	O	O
8 bpp	16 bpp	—	O	O	O	X	X
16 bpp	8 bpp	—	O	O	O	X	X
16 bpp	16 bpp	—	O	O	O	X	X
8 bpp	—	16 bpp	O	O	O	X	X
16 bpp	—	16 bpp	O	O	O	X	X
8 bpp	8 bpp	16 bpp	O	O	O	X	X
8 bpp	16 bpp	16 bpp	O	O	O	X	X
16 bpp	8 bpp	16 bpp	O	O	O	X	X
16 bpp	16 bpp	16 bpp	O	O	O	X	X

Legend

O: Display synthesis possible

X: Display synthesis may not be possible

\: Display synthesis not possible

bpp: Bits per pixel

Note: 1. O if there is no video input

Table E.2 32-Bit UGM Bus Width, 60 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz *
8 bpp	—	—	O	O	O	
16 bpp	—	—	O	O	O	
8 bpp	8 bpp	—	O	O	O	
8 bpp	16 bpp	—	O	O	X	
16 bpp	8 bpp	—	O	O	X	
16 bpp	16 bpp	—	O	O	X	
8 bpp	—	16 bpp	O	O	X	
16 bpp	—	16 bpp	O	O	X	
8 bpp	8 bpp	16 bpp	O	O	X	
8 bpp	16 bpp	16 bpp	O	O	X	
16 bpp	8 bpp	16 bpp	O	O	X	
16 bpp	16 bpp	16 bpp	O	X	X	

Note: * Not possible since Q2SD operating frequency > twice dot clock.
Video input is possible if the Q2SD operating frequency is 64 MHz or higher.

Table E.3 32-Bit UGM Bus Width, 50 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz *
8 bpp	—	—	O	O	O	
16 bpp	—	—	O	O	O	
8 bpp	8 bpp	—	O	O	X	
8 bpp	16 bpp	—	O	O	X	
16 bpp	8 bpp	—	O	O	X	
16 bpp	16 bpp	—	O	O	X	
8 bpp	—	16 bpp	O	O	X	
16 bpp	—	16 bpp	O	O	X	
8 bpp	8 bpp	16 bpp	O	O	X	
8 bpp	16 bpp	16 bpp	O	X	X	
16 bpp	8 bpp	16 bpp	O	X	X	
16 bpp	16 bpp	16 bpp	O	X	X	

Note: * Not possible since Q2SD operating frequency > twice dot clock.
Video input is possible if the Q2SD operating frequency is 64 MHz or higher.

Table E.4 32-Bit UGM Bus Width, 40 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz *	800 × 480 33 MHz *
8 bpp	—	—	O	O		
16 bpp	—	—	O	O		
8 bpp	8 bpp	—	O	O		
8 bpp	16 bpp	—	O	O		
16 bpp	8 bpp	—	O	O		
16 bpp	16 bpp	—	O	O		
8 bpp	—	16 bpp	O	O		
16 bpp	—	16 bpp	O	O		
8 bpp	8 bpp	16 bpp	O	X		
8 bpp	16 bpp	16 bpp	O	X		
16 bpp	8 bpp	16 bpp	O	X		
16 bpp	16 bpp	16 bpp	X	X		

Note: * Not possible since Q2SD operating frequency > twice dot clock.
Video input is possible if the Q2SD operating frequency is 64 MHz or higher.

Table E.5 16-Bit UGM Bus Width, 66 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz
8 bpp	—	—	O	O	O	O
16 bpp	—	—	O	O	O	X
8 bpp	8 bpp	—	O	O	O	X
8 bpp	16 bpp	—	O	O	X	X
16 bpp	8 bpp	—	O	O	X	X
16 bpp	16 bpp	—	O	O	X	X

Table E.6 16-Bit UGM Bus Width, 60 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz *
8 bpp	—	—	O	O	O	
16 bpp	—	—	O	O	X	
8 bpp	8 bpp	—	O	O	X	
8 bpp	16 bpp	—	O	O	X	
16 bpp	8 bpp	—	O	O	X	
16 bpp	16 bpp	—	O	O	X	

Note: * Not possible since Q2SD operating frequency > twice dot clock.

Table E.7 16-Bit UGM Bus Width, 50 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz
8 bpp	—	—	O	O	O	
16 bpp	—	—	O	O	X	
8 bpp	8 bpp	—	O	O	X	
8 bpp	16 bpp	—	O	O	X	
16 bpp	8 bpp	—	O	O	X	
16 bpp	16 bpp	—	O	O	X	

Table E.8 16-Bit UGM Bus Width, 40 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz *	800 × 480 33 MHz *
8 bpp	—	—	O	O		
16 bpp	—	—	O	O		
8 bpp	8 bpp	—	O	O		
8 bpp	16 bpp	—	O	O		
16 bpp	8 bpp	—	O	O		
16 bpp	16 bpp	—	O	X		

Note: * Not possible since Q2SD operating frequency > twice dot clock.

Appendix F Example of System Configuration for SuperH

HD64413A, a chip set of SuperH, is designed to facilitate the connection of the SuperH Series CPU. For memory, SDRAM is directly connected. The HD64413A initializes SDRAM mode registers.

For a dot clock signal CLK1 for display and the operating clock (MCLK) of HD64413A, a non-synchronous clock can be used.

The display size is determined by the maximum clock frequency that can be input to CLK1. For example, the display size when HD64413A operates under non-interlace mode is roughly 320 × 240 to 480 × 240 dots, and under interlace sink & video mode, it is about 640 × 480 dots.

A synthetic display with external video signals can be performed by setting HD64413A to TV-synchronous mode and by supplying HSYNC, VSYNC, ODDF and CKL1 from an external device to HD64413A.

Also, a video display can be performed by video-capturing by digitally encoding video signals.

Figure F.1 shows an example of the system configuration for the HD64413A. The HD64413A is an application specific IC which is oriented to the realization of a low-cost system for combined display of video, graphics, still picture, and cursor.

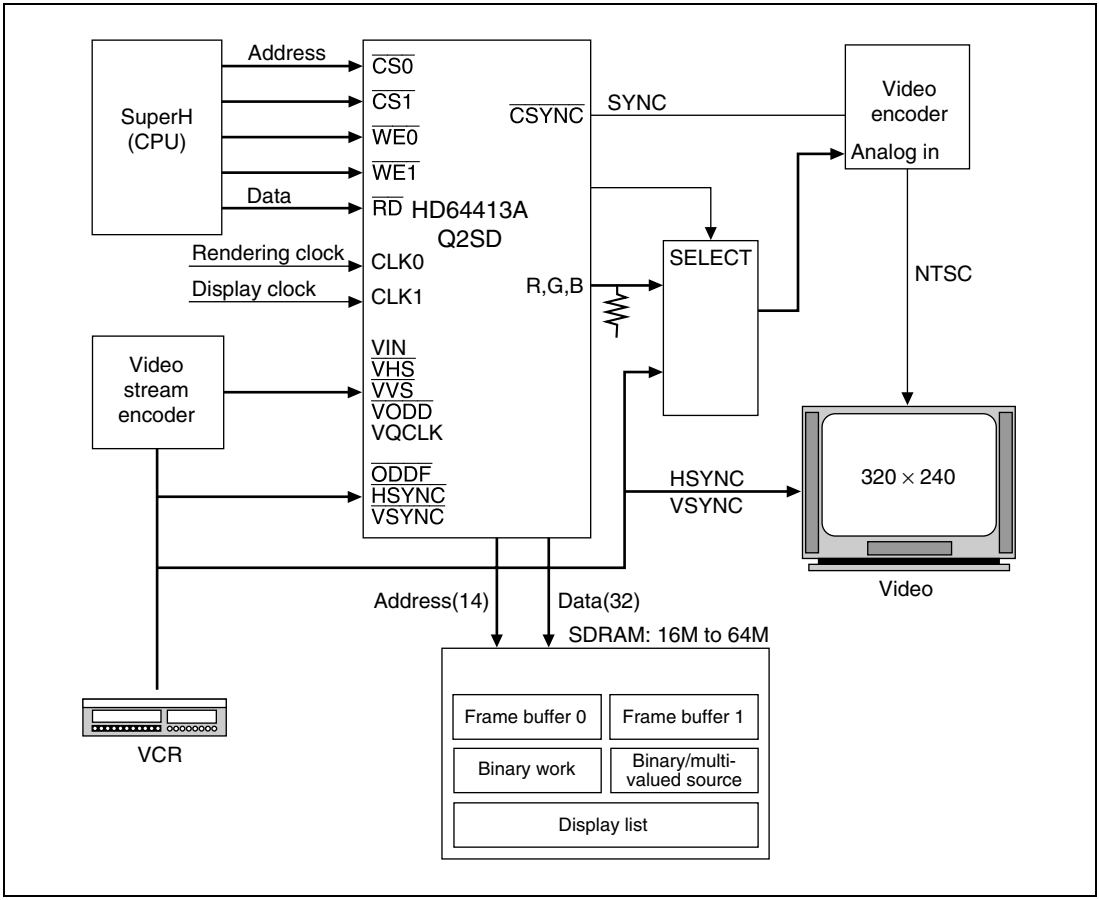


Figure F.1 Example of System Configuration Overview

F.1 Determination of Clock

The clocks supplied to HD64413A are clocks input to the CLK1 pin and those input to the CLK0 pin. The clocks input to the CLK1 pin are used as clocks for display control, and the clocks input to the CLK0 pin are used as operating clocks.

1. For the CLK0 pin, the following clock type a or b can be used.

   a. Method for using clocks output from CKIO pin of SuperH

      When a SuperH (SH-3, SH-4) operating with 3.3V is used as the CPU, clocks output from the CKIO pin can be used as input clocks for the CLK0 pin.

      Also, to increase the fan-out of CKIO pin, input the output clock of the CKIO pin to the CLK0 pin of HD64413A via a buffer circuit.

   b. Method for using clocks other than those output from CKIO pin of CPU

Clocks of 3.3V level can be used as input clocks for the CLK0 pin.

2. Input clocks for the CLK1 pin must satisfy the following conditions:

$$MCLK\ [Hz] \geq 2 \times CLK1\ [Hz]\ (CLK1 \leq 33.3\ MHz)$$

$$MCLK = N \times CLK0\ (N: \text{either of multiple of 1, 2 or 4})$$

F.2 Setting of Software Weight

The software weight cycle of SuperH is determined by the relationship of the external bus operating frequency (CKIO) of SuperH and the internal operating frequency (MCLK) of HD64413A.

Set the software cycle so that SuperH can detect the $\overline{\text{WAIT}}$ signal output by HD64413A, taking into consideration the AC timing of both SuperH and HD64413A.

Here a case in which CKIO = 20MHz and MCLK = 66MHz are used using SH-3 is described. As shown in figure F.2, by setting the software cycle (Tw) of SuperH to 2, the rule of tWTS and tWTH, which governs the $\overline{\text{WAIT}}$ pin of SuperH can be observed and the hardware cycle (Twx) between SuperH and HD64413A can be defined. (tWAS1 = 3 tcyc0 + 15 ns (MAX))

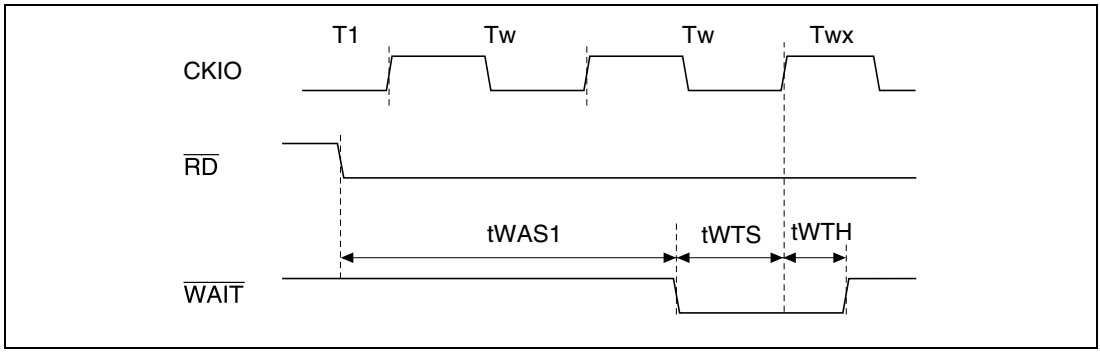


Figure F.2 Example of Interface Timing

F.3 Special Notes on Connection

When connecting SuperH to HD64413A, note the following:

1. When the initial value of $\overline{CS}$ pin of SuperH is an input port and signals connected to the $\overline{CS0}$ and $\overline{CS1}$ pins of HD64413A are generated from this pin, pull up the $\overline{CS}$ pin of SuperH so that the voltage level not to become unstable after canceling hardware reset.
2. When the DMAC built in SuperH is used and the DACK pin is set to active high by initial value setting, connect the inverted signal of DACK pin to the DACK pin of HD64413A by the external circuit. Incidentally, use the DACK pin set to active high, as is.
3. When using SH-4 for SuperH, invert signals output from the $\overline{WAIT}$ pin of HD64413A by the external circuit and input them to the $\overline{RDY}$ pin of SH-4.

F.4 Initialization Procedures of Address-Mapped Register

Standard procedures of setting initial value to the address-mapped register of HD64413A is described below. Follow the steps 1 to 4.

1. Set SRES = 0, DRES = 1 and DEN = 0 to the system control register and stop the display synchronous operation.

   Additionally, do not allow access to UGM by SuperH and DMAC after setting these values and before the display synchronous operations start.
2. Set initial values to registers between register addresses H′004 to H′04A and 056. In particular, depending on the initial values of each bit of H′056, initial values are required to be set to the registers related to these bits.
3. When displaying 8-bit/pixel displays or performing cursor display by combining GBM2 to GBM0, set initial values to the color palette register.
4. Set SRES = 0 and DRES = 0 to the system control register and start display synchronous operations.

   By setting this way, SuperH can make access to UGM. Additionally, to enable the graphics drawn by HD64413A to be checked, normally the DBM of system control register is specified with auto rendering mode or manual display change mode.

F.5 Memory Assignment

F.5.1 Memory Mapping of HD64413A

The address-mapped registers of HD64413A and UGM are mapped in the cache through space of memory space of SuperH. An example of memory map using a 64-Mbit synchronous RAM as UGM is shown in figure F.3. Also, pins A22 to A1 of HD64413A require the UGM address of HD64413A to be input directly. In this example, A1 to A22 are used as address signals for directly showing the UGM address. For example, when access is made by SuperH to address H′000000 of UGM, clear all A22 to A1 pins of HD64413A to 0.

In figure F.3, UGM is placed from H′A8000000 so that access is made to the cache through space when SuperH makes access to UGM.

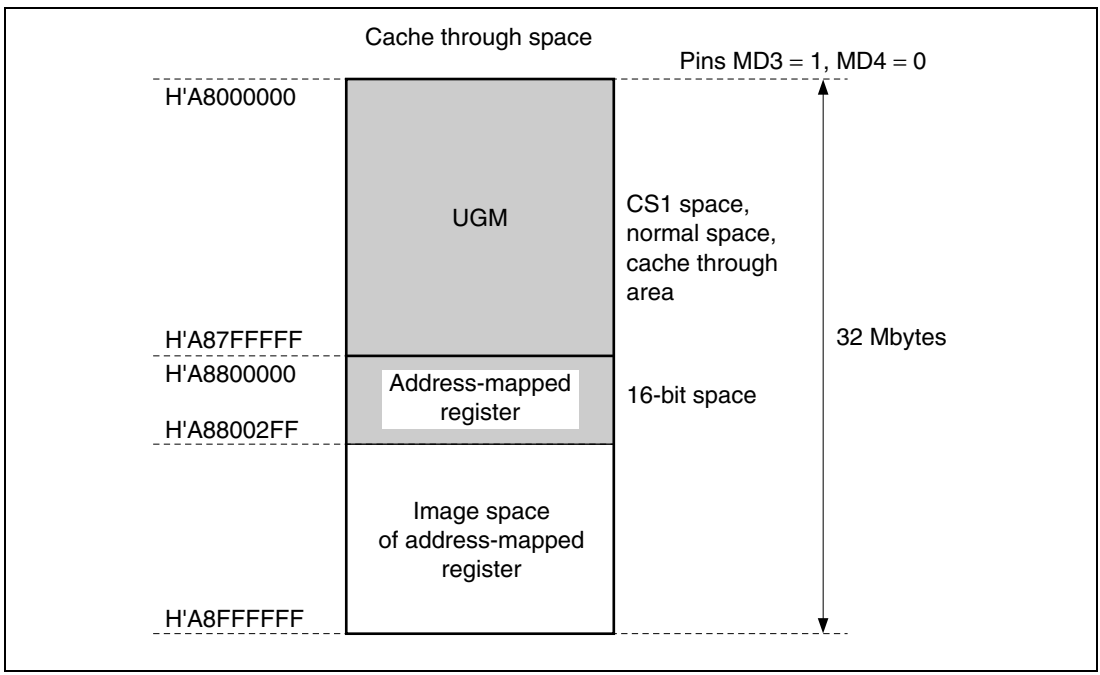


Figure F.3 Example of Memory Mapping (Using SH7709)

F.5.2 Example of Area Placement in UGM

An example of area placement in UGM is shown in figure F.4. This figure shows only an example meaning that other area placement styles are allowed.

1. Frame buffer area (FB0, FB1)

   Under double-buffer control, these areas are used as a display area (screen coordinates) and drawing area (rendering coordinates).

   For the display addresses (DSA0, DSA1) of these areas, set the UGM addresses that correspond to every 256-dot position touching Y-axis.

2. Video store area (V0, V1, V2)

   When using the video capture function, the captured data streams are stored in these areas. The areas are used in order of V0, V1 and V2 each time a synchronous signal is input to the $\overline{VVS}$ pin. Here the read size is 320 × 240 pixels.

   For the display addresses of these areas (VSAR0 to VSAR2), set the UGM addresses corresponding to every 16-dot position along Y-axis and every 32-dot position along X-axis, considering that UGM is 16 bit/pixel.

   Additionally, when the video capture function and video window are not displayed, these areas are not used and are not necessary.

3. Work area (BWAREA)

   This area is used as a work area. The maximum pixel of X-axis of work coordinates is the pixel quantity specified by the MWX bit of rendering mode register. Accordingly, regardless of the GBM bit of rendering mode register, the memory capacity required as work coordinates is (pixel quantity specified by MWX bit) × (display pixel quantity along Y-axis)/8[Bytes].

   For work area addresses (WASH, WASL), set UGM addresses corresponding to every 16-dot position touching Y-axis.

   Additionally, when the drawing of optional patterns, such as polygons, is not performed, this area is not used and is not necessary.

4. Display list area (DL0, DL1)

   These areas are used for storing display lists. Either one of DLO and DL1 is used as the read area for HD64413A to fetch display lists, and the other as the write area for SuperH to place display lists. DL0 and DL1 are used alternately by software control. Display list start addresses (DLSAH, DLSAL) can be specified with optional word (16-bit) addresses.

5. Cursor 1, 2 area (CU1, CU2)

   These areas are used for storing the shape patterns of cursors. For HD64413A, two cursors can be displayed, so each shape is stored respectively in CU1 and CU2.

   Also, as cursors themselves are displayed as 8-bit/pixel, surely set the display colors of cursors in the color palette.

Additionally, for both CU1 and CU2, the memory capacity used is 2kB.

6. Display size

   640 × 240 dots (the maximum of 640 × 480 dots)

7. Background area (BG)

   This area is used for a background screen. The start address for this area is specified in screen coordinates.

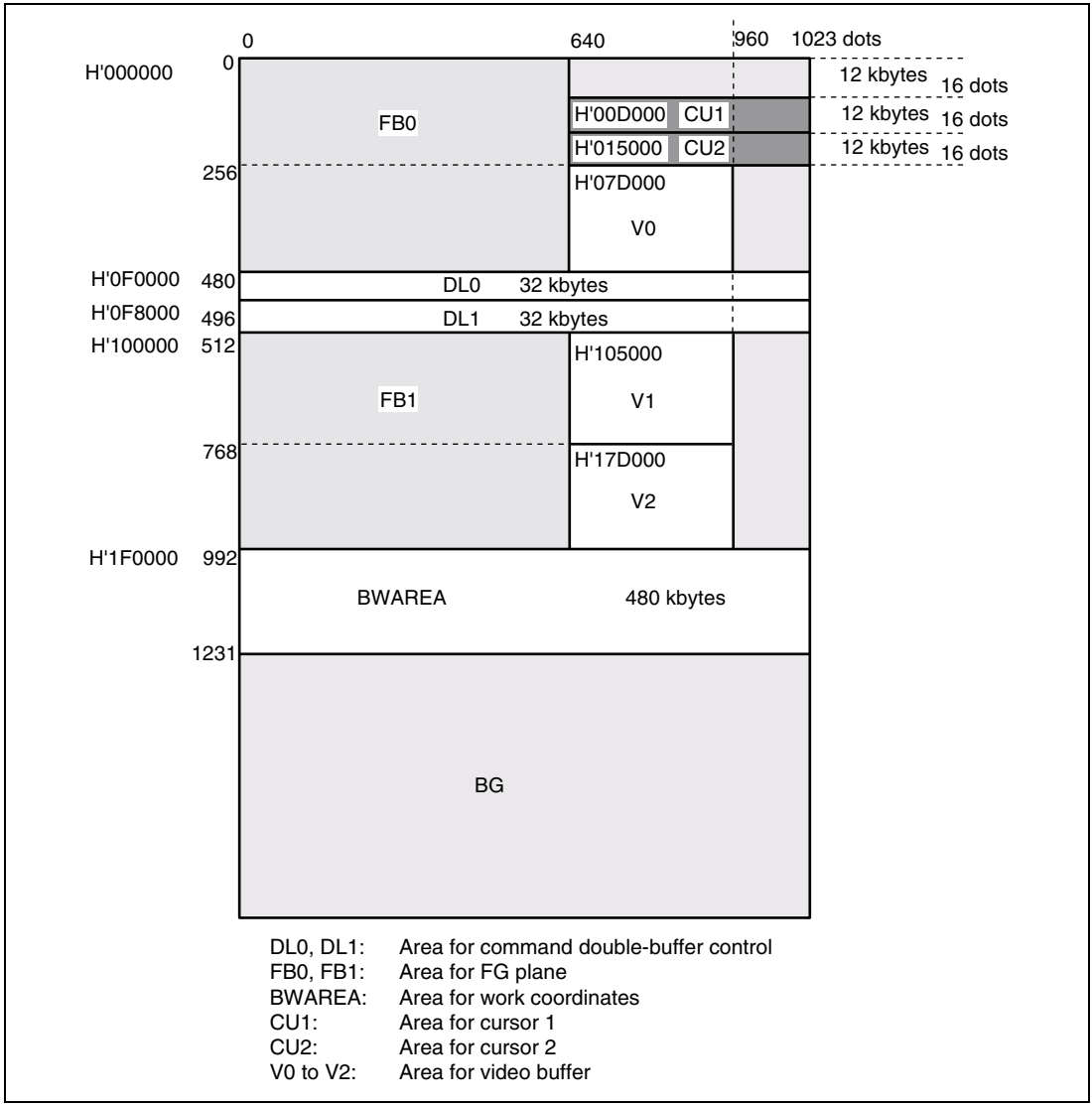


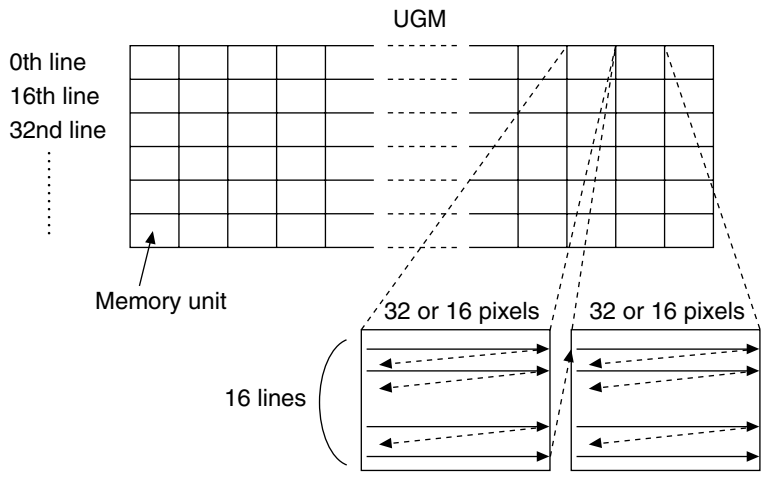
Figure F.4 UGM Memory Map

F.5.3 Address Seriation in UGM

As shown in figure F.5, when UGM is viewed from SuperH, UGM addresses look as a series of tiles arranged by memory unit. Thus, by using more than one memory units that were not used in area assignment of FB0, FB1, etc., the space can be used as a memory space with a series of addresses.

In case of HD64413A, items that can be placed in a memory space with a series of addresses include binary and multi-valued sources and cursor patterns, so normally these are placed in this area.

For example, on the right of FB0, a memory space with a series of addresses having (1024-640) pixels × 16 lines = 6114 pixels from the position X = 640, Y = 0, or a capacity of 12 kbytes from the relationship 1 pixel = two bytes, can be secured. Here CU1 assignment or others is performed.



When UGM is viewed from SuperH, UGM addresses turn down within a range of 32×16 pixels (8-bit/pixel) or 16×16 pixels (16-bit/pixel) and go to the top left of the following memory unit.

Figure F.5 UGM Address Transition Overview

F.6 Special Notes on Data Transfer to UGM

To transfer data such as binary data and display lists by SuperH or the DMA controller to UGM, first do the initial setting to the address-mapped register of HD64413A and start display synchronous operations so as to enable data transfer between SuperH and UGM.

Since an access made by SuperH or the DMA controller to UGM may stop data transfer when display synchronous operations are not performed, do not attempt to make access to UGM when display synchronous operations are not performed.

Additionally, there is only one bus master that can make access to UGM. Accordingly, when the DMA mode in system control register of HD64413A is normal mode, only SuperH can make access to UGM. Likewise, when the DMA mode is DMA transfer mode, only the DMA controller can make access to UGM.

Data transfer is possible even in the midst of drawing processing by HD64413A.

When the DMAC built in SuperH is used, surely check TE (transfer end flag bit) and then the DMF flag of status register of HD64413A before finishing DMA transfer.

Appendix G Example of Display Control

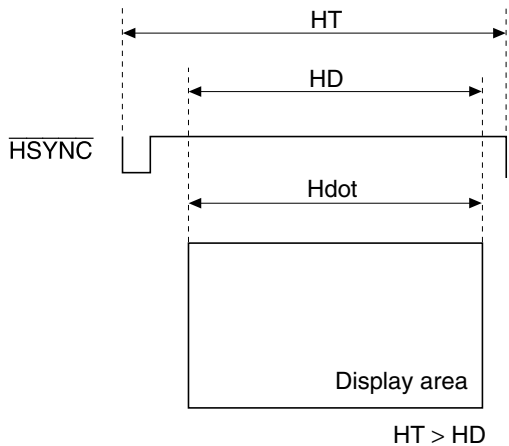
G.1 Determination of Display Size

Display pixels along horizontal direction (Hdot) are required to be values satisfying the following formula. For example, if CLK0 = 33MHz, N = 1, HD = 44.7 μ/s, Hdot must be 737 pixels or less.

Also, the frequency of display dot clock (CLK1) must be CLK1 = Hdot/HD (Hz).

$$\frac{Hdot}{HD} \leq \frac{CLK0 \times N}{2} = MCLK$$

Where, N is a multiple of Q2SD
CLK0 is a clock (Hz) input to the CLK0 pin of Q2SD.



HT: $\overline{HSYNC}$ cycle (sec)
HD: Display time in $\overline{HSYNC}$ (sec)
Hdot: Quantity of display pixels along horizontal direction (pixel)

Figure G.1 Example of Display Timing

G.2 Selection of Display Screen

HD64413A has the following three display screens:

1. Foreground screen

   Displayed at the frontmost. It can be displayed with 8 or 16 bit/pixel and is used mainly for realizing dynamic images in drawing processing.

2. Background screen

   Displayed at the rearmost. It can be displayed with 8 or 16 bit/pixel and is used mainly for realizing scroll by pixel.

3. Video screen

   Displayed between the foreground and background screens. It is used for displaying the stream data captured by the video capture function.

Each display screen can be selected as the foreground screen by the FBD bit, the background screen by the BG bit, and the video window by the VWE bit.

G.3 Setting of Synchronous Signal

To enable display control, HD64413A requires synchronous signals to be set in the address-mapped register. An example of register setting of the synchronous signals used for this application note is shown below:

1. Setting example of synchronous signals when the TV synchronous mode is master mode and the scan mode is non-interlace is shown. The display size is 320 × 240 dots.
   Here, CLK1 = (horizontal display pixel)/(xw time) (Hz).

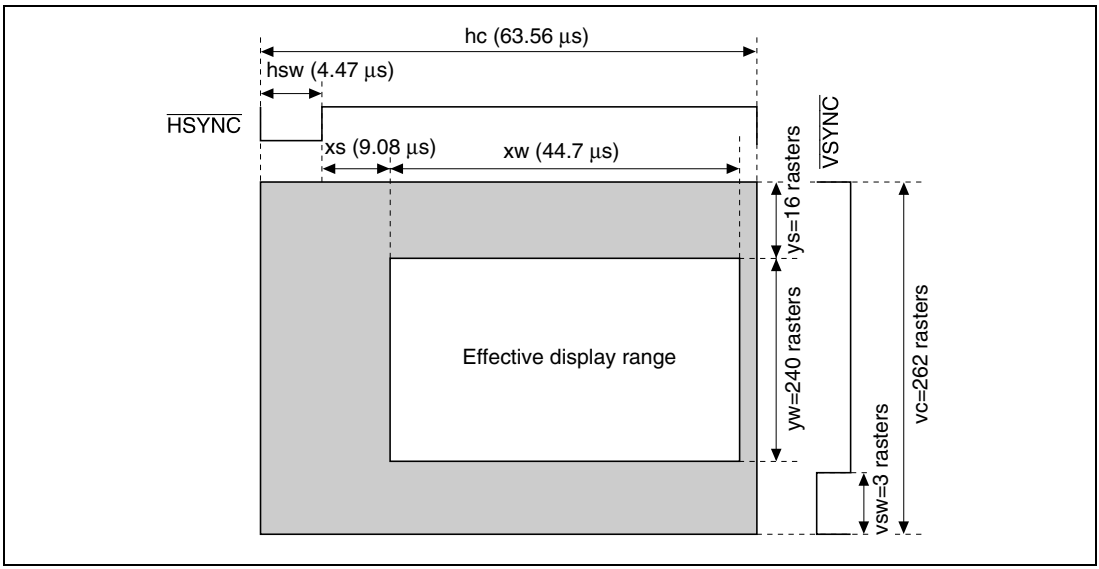


Figure G.2 Example of Display Timing under Non-interlace Mode

Table G.1 Setting Example of Variables ((TVM1,0) = (0,0), (SCM1,0) = (0,0))

Variable	Calculation Formula	Value in Display Example
hsw	4.47 μs × CLK1	32
xs	9.08 μs × CLK1	65
xw	44.7 μs × CLK1	320
hc	63.56 μs × CLK1	455

CLK1 = 7.159 MHz

Table G.2 Register Setting Example ((TVM1,0) = (0,0), (SCM1,0) = (0,0))

Register	Calculation Formula (Master Mode)	Setting Value in Display Example
DSX	xw	320
DSY	yw	240
HDS	hsw + xs – 11	68
HDE	hsw + xs – 11 + xw	406
VDS	ys – 2	14
VDE	ys – 2 + yw	254
HSW	hsw – 1	31
HC	hc – 1	454
VSP	vc – vsw – 1	258
VC	vc – 1	261

2. Setting example of synchronous signals when the TV synchronous mode is master mode and the scan mode is interlace & video mode is shown. The display size is 640 × 480 dots.
   Here, CLK1 = (horizontal display pixel)/(xw time) (Hz).

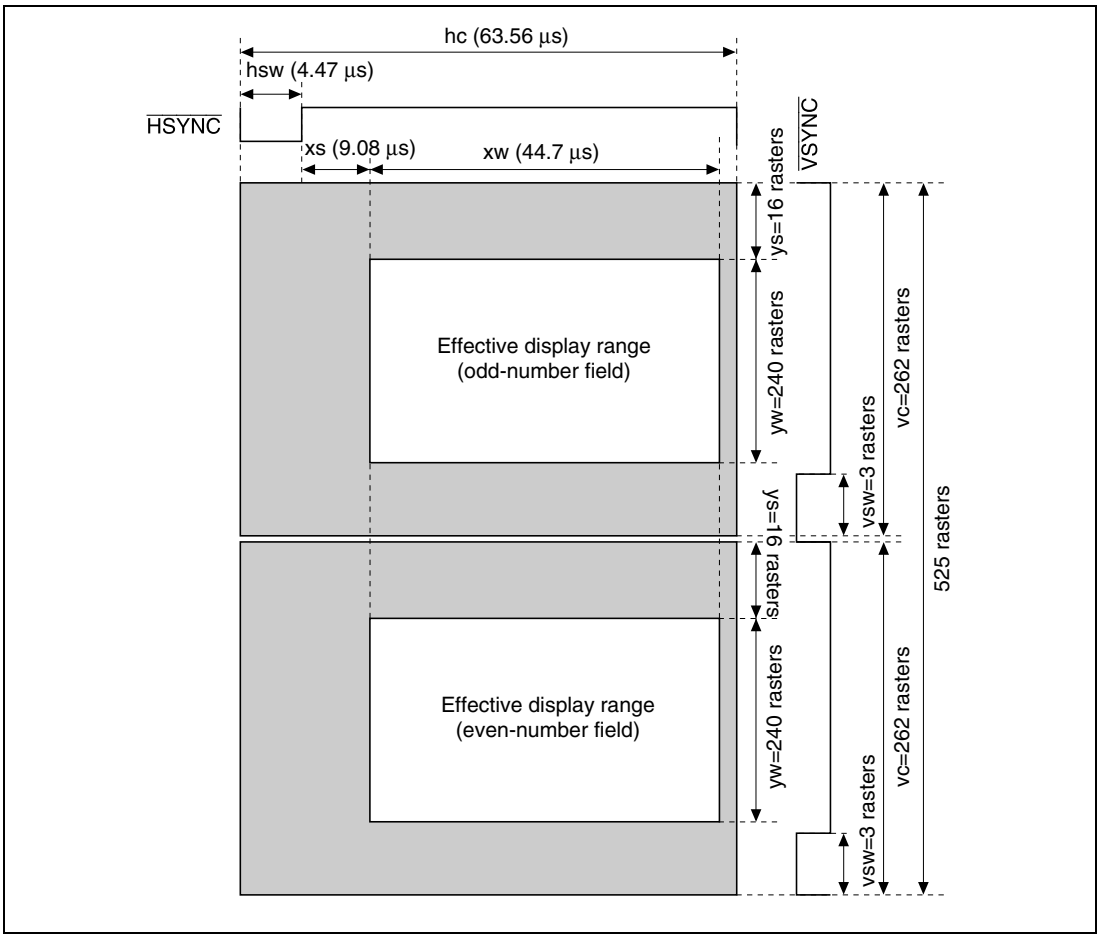


Figure G.3 Example of Display Timing under Interlace Sink & Video Mode

Table G.3 Setting Example of Variables ((TVM1,0) = (0,0), (SCM1,0) = (1,1))

Variable	Calculation Formula	Value in Display Example
hsw	4.47 μs × CLK1	64
Xs*	9.08 μs × CLK1	131
xw	44.7 μs × CLK1	640
hc	63.56 μs × CLK1	910

CLK1 = 14.318 MHz

Note: When using a video encoder, determine xs so that the effective display range does not overlap the color burst.

Table G.4 Register Setting Example ((TVM1,0) = (0,0), (SCM1,0) = (1,1))

Register	Calculation Formula (Master Mode)	Setting Value in Display Example
DSX	xw	640
DSY	yw × 2 cycles of $\overline{\text{VSYNC}}$	240
HDS	hsw + xs – 11	184
HDE	hsw + xs – 11 + xw	824
VDS	ys – 2	14
VDE	ys – 2 + yw	254
HSW	hsw – 1	63
HC	hc – 1	909
VSP	vc – vsw – 1	258
VC	vc – 1	261

G.4 Setting and Changing Register Values related to Display Control

G.4.1 Setting of Color Palette

The color palette of HD64413A is designed to write or read color palettes by two-word continuous access. So, when setting values to color palettes, surely set registers containing G and B, following a register containing R.

Likewise, when reading values from color palettes, surely read out registers containing G and B, following a register containing R.

G.4.2 Switching Procedure of Synchronous Mode

A change in synchronous mode, from master mode to TV synchronous mode and the like, is performed by way of synchronous switching mode. Switching to synchronous switching mode can be performed by setting TVM1 = 0, TVM0 = 1.

Also, since HD64413A does not refresh UGM under synchronous switching mode, set DRES = 1, DEN = 0 and switch the mode to one under which HD64413A refreshes UGM, before entering synchronous switching mode. Procedures are shown below.

Additionally, as HD64413A refreshes UGM while DRES = 1, DEN = 0 is valid, do not attempt access to UGM by SuperH or DMAC.

Switching Procedure to synchronous switching mode:

1. Set BG = 0, VWE = 0, CE1 = 0, CE2 = 0.
2. Set DRES = 1, DEN = 0. Now only refreshing to UGM can be performed.
3. Set TVM1 = 0, TVM0 = 1. HD64413A switches to synchronous switching mode.

Returning Procedure from synchronous switching mode:

4. Input a clock to the CLK1 pin. For a switch to TV synchronous mode (TVM1 = 1, TVM0 = 0), also input signals to $\overline{\text{EXHSYNC}}$, $\overline{\text{EXVSYNV}}$ and $\overline{\text{ODDF}}$ pins.
5. To change the display size, setting values to the address-mapped register of HD64413A.
6. By setting TVM1 = 0 and TVM0 = 0, or TVM = 1 and TVM0 = 0, the input clock from the CLK1 pin is effective. Further, set BG = 1, VWE = 1, CE1 = 1, CE2 = 1, as needed.
7. Set DRES = 0, DEN = 1. After internal updating, HD64413A starts displaying.

G.5 Use of Cursor Display

The Hd64413A can display two cursors with 32×32 pixels placed in the UGM. One cursor has two shape data: cursor blink shape A and cursor blink shape B. They are alternatively displayed at

the timing specified by BLINKA and BLINKB. Therefore, an area of continuous 2-kbyte addresses per one cursor is required.

Using four memory units in the horizontal direction can allocate the continuous 2-kbyte area in the UGM as shown in figure G.4. For details of a single memory unit, see section F.5.3, Address Seriation in UGM.

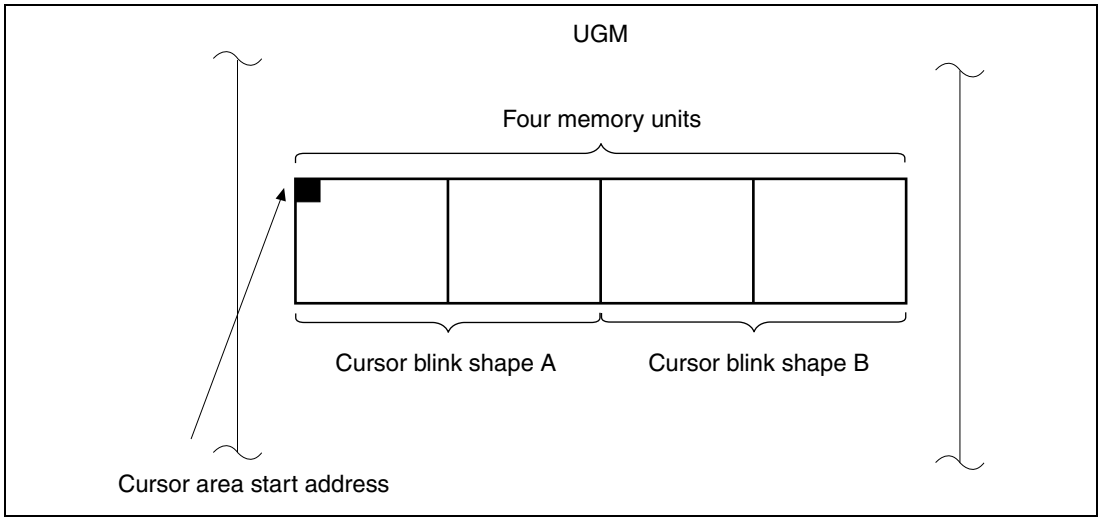


Figure G.4 Cursor Allocation

When the HD64413A displays a cursor, a cursor shape data is first read from an address specified by the cursor area start address register. The cursor is painted by referencing the cursor shape data and is displayed.

Appendix H Example of Drawing Control

H.1 Example of Starting Drawing

HD64413A performs drawing on rendering coordinates and work coordinates based on command groups called display lists. The drawing procedures are shown below:

1. Using SuperH, place LCOFS and SCLIP commands as a display list to UGM. This display list is intended to set initial values of the local offset and system clip ranges of HD64413A.
2. To synchronize the frame change timing and draw start timing, place the VBKEM command following the display list placed in 1 to UGM using SuperH or use the frame change function specified by the DBM bit in the system control register (SYSR).
3. Following the display list placed in 2, place the display list using POLYGON4-series commands and the like to UGM using SuperH to let HD64413A perform drawing.
4. Following the display list placed in 3, place the TRAP command to show the end of display listing. At this moment, the display list preparation is finished.
5. After setting the rendering start address, set 1 to RS bit.

   By this register setting, you can let HD64413A perform drawing.

H.2 Example of Frame Change by Internal Updating

An example of a frame change by internal updating is described below. In this case, a frame change is performed by internal updating, while fixing the DBM bit at manual display change mode and controlling display start addresses DSA0, DSA1, and RSAR by SuperH.

When using the suspend/resume function of drawing, method by which the draw start address and display start address can be controlled is effective. In this case, first the DBF bit in status register should be checked to judge which of DSA0 or DSA1 is the register that determines the display start address. When DBF = 0, DSA0 is the register determining the display start address. Likewise, when DBF = 1, DSA1 is the register determining the display start address.

Table H.1 shows the relationship of DBF, DSA0 and DSA1.

Table H.1 Relationship of DBF and Display Screen (FG)

	DSA0	DSA1
DBF = 0	Display screen	Drawing screen
DBF = 1	Drawing screen	Display screen

As an example, control procedures 1 to 4 of DSA0 and DSA1 of a case DBF = 0 are shown below:

1. Wait until the internal updating cycle is finished. To confirm the end of internal updating, clear FRM bit and see that the FRM bit becomes 1.
2. Using the WPR command, set in DSA0 the display start address of a position to do displaying in the next internal updating.

   The display start address set to DSA0 is not reflected as an effective value. This setting value becomes effective only passing an internal updating.
3. Using the WPR command, set 1 to RSAE and the draw start address to RSAR.
4. After transferring display lists, read dummy data from the UGM and then set the RS bit in the system control register to 1 to start drawing.

By repeating the steps 1 to 4 above, the display start address set to DSA0 becomes effective by internal updating and frame changing is enabled.

The drawing and display timing using the frame change by internal updating are shown in figure H.1:

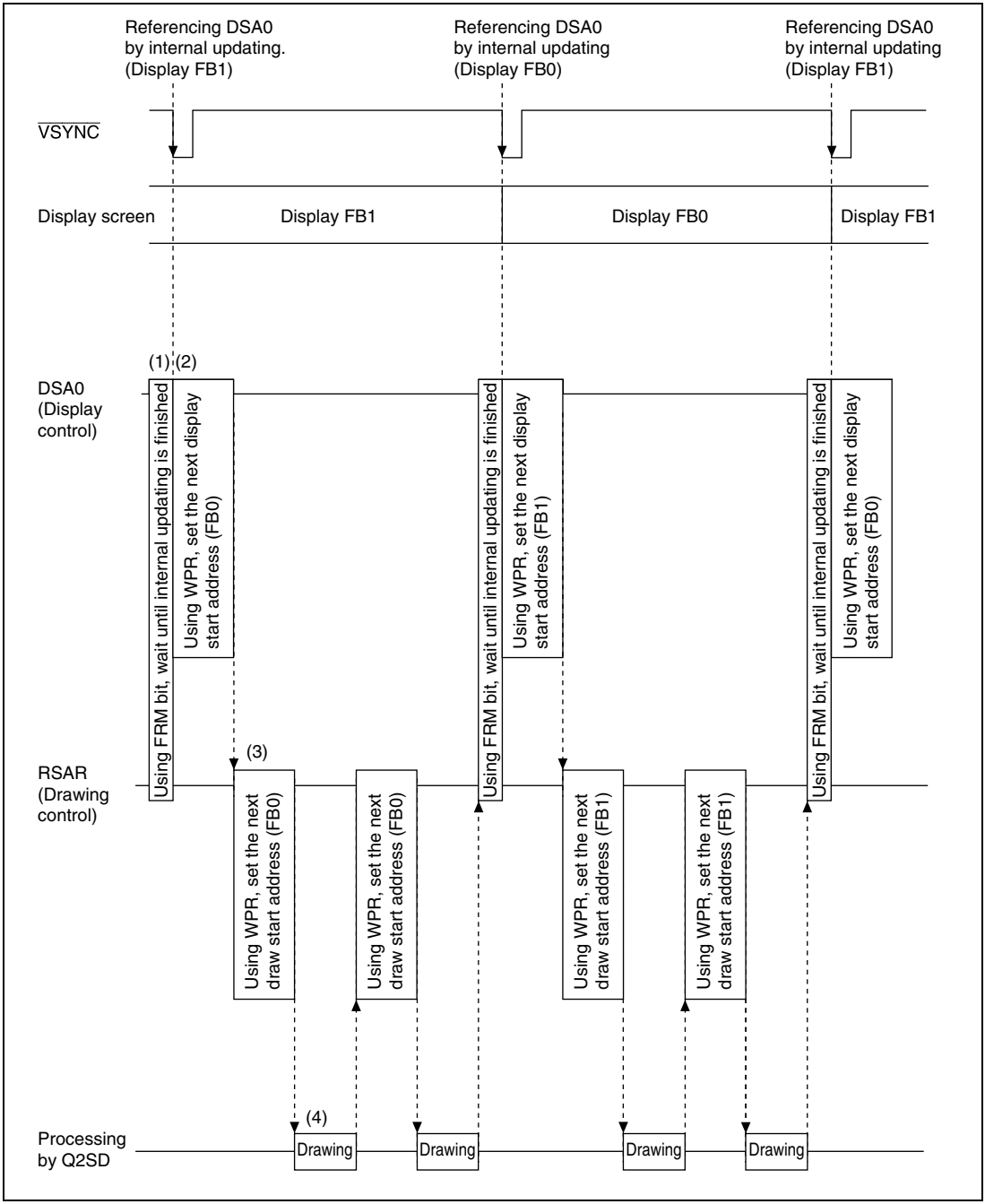


Figure H.1 Display/Drawing Control Timing Chart (DBF = 0)

H.3 Using Example of Draw Commands

H.3.1 Drawing Polygons

Drawing polygons on rendering coordinates using HD64413A can be performed by using work reference, one of rendering attributes, and work coordinates.

Drawing procedures by HD64413A are shown below:

1. To clear the work area, execute the CLRW command.
2. Using the FTRAP command, draw on work coordinates the shape of polygon to draw.
3. Using the POLYGON4C command of which the WORK bit with rendering attribute is set to 1, draw a polygon with the shape drawn on the work coordinates.
4. Using the LINE command, draw an outline of the polygon.

Practically, the display list to perform the above procedures is generated by SuperH, and drawing is performed by HD64413A based on the display list generated.

H.3.2 Drawing Optional Shapes

An optional shape which is a fixed shape with binary pattern having been placed on work coordinates by partially referencing can be drawn.

Before placing a binary pattern on work coordinates, the work coordinates must be zero-cleared. To avoid concurrent drawing on work coordinates by SuperH and HD64413A, the zero-clearing of the work coordinates is performed not by the CLRW command but directly by SuperH.

H.3.3 Drawing Circles and Ellipses

To draw a circle or an ellipse by HD64413A, the orbit of ellipse is calculated by SuperH, and drawing is performed by the LINE command using the calculated result as parameters. Using Bresenham's circle algorithm, the ellipse orbit is worked out. Drawing a circle is enabled by converting the x, y radiuses of ellipse to same dot quantities.

When drawing is required to be performed in a work area, the LINE command should be used.

H.3.4 Drawing using Source Data

When using a draw command that references a source by HD64413A, generally it is necessary to judge whether or not source data is stored in UGM on the application software side. In a certain system, the judgment is difficult or processing requires time. As an example to avoid this, there is one method that relates the draw command and the reference position of source by including source data in the display list.

To embed source data into the display list, place the JUMP command immediately after the draw command so that the source data is skipped as shown in figure H.2.

When a multi-valued source is included in the display list, the same method can be applied. In this case, use the POLYGON4A command by setting 1 to the LNi bit with rendering attribute.

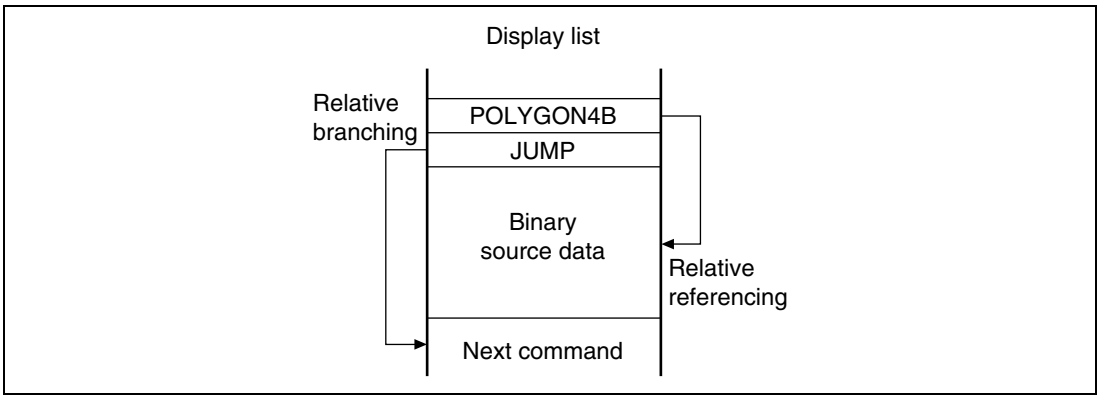


Fig. H.2 Example of Referencing and Branching

H.3.5 Expressing 3D Space

A solid graphics formed with multiple rectangles are rotated by rotating each rectangle. Processing procedures are described below:

1. Define the rectangles that are expressed with 3D coordinates. A set of the rectangles defined with the function forms one solid graphic.

2. Do rotational operation of coordinate values for each rectangle.

3. Determine the order of drawing rectangles. Drawing order is from the depth to the front. First the mean value of Z values of each rectangle is calculated, and the order is set based on the results. In a bubble sorting which is easily described by a source program, sorting is performed by approximately $n \times n$ times where the quantity of elements to be sorted is n. In a high-speed sorting method like heap sorting is used, sorting can be finished by approximately $n \times \log n$ times.

4. Convert 3D coordinate values into 2D coordinate values for each rectangle. Firstly, a position in which the Z value of each vertex exists in the depth of Z-axis is given by the ratio of the position to the Z value. Then, conversion is achieved by multiplying each of four vertices by its ratio.

5. Using the order determined in 3 and the 2D coordinate values obtained in 4, drawing is performed on UGM with the POLYGON4C command as a display list.

After finishing the above procedures, the display list is generated on UGM, and a 3D space can be expressed by drawing using HD64413A.

H.4 Special Notes on Using Draw Commands

H.4.1 Notes on the Relationship of Local Offset and Current Pointer

Local offset and the current pointer are given their respective values by the order of command execution. So, place commands while taking into consideration the relationship of local offset and the current pointer. The priority order of command placement is shown below. Draw commands having low priority are to be placed first.

1. lcofs command
   Sets the initial value of local offset.
2. rlcofs command
   Moves local offset by a relative value to the current local offset.
3. move command
   Sets the current pointer by adding the current local offset.
4. remove command
   Moves the current pointer by a relative value to the current pointer currently used.

H.4.2 Notes on Using Relative-Series Commands

Commands that control coordinate parameters on relative coordinates are called relative-series commands. When using the relative-series commands, it is necessary to generate a current pointer using the move command and the like beforehand. Also, commands other than relative-series commands use the current pointer as a register for operation and break it. Therefore, when using relative-series commands performing drawing, do not insert other commands between relative-series commands.

H.4.3 Notes on Using Source Data

When HD64413A uses the binary and multi-valued sources placed in UGM, source data is taken to the source buffer existing in HD64413A, and drawing is performed using the accumulated source data. The source buffer has a capacity of 16 words, and HD64413A stores every 32-byte data to the source buffer each time the UGM address passes a 16-word border. Because of this, when using binary and mullet-valued sources, it is necessary to let HD64413A perform drawing while taking into consideration to cause source buffer updating. Also, how the source buffer updating is performed is determined by the STYL bit with rendering attribute as described in 1 and 2 below:

1. When STYL with rendering attribute is set to 0

   When STYL = 0, consideration must be taken so as to cause source buffer updating when the source capacity is within 32 bytes. The following methods can be considered:

   a. Specify different source addresses for each command.

      For example, when referencing binary sources within 32 bytes by the POLYGON4B command, this method can be performed by specifying different addresses for each of POLYGON4B command parameters SOURCE ADDRESSH and SOURCE ADDRESSL.

   b. Use transparent designation

      By this method, by preparing binary sources exceeding 32 bytes, only the binary source of a necessary part is drawn when drawing using the draw command of which transparent designation is enabled.

2. When STYL with rendering attribute is set to 1

   When STYL = 1, source referencing is performed repeatedly. Accordingly, when a source referencing is finished at an address within 32 bytes, counting from the source reference start address, consideration must be given so as to cause source buffer updating. The following methods can be considered:

   a. Specify different source addresses for each command.

      For example, when referencing binary sources within 32 bytes by the POLYGON4B command, this can be performed by specifying different addresses for each of POLYGON4B command parameters SOURCE ADDRESSH and SOURCE ADDRESSL.

H.5 Functions to Support Drawing Processing

H.5.1 Suspension/Resumption of Drawing

Suspension/resumption of drawing is intended to support drawing functions and is supported from HD64412 (Q2i) on. This function is used when doing drawing processing to the frame buffer (FB) during a background screen (BG) drawing or for forcible interruption with drawing processing. Use of suspension/resumption of drawing is described below.

Additionally, the function is available only when 10 is set to the DBM bit of system control register and the double-buffer control is fixed at manual display change.

Suspension of Drawing: "Suspension of drawing" is intended to suspend the drawing that is currently being performed. Suspension of drawing can be performed by setting 1 to the RBRK bit of system control register (SYSR). Setting 1 to the RBRK bit by SuperH, HD64413A sets values set to the register inside LSI (current pointer, local offset, clipping range, return address of GOSUB command) to rendering control register 2 at the top of next command that follows after the execution of current draw command is finished, and suspends the drawing.

To determine suspension of drawing by SuperH, after setting 1 to the RBRK bit, read out the TRA and BRK bits. If the TRA bit is 1, meaning that drawing is finished by executing the TRAP command, and not suspension by RBRK, do not resume drawing thereafter. If the BRK bit is 1, it means suspension of drawing. Thus, suspension of drawing can be judged by confirming BRK = 1.

When the BRK bit becomes 1, read values set to the rendering control register 2, draw start address enable (RSAE) of rendering mode register, draw start address register (RSAR) and the command status register (CSTR) by SuperH software processing, and shelter them on the SuperH memory. Sheltered values are used when resuming the suspended drawing.

Thereafter, generate the display list to draw during suspension and execute.

Resumption of Drawing: "Resumption of drawing" is intended to resume a drawing suspended by "suspension of drawing". To resume the drawing, place a display list for resuming drawing to UGM using SuperH, start resumption of drawing to the display list (by setting 1 to the RS bit of system control register) and confirm that the RS bit returns to 0. The composition of display list for resuming drawing is described in 1 to 8 below:

- Order of display list commands used to resume drawing (1 to 8 in this order)

1. WPR command: Sets the draw start address register values sheltered when suspending drawing to the draw start address register (RSAR).
2. WPR command: Sets the draw start address enable values sheltered when suspending drawing to the start address enable (RSAE).

3. WPR command: Sets the return address of GOSUB command sheltered when suspending drawing to the return address register (RTNR).
4. UCLIP command: Returns the UCLIP values sheltered when suspending drawing.
5. SCLIP command: Returns the SCLIP values sheltered when suspending drawing.
6. LCOFS command: Returns the local offset values sheltered when suspending drawing.
7. MOVE command: Returns the current pointer values sheltered when suspending drawing.
8. JUMP command: Returns the command status register values sheltered when suspending drawing.

Appendix I Drawing Performance

Figures I.1 to I.3 show graphs of HD64413A drawing performance. The graphs show the time required for drawing within the range 320 (H) × 240 (V).

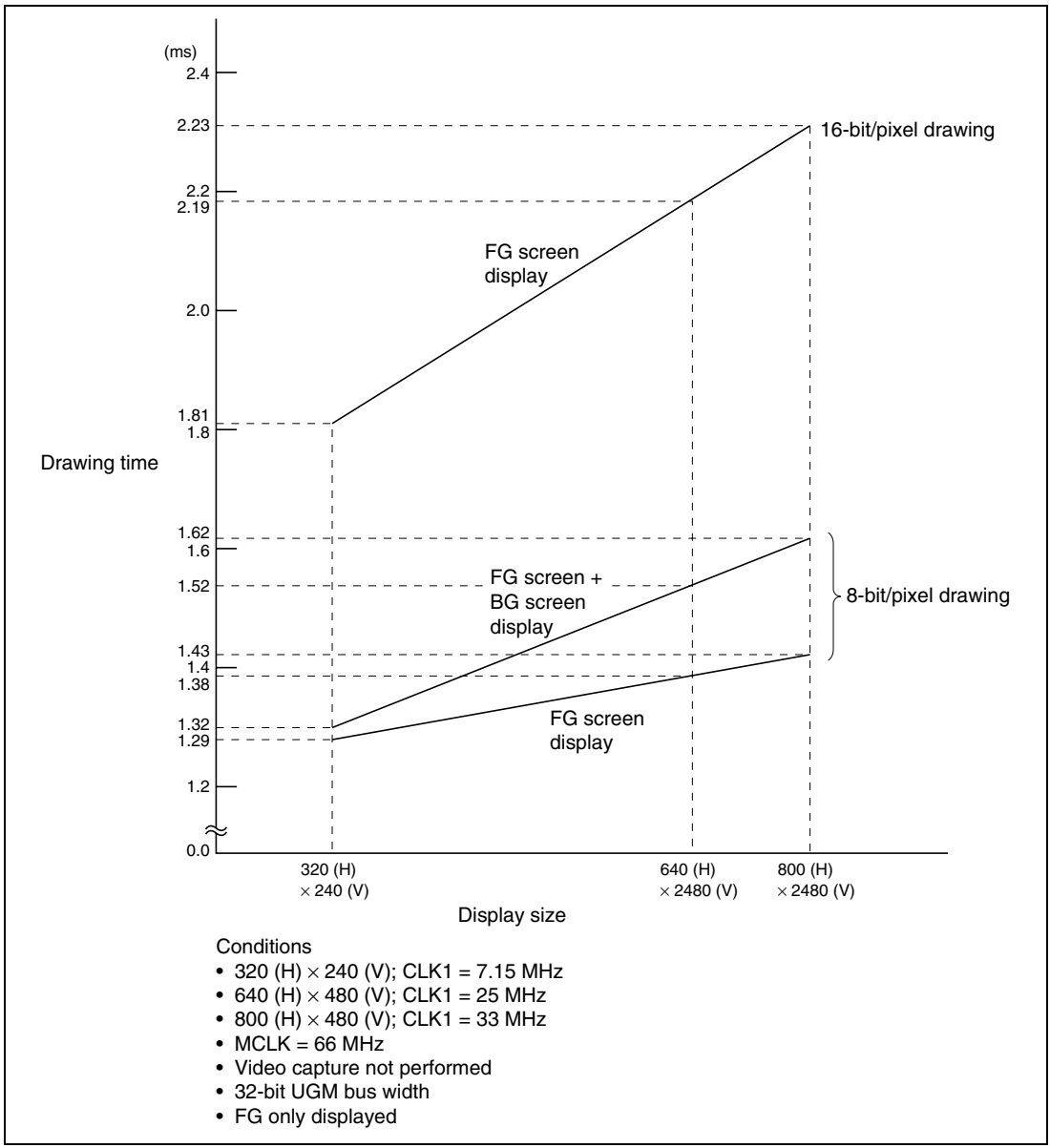


Figure I.1 POLYGON4C Drawing Performance when FST = 0 (Drawing Range: 320 (H) × 240 (V))

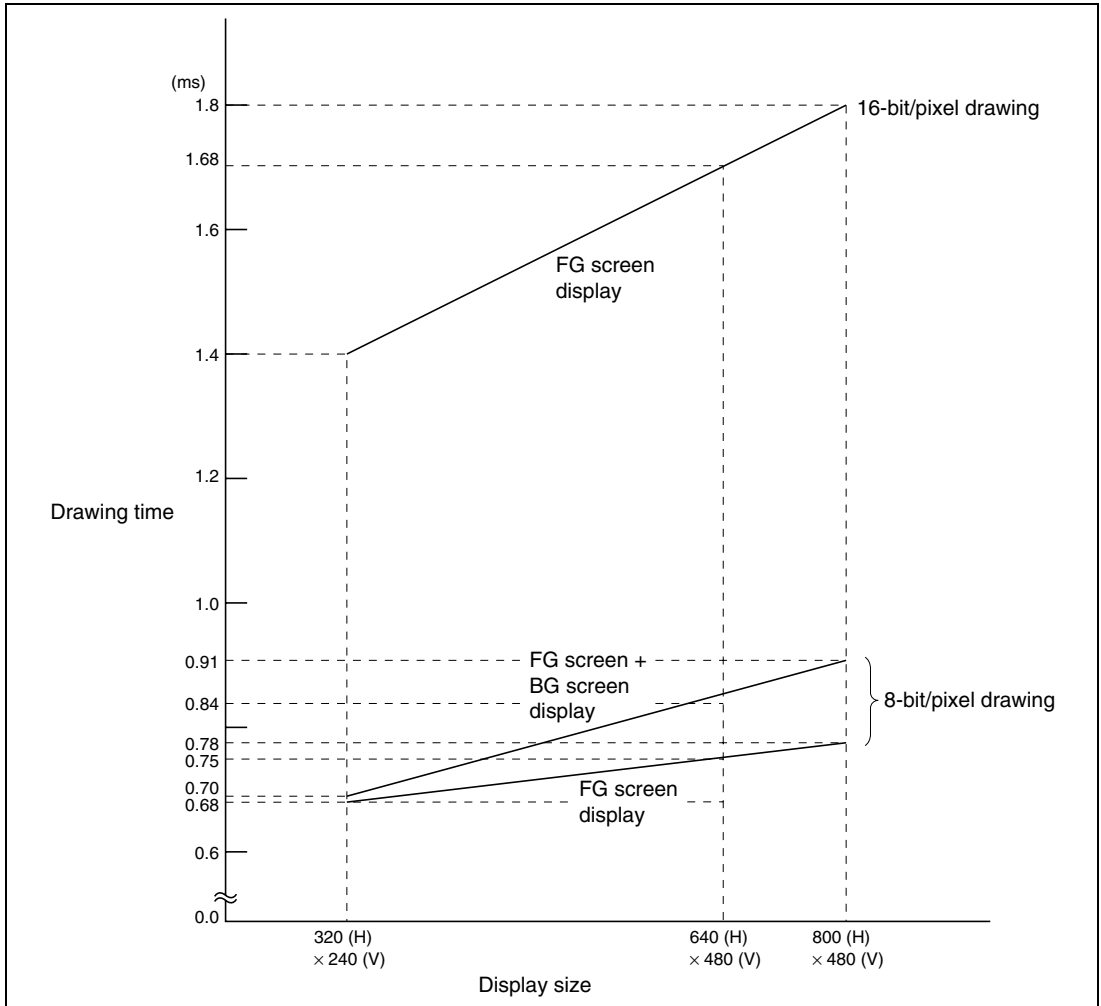


Figure I.2 POLYGON4C Drawing Performance when FST = 1 (Drawing Range: 320 (H) × 240 (V))

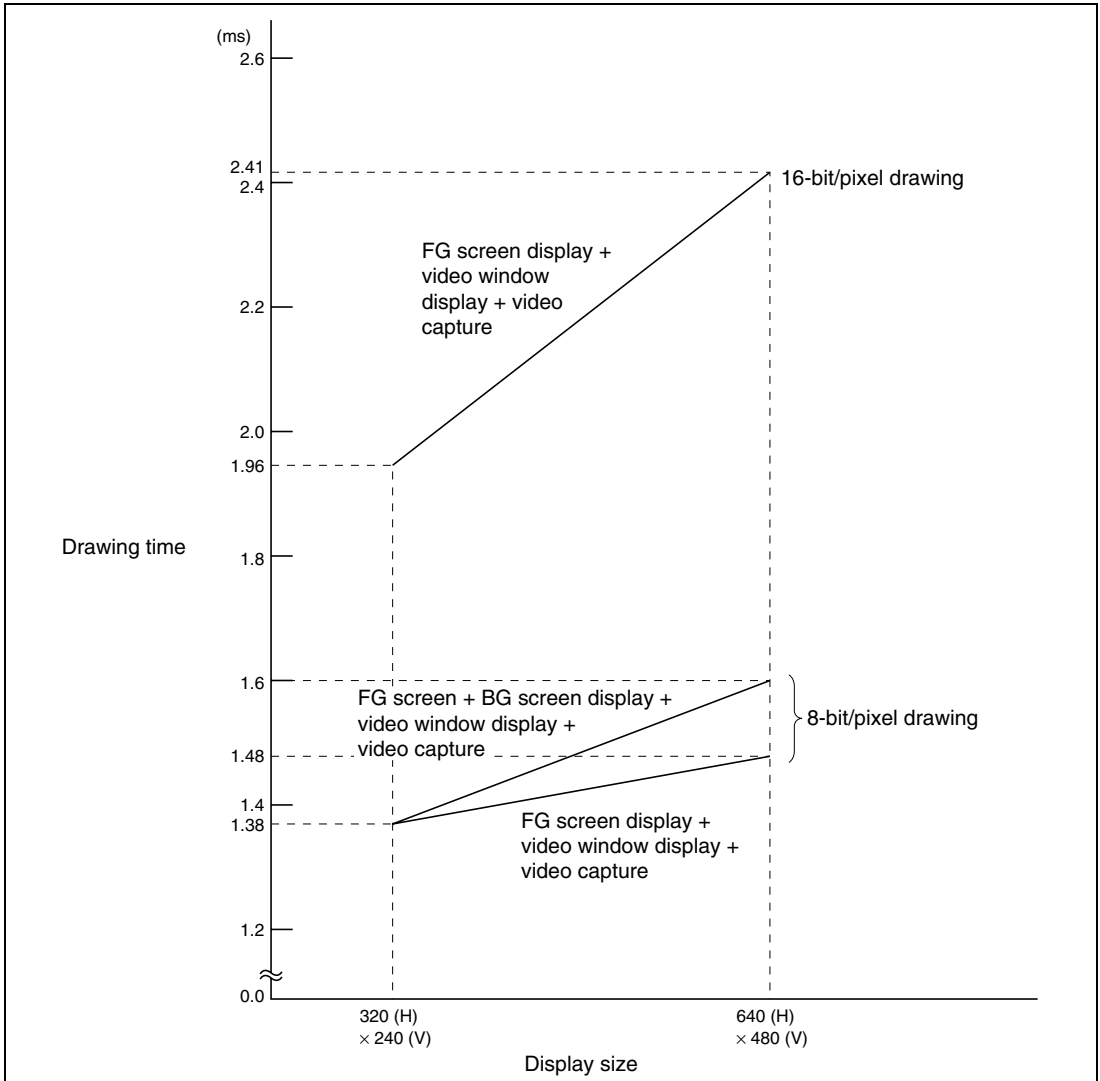


Figure I.3 POLYGON4C Drawing Performance when FST = 0 (Drawing Range: 320 (H) × 240 (V))

Appendix J Usage of Video Capture Function

J.1 Example of Video Capture Settings

J.1.1 Example of Interlace Composite Capture

- Description

  Video data with 640 × 480 is captured in interlace mode. Video screen data with 640 × 480 is displayed on the full-size screen.

- Q2SD register setting

  Video decoder initialization: Interlace output 640 × 480 mode

  MEMR : H′0031 (64 Mbits × 32 bits × 1)
  DSMR : H′0003 (non-interlace, master mode, refresh 3)
  REMR : H′0040 (BG: OFF, FG/BG: 8 bits, 1024 mode)
  DSX : H′0280 (640)
  DSY : H′01E0 (480)
  DSA0R : H′0000 (B′0000000)
  DSA1R : H′0008 (B′0080000)
  DSMR2 : H′0409 (video display ON, cursor1 display OFF, cursor2 display OFF, FG display OFF, YC → RGB conversion ON)
  HVPR : H′0000 (X coordinate 0)
  VVPR : H′0000 (Y coordinate 0)
  VSAH0 : H′0018 (B′0180000)
  VSAL0 : H′0000
  VSAH1 : H′0028 (B′0280000)
  VSAL1 : H′0000
  VSAH2 : H′0038 (B′0380000)
  VSAL2 : H′0000
  VSIZEX : H′0280 (640)
  VSIZEY : H′01E0 (480)
  VIMR : H′0005 (YC → RGB conversion OFF, interlace composite capture, horizontal reduction ratio 1, vertical reduction ratio 1)

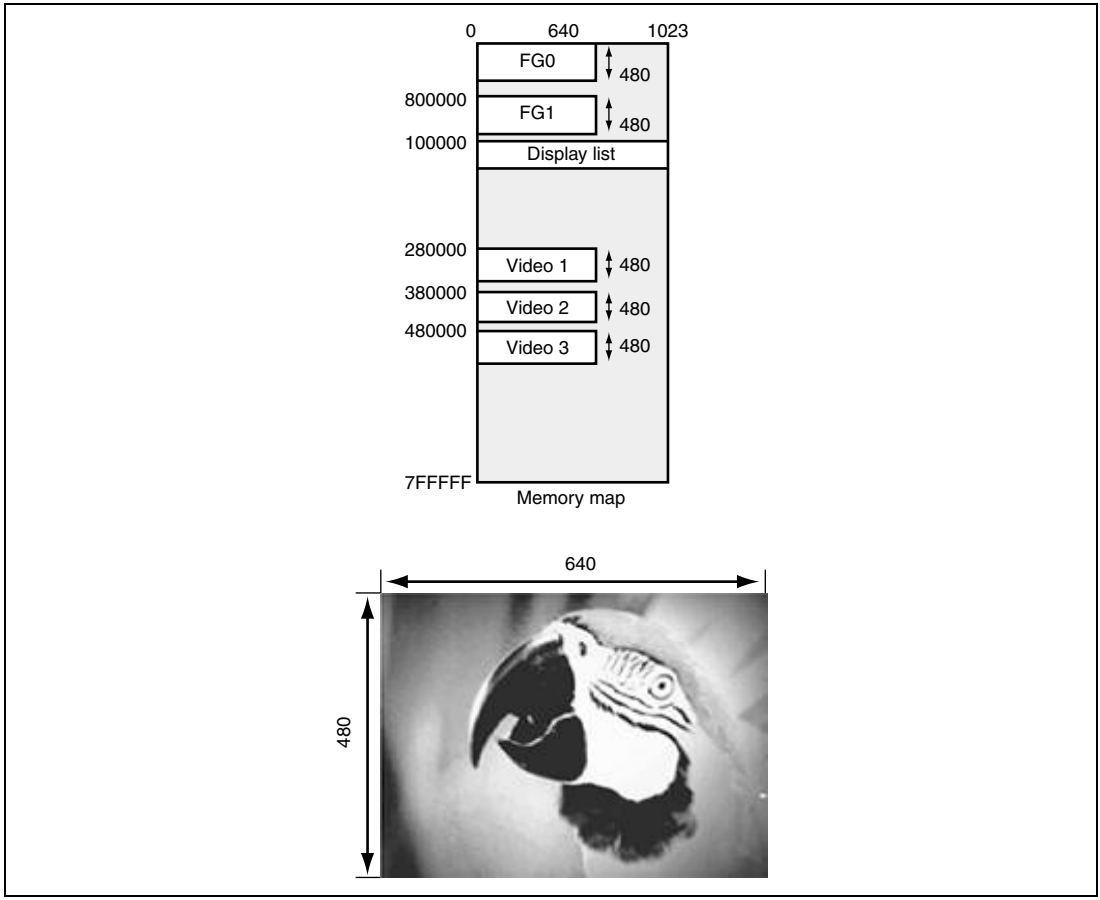


Figure J.1 Interlace Composite Capture

J.1.2 Example of Modifying Video Data Size

- Description

  Video data with 640 × 480 is captured. Both the horizontal and vertical reduction ratios are specified to 1/4 and the video display positions are shifted by 80 in the X and Y direction. The video screen data with 160 × 120 is displayed on the screen with 320 × 240.

- Q2SD register setting

  BT initialization program: Monitor command WW (video display size 640 × 480 mode)

  MEMR : H′0011 (16 Mbits × 16 bits × 2)
  DSMR : H′0003 (non-interlace, master mode, refresh 3)
  REMR : H′0400 (BG: ON, FG/BG: 8 bits, 512 mode)
  DSX : H′0140 (320)

DSY : H′00F0 (240)

DSA0R : H′0000 (B′0000000)

DSA1R : H′0002 (B′0020000)

DSMR2 : H′0409 (video display ON, cursor 1 display OFF, cursor 2 display OFF, FG display OFF, YC → RGB conversion ON)

HVPR : H′0050 (X coordinate 80)

VVPR : H′0050 (Y coordinate 80)

VSAH0 : H′0008 (B′0080000)

VSAL0 : H′0000

VSAH1 : H′0008 (B′0100000)

VSAL1 : H′0000

VSAH2 : H′0018 (B′0180000)

VSAL2 : H′0000

VSIZEX : H′00A0 (160)

VSIZEY : H′0078 (120)

VIMR : H′0385 (YC → RGB conversion OFF, interlace composite capture, horizontal reduction ratio 1/4, vertical reduction ratio 1/4)

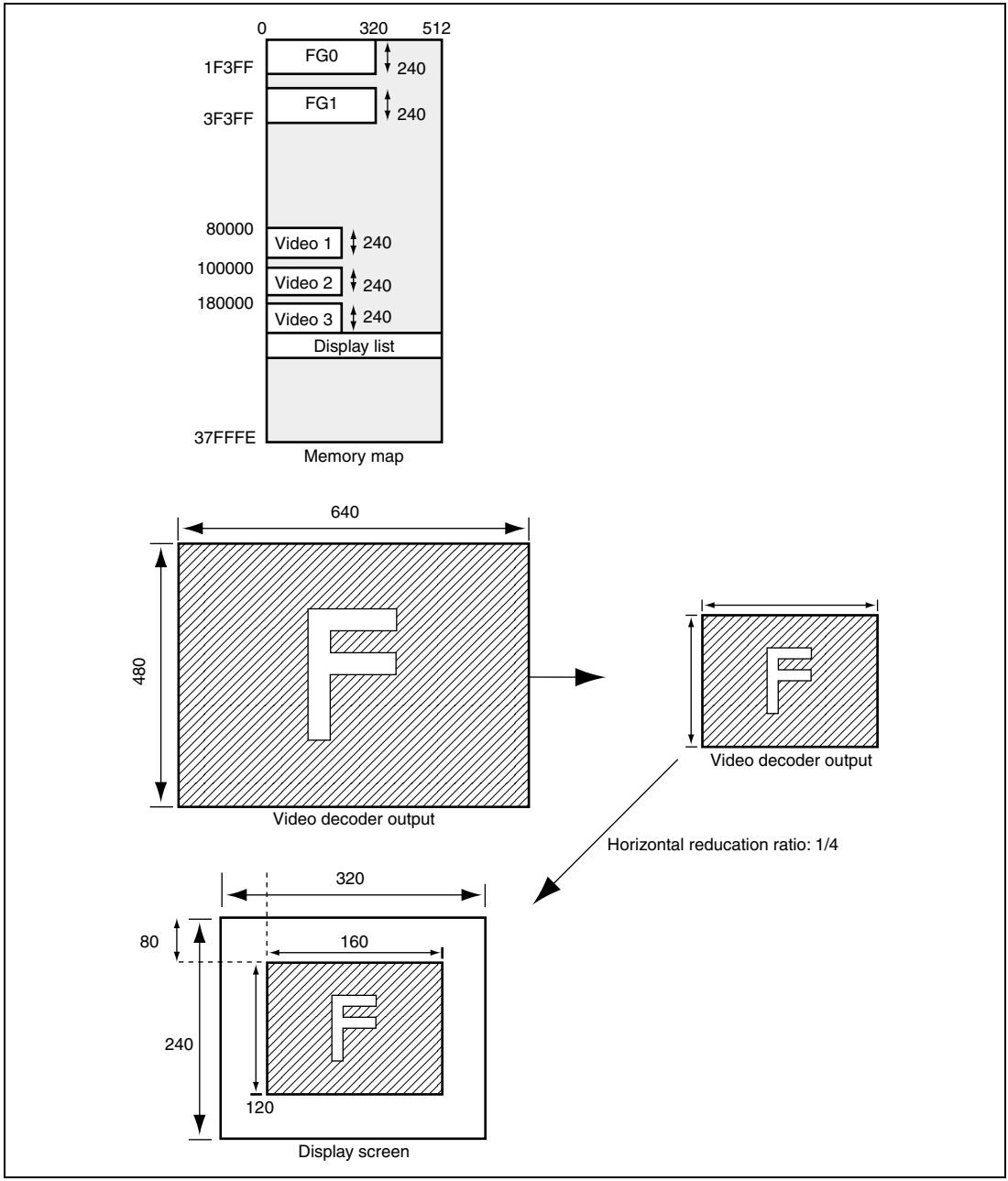


Figure J.2 Interlace Composite Capture (Horizontal and Vertical Reduction Ratios = 1/4)

J.2 Example of Usage of Captured Data

J.2.1 When Displaying Captured Data on Realtime Video Screen

When the VIE bit in VIMR is set to 1 and the VWE bit in DSMR2 is set to 1, the latest video stream data stored in the video storage area is displayed realtime. In this case, either of the following settings must be made.

- When the RGB bit in VMIR is 1, clear the VWRY in DSMR2 to 0.
- When the RGB bit in VMIR is 0, set the VWRY in DSMR2 to 1.

J.2.2 When Handling Captured Data as Multi-Valued Source Data

When VIE = 0 is set and video capturing is stopped, the video storage area where the latest video stream data is stored in the VID1,0 bits of VIMR is shown. If video capture function is executed when the RGB bit in VMIR is 1, it is possible to reference the video storage area specified by VID1,0 as a 16-bit/pixel multi-valued source. Additionally, VID1,0 has no meaning while video capturing is going on (VIE = 1). To reference VID1,0, first stop video capturing (VIE = 0).

- Description

  Video captured data is converted into RGB format and stored in the BG screen. At this time, the video captured data as multi-valued source is mapped onto figures and is drawn using drawing function.
- Q2SD register setting

  BT initialization program: Monitor command WW (video display size 640 × 480 mode)

  MEMR : H′0010 (16 Mbits × 16 nits × 2)
  DSMR : H′0405 (Non-interlace, master mode, refresh 5, BG: ON)
  REMR : H′0001 (FG/BG: 16 bits, 512 mode)
  DSX : H′0140 (320)
  DSY : H′00F0 (240)
  DSA0R : H′0000 (B′0000000)
  DSA1R : H′0004 (B′0040000)
  BGSX : H′0000 (0)
  BGSY : H′0200 (512)
  DSMR2 : H′0001 (video display ON, cursor 1 display OFF, cursor 2 display OFF, FG display ON, YC → RGB conversion OFF)
  HVPR : H′00A0 (X coordinate 160)
  VVPR : H′0078 (Y coordinate 120)
  VSAH0 : H′0008 (B′0080000)

VSAL0 : H′0000

VSAH1 : H′0008 (B′0081400)

VSAL1 : H′1400

VSAH2 : H′0009 (B009C100)

VSAL2 : H′C100

VSIZEX : H′00A0 (160)

VSIZEY : H′0078 (120)

VIMR : H′0183 (YC → RGB conversion ON, Non-interlace capture, horizontal reduction ratio 1/4, vertical reduction ratio 1/4)

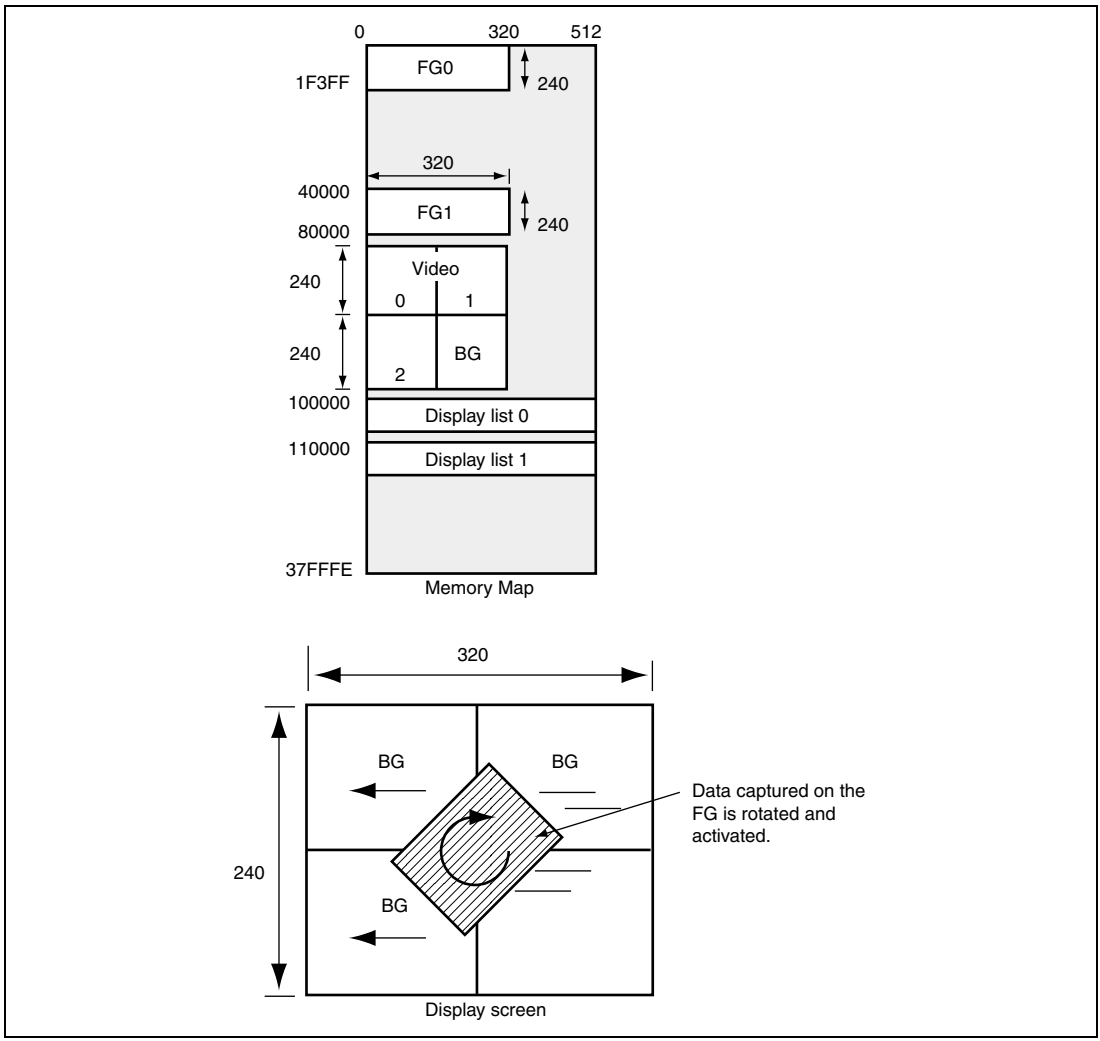


Figure J.3 Example of Video Data Usage

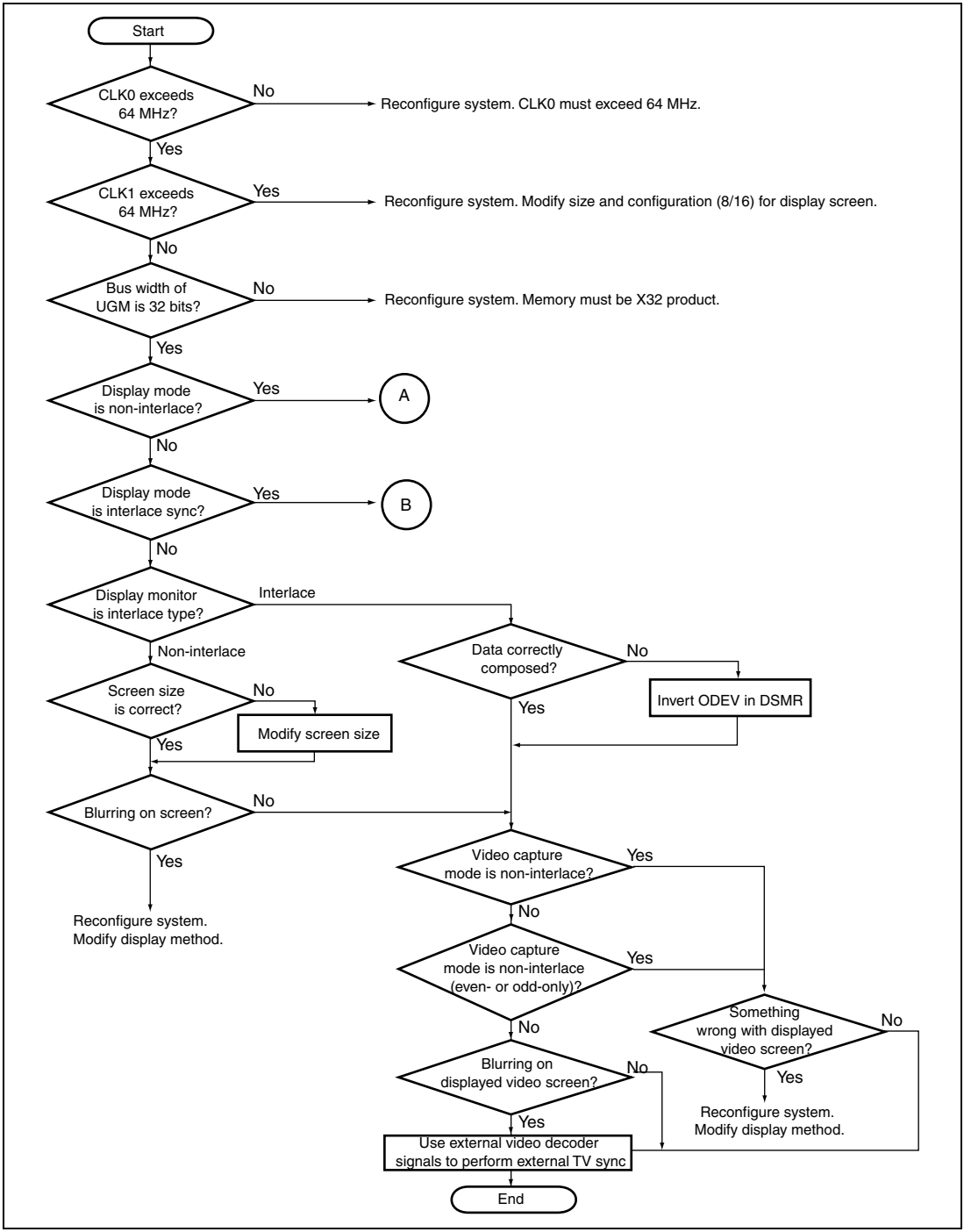


Figure J.4 Q2SD Video Setting Flow (1)

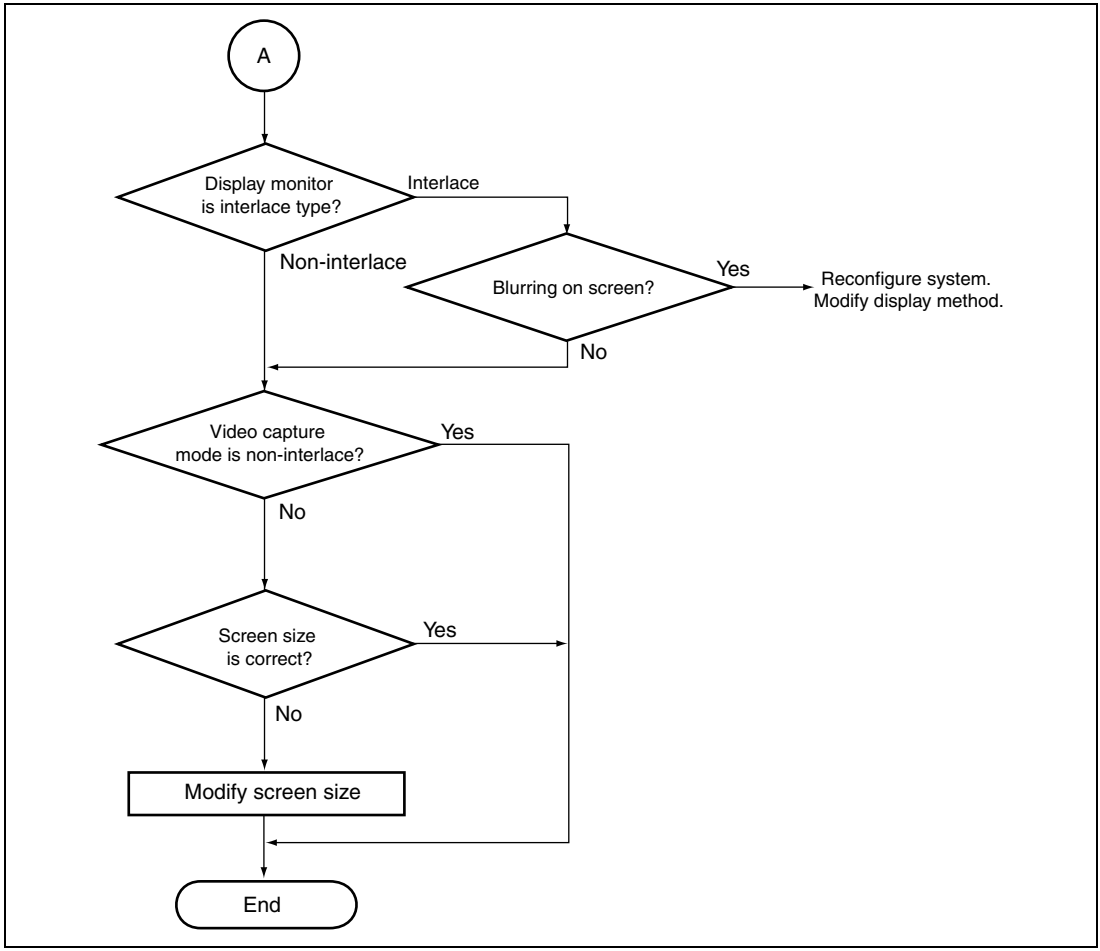


Figure J.5 Q2SD Video Setting Flow (2)

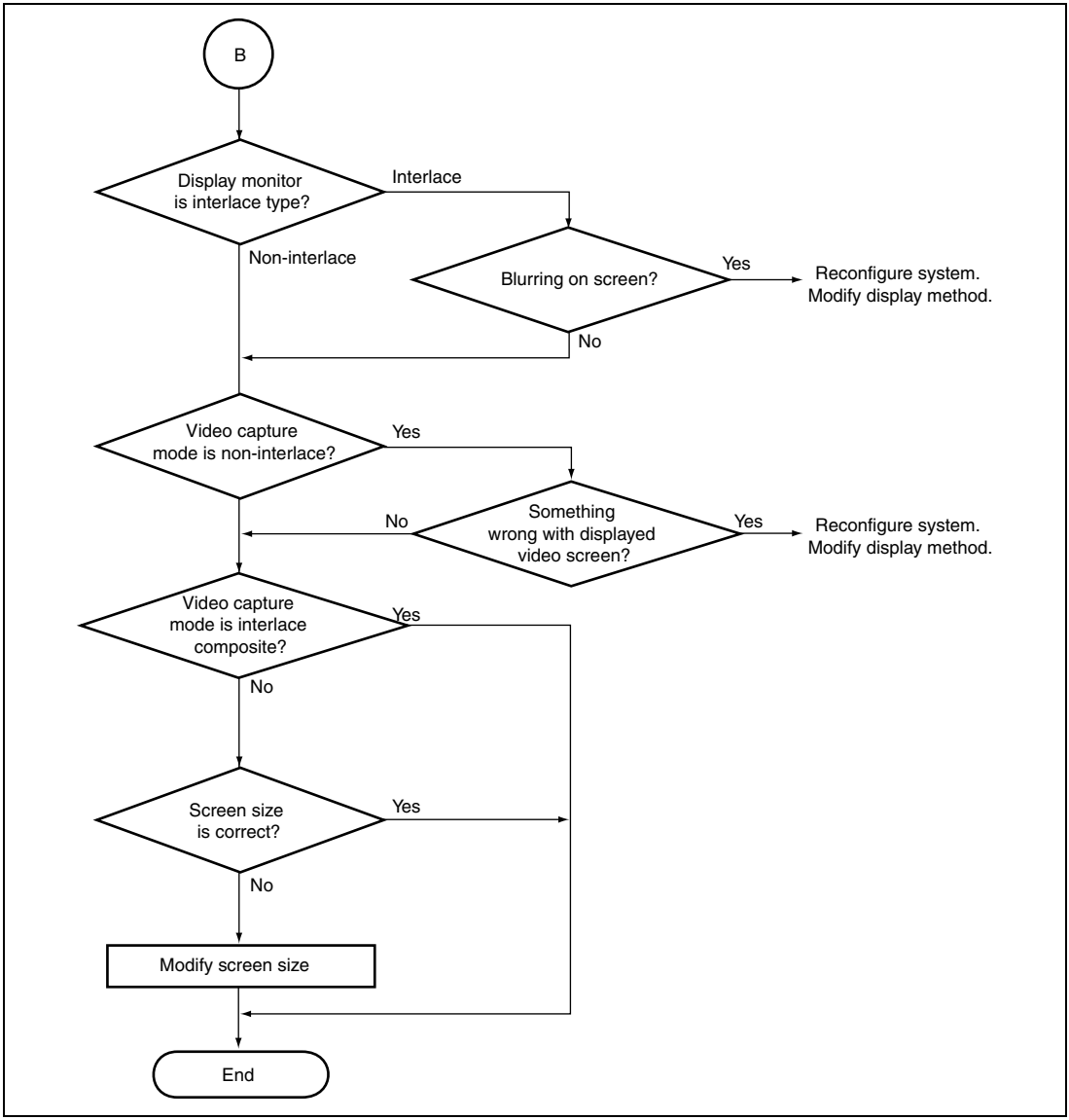


Figure J.6 Q2SD Video Setting Flow (3)

J.3 Video Decoder

J.3.1 Field Control by Video Decoder

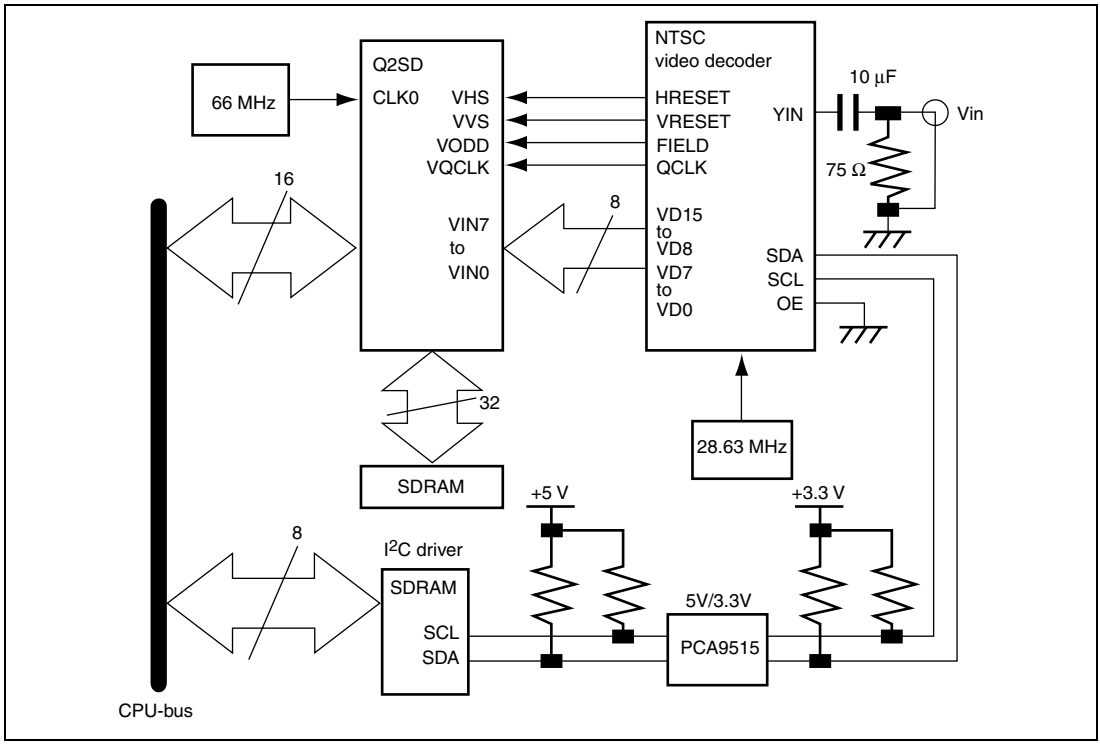


Figure J.7 Example of Connection of Video Capture Circuit

Since the video decoder in this figure is a mixed-analog-digital device with a 5-V power-supply and a 3.3-V digital interface, the I^2C interface requires conversion from 5 V to 3.3V.

The Q2SD and video decoder are only connected by the eight data lines (VIN0 to VIN7), sync-signal lines (VHS and VVS), sync-clock line (VQCLK), and field-signal line (VODD).

The I^2C driver connected to the video decoder via the PCA9515 is used to set the video decoder by the CPU.

The combination of fields in interlacing by the Q2SD can be switched to match the source. Since the combination of fields (top and bottom fields) is not explicitly stipulated in the NTSC specification, two combinations are possible. Most video decoders, therefore, include a polarity-inversion function for the FIELD signal.

Frame	1		2		3		4		1		2		3		4	
Top	1		3		5		7			2		4		6		8
Bottom		2		4		6		8	1		3		5		7	
Format			Top first (TV, DVD)								Bottom first					

An example of the timing of the output of data in the interlaced operation of an NTSC video decoder is shown in figure J.8. For most video decoders, the timing of the transitions of the FIELD signal in interlaced operation differs between the odd and even fields.

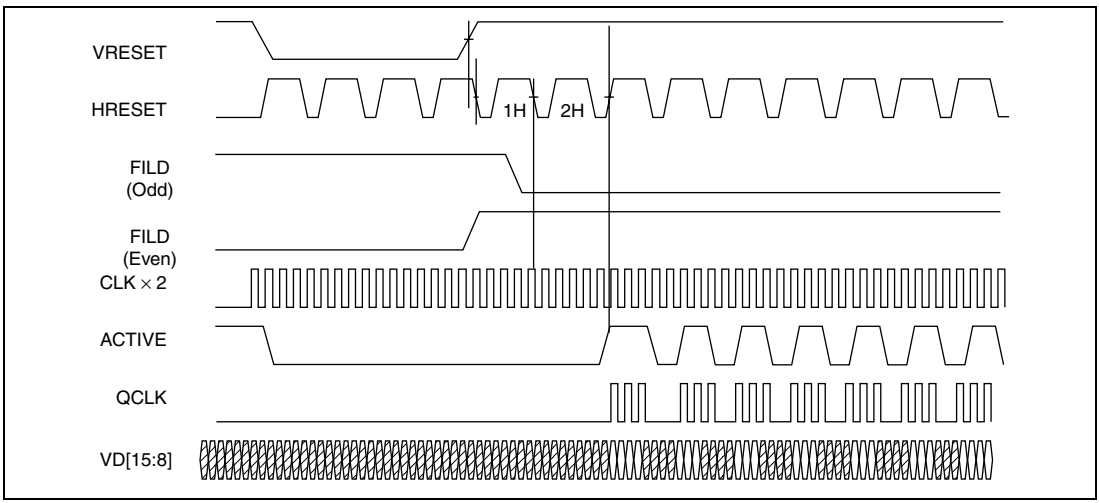


Figure J.8 Example of Interlaced Data Output Timing for Decoder

J.3.2 Video Decoder Settings

The Q2SD's video-input function should be configured to operate with a video decoder which outputs data in the 8-bit streaming video format prescribed in ITU-601. The operation of the following decoders has been examined at our company: the Bt815A, Bt817A, Bt819A, Bt827A/B, Bt829A/B, and Bt835. All of these decoders are manufactured by Rockwell.

When the video decoder is connected to the Q2SD, the video decoder is controlled via the I2C interface. The video decoder thus must be initialized by the CPU via the I2C interface or I2C driver before the video data is captured. The following settings are needed.

- Data output format : Any mode of NTSC
- Data size : VGA/QVGA/Any
- Output format: Interlaced/non-interlaced
- Interface : 8-bit video stream
- Contrast : Any

- Luminance : Any
- Hue : Any

The data size should be specified as the maximum size except where the reduction size for video capture cannot be specified. However, when the size in the Y direction is specified in the video decoder, an external circuit in which the VHS and VQCLK signals are not output on the invalid line may be required.

Contrast, luminance, and hue values for the sequence of images to be captured should be specified to registers in the video decoder.

Appendix K Product Lineup

		Operating Temperature	Electrical Characteristics	Reliability
HD64413ASF	Regular specification products	0°C to +70°C	Shown in section 7	Standard
HD64413ASFI	Wide-range specification products	–40°C to +85°C	Shown in section 7 Ta = –40°C to +85°C	Standard
HD64413ASFD	High reliability products for automobile application	–40°C to +85°C	Shown in section 7 Ta = –40°C to +85°C	High reliability

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