

Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \text{ max}}$	I_D $T_A = 25^\circ\text{C}$
45V	46m Ω @ $V_{GS} = 10\text{V}$	4.8A
	62m Ω @ $V_{GS} = 4.5\text{V}$	4.1A

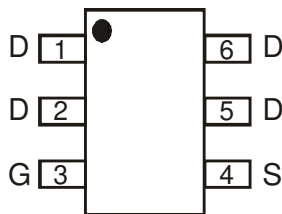
Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

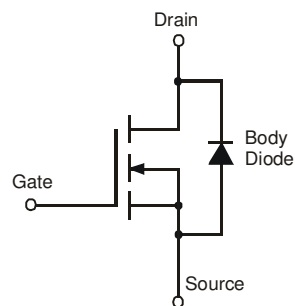
- DC-DC Converters
- Power management functions
- Backlighting



Top View



Top View
Pin Configuration



Equivalent Circuit

Features and Benefits

- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Lead, Halogen, and Antimony Free, RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

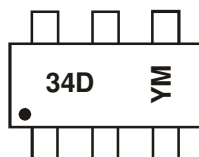
- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.013 grams (approximate)

Ordering Information (Note 3)

Part Number	Case	Packaging
DMN4060SVT-7	TSOT26	3,000/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. No purposely added lead. Halogen and Antimony free.
 2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
 3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



34D = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: Z = 2012)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	45	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	4.8 3.8	A
	$t < 10\text{s}$	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	6.1 4.8	A
Continuous Drain Current (Note 5) $V_{GS} = 5\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	4.1 3.2	A
	$t < 10\text{s}$	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	5.2 4.1	A
Maximum Body Diode Forward Current (Note 5)			I_S	2.1	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	30	A
Avalanche Current (Note 6) $L = 0.1\text{mH}$			I_{AR}	14.2	A
Avalanche Energy (Note 6) $L = 0.1\text{mH}$			E_{AR}	10	mJ

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 4)	$T_A = 25^\circ\text{C}$	P_D	1.2	W
	$T_A = 70^\circ\text{C}$		0.75	
Thermal Resistance, Junction to Ambient (Note 4)	Steady state	$R_{\theta JA}$	106	$^\circ\text{C/W}$
	$t < 10\text{s}$		69	$^\circ\text{C/W}$
Total Power Dissipation (Note 5)	$T_A = 25^\circ\text{C}$	P_D	1.8	W
	$T_A = 70^\circ\text{C}$		1.1	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	68	$^\circ\text{C/W}$
	$t < 10\text{s}$		44	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	20	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

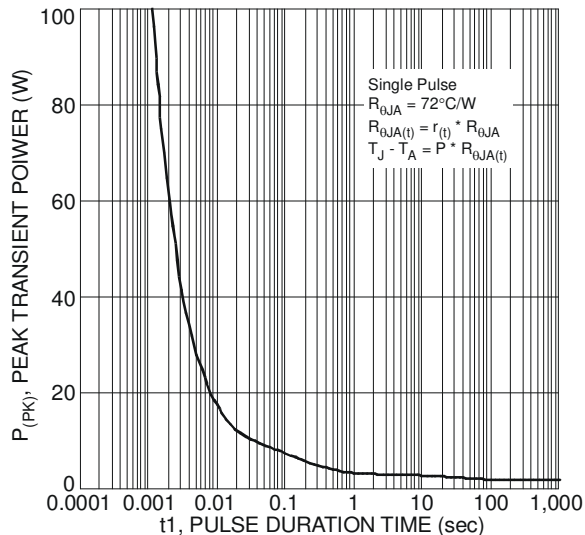


Fig. 1 Single Pulse Maximum Power Dissipation

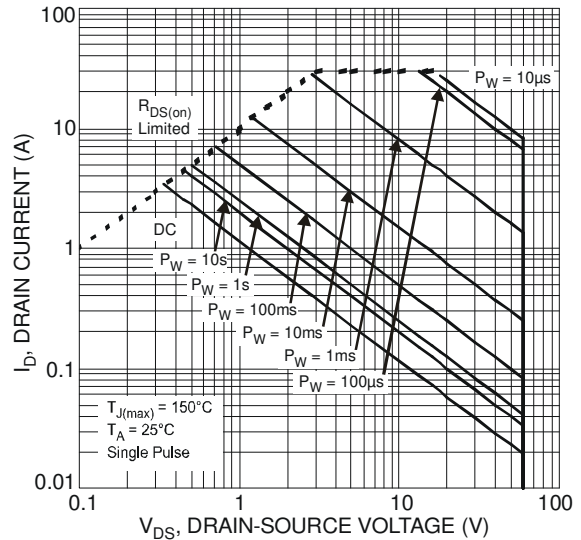


Fig. 2 SOA, Safe Operation Area

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	45	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	100	nA	V _{DS} = 45V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	1	—	3	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	37	46	mΩ	V _{GS} = 10V, I _D = 4.3A
		—	52	62		V _{GS} = 4.5V, I _D = 4A
Forward Transfer Admittance	Y _{fs}	—	4.5	—	S	V _{DS} = 10V, I _D = 4.3A
Diode Forward Voltage	V _{SD}	—	0.7	1.2	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	1287	—	pF	V _{DS} = 25V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	57	—		
Reverse Transfer Capacitance	C _{rss}	—	44	—		
Gate Resistance	R _G	—	1.2	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = 10V)	Q _g	—	22.4	—	nC	V _{DS} = 30V, I _D = 4.3A
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	10.4	—		
Gate-Source Charge	Q _{gs}	—	4.9	—		
Gate-Drain Charge	Q _{gd}	—	3.0	—		
Turn-On Delay Time	t _{D(on)}	—	6.6	—	nS	V _{GS} = 10V, V _{DD} = 30V, R _G = 6Ω, I _D = 4.3A
Turn-On Rise Time	t _r	—	8.1	—		
Turn-Off Delay Time	t _{D(off)}	—	20.1	—		
Turn-Off Fall Time	t _f	—	4.0	—		
Body Diode Reverse Recovery Time	t _{rr}	—	18	—	nS	I _S = 4.3A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	—	11.9	—	nC	I _S = 4.3A, di/dt = 100A/μs

- Notes: 4. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch square copper plate.
6. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J = 25°C
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

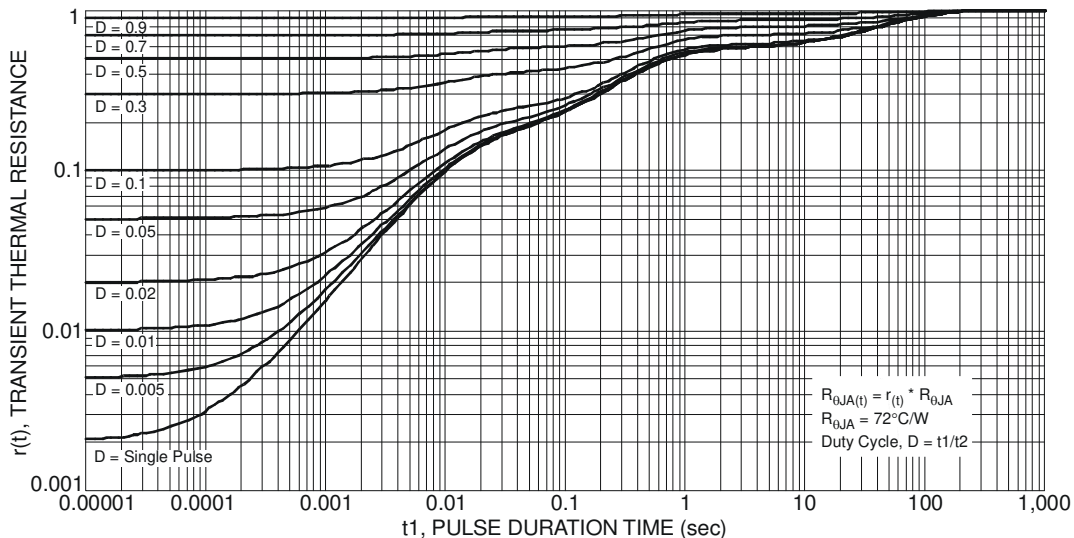


Fig. 3 Transient Thermal Resistance

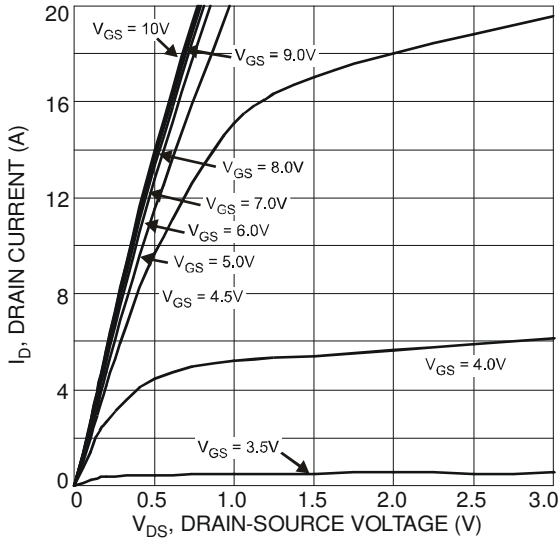


Fig. 4 Typical Output Characteristic

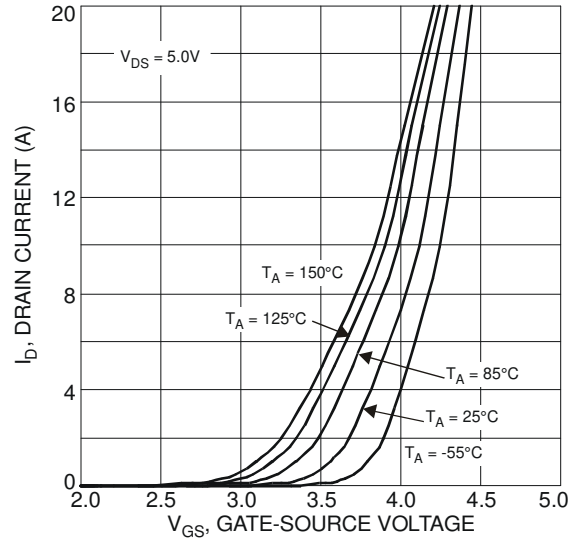


Fig. 5 Typical Transfer Characteristics

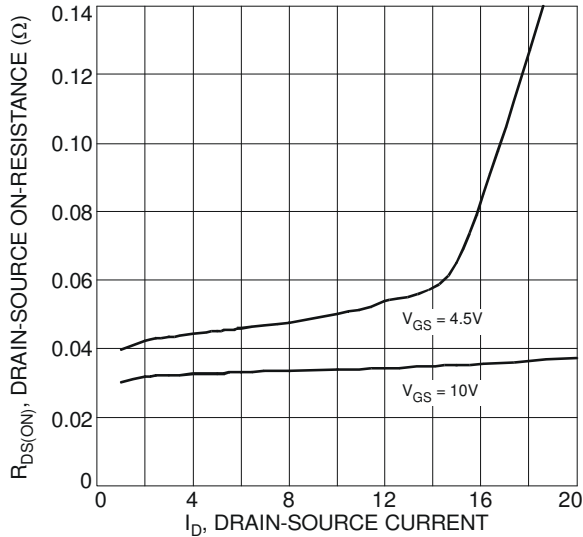


Fig. 6 Typical On-Resistance vs. Drain Current and Gate Voltage

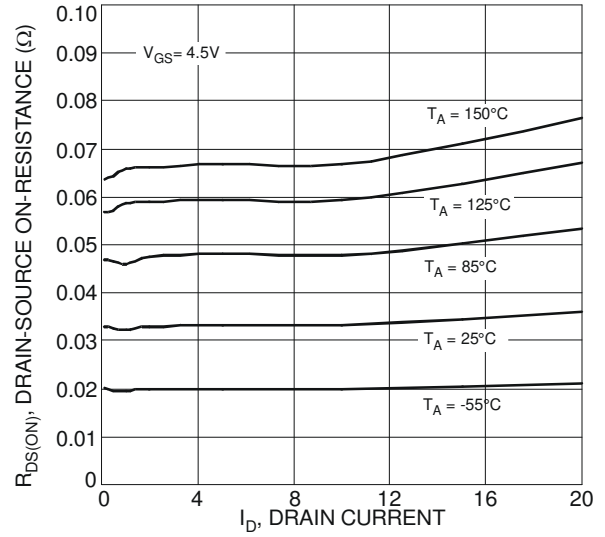


Fig. 7 Typical On-Resistance vs. Drain Current and Temperature

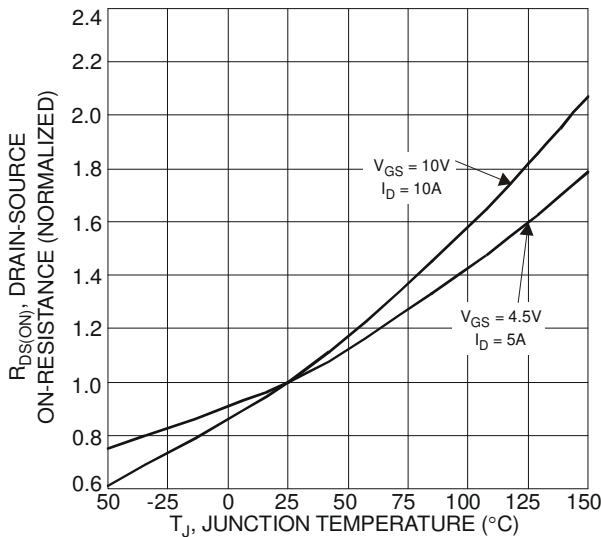


Fig. 8 On-Resistance Variation with Temperature

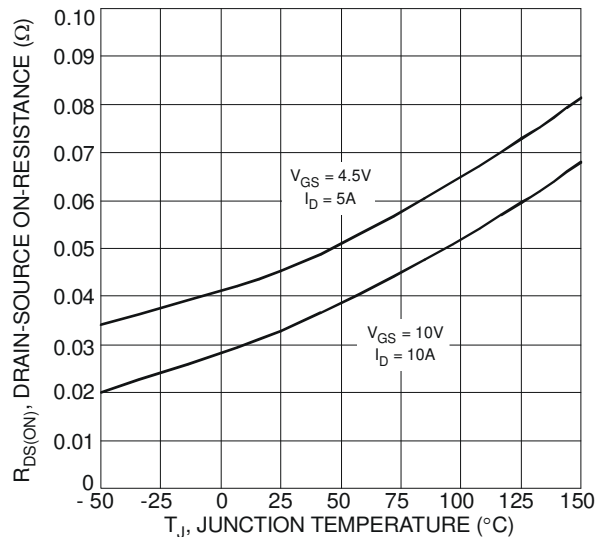


Fig. 9 On-Resistance Variation with Temperature

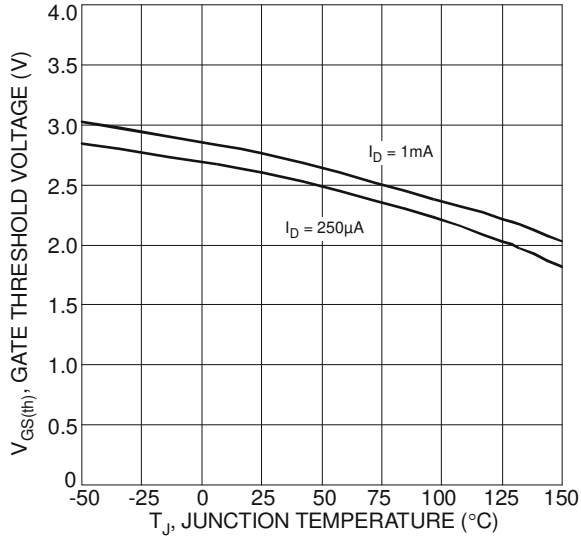


Fig. 10 Gate Threshold Variation vs. Ambient Temperature

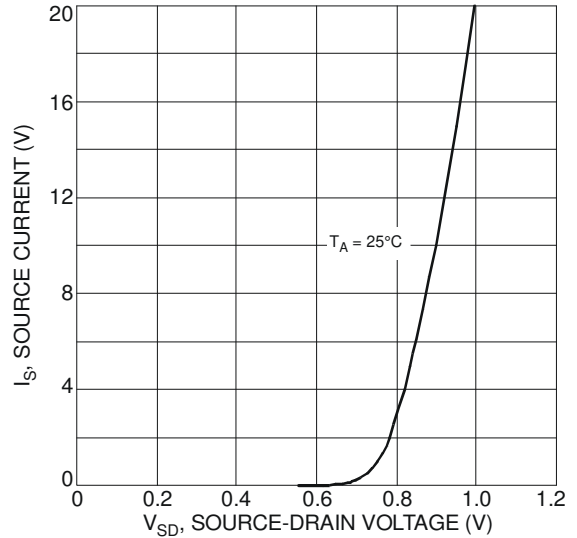


Fig. 11 Diode Forward Voltage vs. Current

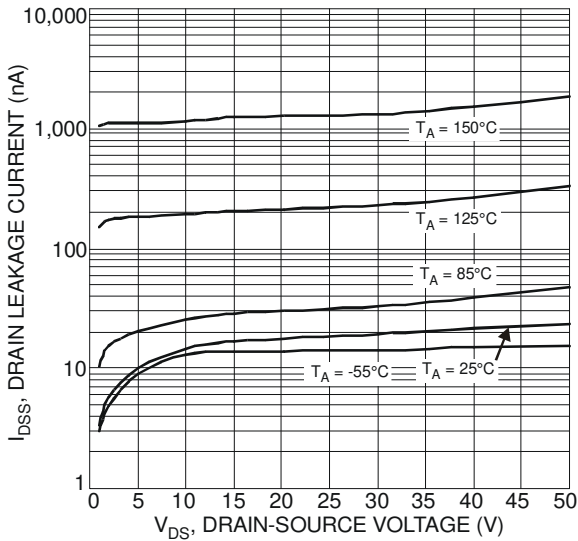


Fig. 12 Typical Drain-Source Leakage Current vs. Voltage

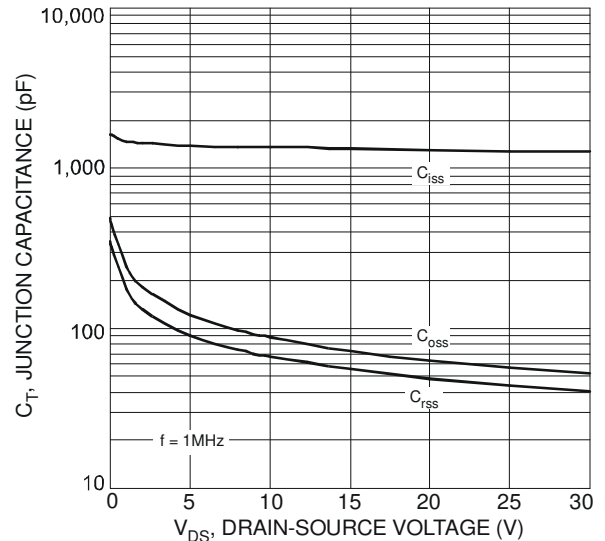


Fig. 13 Typical Junction Capacitance

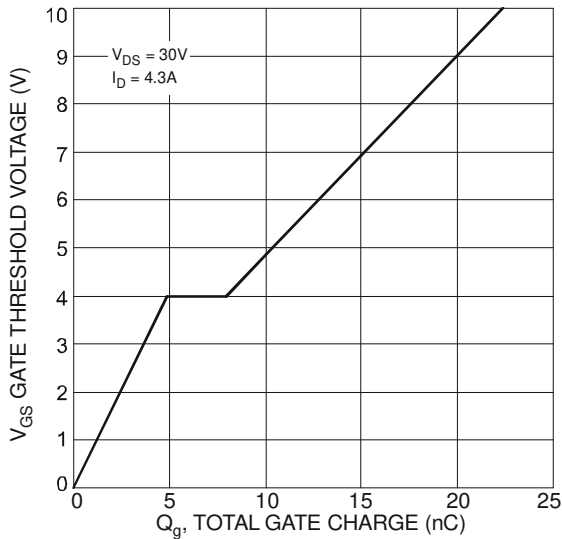
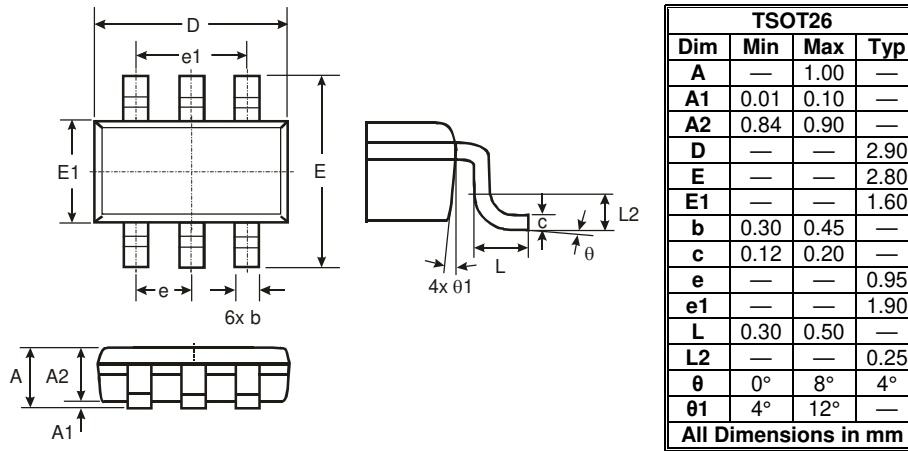
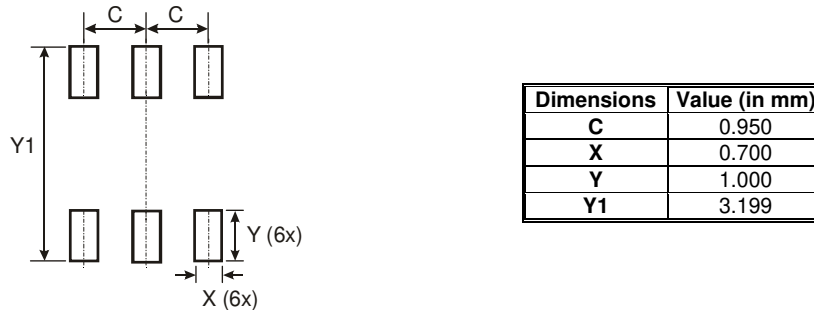


Fig. 14 Gate Charge

Package Outline Dimensions



Suggested Pad Layout



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