



# IS31FL3726

## TYPICAL APPLICATION CIRCUIT

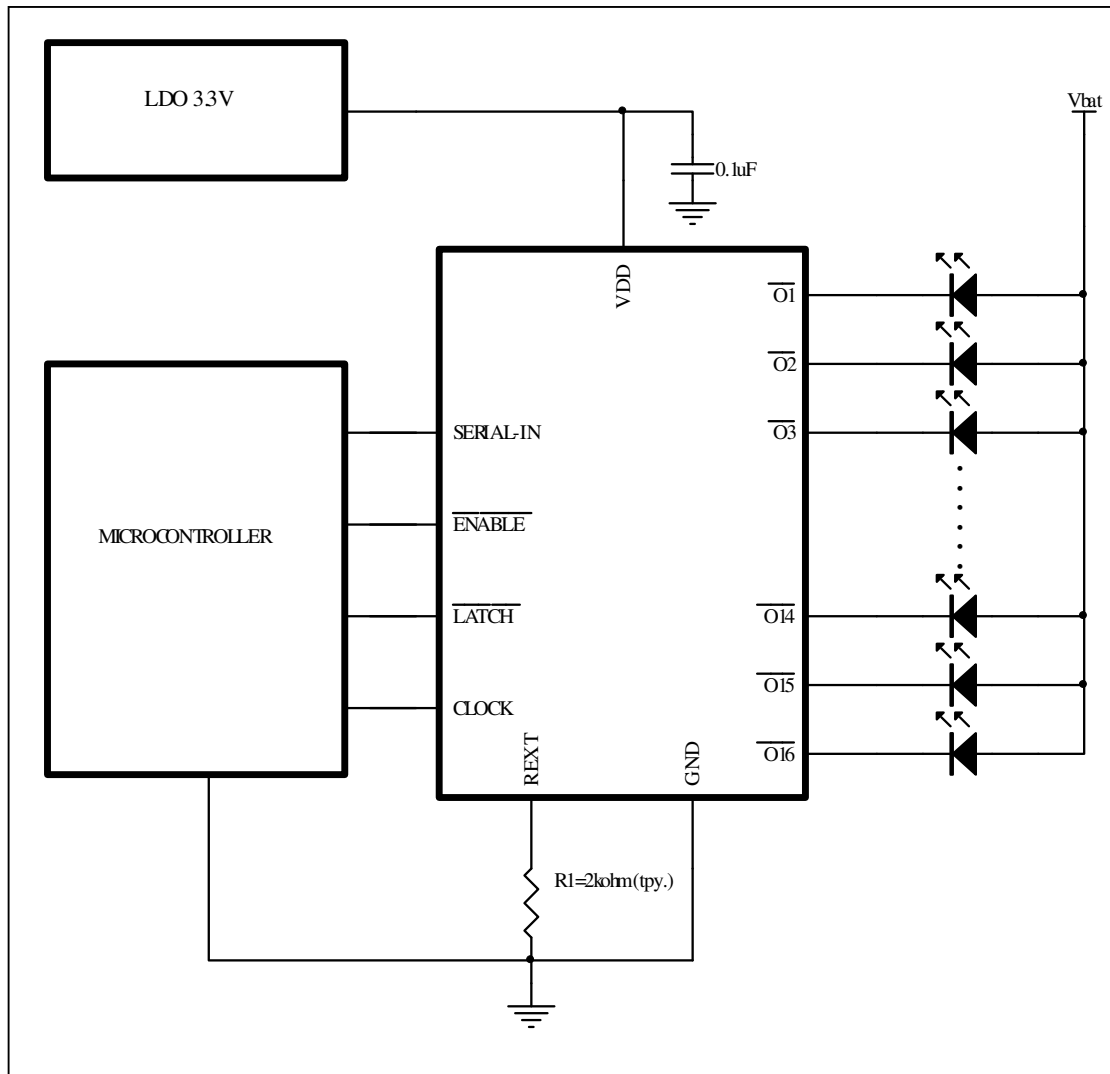
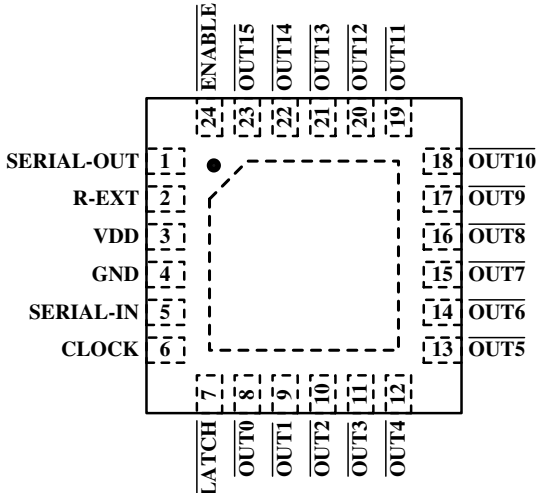
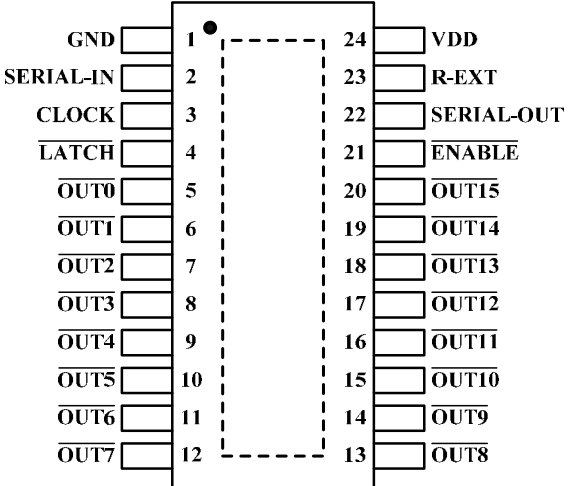


Figure 2 Typical Application Figure

# IS31FL3726

## PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	
TSSOP-24	

# IS31FL3726

## PIN DESCRIPTION

No.		Pin	Description
QFN	TSSOP		
1	22	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal.
2	23	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
3	24	VDD	Supply voltage terminal.
4	1	GND	GND terminal for control logic.
5	2	SERIAL-IN	Input terminal for serial data for data shift register.
6	3	CLOCK	Input terminal for clock for data shift on rising edge.
7	4	$\overline{\text{LATCH}}$	Input terminal for data strobe. When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low, data is latched.
8 ~ 23	5~20	$\overline{\text{OUT0}}\sim\overline{\text{OUT15}}$	Constant-current output terminals.
24	21	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ( $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ ) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High. And are turned on, when the terminal is driven Low.
		Thermal Pad	Connect to GND.



# IS31FL3726

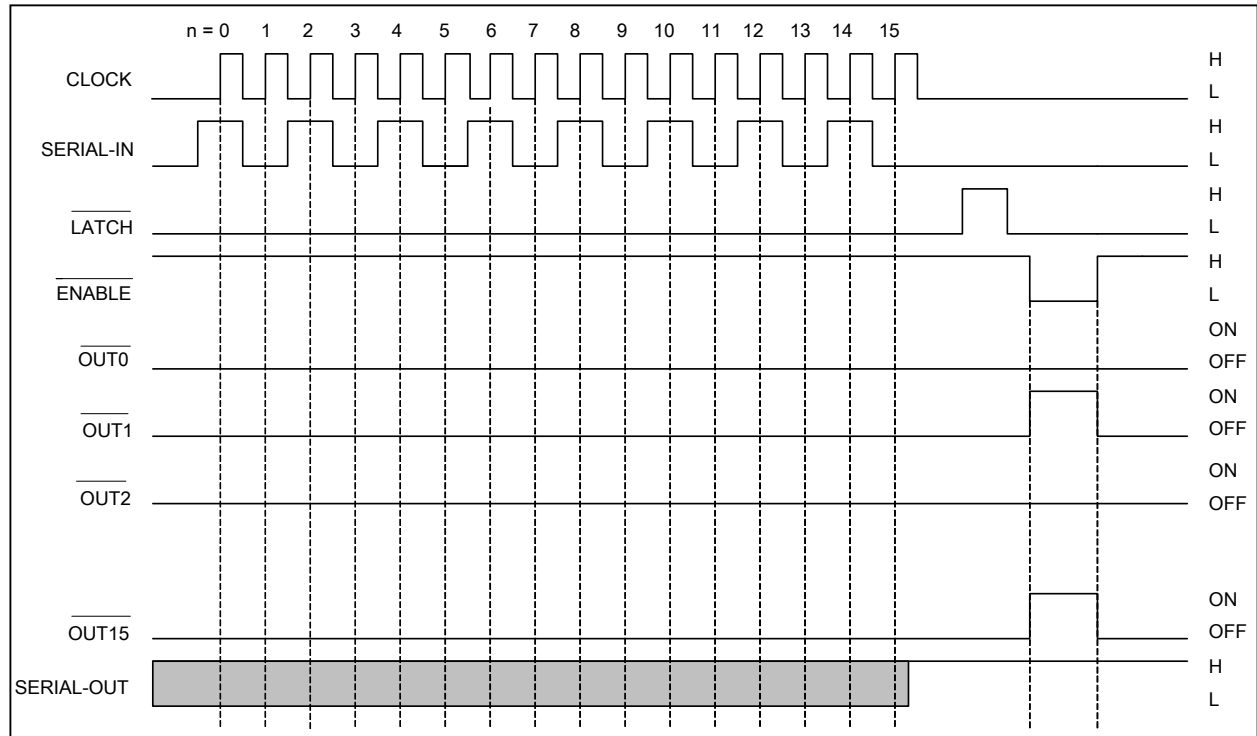
## ORDERING INFORMATION

**Industrial Range: -40°C to +85°C**

Order Part No.	Package	QTY/Reel
IS31FL3726-QFLS2-TR	QFN-24, Lead-free	2500/Reel
IS31FL3726-ZLS2-TR	TSSOP-24, Lead-free	2500/Reel
IS31FL3726-ZLS2		62/Tube

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances



**Figure 3** Timing Diagram

**Warning:** Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

**Note :** The latches circuit holds data by pulling the L A T C H terminal Low. And, when L A T C H terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output. When E N A B L E terminal is a Low level, output terminal O U T 0 to O U T 1 5 respond to the data, and on and off does. And, when E N A B L E terminal is a High level, it offs with the output terminal regardless of the data.

### Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ...OUT7 ... OUT15	SERIAL-OUT
↑	H	L	D <sub>n</sub>	D <sub>n</sub> ...D <sub>n-7</sub> ...D <sub>n-15</sub>	D <sub>n-15</sub>
↑	L	L	D <sub>n+1</sub>	No change	D <sub>n-14</sub>
↑	H	L	D <sub>n+2</sub>	D <sub>n+2</sub> ...D <sub>n-5</sub> ...D <sub>n-13</sub>	D <sub>n-13</sub>
↓	X	L	D <sub>n+3</sub>	D <sub>n+2</sub> ...D <sub>n-5</sub> ...D <sub>n-13</sub>	D <sub>n-13</sub>
↓	X	H	D <sub>n+3</sub>	OFF	D <sub>n-13</sub>

**Note :** OUT0 to OUT15 =On when D<sub>n</sub> = H; OUT0 to OUT15 =Off when D<sub>n</sub> = L. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

**Warning:** The following conditions, ENABLE=0, LATCH=1, SERIAL-IN=1, cannot be configured at the same time when power on, or IS31FL3726 will be abnormal.



# IS31FL3726

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}$	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{DD}+0.2V$
Maximum junction temperature, $T_{JMAX}$	150°C
Storage temperature range, $T_{STG}$	-65°C ~ +150°C
Operating temperature range, $T_A$	-40°C ~ +85°C

### Note:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITION

$T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
$V_{OUT}$	Output voltage			0.7	4	V
$f_{CLK}$	Clock frequency (Note 1)	Cascade connected			20	MHz
$t_{WLAT}$	$\overline{\text{LATCH}}$ pulse width		50			ns
$t_{WCLK}$	CLOCK pulse width		25			ns
$t_{WENA}$	$\overline{\text{ENABLE}}$ pulse width (Note 1,2)	Upper $I_{OUT} = 20\text{mA}$	20			$\mu\text{s}$
		Lower $I_{OUT} = 20\text{mA}$	20			
$t_{SETUP1}$	Set-up time for CLOCK terminal		10			ns
$t_{HOLD}$	Hold time for CLOCK terminal		10			ns
$t_{SETUP2}$	Set-up time for $\overline{\text{LATCH}}$ terminal		50			ns

**Note 1:** Guaranteed by design.

**Note 2:** When the pulse of the Low level is input to the  $\overline{\text{ENABLE}}$  terminal held in the High level.

# IS31FL3726

## ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \sim 5.5\text{V}$ , unless otherwise specified.

Symbol	Characteristic	Condition		Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	Normal operation		3.3		5.5	V
$I_{OUT1}$	Output current	$V_{OUT} = 0.4\text{V}$ $V_{DD} = 3.3\text{V}$	$R_{EXT} = 1\text{k}\Omega$	15	18.7	22	mA
$I_{OUT2}$		$V_{OUT} = 0.4\text{V}$ $V_{DD} = 5.5\text{V}$		15	18.9	22	
$\Delta I_{OUT1}$	Output current error between bits	$V_{OUT} \geq 0.4\text{V}$ , All outputs on	$R_{EXT} = 1\text{k}\Omega$		$\pm 3$	$\pm 4$	%
$I_{OZ}$	Output leakage current input voltage	$V_{OUT} = 5.0\text{V}$				1	$\mu\text{A}$
$V_{IH}$	Input voltage			1.4			V
$V_{IL}$						0.4	
$V_{OL}$	SOUT terminal voltage	$I_{OL} = 1.0\text{mA}$ , $V_{DD} = 3.3\text{V}$				0.3	V
		$I_{OL} = 1.0\text{mA}$ , $V_{DD} = 5\text{V}$				0.3	
$V_{OH}$		$I_{OH} = -1.0\text{mA}$ , $V_{DD} = 3.3\text{V}$		3			
		$I_{OH} = -1.0\text{mA}$ , $V_{DD} = 5\text{V}$		4.7			
$\%/V_{DD}$	Output current supply voltage regulation	When $V_{DD}$ is changed 3.3V to 5.5V			-1		%
$R_{(Up)}$	Pull-up resistor	ENABLE terminal		250	500	750	$\text{k}\Omega$
$R_{(Down)}$	Pull-down resistor	LATCH terminal					
$I_{DD(OFF)1}$	Supply current	$V_{OUT} = 5\text{V}$	$R_{EXT} = \text{OPEN}$		1		mA
$I_{DD(OFF)2}$		$V_{OUT} = 5\text{V}$ All outputs off	$R_{EXT} = 1\text{k}\Omega$		4.5		
$I_{DD(ON)1}$		$V_{OUT} = 0.7\text{V}$ All outputs on	$R_{EXT} = 1\text{k}\Omega$		5		



# IS31FL3726

## SWITCHING CHARACTERISTICS

T<sub>A</sub> = 25°C, unless otherwise specified.

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
t <sub>pLH1</sub>	Propagation delay	CLK-OUT <sub>n</sub> , LATCH = "H" ENABLE = "L"		80	200	ns
t <sub>pLH2</sub>		LATCH-OUT <sub>n</sub> , ENABLE = "L"		80	200	
t <sub>pLH3</sub>		ENABLE-OUT <sub>n</sub> , LATCH = "H"		2000		
t <sub>pLH</sub>		CLK-SERIAL OUT	3	5		
t <sub>pHL1</sub>		CLK-OUT <sub>n</sub> , LATCH = "H" ENABLE = "L"		160	250	
t <sub>pHL2</sub>		LATCH-OUT <sub>n</sub> , ENABLE = "L"		160	250	
t <sub>pHL3</sub>		ENABLE-OUT <sub>n</sub> , LATCH = "H"		200	350	
t <sub>pLH</sub>		CLK-SERIAL OUT	4	6		
t <sub>or</sub>	Output rise time	10%~90% of voltage waveform	30	150	200	ns
t <sub>of</sub>	Output fall time	90%~10% of voltage waveform	150	200	250	ns
t <sub>r</sub>	Maximum CLOCK rise time	When not on PCB (Note)			5	us
t <sub>f</sub>	Maximum CLOCK fall time				5	us

**Conditions:** (Refer to test circuit.)

T<sub>opr</sub> = 25°C, V<sub>DD</sub>=V<sub>IH</sub> = 3.3V and 5V, V<sub>OUT</sub> = 0.7V, V<sub>IL</sub> = 0V, R<sub>EXT</sub> = 1000Ω, V<sub>L</sub> = 3.0V, R<sub>L</sub> = 60Ω, C<sub>L</sub> = 10.5pF

**Note:**

1. If the device is connected in a cascade and tr/tf for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.
2. Delay between outputs. The IS31FL3726 has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), OUT1 has 5ns delay, OUT2 has 10 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before ENABLE is low will still turn on and off at the determined delayed time regardless of the state of ENABLE. Therefore, every LED will be illuminated for the amount of time ENABLE is pulled high.

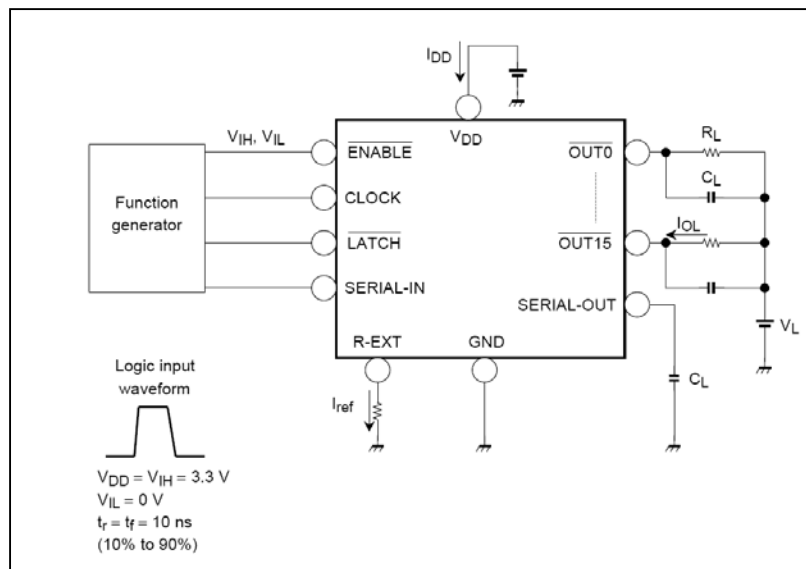
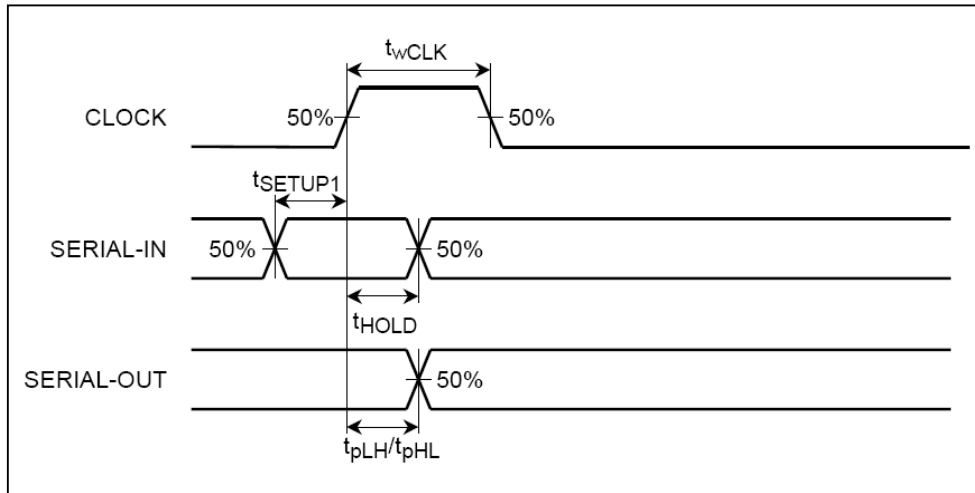


Figure 4 Test Diagram

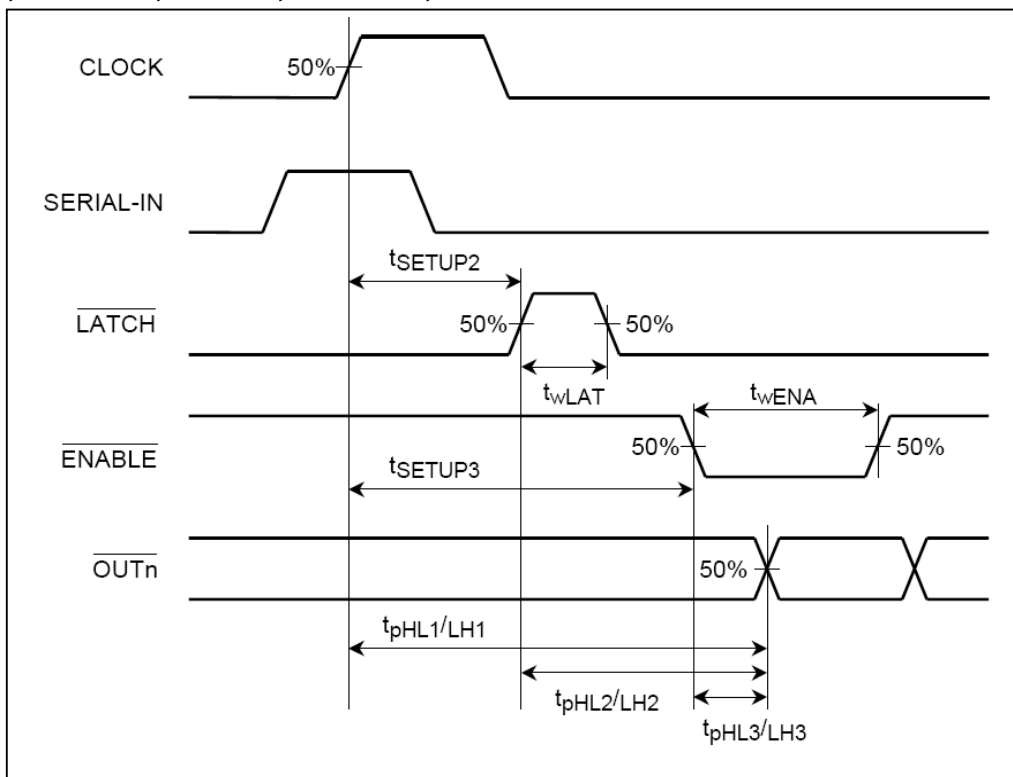
# IS31FL3726

## TIMING WAVEFORM

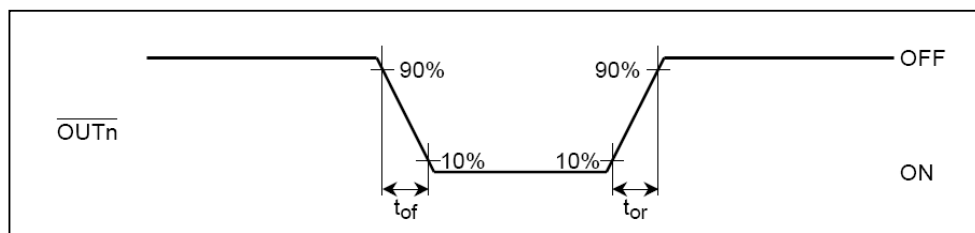
### 1. CLOCK, SERIAL-IN, SERIAL-OUT



### 2. CLOCK, SERIAL-IN, LATCH, ENABLE, OUTn



### 3. OUTn



# IS31FL3726

## TYPICAL OPERATING CHARACTERISTICS

### ADJUSTING OUTPUT CURRENT

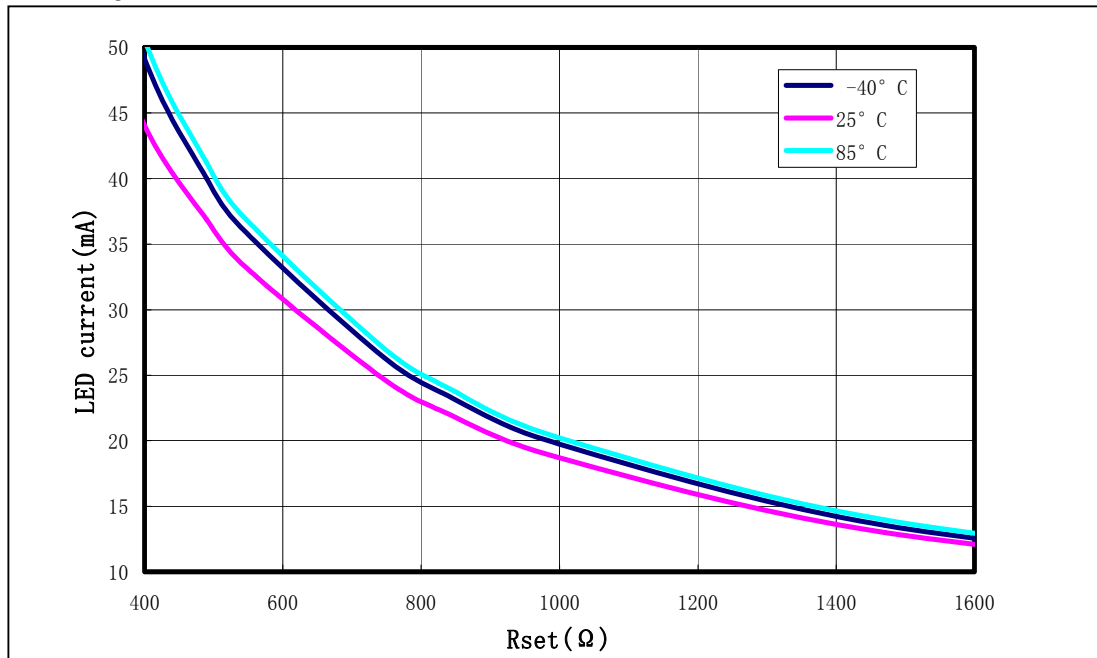
The output current of each channel is set by an external resistor  $R_{ext}$ , the relationship between  $I_{out}$  and  $R_{ext}$  is:

$$I_{out} = (V_{R-ext}/R_{ext}) \times 52$$

the  $V_{R-ext}$  is 0.36V in the IS31FL3726, so we can count the  $I_{out}$  as :

$$I_{out} = 0.36 \times 52 / R_{ext}$$

As show in the figure below:



# IS31FL3726

## CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T <sub>smin</sub> ) Temperature max (T <sub>smax</sub> ) Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	150°C 200°C 60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> ) Time at liquidous (t <sub>L</sub> )	217°C 60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak	8 minutes max.

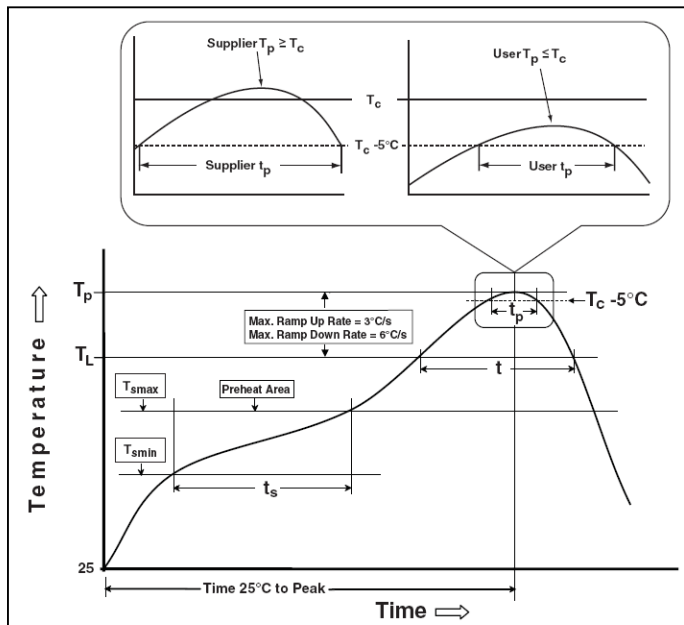
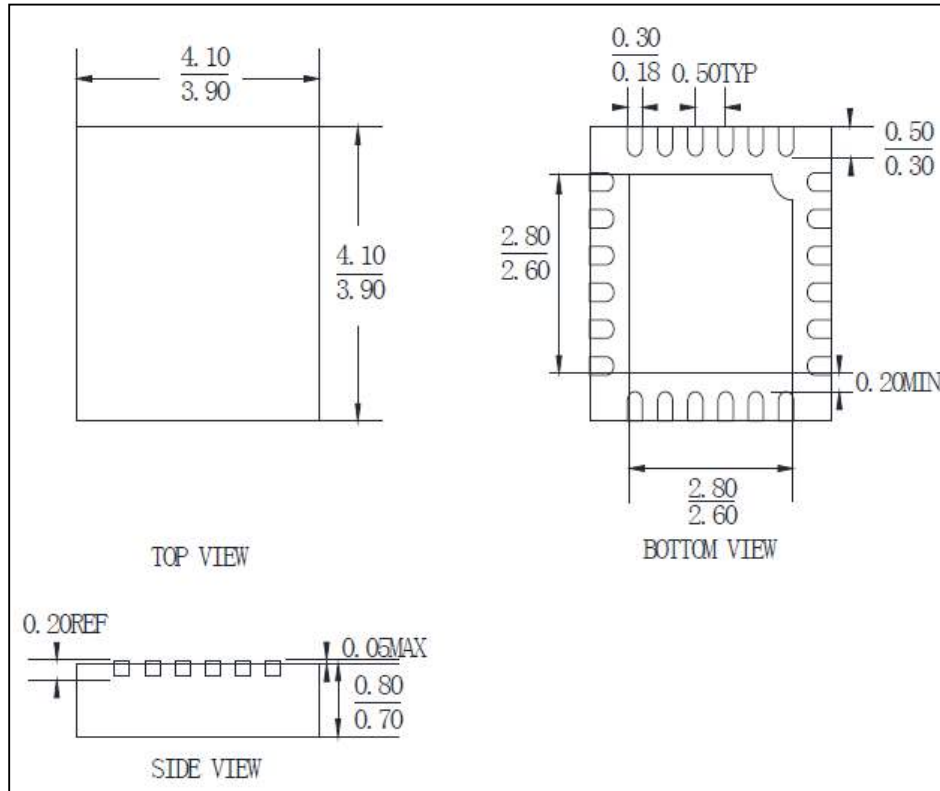


Figure 5 Classification Profile

# IS31FL3726

## PACKAGE INFORMATION

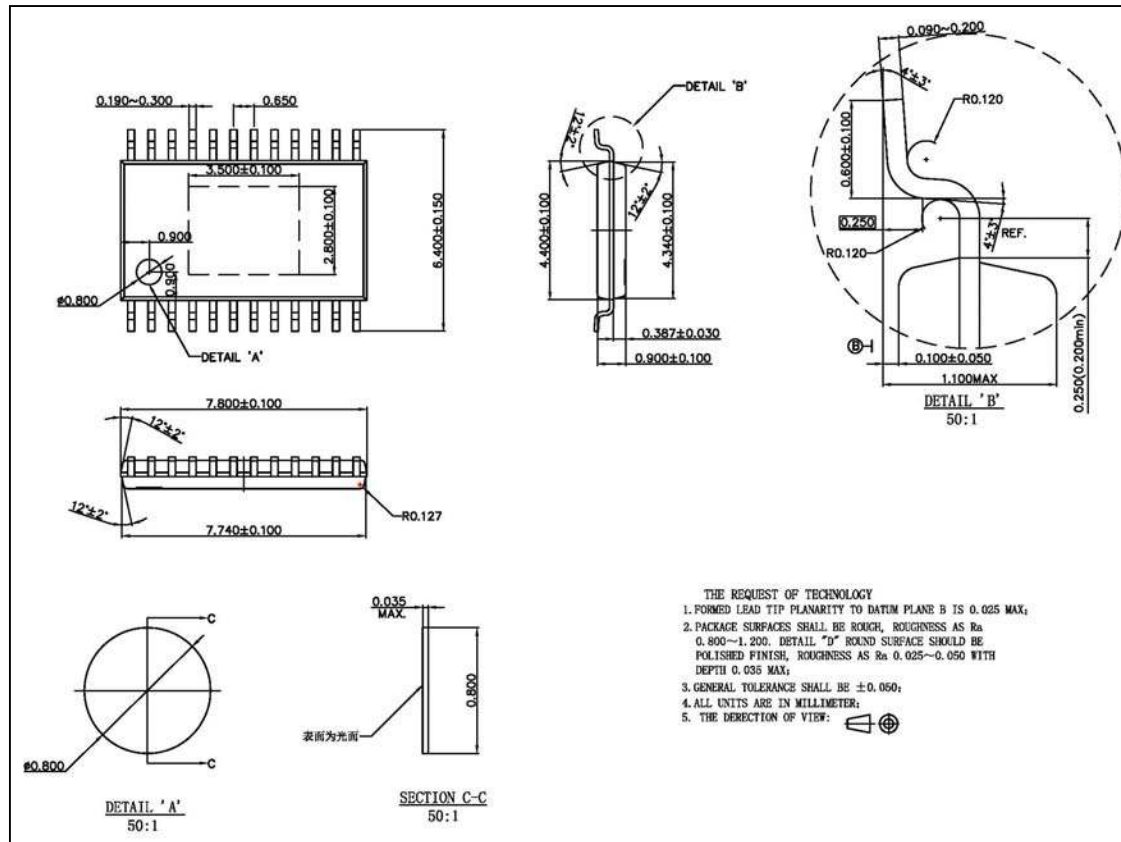
### QFN-24



**Note:** All dimensions in millimeters unless otherwise stated.

# IS31FL3726

TSSOP-24



**Note:** All dimensions in millimeters unless otherwise stated.