TFT LCD Module

Product Specification

DT028BTFT-PTS1

2.8” (240RGB x 320 DOTS) TFT Module
with Projected Capacitive Touch Screen

July 5, 2019

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Revision Record

REV	CHANGES	DATE
1.1	First release	Jul 5, 2019

Table of Content

1. Scope

This data sheet is to introduce the specification of DT028BTFT-PTS1 active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC, CTP and a backlight unit. The 2.8” display area contains 240(RGB) x 320 pixels.

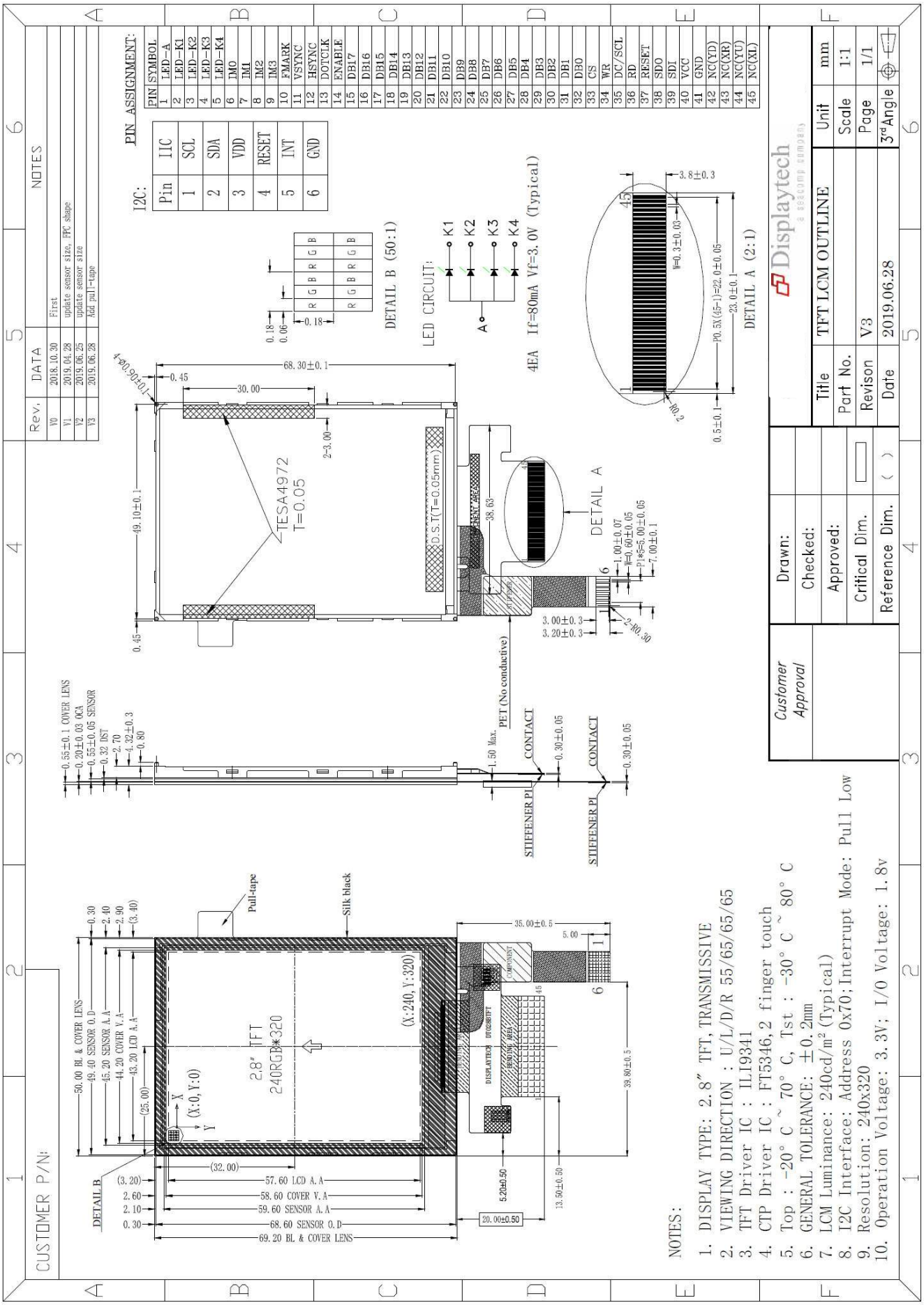
2. Application

Digital equipments which need color display, mobile navigator/video systems.

3. General Information

Item	Contents	Unit
Size	2.8	inch
Resolution	240(RGB)*320	/
Interface	RGB/MCU	/
Technology type	a-Si TFT	/
Pixel Configuration	R.G.B Vertical Stripe	
Outline Dimension (W x H x D)	50.0 x 69.2 x 4.32	mm
Active Area	43.2 x 57.60	mm
Display Mode	Transmissive	/
Backlight Type	LED	/
TFT Driver IC	IL19341	/
CTP Driver IC	FT5346	/
Weight	TBD	g

4. Outline Drawing



5. Interface signals

Recommended mating connector: FH12S-45S-0.5SH (or equivalent)

Pin No.	Symbol	I/O	Function
1	LED-A	P	LED back light(Anode)
2-5	LED-K1-LED-K4	P	LED back light(Cathode)
6-9	IM0-IM3	I	System interface select. Note1
10	FMARK	O	Tearing effect output pin to synchronize MPU to frame writing, activate by S/W command. Normally Low. Leave open when not in use.
11	VSYNC	I	Frame sync signal For RGB interface operation. Fix to VDD or VSS when not in use.
12	HSYNC	I	Line sync signal For RGB interface operation. Fix to VDD or VSS when not in use.
13	DOTCLK	I	Data clock For RGB interface operation. Fix to VDD or VSS when not in use.
14	ENABLE	I	Data enable pin For RGB interface operation. Fix to VDD or VSS when not in use.
15-32	DB17-DBO	I	18-bit parallel data bus for MCU system and RGB interface modes. Fix to VSS when not in use. Refer to Note1 for interface selection.
33	CS	I	Chip select signal: Active low
34	WR	I	8080-I/8080-II Parallel interface: write signal. 4-wire serial interface: Command/Parameter select. Fix to VDD when not in use.
35	DC/SCL	I	8080-I/8080-II Parallel interface: Data/Command select (DCX=1→Data select. DCX=0→Command select.) 3-wire9-bit/4-wire 8-bit serial interface: Serial clock. Fix to VDD or VSS when not in use.
36	RD	I	8080-I/8080-II Parallel interface: Read signal. Fix to VDD when not in use.
37	RESET	I	System Reset Active Low
38	SDO	O	Serial data output in serial bus system interface. Leave open when not in use.
39	SDI	I	Serial input signal IM[3] Low: Serial in/out, IM[3] High: Serial input. Fix to VDD or VSS when not in use.
40	VCC	P	Power supply
41	GND	P	Ground.
42	YD(NC)	O	Touch control pin
43	XR(NC)	O	
44	YU(NC)	O	
45	XL(NC)	O	

Note 1:

IM3	IM2	IM1	IM0	Interface	DB Pin in use	
					Register/Content	GRAM
0	0	0	0	80 MCU 8-bit bus interface Ⅰ	DB[7:0]	DB[7:0]
0	0	0	1	80 MCU 16-bit bus interface Ⅰ	DB[7:0]	DB[15:0]
0	0	1	0	80 MCU 9-bit bus interface Ⅰ	DB[7:0]	DB[8:0]
0	0	1	1	80 MCU 18-bit bus interface Ⅰ	DB[7:0]	DB[17:0]
0	1	0	1	3-line 9-bit data serial interface Ⅰ	SDA: In/Out	
0	1	1	0	4-line 8-bit data serial interface Ⅰ	SDA: In/Out	
1	0	0	0	80 MCU 16-bit bus interface Ⅱ	DB[8:1]	DB[17:10] DB[8:1]
1	0	0	1	80 MCU 8-bit bus interface Ⅱ	DB[17:10]	DB[17:10]
1	0	1	0	80 MCU 18-bit bus interface Ⅱ	DB[8:1]	DB[17:0]
1	0	1	1	80 MCU 9-bit bus interface Ⅱ	DB[17:10]	DB[17:9]
1	1	0	1	3-line 9-bit data serial interface Ⅱ	SDI: In, SDO: Out	
1	1	1	0	4-line 8-bit data serial interface Ⅱ	SDI: In, SDO: Out	

Must select Serial MCU(system) interface to use RGB data interface.

TP Interface Signal:

Pin No.	Symbol	Function
1	SCL	I^2C clock signal
2	SDA	I^2C data signal
3	VDD	Power supply for TP
4	RESET	Reset pin
5	INT	Interrupt output pin
6	GND	Power ground

Recommended mating connector: FH12-6S-1SH(55) (or equivalent)

6. Absolute maximum Ratings

6.1 Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	VCC	-0.3	4.6	V	
Logic Supply Voltage	VDD	-0.3	4.6	V	

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	70	℃	
Storage Temperature	TSTG	-30	80	℃	

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply	VCC	2.5	2.8	3.3	V	
Input Signal Voltage	VIL	0	--	0.3*VCC	V	
	VIH	0.7*VCC	--	VCC	V	
Output Signal Voltage	VOL	0	--	0.2*VCC	V	
	VOH	0.8*VCC	--	VCC	V	

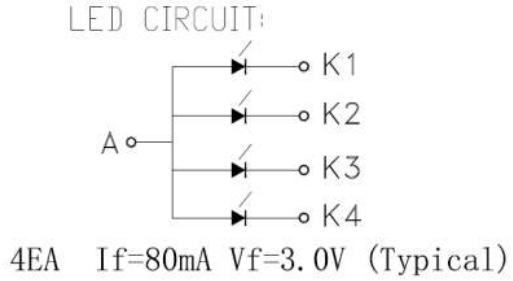
7.2 LED Backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	-	80	-	mA	
Forward Voltage	VF	-	3.0	-	V	
LED life time	--	-	30000	-	Hr	Note

Notes：

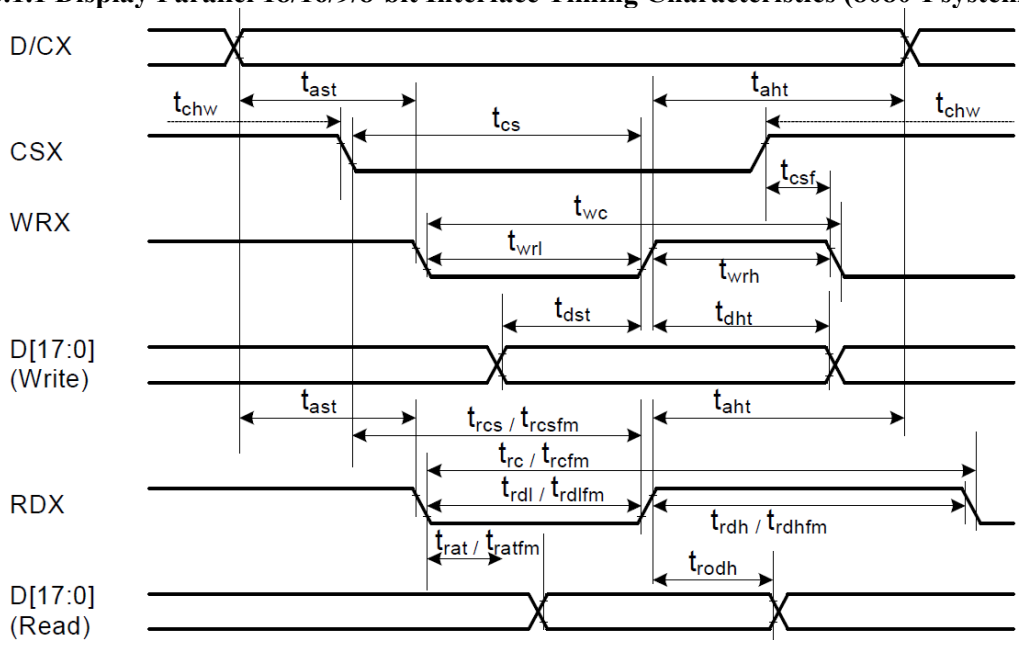
1: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL =80mA. The LED lifetime could be decreased if operating IL is larger than 80mA.



8. Command/AC Timing

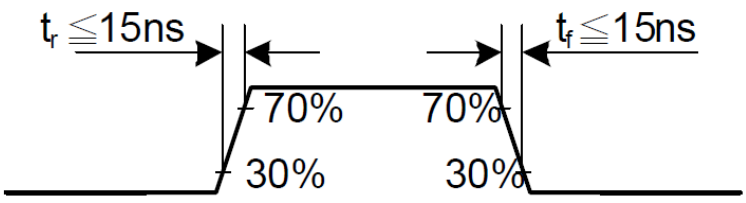
8.1 AC Characteristics

8.1.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-I system)

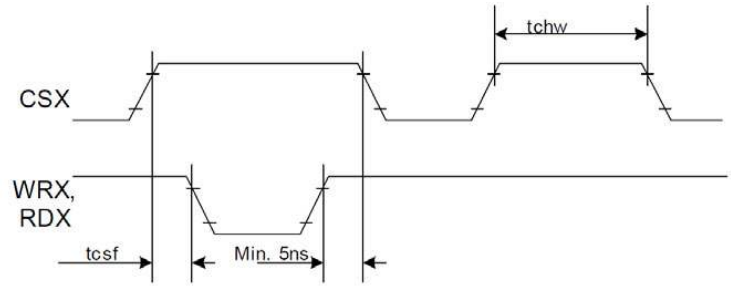


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ° C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

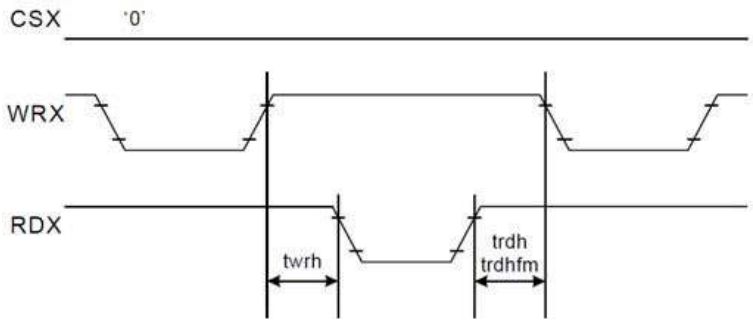


CSX timings :



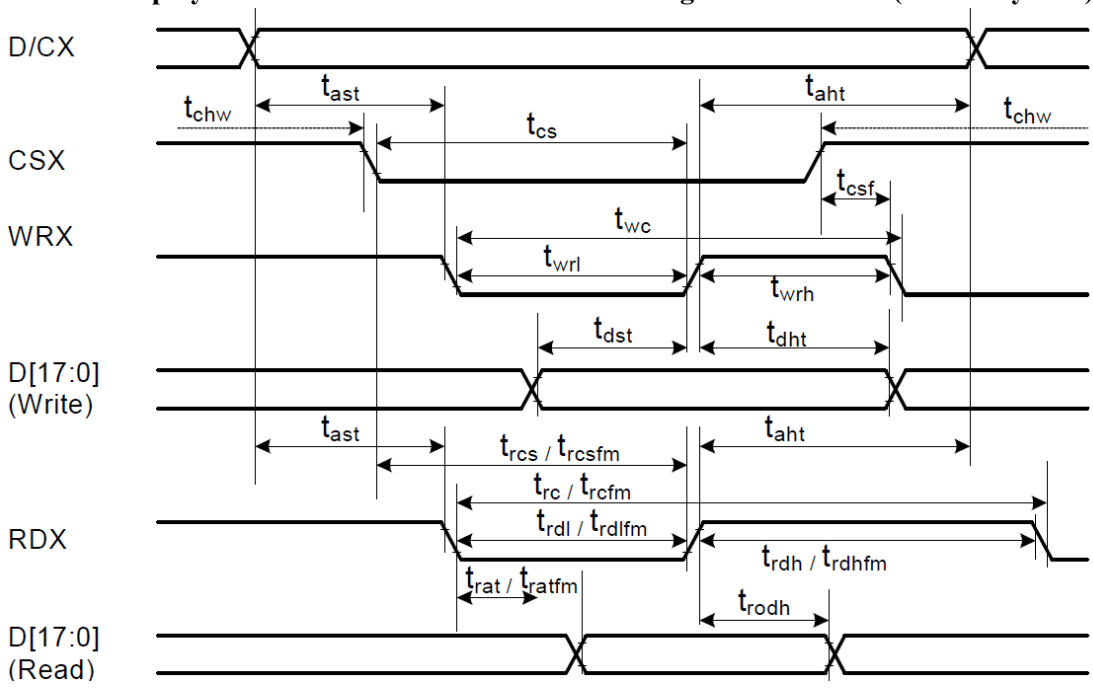
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



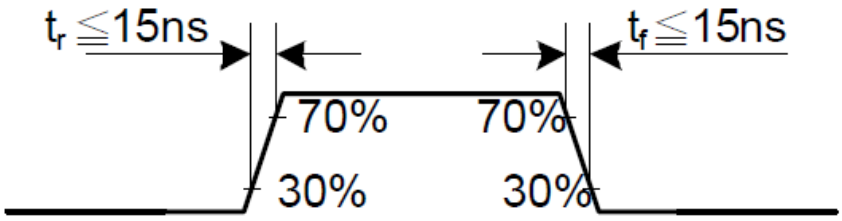
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.1.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)

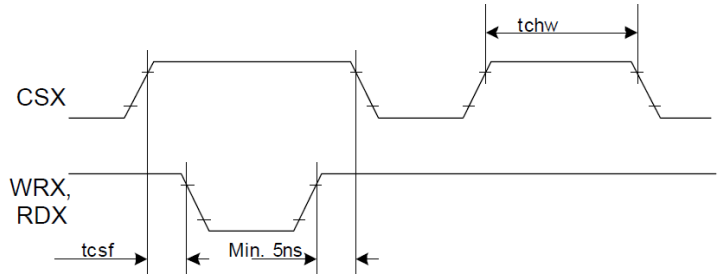


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

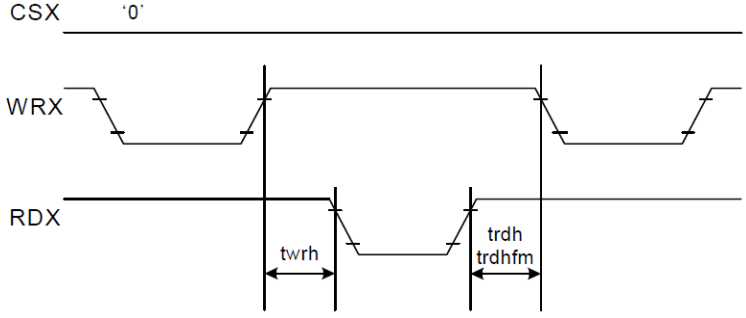


CSX timings :



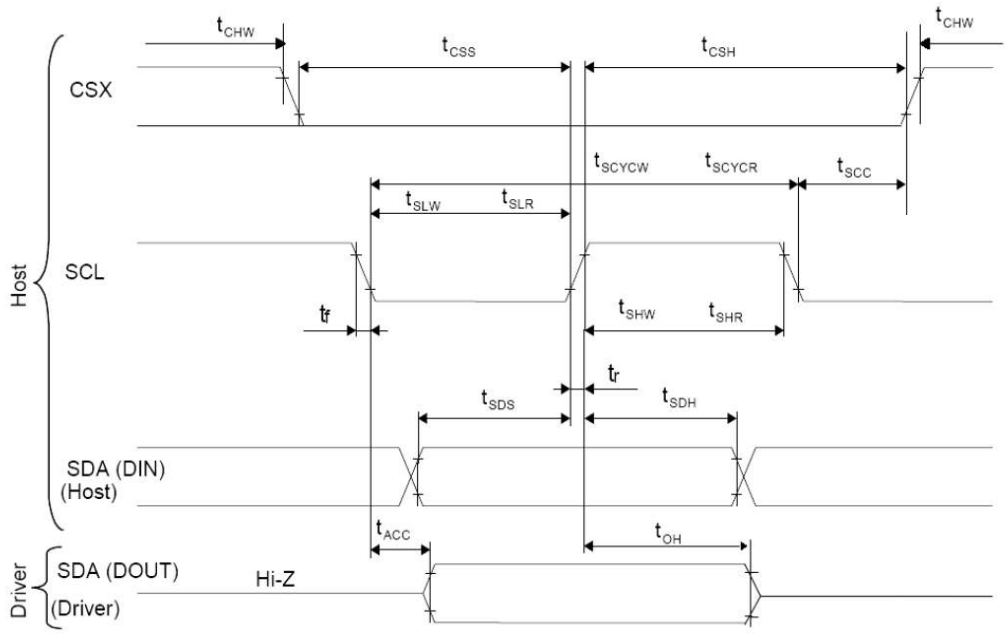
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



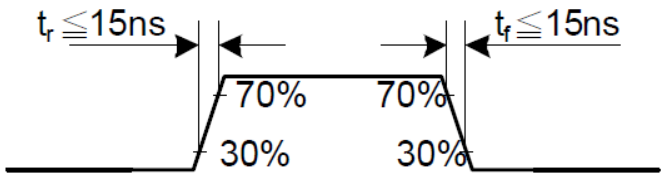
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.1.3 Display Serial Interface Timing Characteristics (3-line SPI system)

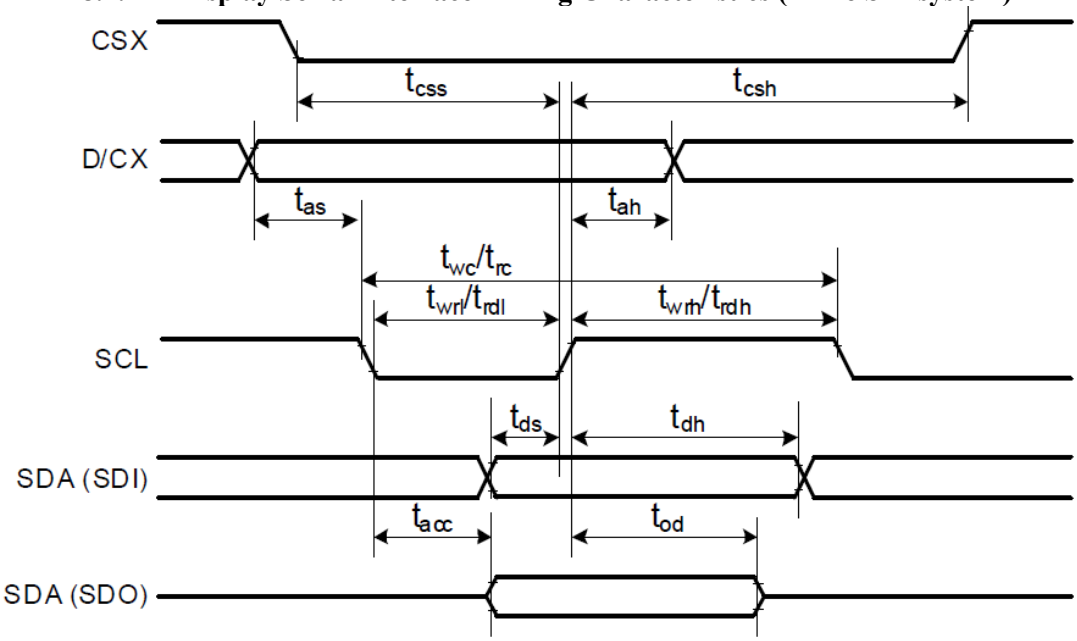


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width (Write)	40	-	ns	
	tslw	SCL “L” Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

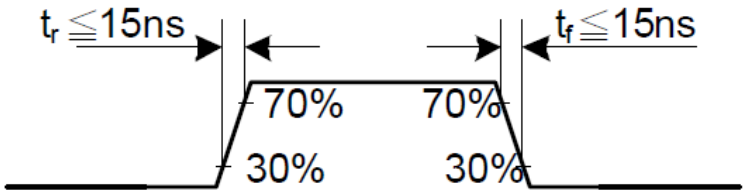


8.1.4 Display Serial Interface Timing Characteristics (4-line SPI system)

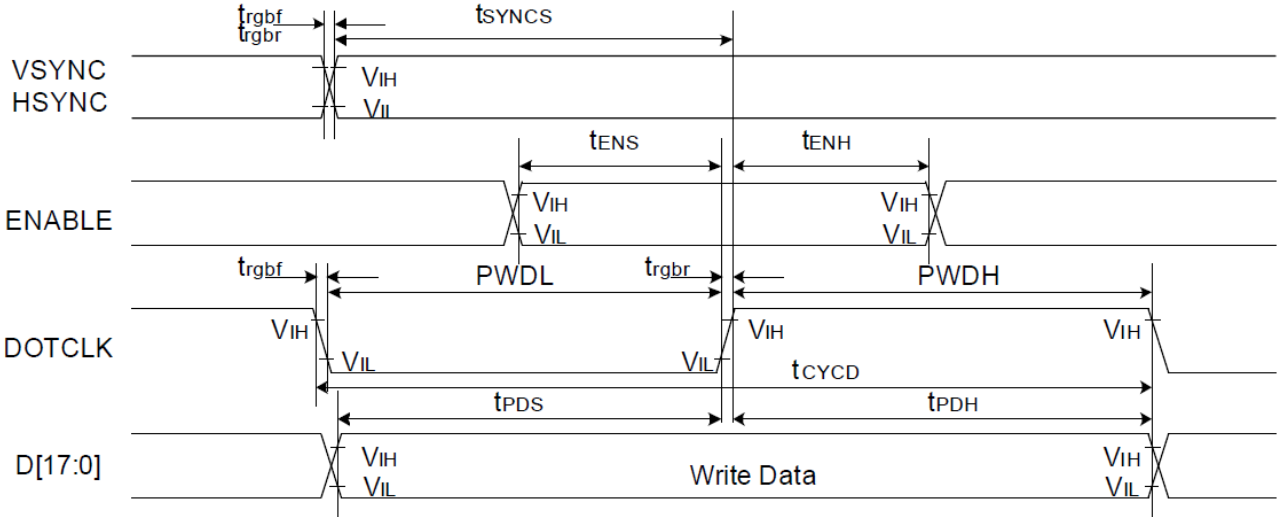


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

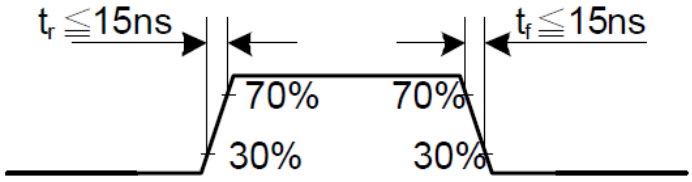


8.1.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics

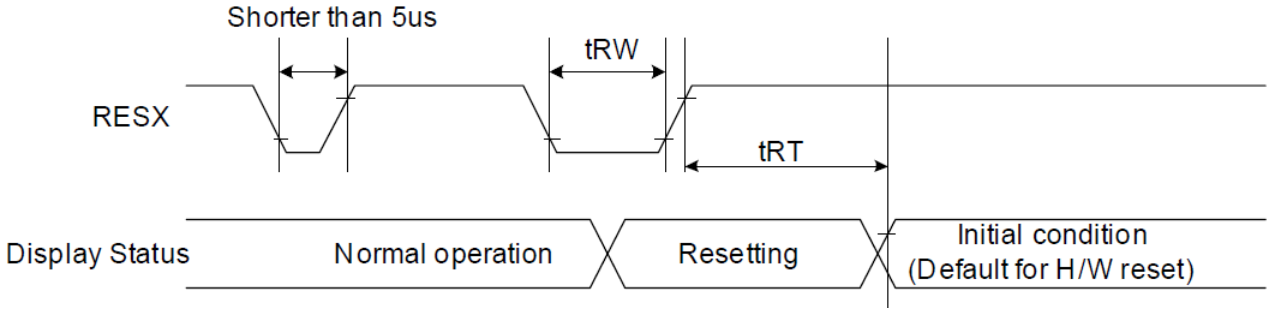


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



8.2 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

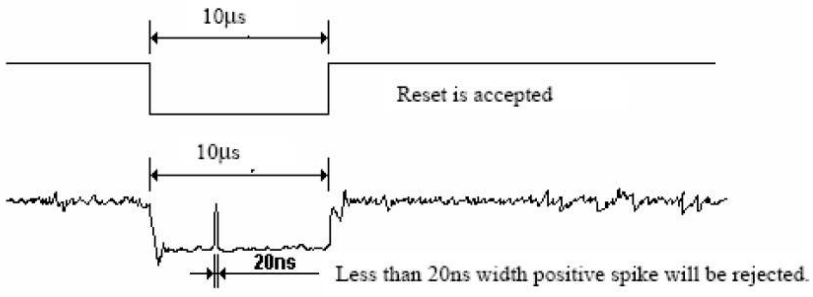
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

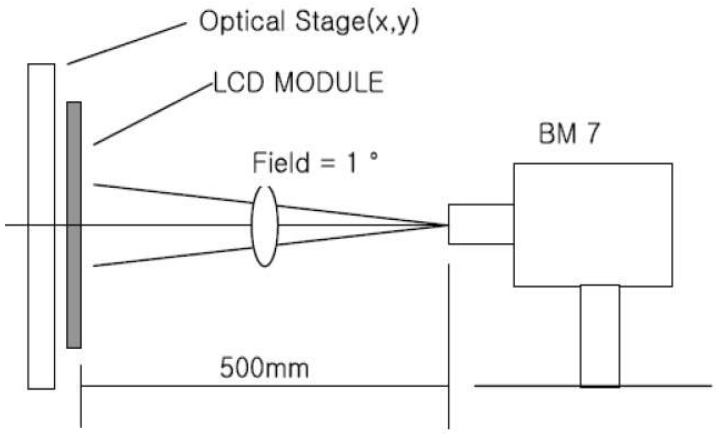
9. Optical Specification

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	Θ=0^0	300	500	-		Note1 Note2
Response Time		Tr	25℃	-	10	-	ms	Note1
		Tf			10	-	ms	Note3
View Angles		ΘT	CR≧10	-	55	-	Degree	Note4
		ΘB		-	65	-		
		ΘL		-	65	-		
		ΘR		-	65	-		
Chromaticity	White	X	Brightness is on		0.28	-	C	Note5 Note1
		Y			0.33	-		
	Red	X			0.51	-		
		Y			0.34	-		
	Green	X			0.31	-		
		Y			0.56	-		
	Blue	X			0.15	-		
		Y			0.14	-		
NTSC		S		50	60	-	%	Note5
Luminance		L			210	--	cd/m2	Note1 Note6
Uniformity		U		-	80	--	%	Note1 Note7

Note 1: Definition of optical measurement system.

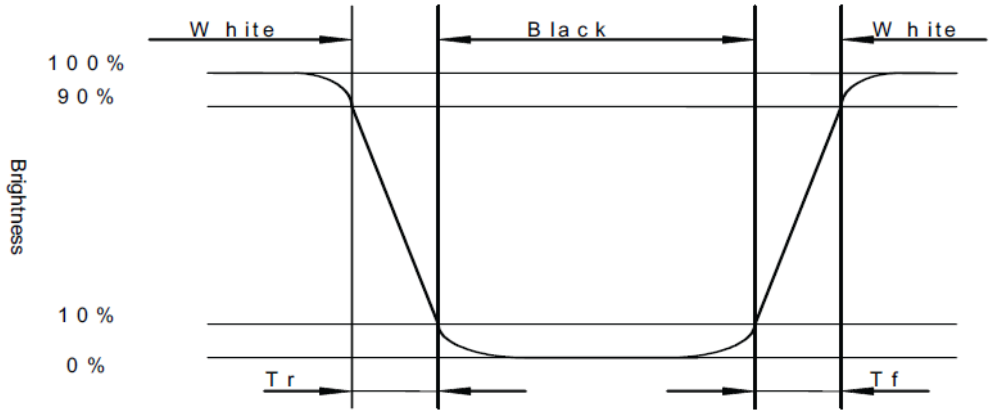
Temperature = 25℃(±3℃); LED back-light: ON, Environment brightness < 150 lx



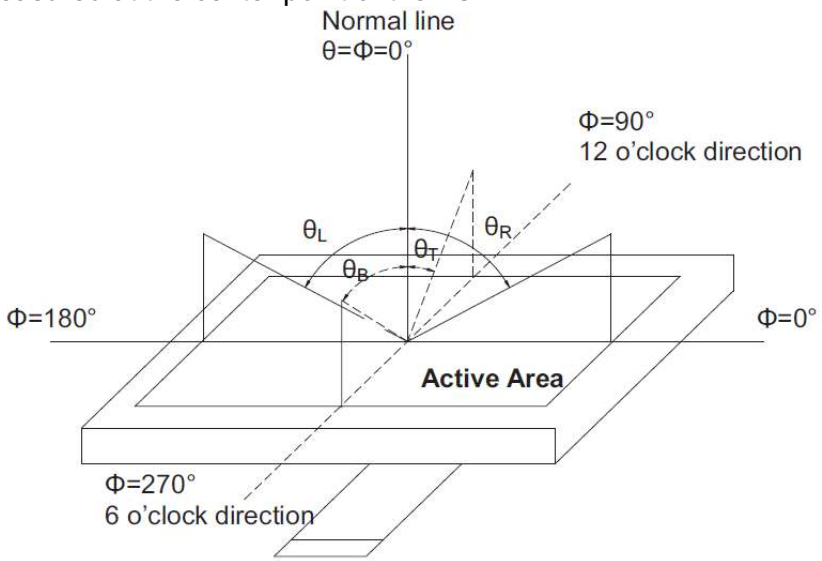
Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

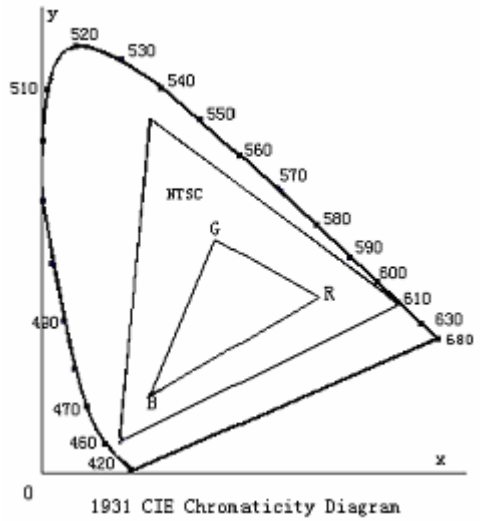
Note 3: Response time is defined as follow:
Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



Note 4: Viewing angle range is defined as follow:
Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)
Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:
Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

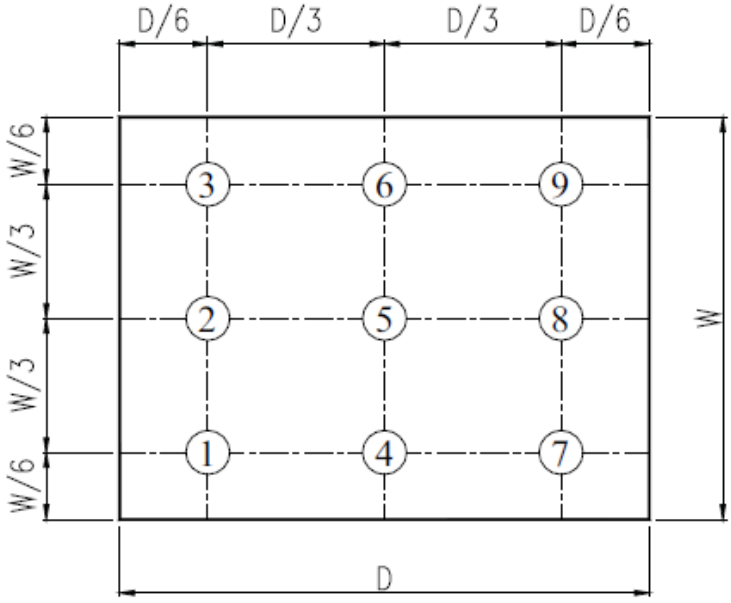


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ts=+80℃, 120hrs	Per table in below
4	Low Temp Storage	Ts=-30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ts=+60℃, 90% RH ,120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30℃ 30 min~+80℃ 30 min, Change time:5min, 5 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω , 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	10Hz~150Hz, 100m/s2,120min	Per table in below
9	Shock (Non-operation)	Half-sine wave,300m/s2,11ms	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or
clothes, wash it off immediately using soap and water.

11.2 Handling

A. The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the LCD module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4 Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not

allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.

B. In order to make the display assembly stable and firm, Displaytech recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.

C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.