AAT2822/2823/2824/2825

TFT-LCD DC/DC Converter with WLED Driver and VCOM Buffer

General Description

The AAT2822-AAT2825 family of integrated panel power solutions provides the regulated voltages required by an active-matrix thin-film transistor (TFT) liquid-crystal display (LCD). The AAT2822 includes a triple-output DC-DC converter, a LED backlight driver, and a VCOM buffer in a 4 mm x 4mm TQFN package. The primary 1.3MHz DC-DC boost converter uses an ultra-small inductor and ceramic capacitor to generate output voltage (V_{AVDD}) of up to 14.5V for the charge pumps. The low on-resistance of the integrated power MOSFET allows for efficiency up to 93%.

The two charge pumps independently regulate a positive output (VGH) and a negative output (VGL). These low-power outputs use external diode and capacitor stages to regulate output voltages up to +30V and down to -30V. A proprietary regulation algorithm minimizes output ripple when using small capacitors.

The high efficiency backlight driver provides a constant current output capable of boosting up to 28V. The driver is an ideal power solution for backlight applications with up to seven white LEDs in series or up to 39 white LEDs in a parallel and series configuration. LED brightness is PWM controlled up to 1kHz. Filtered PWM is supported for higher frequencies.

The high slew rate operational amplifier is suitable for VCOM buffering and gain adjustment.

The sequencing of the power supplies ensures proper panel startup and avoid damage to the device.

The AAT2822 family is available in a Pb-free, 24-pin 4 x 4mm TQFN package and operates over the -40°C to +85°C temperature range.

Features

LCD Bias Power
- 2.5V to 5.5V Input Supply Range
- 1.3MHz Fixed Frequency Current-Mode Step-Up Regulator
- Fast Transient Response
- Adjustable Voltage up to 14.5V
  - ±1% Typical Accuracy
- Small External Inductor and Capacitors
- Integrated Soft Start and Sequencing of All Rails
- Short-Circuit, Over-Voltage, and Over-Temperature Protection

Positive Output, VGH
- Up to 13.2V Input Supply (V_{DD})
- Adjustable Voltage up to 30V @ 20mA
  - ±3% Typical Accuracy

Negative Output, VGL
- Up to 13.2V Input Supply (V_{DD})
- Adjustable Voltage down to -30V @ 20mA
  - ± 3% Typical Accuracy

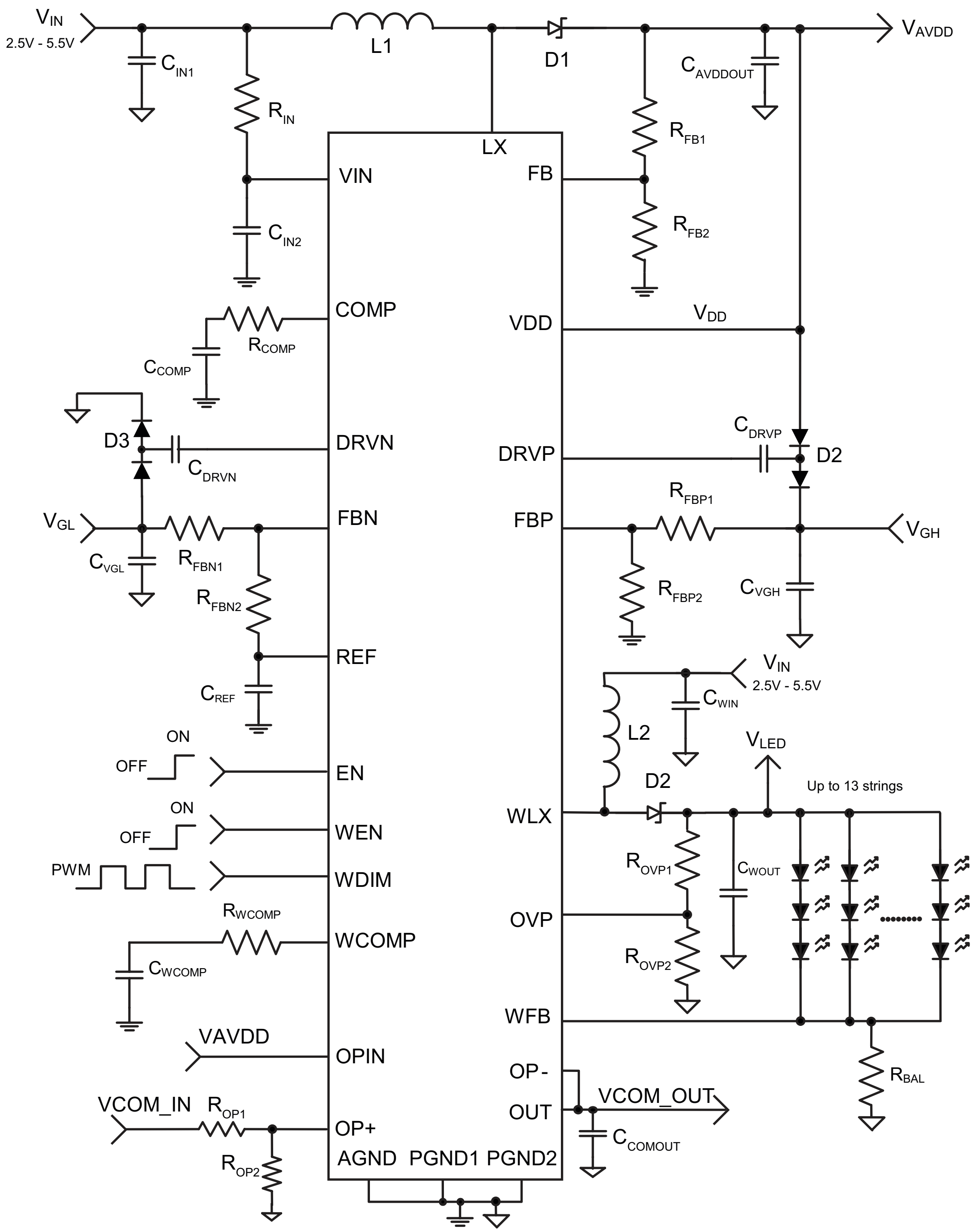
WLED Driver
- Input Voltage Range: 2.5V to 25V
- Maximum Continuous Output:
  - 12V @ 260mA
  - 28V @ 50mA
- Panel sizes from 5" – 10"
  - 5.0" 3S5P
  - 5.6" 3S6P
  - 7.0" 3S9P
  - 8.0" 3S10P/11P
  - 10" 3S13P
- Constant LED Current with 6% Accuracy
- PWM Dimming Control
  - Up to 1kHz
- 1.3MHz Switching Fixed Frequency
  - Up to 90% Efficiency

VCOM Buffer
- High-Performance
  - 13V/µs Slew Rate
  - 12MHz, -3dB Bandwidth
- ±75mA Output Short-Circuit Current
- Low 1.5mA Quiescent Current

Applications

- Automotive Displays
- Digital Photo Frames
- Netbooks
- PNDs

Typical Application



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Pin Descriptions

Pinout is preliminary and subject to change during development.

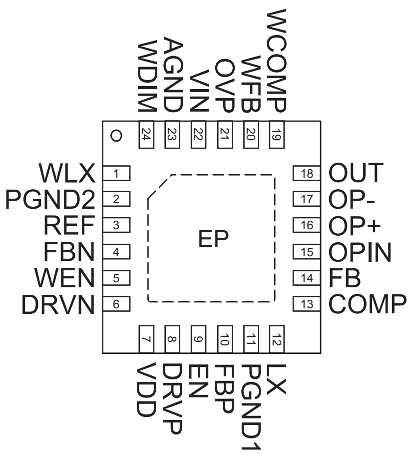
Pin Number				Symbol	Function	Description
AAT2822	AAT2823	AAT2824[1]	AAT2825[1]			
1	1	n/a	n/a	WLX	O	Boost inductor node. Connect an inductor between IN and WLX. WLX is high impedance in shutdown.
2	2	2	2	PGND2	I/O	Power ground. Connect to GND underneath the IC.
3	3	3	3	REF	O	Internal reference bypass terminal. Connect a 0.1µF capacitor from this terminal to analog ground (GND). External load capability to 50µA.
4	4	4	4	FBN	I	Negative charge-pump regulator feedback input. Regulates to 0V nominal.
5	5	n/a	n/a	WEN	I	Active high logic level enable for WLED Driver.
6	6	6	6	DRVN	O	Negative charge-pump driver output. Output high level is VDD, and low level is PGND.
7	7	7	7	VDD	PI	Positive and negative charge-pump driver supply voltage. Bypass to PGND with a 0.1µF capacitor.
8	8	8	8	DRVP	O	Positive charge-pump driver output. Output high level is VINP, and low level is PGND.
9	9	9	9	EN	I	Active high logic level enable input. Connect EN to IN for normal operation.
10	10	10	10	FBP	I	Positive charge-pump regulator feedback input. Regulates to 0.6V nominal. Connect feedback resistive divider to analog ground (GND).
11	11	11	11	PGND1	I/O	Power ground. Connect to GND underneath the IC.
12	12	12	12	LX	O	Main boost regulator power MOSFET N-channel drain. Connect output diode and output capacitor as close to PGND as possible.
13	13	13	13	COMP	I	Step-up regulator error-amplifier compensation point. Connect a series RC from COMP to AGND.
14	14	14	14	FB	O	Main boost regulator feedback input. Regulates to 0.6V nominal. Connect feedback resistive divider to analog ground (GND) to set output voltage.
15	n/a	15	n/a	OPIN	I	Operational-amplifier power input. Power supply rail for the operational amplifiers. Typically connected to VAVDD. Bypass OPIN to GND with a 0.1µF capacitor.
16	n/a	16	n/a	OP+	I	Operational-amplifier non-inverting input.
17	n/a	17	n/a	OP-	I	Operational-amplifier inverting input.
18	n/a	18	n/a	OUT	O	Operational-amplifier output.
19	19	n/a	n/a	WCOMP	I	White LED driver error-amplifier compensation point. Connect a series RC from WCOMP to AGND.
20	20	n/a	n/a	WFB	O	Feedback pin. Connect a resistor to ground to set the maximum LED current.
21	21	n/a	n/a	OVP	O	Feedback pin for over-voltage protection sense. Connect a resistive divider between the boost converter output and ground.
22	22	22	22	VIN	I	Supply input. +2.5V to +5.5V input range. Bypass with a 0.1µF capacitor between IN and GND, as close to the pins as possible.
23	23	AGND	AGND	AGND	I/O	Analog ground. Connect to power ground (PGND) underneath the IC.
24	24	n/a	n/a	WDIM	I	Dimming control input. Apply a PWM signal up to 1kHz to adjust the WLED brightness from 100% to 5%, proportional to the duty cycle of the PWM signal.
n/a	15, 16, 17, 18	1, 19, 20, 21	1, 15, 16, 17, 18, 19, 20, 21	N/C		Not connected.
EP	EP	5, 24, EP	5, 24, EP	GND		Ground. EP = Exposed paddle, connect to PCB ground plane.

1. Future products. Please contact factory for availability.

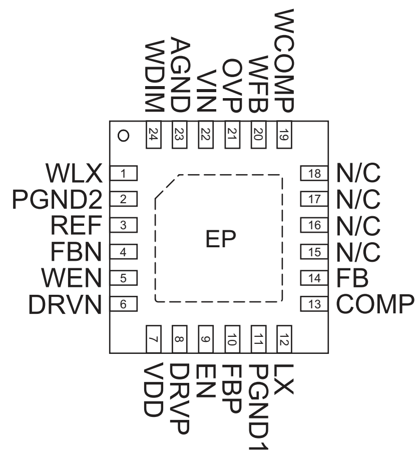
Pin Configurations

TQFN44-24
(Top View)

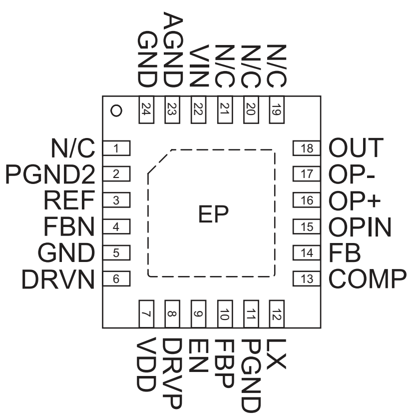
AAT2822



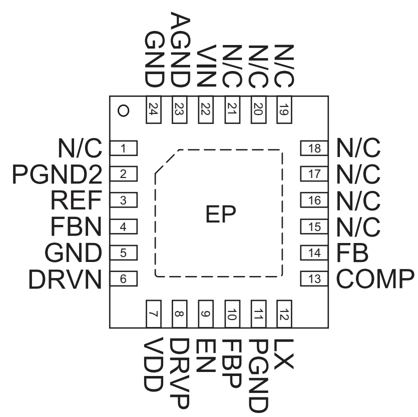
AAT2823



AAT2824



AAT2825



TFT-LCD DC/DC Converter with WLED Driver and VCOM Buffer

Part Number Descriptions

Part Number	LCD Bias	Startup Sequence	Backlight	VCOM Buffer
AAT2822	✓	VAVDD->VGH->VGL	✓	✓
AAT2822-1	✓	VAVDD->VGL->VGH	✓	✓
AAT2823	✓	VAVDD->VGH->VGL	✓	
AAT2823-1	✓	VAVDD->VGL->VGH	✓	
AAT2824	✓	VAVDD->VGH->VGL		✓
AAT2824-1	✓	VAVDD->VGL->VGH		✓
AAT2825	✓	VAVDD->VGH->VGL		
AAT2825-1	✓	VAVDD->VGL->VGH		

Absolute Maximum Ratings[1]

Description	Value	Units
V_{IN}, EN	-0.3 to 7	V
V_{DD}, OPIN, OUT, OP+, OP-	-0.3 to 15	
LX, WLX	-0.3 to 30	
WCOMP, COMP, FB, FBP, FBN, REF, WEN, PWM, WFB, OVP	-0.3 to V_{IN} + 0.3	
DRVP	-0.3 to (V_{DD} + 0.3)	
DRVN	-0.3 to (V_{DD} + 0.3)	

Thermal Information[2]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance[3]	50	°C/W
P_D	Maximum Power Dissipation	2	W
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.
3. Derate 20mW/°C above 25°C.

Electrical Characteristics

V_{IN} = 5V, EN = WEN = WDIM = V_{IN}, V_{AVDD} = V_{DD} = 12V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{IN}	Input Voltage Range		2.5		5.5	V
V_{UVLO}	Under-Voltage Lockout Threshold	Rising Edge		2.4	2.5	V
$UVLO_{HYS}$	UVLO Hysteresis			50		mV
I_{IN}	IN Quiescent Current	V_{FB} = V_{FBP} = 0.7V, V_{FBN} = -0.1, LX not switching		1.1	1.6	mA
I_{SHDN}	Shutdown Current	EN = WEN = Low, I_{SHDN} = I_{IN} + I_{DD}, V_{DD} = 5V			1	µA
V_{REF}	REF Output Voltage	No load	1.182	1.20	1.218	V
	REF Load Regulation	0 < I_{LOAD} < 50µA			10	mV
	REF Current	In regulation	50			µA
T_{SD}	Thermal Shutdown	Temperature rising		+140		°C
		Hysteresis		15		
Main Step-Up Regulator						
V_{AVDD}	Output Voltage Range		V_{IN} - V_{DIODE}		14.5	V
F_{OSC}	Operating Frequency		910	1300	1690	kHz
DC_{MAX}	Maximum Duty Cycle		86	90		%
V_{FB}	FB Regulation Voltage	No Load	0.588	0.6	0.612	V
	FB Fault Trip Level	V_{FB} falling	0.535	0.546	0.557	V
	FB Load Regulation	0 < I_{AVDD} < full load		0.01		%/mA
	FB Line Regulation	V_{IN} = 2.5V to 5.5V		0.1	±0.4	%/V
	FB Input Bias Current	V_{FB} = 0.7V	-1		+1	µA
$R_{LX(ON)}$	LX On-Resistance	I_{LX} = 200mA		350	700	mΩ
I_{LX}	LX Leakage Current	V_{LX} = 13.2V		0.01	20	µA
I_{LIM}	LX Current Limit	V_{FB} = 0.7V, duty cycle = 75%	1			A
t_{SS}	Soft-Start Period			1.3		ms
Gate High Charge Pump (VGH)						
V_{DD}	V_{DD} Input Supply Range		2.7		13.2	V
	Operating Frequency			F_{OSC}		kHz
V_{FBP}	FBP Regulation Voltage		0.588	0.6	0.612	V
	FBP Fault Trip Level	V_{FBP} Falling	470		530	mV
I_{FBP}	FBP Input Bias Current	V_{FBP} = 0.7V	-1		+1	µA
$DRVPP_{RDS}$	DRVP PCH ON-Resistance			3	6	Ω
$DRVPN_{RDS}$	DRVP NCH On-Resistance	V_{FBP} = 0.585V		1.5	3	Ω
		V_{FBP} = 0.615V	20			kΩ
Gate Low Charge Pump (VGL)						
V_{DD}	V_{DD} Input Supply Range		2.7		13.2	V
	Operating Frequency			F_{OSC}		Hz
V_{FBN}	FBN Regulation Voltage		-50	0	+50	mV
	FBN Fault Trip Level	V_{FBN} Rising	408	425	442	mV
I_{FBN}	FBN Input Bias Current	V_{FBN} = -0.1V	-1		+1	µA
$DRVNP_{RDS}$	DRVN PCH ON-Resistance			3	6	Ω
$DRVNN_{RDS}$	DRVN NCH On-Resistance	V_{FBN} = 0.035V		1.5	3	Ω
		V_{FBN} = -0.025V	20			kΩ

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Electrical Characteristics

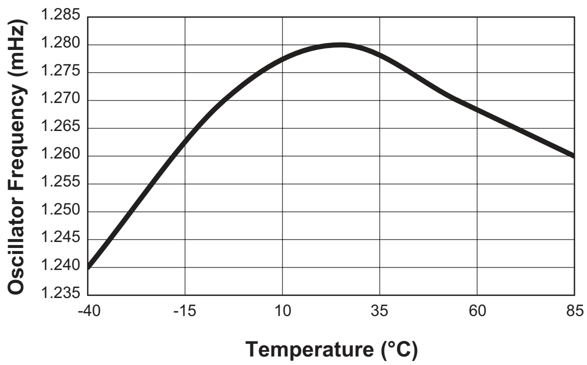
V_{IN} = 5V, EN = WEN = WDIM = V_{IN}, V_{AVDD} = V_{DD} = 12V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
WLED Driver (AAT2822, AAT2823 Only)						
V_{LED}	Output Voltage		V_{IN} - V_{DIODE}		28	V
I_{OUT}	Maximum Continuous Output Current	V_{LED} = 28V		50		mA
$\geq V_{FB}$/ $\geq V_{IN}$	Line Regulation	V_{IN} = 2.5V to 5.5V		0.7		%/V
$R_{DS(ON)}$	Low Side Switch On-Resistance			300		mΩ
V_{WFB}	WFB Pin Regulation		0.282	0.3	0.318	V
T_{SS}	Soft-Start Time	From Enable to Output Regulation; V_{FB} = 300mV		300		µs
V_{OVP}	Over-Voltage Protection Threshold	V_{LED} Rising	0.55	0.60	0.65	V
OV_{HYS}	Over-Voltage Hysteresis	V_{LED} Falling		25		mV
I_{LIMIT}	N-Channel Current Limit		1.3			A
F_{PWM}	Maximum W_{DIM} PWM Frequency				1	kHz
DC_{MIN}	Minimum Duty Cycle		5			%
VCOM Buffer (AAT2822 , AAT2824 Only)						
V_{OPIN}	Supply Range		4.5		13.2	V
I_{OPIN}	Supply Current			1.5	2.5	mA
V_{OS}	Input Offset Voltage	(V_{NEG}, V_{POS}, V_{OUT}) ≡ V_{SUP}/2			12	mV
V_{CM}	Input Common-Mode Range		0		V_{SUP}	V
V_{OH}	Output Voltage Swing, High	I_{OUT} = 5mA	V_{SUP} - 150			mV
V_{OL}	Output Voltage Swing, Low	I_{OUT} = -5mA			150	mV
I_{SC}	Short-Circuit Current	V_{SUP}/2 Source	75			mA
		Sink	75			
GBW	Gain Bandwidth Product			12		MHz
SR	Slew Rate			13		V/µs
Logic						
WDIM/ WEN_L/EN_L	Enable Input Low Voltage	V_{IN} = 2.5V			0.4	V
WDIM/ WEN_H/EN_H	Enable Input High Voltage	V_{IN} = 5.5V	1.4			V
I_{EN}	WDIM/WEN/EN Input Current				1	µA

TFT-LCD DC/DC Converter with WLED Driver and VCOM Buffer

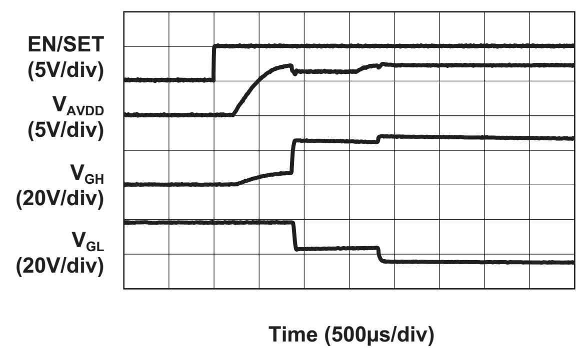
Typical Characteristics

Oscillator Frequency vs. Temperature



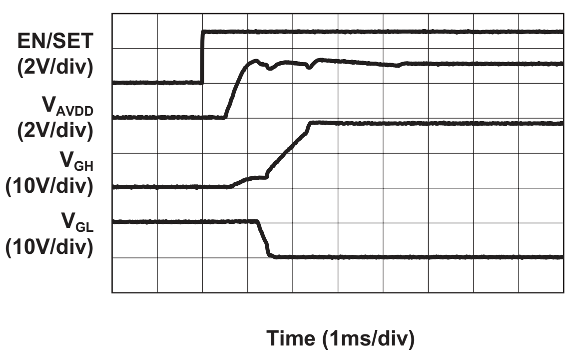
Power Up Sequencing

(VAVDD→VGH→VGL; V_{IN} = 5.0V)



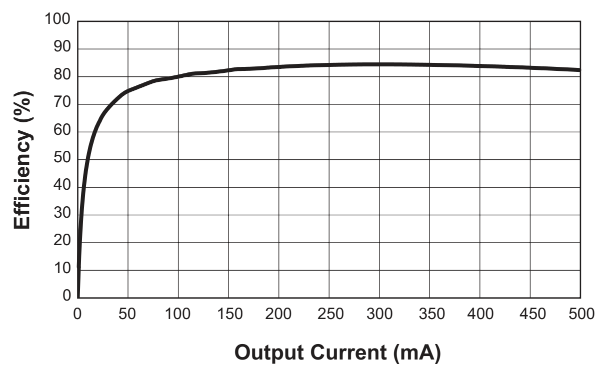
Power Up Sequencing

(VAVDD->VGL->VGH; V_{IN} = 5.0V)



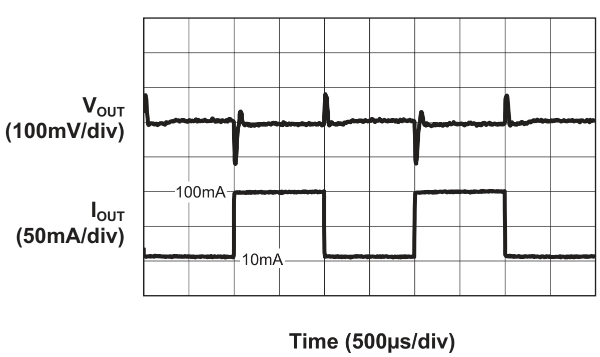
Main Boost Efficiency

(V_{OUT} = 12V)

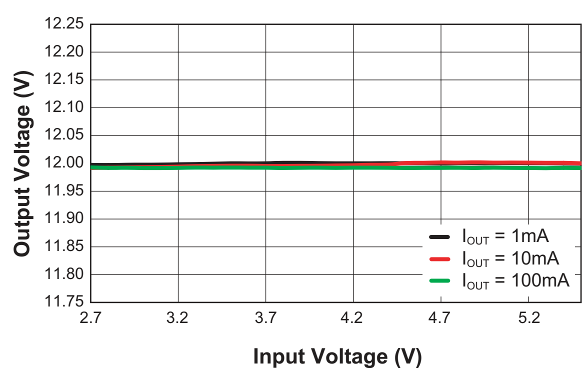


Main Boost Load Transient

(V_{IN} = 5.0V)

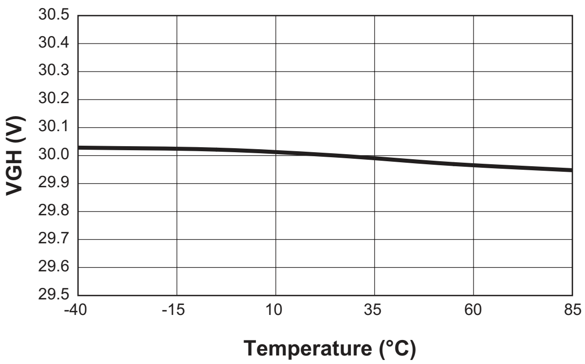


Line Regulation

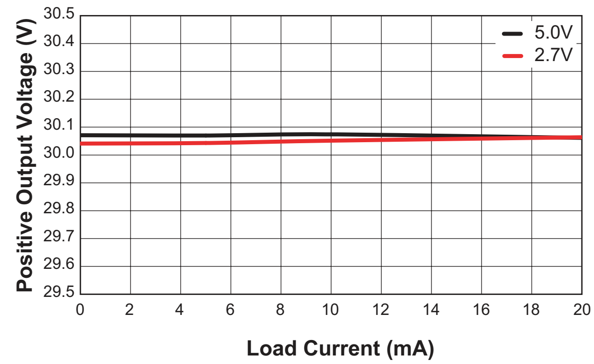


Typical Characteristics

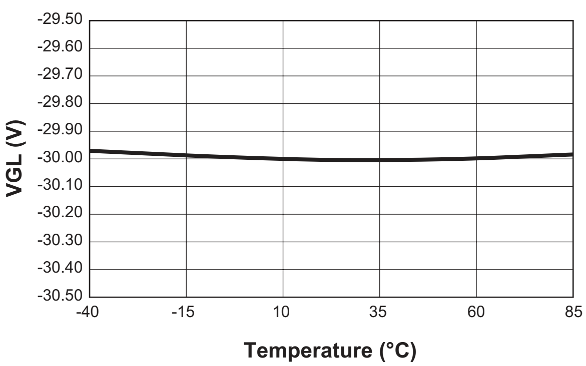
VGH vs. Temperature



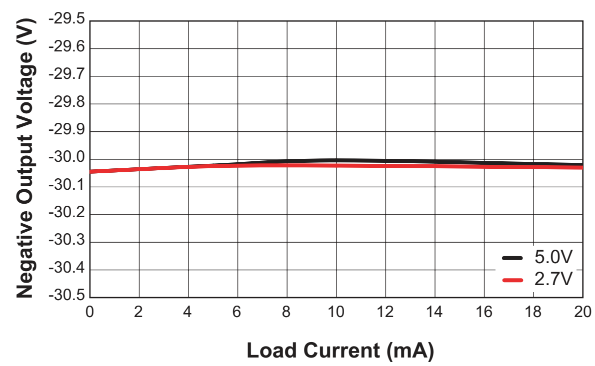
VGH Load Regulation



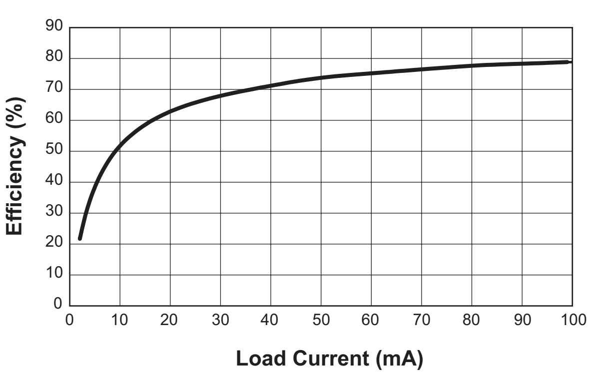
VGL vs. Temperature



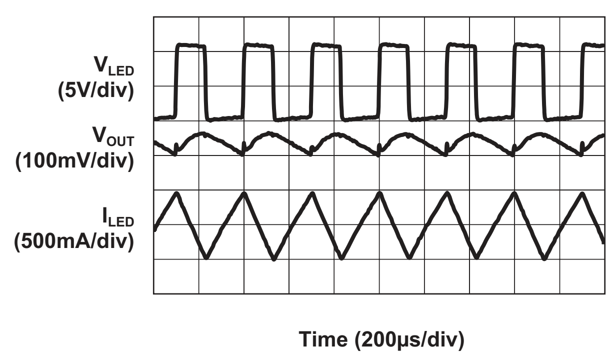
VGL Load Regulation



WLED Efficiency vs. Load Current
(7S3P; V_{IN} = 5V; V_L = 12V)

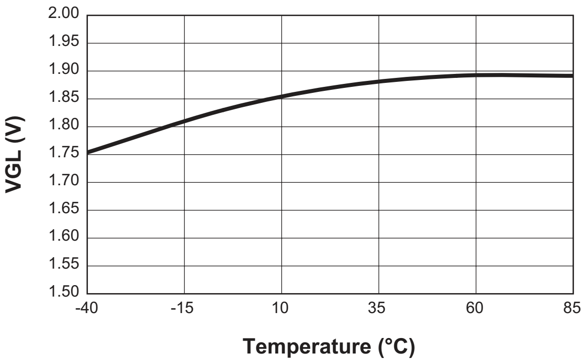


WLED Operation at 300mA Load
(V_{IN} = 5.0V, 3S13P)

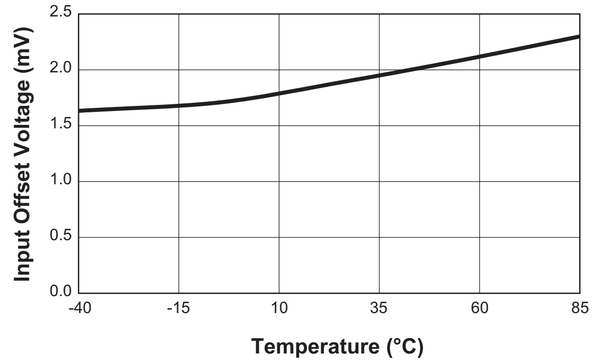


Typical Characteristics

VCOM Buffer Supply Current vs. Temperature
(V_{IN} = 5.0V, V_{OPIN} = 12V)

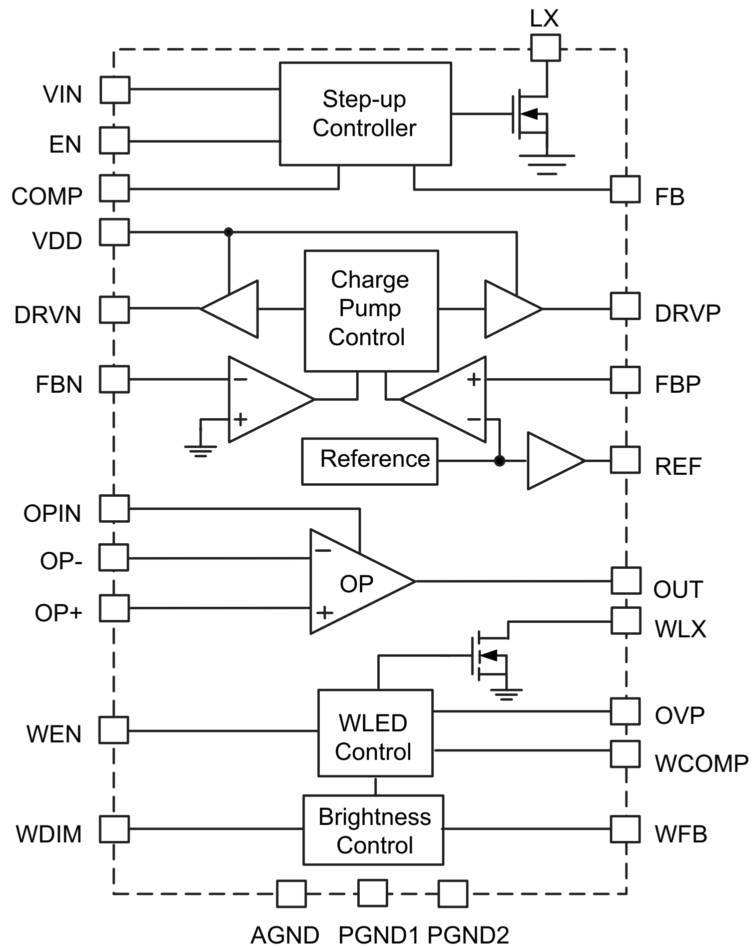


VCOM Input Offset Voltage vs. Temperature
(V_{IN} = 5.0V, V_{OPIN} = 12V)



Functional Block Diagram

AAT2822



Functional Description

Main Boost Converter

The main boost regulator contains a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT-LCD panel source drivers. The 1.3MHz switching frequency allows the use of low profile, low value inductors and ceramic capacitors to minimize the thickness of LCD panel designs.

Dual Charge-Pump Regulator

The AAT2822 provides low-power regulated output voltages from two individual charge pumps to provide the VGH and VGL supplies. Using a single stage, the VGL charge pump inverts the supply voltage (V_{DD}) and provides a regulated negative output voltage. The VGH charge pump doubles V_{DD} and provides a regulated positive output voltage. These outputs use external Schottky diodes and capacitor multiplier stages (dependent upon the required output voltage) to regulate up to ±30V. Integrated soft-start circuitry minimizes the start-up inrush current and eliminates output voltage overshoot across the full input voltage range and all load conditions. A constant switching frequency of 1.3MHz minimizes output ripple and capacitor size.

White LED Backlight Applications

The AAT2822 consists of a 1.3MHz fixed-frequency DC/DC boost controller, and an integrated high voltage MOSFET power switch. A high-voltage rectifier, power inductor, output capacitor, and sense resistors are required to implement a DC/DC constant current boost converter. Integrated soft-start circuitry minimizes the start-up inrush current and eliminates output voltage overshoot across the full input voltage range and all load conditions. The backlight current is set by an external ballast resistor up to a maximum of 260mA at 12V or 50mA at 28V output. Brightness control is via PWM dimming at up to 1kHz. Higher frequencies are achieved by filtered PWM. The AAT2822 can drive from 3 LEDs in series up to a maximum of 7 LEDs, making it suitable for screen sizes from 5” up to 10”. Depending upon the number of LEDs required, up to 9 parallel strings can be successfully driven.

If the OVP input voltage is exceeded the WLED driver continues to regulate at the OVP threshold.

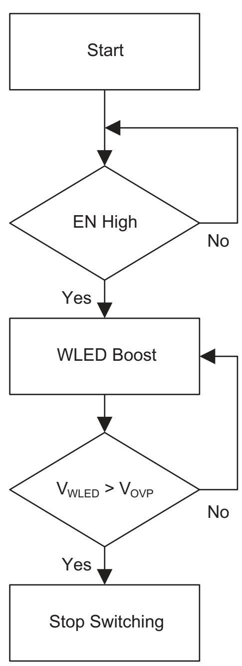


Figure 1: WLED Driver Operation.

VCOM Buffer: Operational Amplifier

The operational amplifier drives the LCD backplane VCOM. The operational amplifier features +/- 75mA(min) output short-circuit current, 13V/μs slew rate, and 12MHz bandwidth. Internal short-circuit protection limits the short circuit current while the output is directly shorted.

Power Supply Sequencing

The AAT2822 family has integrated power supply sequencing to prevent damage to the LCD screen. Two sequences are available to swap the startup of the positive and negative gate drive voltages. The startup sequence for the “-1” option establishes main boost supply (V_{AVDD}) first, followed by the gate voltages VGL then VGH. The sequence for the plain option is to establish V_{AVDD} first followed by VGH then VGL. The WLED backlight driver is independently controlled by WEN and WDIM.

Operating Faults

The AAT2822 family continuously monitors for fault conditions on the main boost converter and charge pumps according to defined fault trip levels. During operation if any fault conditions persist the controller will shut down all supplies. After removing the fault conditions, recycle the enables to start up the supplies.

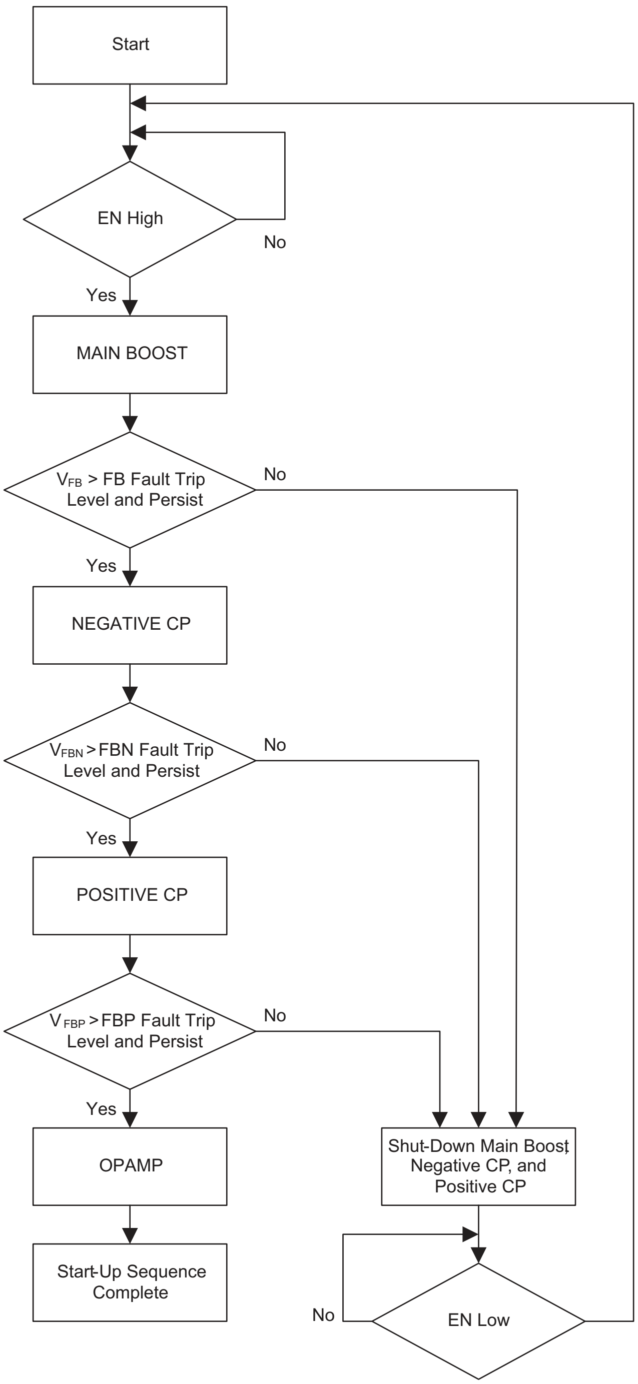


Figure 2: Startup Sequence for AAT282X-1[1].

1. For AAT282x the startup sequence is positive charge pump followed by the negative charge pump.

Application Information

Main Step-Up Converter

Output Capacitor

The high output ripple inherent in the boost converter necessitates low impedance output filtering. Multi-layer ceramic (MLC) capacitors provide small size and adequate capacitance, low parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL), and are well suited for use with the primary step-up converter. MLCs of type X7R or X5R are recommended to ensure good capacitance stability over the full operating temperature range.

The output capacitor is sized to maintain the output load without significant voltage droop during the power switch ON interval, when the output diode is not conducting. And because the VGH, VGL also have their input power from the main step-up converter output, the output capacitor may also decrease the inrush current during VGH and VGL start up. A ceramic output capacitor with a minimum value of 22µF is recommended. For inrush current sensitive applications, two 22µF are recommended. Typically, 25V rated ceramic capacitors are required for the 24V boost output. Ceramic capacitors sized as small as 0805 are available which meet these requirements. MLCs exhibit significant capacitance reduction with applied voltage. Output ripple measurements should confirm that output voltage droop is acceptable.

Input Capacitor

The boost converter input current flows during both ON and OFF switching intervals. The input ripple current is less than the output ripple and, as a result, less input capacitance is required. However, the AAT2822 input voltage is shared among other channels; a ceramic input capacitor from 4.7µF to 10µF is recommended. Minimum 6.3V rated ceramic capacitors are required at the input. Ceramic capacitors sized as small as 0603 are available which meet these requirements.

Large capacitance tantalum or solid-electrolytic capacitors may be necessary to meet stringent output ripple and transient load requirements. These can replace (or be used in parallel with) ceramic capacitors. Both tantalum and OSCON-type capacitors are suitable due to their low ESR and excellent temperature stability (although they exhibit much higher ESR than MLCs). Aluminum-electrolytic types are less suitable due to their high ESR characteristics and temperature drift. Unlike MLCs, these types are polarized and proper orientation on input and output pins is required. 30% to 70% voltage derating is recommended for tantalum capacitors.

Selecting the Schottky Diode

To ensure minimum forward voltage drop and no recovery, high voltage Schottky diodes are the best choice for the primary step-up converter. The output diode is sized to maintain acceptable efficiency and reasonable operating junction temperature under full load operating conditions. Forward voltage (V_F) and package thermal resistance (θ_{JA}) are the dominant factors to consider in selecting a diode. The diode's published current rating may not reflect actual operating conditions and should be used only as a comparative measure between similarly rated devices. 20V rated Schottky diodes are recommended for outputs less than 15V, while 30V rated Schottky diodes are recommended for outputs greater than 15V.

The average diode current is equal to the output current:

$$I_{AVG} < I_{OUT}$$

The average output current multiplied by the forward diode voltage determines the loss of the output diode.

$$P_{LOSS\_DIODE} = I_{AVG} \cdot V_F = I_{OUT} \cdot V_F$$

Diode junction temperature can be estimated:

$$T_J = T_A + \theta_{JA} \cdot P_{LOSS\_DIODE}$$

The junction temperature should be maintained below 110°C, but may vary depending on application and/or system guidelines. The diode θ_{JA} can be minimized with additional PCB area on the cathode. PCB heat sinking the anode may degrade EMI performance.

The reverse leakage current of the rectifier must be considered to maintain low quiescent (input) current and high efficiency under light load. The rectifier's reversed current increases dramatically at high temperatures.

Selecting the Main Step-Up Inductor

The primary step-up converter is designed to operate with a 2.2µH inductor for all input and output voltage combinations. The inductor saturation current rating should be greater than the NMOS current limit. If necessary, the peak inductor current can exceed the saturation level by a small amount with no significant effect on performance. The maximum duty cycle can be estimated from the relationship for a continuous mode boost converter. Maximum duty cycle (D_{MAX}) is the duty cycle at minimum input voltage ($V_{IN(MIN)}$).

$$D_{MAX} = \frac{(V_{OUT} + V_F - V_{IN(MIN)})}{V_{OUT} + V_F}$$

Where V_F is the Schottky diode forward voltage and can be estimated at 0.5V. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and peak inductor current rating, which is determined by the saturation characteristics. Measurements at full load and high ambient temperature should be completed to ensure that the inductor does not saturate or exhibit excessive temperature rise.

The output inductor (L) is selected to avoid saturation at minimum input voltage, maximum output load conditions. Peak current may be calculated from the following equation, again assuming continuous conduction mode. Worst-case peak current occurs at minimum input voltage (maximum duty cycle) and maximum load. Switching frequency (F_S) is at 1.3MHz with a 2.2µH inductor.

$$I_{PEAK} = \frac{I_{OUT}}{1 - D_{MAX}} + \frac{D_{MAX} \cdot V_{IN(MIN)}}{2 \cdot F_S \cdot L}$$

The RMS current flowing through the boost inductor is equal to the DC plus AC ripple components.

Under worst-case RMS conditions, the current waveform is critically continuous. The resulting RMS calculation yields worst-case inductor loss. The RMS value should be compared against the manufacturer's temperature rise or thermal derating guidelines.

$$I_{RMS} = \frac{I_{PEAK}}{\sqrt{3}}$$

For a given inductor type, smaller inductor size leads to an increase in DCR winding resistance and, in most cases, increased thermal impedance. Winding resistance degrades boost converter efficiency and increases the inductor operating temperature.

$$P_{LOSS\_INDUCTOR} = I_{RMS}^2 \cdot DCR$$

Setting the Output Voltage

The resistive divider network R2 and R3 of Figure 7 programs the output to regulate at a voltage higher than 0.6V as shown in Table 1. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R3 is 6.04kΩ. The resistive divider can be calculated in the following equation:

$$R_3 = R_2 \cdot \left(\frac{V_{AVDD}}{V_{FB}} - 1\right) = R_2 \cdot \left(\frac{V_{AVDD}}{0.6V} - 1\right)$$

V_{AVDD} (V)	R_3 = 6.04kΩ R_2 (kΩ)	R_3 = 59kΩ R_2 (MΩ)
9	84.5	0.825
10	93.1	0.931
11	105	1.02
12	115	1.13
13	124	1.21
15	143	1.4
20	196	1.1
22	215	2.1
24	237	2.3

Table 1: Setting the Output Voltage for the Main Step-Up Converter.

Selecting Compensation Components

The AAT2822 main boost architecture uses peak current mode control to eliminate the double pole effect of the output L&C filter and simplifies compensation loop design. The current mode control architecture simplifies the transfer function of the control loop to a one-pole, one left plane zero and one right half plane (RHP) system in frequency domain. The dominant pole can be calculated by:

$$f_P = \frac{1}{2\pi \cdot R_O \cdot C_6}$$

The ESR zero of the output capacitor can be calculated by:

$$f_{Z\_ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_6}$$

Where:

C_6 is the output filter capacitor
R_O is the load resistor value
R_{ESR} is the equivalent series resistance of the output capacitor.

The right half plane (RHP) zero can be determined by:

$$f_{Z\_RHP} = \frac{V_{IN}^2}{2\pi \cdot L_1 \cdot I_{AVDD} \cdot V_{AVDD}}$$

It is recommended to design the bandwidth to one decade lower than the frequency of RHP zero to guarantee the loop stability. A series capacitor and resistor network (R11 and C8) connected to the COMP pin sets the pole and zero which are given by:

$$f_{P\_COM} = \frac{1}{2\pi \cdot R_{EA} \cdot C_8}$$

$$f_{Z\_COM} = \frac{1}{2\pi \cdot R_{11} \cdot C_8}$$

Where:

C_8 is the compensation capacitor
R_{11} is the compensation resistor
R_{EA} is the output resistance of the error amplifier (MΩ).

A 100pF capacitor and a 200kΩ resistor in series are chosen for optimum phase margin and fast transient response.

Charge Pump

The number of charge pump stages required for a given output (V_{GH}) varies with the input voltage applied (V_{AVDD}) from the main boost. A lower input voltage requires more stages for a given output. If the numbers of stages increases, the maximum load current limitation of the charge pump would be decreased to maintain output voltage regulation.

The number of stages required can be estimated by:

$$n_P = \frac{V_{GH} - V_{AVDD(MIN)}}{V_{AVDD(MIN)} - 2V_F}$$

for the positive output and

$$n_N = \frac{V_{GL}}{2V_F - V_{AVDD(MIN)}}$$

for the negative output where V_F = 0.31V is the forward voltage of the BAT54 Schottky diode at 4mA forward current.

When solving for n_p and n_n, round up the solution to the next highest integer to determine the number of stages required.

Negative Output Voltage (V_{GL})

The negative output voltage is adjusted by a resistive divider from the output (V_{ON}) to the FBN and REF pins. The maximum reference voltage current is 200μA; therefore, the minimum allowable value for R_{10} of Figure

6 is 6.04kΩ. It is best to select the smallest value possible for R_{10}, as this will keep the value of R_9 to a minimum. With R_{10} selected, R_9 can be determined:

$$R_9 = \frac{V_{GL}}{V_{REF}} \cdot R_{10} = \frac{V_{GL}}{1.2V} \cdot R_{10}$$

Positive Output Voltage (V_{GH})

The positive output voltage is set by a resistive divider from the output (V_{GH}) to the FBP and ground pins. Limiting the value of R_7 to 6.04kΩ or lower reduces noise in the feedback circuit.

Once R_7 has been determined, solve for R_6:

$$R_6 = R_7 \cdot \left(\frac{V_{GH}}{V_{FBP}} - 1\right) = R_7 \cdot \left(\frac{V_{GH}}{0.6V} - 1\right)$$

Flying and Output Capacitors

The minimum value for the flying capacitor is limited by the output power requirement, while the maximum value is set by the bandwidth of the power supply. If C_{FLY} is too small, the output may not be able to deliver the power demanded, while too large of a capacitor may limit the bandwidth and time required to recover from load and line transients. A 0.1µF X7R or X5R ceramic capacitor is typically used. The voltage rating of the flying and reservoir output capacitors varies with the number of charge pump stages. The reservoir output capacitor value should be roughly 10 times the value of the flying capacitor. Use larger capacitors for reduced output ripple.

Input Capacitor

The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the IC. A low ESL X7R or X5R type ceramic capacitor is ideal for this function. The size required will vary depending on the load, output voltage, and input voltage characteristics. Typically, the input capacitor value should be 5 to 10 times the value of the flying capacitor. If the source impedance of the input supply is high, a larger capacitor may be required. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing radiated and conducted EMI.

Rectifier Diodes

For the rectifiers, use Schottky diodes with a voltage rating of 1.5 times the input voltage. The maximum steady-state voltage seen by the rectifier diodes for both the positive and negative charge pumps (regardless of the number of stages) is:

$$V_{REVERSE} = V_{IN} - V_F$$

The BAT54SDW quad Schottky diode in a SOT363 (2x2mm) package is a good choice for multiple-stage charge pump configuration.

White LED Driver

The white LED backlight driver can be enabled when input supply rises above under voltage lockout threshold. To reduce inrush current it is recommended that the main boost and white LED driver are not enabled concurrently.

Over-Voltage Protection (OVP) with Open Circuit Failure

The OVP protection circuit consists of a resistor network tied from the output voltage to the OVP pin (see Figure 3). To protect the device from open circuit failure, the resistor divider can be selected such that the over-voltage threshold occurs prior to the output reaching $V_{LED+(MAX)}$. The value of R_5 should be selected from 10kΩ to 20kΩ to minimize losses without degrading noise immunity.

$$R_4 = R_5 \cdot \left(\frac{V_{LED+(MAX)}}{V_{OVP}} - 1\right) = 10k\Omega \cdot \left(\frac{V_{LED+(MAX)}}{0.6V} - 1\right)$$

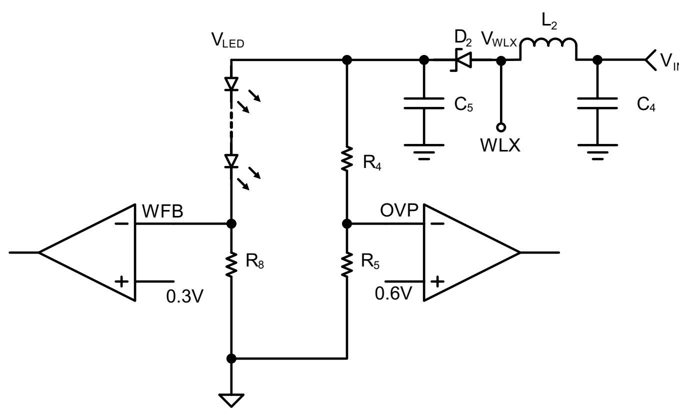


Figure 3: Over-Voltage Protection Circuit.

OVP Constant Voltage Operation

Under closed loop constant current conditions, the output voltage is determined by the operating current, LED forward voltage characteristics (V_{FLED}), quantity of series connected LEDs (N), and the feedback pin voltage (V_{FB}).

$$V_{OUT} = V_{FB} + N \cdot V_{FLED}$$

When the rising OVP threshold is exceeded, switching is stopped and the output voltage decays. Switching automatically restarts when the output drops below the lower OVP hysteresis voltage (100mV typical), and as a result the output voltage increases. The cycle repeats, maintaining an average DC output voltage proportional to the average of the rising and falling OVP levels (multiplied by the resistor divider scaling factor). High operating frequency and low output voltage ripple ensure DC current and negligible flicker in the LED string(s).

While OVP is active, the maximum LED current programming error (ΔI_{LED}) is proportional to voltage error across an individual LED (ΔV_{FLED}).

$$\Delta V_{FLED} = \frac{N \cdot V_{FLED(TYP)} - V_{OVP(MIN)} - V_{WFB}}{N}$$

To minimize the ΔI_{LED} error, the minimum OVP voltage ($V_{OVP(MIN)}$) may be increased, yielding a corresponding increase in the maximum OVP voltage ($V_{OVP(MAX)}$).

Measurements should confirm that the maximum switching node voltage ($V_{WLX(MAX)}$) is less than 30V under worst case operating conditions.

$$V_{WLX(MAX)} = V_{OVP(MAX)} \cdot \left(\frac{R_2}{R_1} + 1\right) + V_F + V_{RING}$$

V_F is the Schottky diode D_2 forward voltage at turn-OFF.

V_{RING} is the voltage ring occurring at turn-OFF.

White LED Selection and Current Setting

The WLED current is controlled by the WFB voltage and the ballast resistor (R_8). For maximum accuracy, a 1% tolerance resistor is recommended.

The ballast resistor (R_8) value can be calculated as follows:

$$R_8 = \left(\frac{V_{WFB(MAX)}}{I_{LED(MAX)}}\right)$$

Where V_{WFB} = 0.3V

For example, if the maximum current for each string of 3 series LEDs is 20mA, the maximum current for a 10 inch panel (3S13P) is 260mA (20mA x 13), which corresponds to a minimum resistor value of 1.15Ω

$$R_8 = \left(\frac{0.3V}{260mA}\right) = 1.15\Omega$$

Maximum I_{LED} Current (mA)	R_8(Ω)
30	0.768
25	0.909
20	1.15
15	1.54
10	2.32
5	4.64

Table 2: Maximum LED Current and Ballast Resistor (R_8) Values for 10" Panel Size.

Typical white LEDs are driven at maximum continuous currents of 15mA to 20mA. The maximum number of series-connected LEDs is determined by the minimum output voltage of the boost converter (V_{LED}), minus the maximum feedback voltage ($V_{WFB(MAX)}$) divided by the maximum LED forward voltage ($V_{FLED(MAX)}$) which can be estimated from the manufacturers' datasheet at the maximum LED operating current.

$$V_{LED} = V_{OVP(TYP)} \cdot \left(\frac{R_5}{R_4} + 1\right)$$

$$N = \left(\frac{V_{OVP(MIN)} - V_{WFB(MAX)}}{V_{FLED(MAX)}}\right)$$

For example, the typical forward voltage of the white LED is 3.5V at 20mA.

$$V_{LED} = V_{OVP(TYP)} \cdot \left(\frac{R_5}{R_4} + 1\right) = 0.6V \cdot \left(\frac{464k\Omega}{10k\Omega} + 1\right) = 27.8V$$

$$N = \left(\frac{V_{OVP(MIN)} - V_{WFB(MAX)}}{V_{FLED(MAX)}}\right) = \left(\frac{27.8V - 0.6V}{3.5V}\right) = 7.8 \text{ LEDs}$$

Therefore, under these typical operating conditions, 7 LEDs can be used in series for each string.

PWM Dimming Control

The dimming of the white LED can be controlled using a PWM or a filter PWM signal. By connecting a PWM signal to the WDIM pin and adjusting the duty cycle of the PWM signal, the dimming of the white LED changes proportionally to the percentage of the duty cycle as shown in Figure 4. However, the dimming control using PWM connected to the WDIM pin can operate at a frequency up to 1kHz.

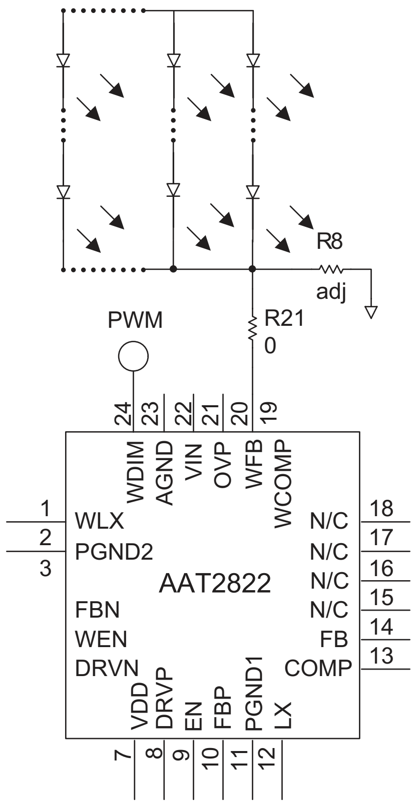


Figure 4: PWM Dimming Control.

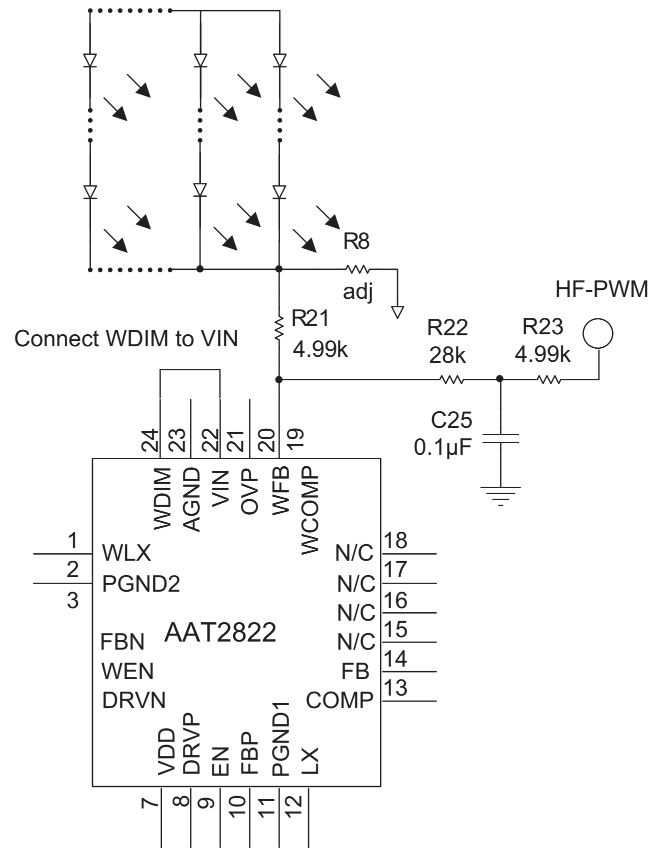


Figure 5: Low-Pass Filter PWM Dimming Control.

For applications requiring a PWM frequency higher than 1KHz, an external filter PWM is connected to the WFB pin to control the dimming of the white LED. This low-pass filter (R_{23}/C_{25}) integrates the high frequency PWM signal to produce a DC dimming control as shown in Figure 5.

When the PWM duty cycle is adjusted, the DC voltage across the ballast resistor (R_8) changes, resulting in change of the white LED current. Apply the KCL at the feedback node (WFB). The voltage across the R_8 resistor can be expressed:

$$V_{R8} = 0.3V - \frac{R_{21}}{R_{22}} \cdot (V_{C25} - 0.3V)$$

For minimum dimming, V_{R8} = 0V.

Choose R_{21} = 4.99kΩ and V_{C25} = 2V, and solve for R_{22}:

$$R_{22} = \frac{R_{21}}{(0.3V - V_{R8}) \cdot (V_{C25} - 0.3V)} = 28k\Omega$$

The low-pass filter should be chosen to produce an acceptable ripple for the DC dimming voltage and a small time constant. For application where the PWM frequency is greater than 10KHz, the optimum values for the low-pass filter are R_{23} = 4.99kΩ and C_{25} = 0.1µF.

Selecting the Schottky Diode

To ensure minimum forward voltage drop and no recovery, high-voltage Schottky diodes are considered the best choice for the WLED boost converter. The output diode is sized to maintain acceptable efficiency and reasonable operating junction temperature under full load operating conditions. Forward voltage (V_F) and package thermal resistance (θ_{JA}) are the dominant factors to consider in selecting a diode. The diode's non-repetitive peak forward surge current rating (I_{FSM}) should be considered for high pulsed load applications such as camera flash. The I_{FSM} rating drops with increasing conduction period. Manufacturers' datasheets should be consulted to verify reliability under peak load conditions. The diode's published current rating may not reflect actual operating conditions and should be used only as a comparative measure between similarly rated devices.

40V rated Schottky diodes are recommended for outputs less than 30V, while 60V rated Schottky diodes are recommended for outputs greater than 35V.

The average diode current is equal to the output current:

$$I_{AVG} = I_{OUT}$$

The average output current multiplied by the forward diode voltage determines the loss of the output diode.

$$P_{LOSS\_DIODE} = I_{AVG} \cdot V_F = I_{OUT} \cdot V_F$$

Diode junction temperature can be estimated:

$$T_J = T_A + \theta_{JA} \cdot P_{LOSS\_DIODE}$$

Output diode junction temperature should be maintained below 110°C, but may vary depending on application and/or system guidelines. The diode θ_{JA} can be minimized with additional PCB area on the cathode. PCB heat-sinking the anode may degrade EMI performance. The reverse leakage current of the rectifier must be considered to maintain low quiescent (input) current and high efficiency under light load. The rectifier's reverse current increases dramatically at elevated temperatures.

Selecting the WLED Step-Up Inductor

The WLED step-up converter has the same topology as the main step-up converter. It is designed to operate with a 2.2µH inductor for all input and output voltage combinations. The inductor saturation current rating should be greater than the NMOS current limit.

$$D_{MAX} = \frac{(V_{OUT} + V_F - V_{IN(MIN)})}{V_{OUT} + V_F}$$

The output inductor (L) is selected to avoid saturation at minimum input voltage and maximum output load conditions. Peak current may be calculated from the following equation, again assuming continuous conduction mode. Worst-case peak current occurs at minimum input voltage (maximum duty cycle) and maximum load. Switching frequency is estimated at 1.3MHz with a 2.2µH inductor.

$$I_{PEAK} = \frac{I_{OUT}}{1 - D_{MAX}} + \frac{D_{MAX} \cdot V_{IN(MIN)}}{2 \cdot F_S \cdot L}$$

Selecting the WLED Step-Up Capacitors

The high output ripple inherent in the boost converter necessitates low impedance output filtering.

Multi-layer ceramic (MLC) capacitors provide small size and adequate capacitance, low parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL), and are well suited for use with the WLED boost regulator. MLC capacitors of type X7R or X5R are recommended to ensure good capacitance stability over the full operating temperature range.

The output capacitor is sized to maintain the output load without significant voltage droop (ΔV_{OUT}) during the power switch ON interval, when the output diode is not conducting. A ceramic output capacitor with a value of 2.2µF to 4.7µF is recommended. Typically, 50V rated capacitors are required for the 28V maximum boost output. Ceramic capacitors sized as small as 0805 or 1206 are available which meet these requirements.

MLC capacitors exhibit significant capacitance reduction with applied voltage. Output ripple measurements should confirm that output voltage droop and operating stability are acceptable. Voltage derating can minimize this factor, but results may vary with package size and among specific manufacturers.

The output capacitor size can be estimated using the equation:

$$C_{OUT} = \frac{I_{OUT} \cdot D_{MAX}}{F_S \cdot \Delta V_{OUT}}$$

To maintain stable operation at full load, the output capacitor should be sized to maintain ΔV_{OUT} between 100mV and 200mV.

The WLED boost converter input current flows during both ON and OFF switching intervals. The input ripple current is lower than the output ripple and, as a result, a lower input capacitance is required.

LCD VCOM Buffer

The VCOM buffer is designed to drive the voltage on the backplane of an LCD display. The buffer must be capable of sinking and sourcing capacitive pulse current at low frequency. A 10nF ceramic output capacitor in series with a 100Ω resistor is sufficient for buffer stability at high frequencies.

The VCOM output voltage is typically set to half of the main boost output voltage V_{ADD}. The maximum input bias voltage for the VCOM buffer (V_{OPIN}) cannot exceed 13V. In applications where the main boost output voltage V_{VADD} is greater than 13V, V_{OPIN} should be connected to an external supply to prevent damage to the device; the jumper J_7 should be left open to disconnect V_{AVDD} from V_{OPIN}.

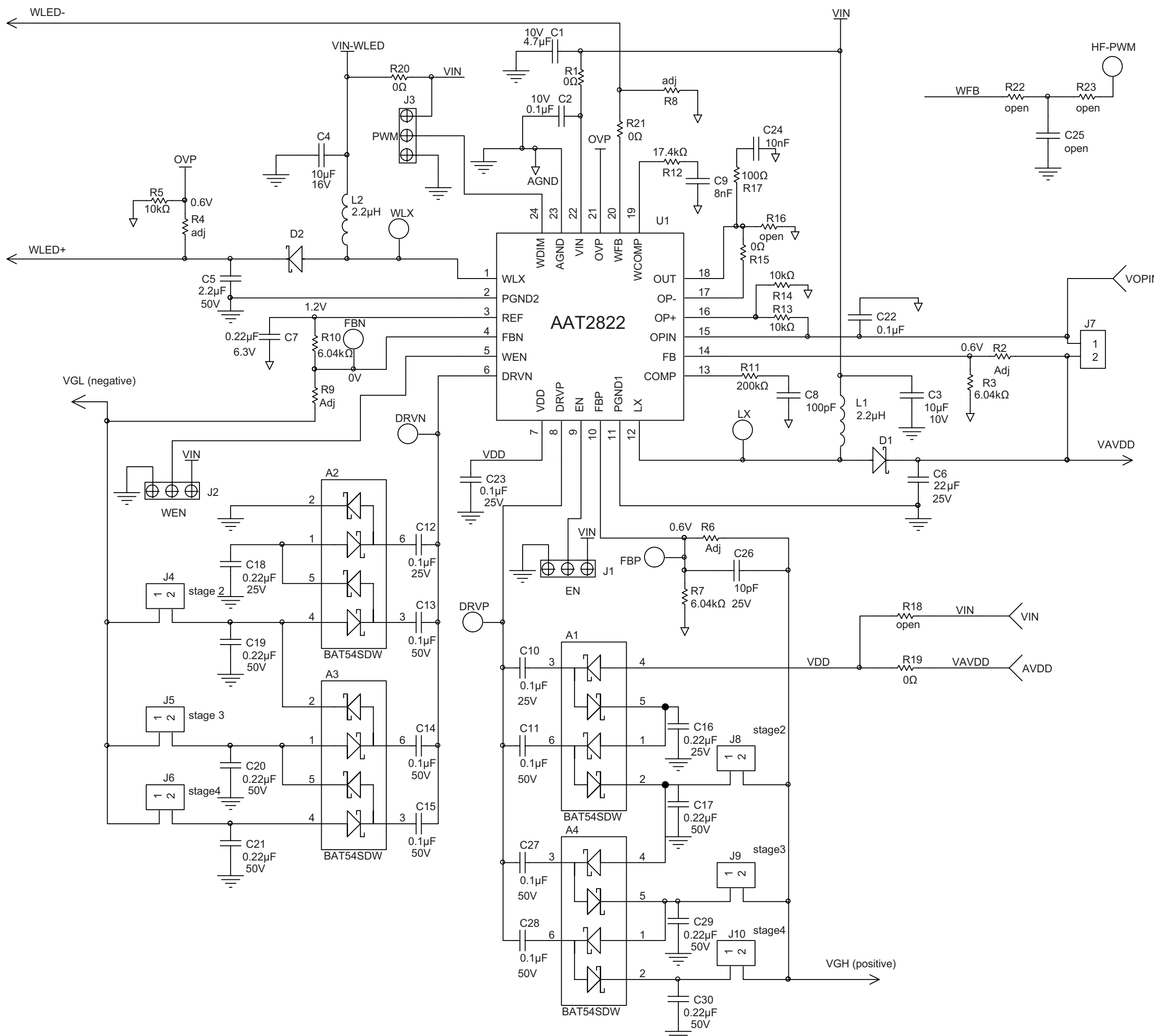


Figure 6: AAT2822IBK Evaluation Board Schematic.

Component	Part Number	Description	Manufacturer
U1	AAT2822IBK	TFT-LCD DC-DC Converter with WLED Driver and VCOM Buffer	Skyworks
C1	GRM188R61A475K	CAP CERAMIC 4.7µF 0603 X5R 10V 10%	Murata
C2	GRM188R71C104K	CAP CERAMIC 0.1µF 0603 X7R 16V 10%	
C3, C4	GRM21BR61C106K	CAP CERAMIC 10µF 0805 X5R 16V 10%	
C5	GRM31CR71H225K	CAP CERAMIC 2.2µF 1206 X7R 50V 10%	
C6	GRM31CR61C226M	CAP CERAMIC 22µF 1206 X5R 16V 20%	
C7	GRM188R71A224K	CAP CERAMIC 0.22µF 0603 X7R 10V10%	
C8	GRM1885C1H101J	CAP CERAMIC 100pF 0603 COG 50V 5%	
C9	GRM2195C1H822J	CAP CERAMIC 8nF 0805 X7R 50V 10%	
C10, C12, C22, C23	GRM188R61E104K	CAP CERAMIC 0.1µF 0603 X5R 25V 10%	
C11, C13, C14, C15, C27, C28	GRM188R71H104K	CAP CERAMIC 0.1µF 0603 X7R 50V 10%	
C16, C18	GRM188R61E224K	CAP CERAMIC 0.22µF 0603 X5R 25V10%	
C17, C19, C20, C21, C29, C30	GRM21BR71H224K	CAP CERAMIC 0.22µF 0805 X7R 50V10%	
C24	GRM188R71H103K	CAP CERAMIC 10nF 0603 X7R 50V 10%	
C25	NC		
C26	GRM1885C1H100J	CAP CERAMIC 10pF 0603 COG 50V 5%	
A1, A2, A3, A4	BAT54SDW-7-F	Schottky Diode Array 30V SC70-6	Diode Inc
D1, D2	SS16L	Schottky Diode 1A 60V Micro SMP	Taiwan Semiconductor
L1, L2	CDRH5D16-2R2	POWER INDUCTOR 2.2µH 3.0A SMD	Sumida
R2, R4, R6, R8, R9		Adjustable Value (See Equations.1 – 5 and Table 5); 0603	Yageo
R3, R7, R10	RC0603FR-0760K4L	Res 6.04kΩ 1/10W 1% 0603 SMD	
R5, R13, R14	RC0603FR-0710KL	Res 10kΩ 1/10W 1% 0603 SMD	
R11	RC0603FR-07200KL	Res 200kΩ 1/10W 1% 0603 SMD	
R12	RC0603FR-0717K4L	Res 17.4kΩ 1/10W 1% 0603 SMD	
R15, R19, R20, R21	RC0603FR-070RL	Res 0Ω 1/10W 1% 0603 SMD	
R17	RC0603FR-07100RL	Res 100Ω 1/10W 1% 0603 SMD	
R18, R22, R23, R25	NC		

Table 3: AAT2822IBK Evaluation Board Bill Of Materials (BOM).

Panel Sizes (inches)	WLED Matrix (Series and Parallel)	Ballast Resistor R_8 (Ω)
5	3S5P	2.37
5.6	3S6P	2.0
7	3S9P	1.3
8	3S10P/11P	1.2
10	3S13P	1.0
5	7S2P	4.7

Table 4: Ballast Resistor Selection for Different Panel Sizes.

Eq. 1: $$R_2 = R_3 \cdot \left(\frac{V_{AVDD}}{V_{FB}} - 1\right) = 6.04k\Omega \cdot \left(\frac{V_{AVDD}}{0.6V} - 1\right)$$

Eq. 2: $$R_9 = \frac{V_{GL}}{V_{FBN}} \cdot R_{10} = \frac{V_{GL}}{1.2V} \cdot 6.04k\Omega$$

Eq. 3: $$R_6 = R_7 \cdot \left(\frac{V_{GH}}{V_{FBP}} - 1\right) = 6.04k\Omega \cdot \left(\frac{V_{GH}}{0.6V} - 1\right)$$

$$\textbf{Eq. 4: } R_4 = R_5 \cdot \left(\frac{V_{LED+(MAX)}}{V_{OVP}} - 1\right) = 10k\Omega \cdot \left(\frac{V_{LED+(MAX)}}{0.6V} - 1\right)$$

$$\textbf{Eq. 5: } R_8 = \frac{V_{WFB(MAX)}}{I_{LED(MAX)}} = \frac{0.3V}{I_{LED(MAX)}}$$

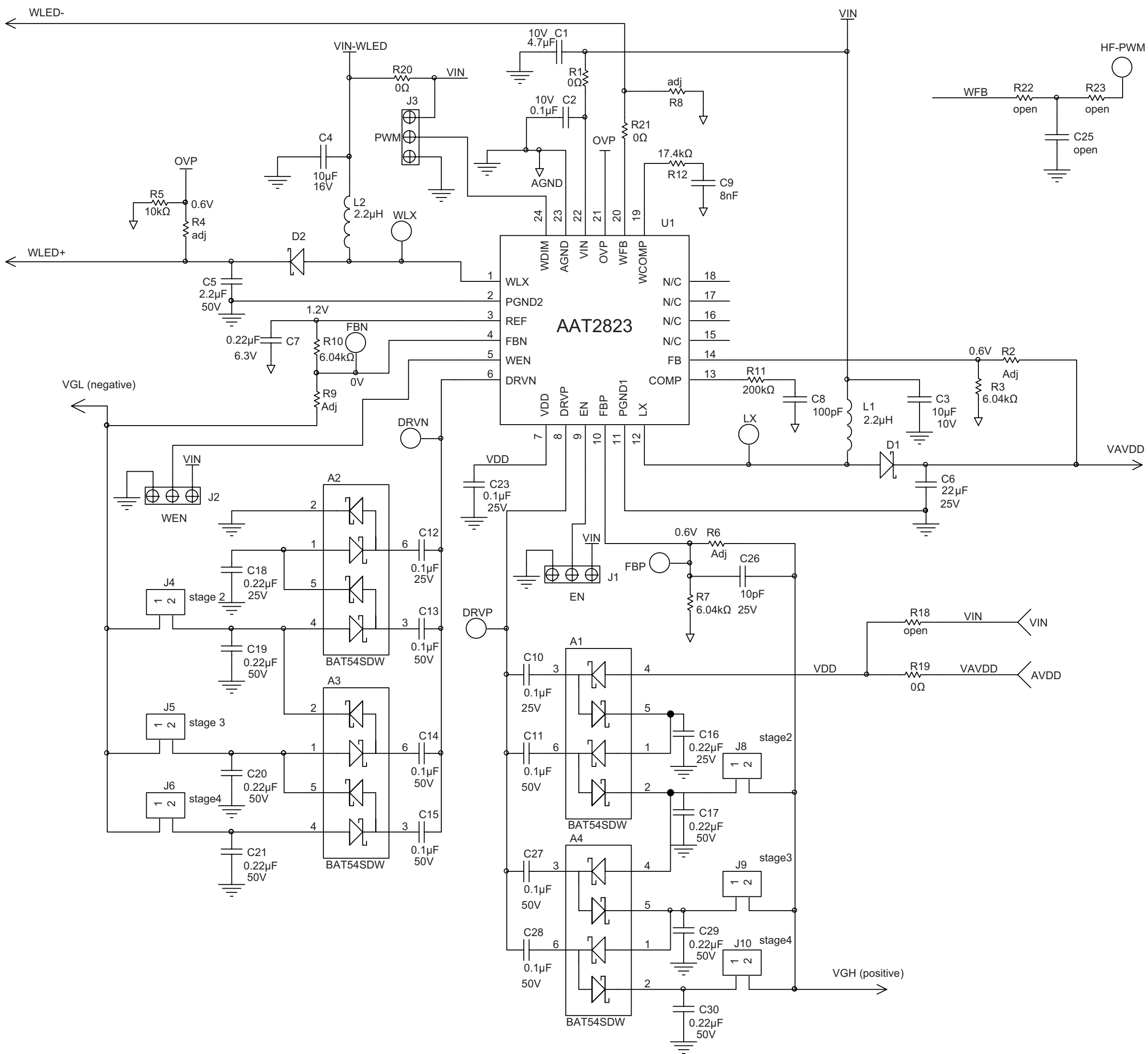


Figure 7: AAT2823IBK Evaluation Board Schematic.

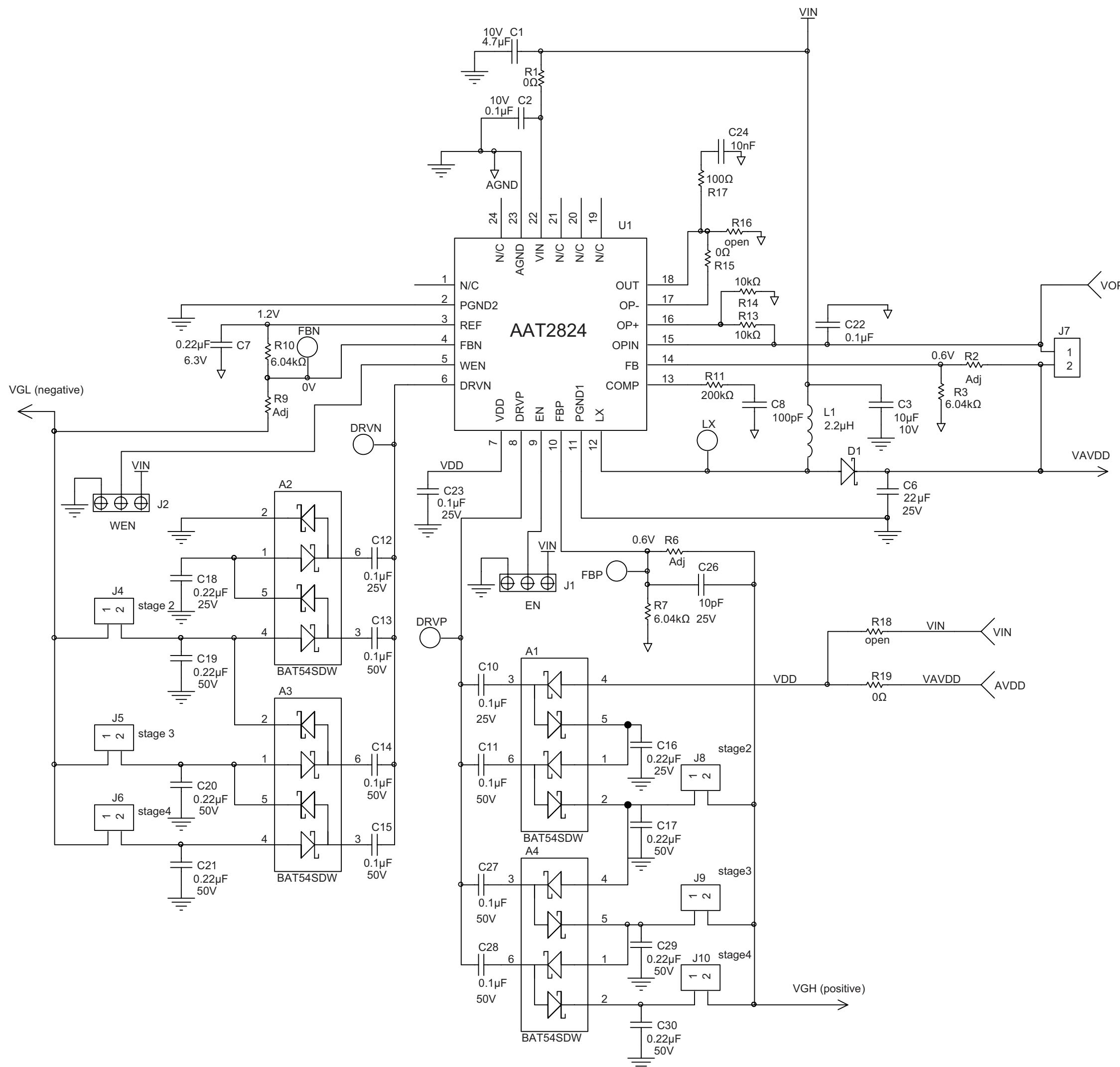


Figure 8: AAT2824IBK Evaluation Board Schematic.

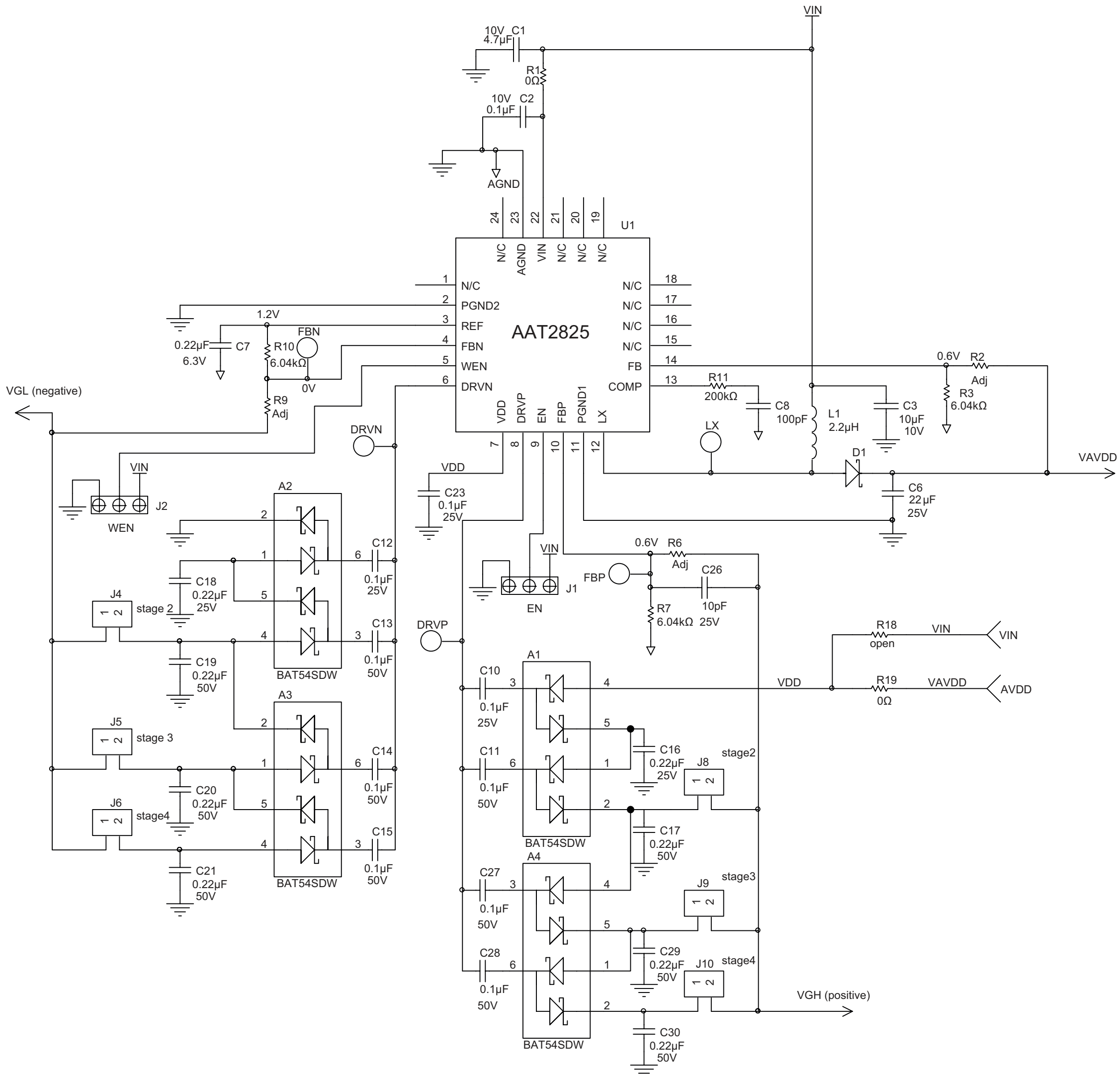


Figure 9: AAT2825IBK Evaluation Board Schematic.

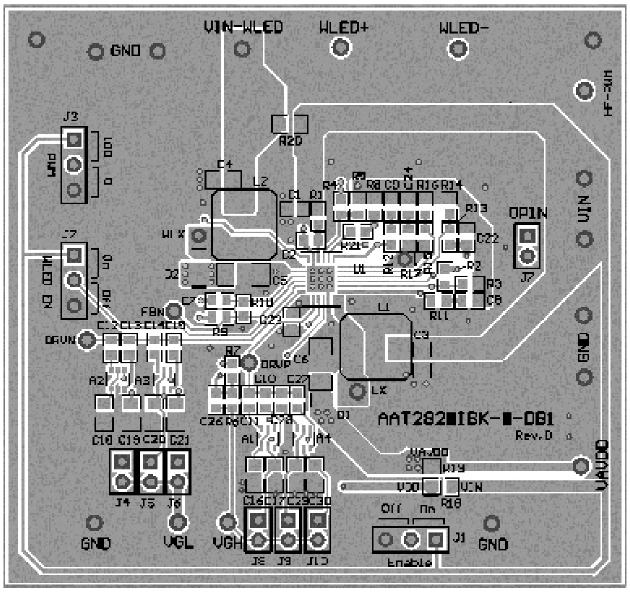


Figure 10: AAT28XXIBK Evaluation Board Top Side Layout.

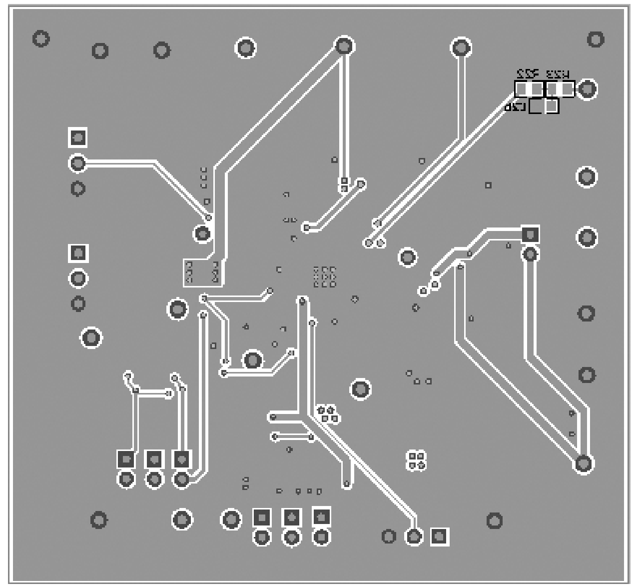


Figure 11: AAT28XXIBK Evaluation Board Bottom Side Layout.

AAT2822/2823/2824/2825

TFT-LCD DC/DC Converter with WLED Driver and VCOM Buffer

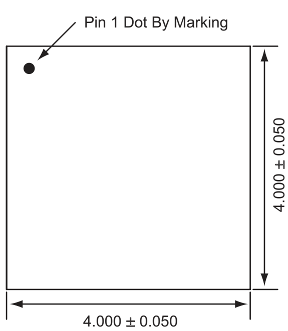
Ordering Information[1,2]

Package	Part Marking[1]	Part Number (Tape and Reel)[2]
TQFN44-24	8XXYY	**AAT2822IBK-T1**
TQFN44-24	F8XYY	**AAT2822IBK-1-T1**
TQFN44-24	B7XYY	**AAT2823IBK-T1**
TQFN44-24	F9XYY	**AAT2823IBK-1-T1**
TQFN44-24		AAT2824IBK-T1
TQFN44-24		AAT2824IBK-1-T1
TQFN44-24		AAT2825IBK-T1
TQFN44-24		AAT2825IBK-1-T1

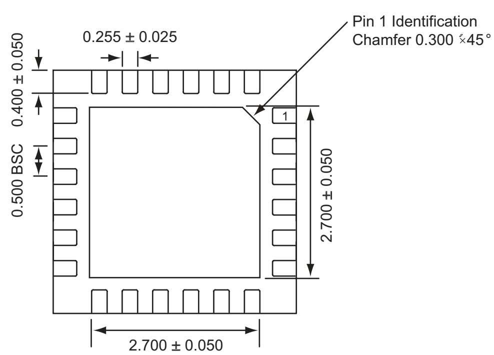
Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Package Information[3]

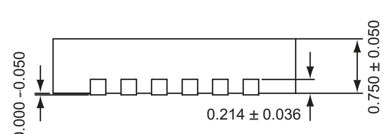
TQFN44-24



Top View



Bottom View



Side View

All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.