PT5500 Series

3-A 5-V/3.3-V Input Adjustable Integrated Switching Regulator

EXCALIBUR

SLTS132A

(Revised 10/5/2001)

Features

- Single-Device: 5V/3.3V Input
- DSP Compatible
- 90% Efficiency
- Small Footprint
- Space-Saving package
- Adjustable Output Voltage
- Output Inhibit Function
- Short Circuit Protection
- Solderable Copper Case

Description

The PT5500 Excalibur™ power modules are a series of high-performance Integrated Switching Regulators (ISRs). Rated 3A, these modules operate from input voltages as low as 3.1V to provide a local step-down power source. They are an ideal compliment to the industry's latest high-performance DSPs and microprocessors. The series includes output voltage options as low as 1.0VDC.

The PT5500 series is packaged in a 5-pin thermally efficient copper case. The case is solderable, has a small footprint, and can accommodate both through-hole and surface mount pin configurations.

The product features external output voltage adjustment, an inhibit function, and short circuit protection. A 100µF capacitor is required for proper operation.

Ordering Information

PT 5501☐ =3.3 Volts
PT 5502☐ =2.5 Volts
PT 5503☐ =2.0 Volts
PT 5504☐ =1.8 Volts
PT 5505☐ =1.5 Volts
PT 5506☐ =1.2 Volts
PT 5507☐ =1.0 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(EFK)
Horizontal	**A**	(EFL)
SMD	**C**	(EFM)

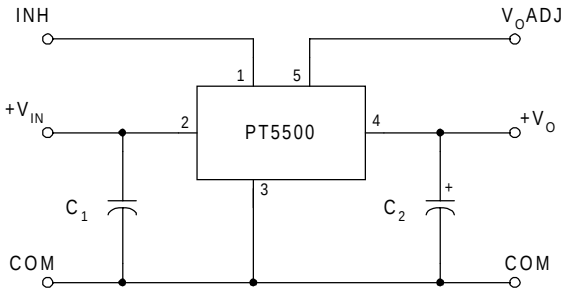
(Reference the applicable package code drawing for the dimensions and PC board layout)

Pin-Out Information

Pin	Function
1	Inhibit *
2	Vin
3	GND
4	V_o
5	V_o Adjust

** For Inhibit pin:*
Open = output enabled
Ground = output disabled

Standard Application



C_1 = Optional 1µF ceramic
C_2 = Required 100µF (See Notes)

Specifications (Unless otherwise stated, T_a =25°C, V_{in} =5V, C_{out} =100µF, and I_o =$I_o$max)

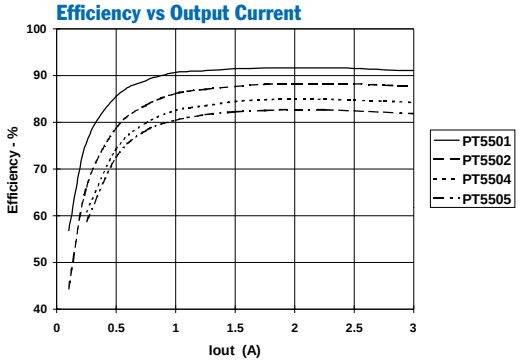
Characteristics	Symbols	Conditions		PT5500 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range		0.1 (1)	—	3.0	A
Input Voltage Range	V_{in}	Over I_o range	V_o =3.3V V_o≤2.5V	4.5 3.1	— 	5.5 5.5	V
Set-Point Voltage Tolerance	V_o tol			—	—	±2	%V_o
Temperature Variation	ΔReg_{temp}	–40°C <T_a < +85°C		—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range		—	—	±6	mV
Load Regulation	ΔReg_{load}	Over I_o range		—	—	±10	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40°C ≤ T_a ≤ +85°C		—	—	±3	%V_o
Efficiency	η		PT5501 PT5502 PT5503 PT5504 PT5505 PT5506 PT5507	— — — — — — —	90 87 85 83 81 79 76	— — — — — — —	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth		—	25	45	mV
Transient Response	t_{tr} ΔV_{tr}	1A/µs load step from 50% to 100% $I_o$max V_o over/undershoot		— —	50 50	— 100	µSec mV
Current Limit	I_{lim}			—	5	—	A
Switching Frequency	f_o	Over V_{in} and I_o ranges		—	350 (2)	—	kHz
Inhibit Control (pin1) Input High Voltage Input Low Voltage Input Low Current	 V_{IH} V_{IL} I_{IL}	 Referenced to GND (pin3) Pin 1 to GND		 V_{in} –0.5 –0.2 —	 — –0.5	 Open (3) 0.5 —	 V mA
External Capacitance	C_{out}			100 (4)	—	—	µF
Absolute Maximum Operating Temperature Range	T_a	Over V_{in} range		–40 (5)	—	+85 (6)	°C
Storage Temperature	T_s	—		-40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 , 1 msec, Half Sine, mounted to a fixture		—	500	—	G's
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2, 20-2000 Hz, Soldered in a PC board		—	15 (7)	—	G's
Weight	—	—		—	6.5	—	grams
Flammability	—	Materials meet UL 94V-0					

Notes: *(1) The ISR will operate down to no load with reduced specifications.*
(2) This is a typical value only. The switching frequency will vary with input voltage.
(3) The Inhibit control (pin 1) has an internal pull-up, and if left open-circuit the module will operate when input power is applied. A small low-leakage (<100nA) MOSFET is recommended to control this input. Ensure an On/Off transition time of ≤10µs. See application notes for more information.
(4) The PT5500 Series requires a 100µF electrolytic or tantalum output capacitor for proper operation in all applications.
(5) For operation below 0°C, the output capacitor C_2 must have stable characteristics. Use either a low ESR tantalum or Oscon® capacitor.
(6) See SOA curves or consult factory for the appropriate derating.
(7) The case pins on the through-hole package types (suffixes N & A) must be soldered. For more information see the applicable package outline drawing.

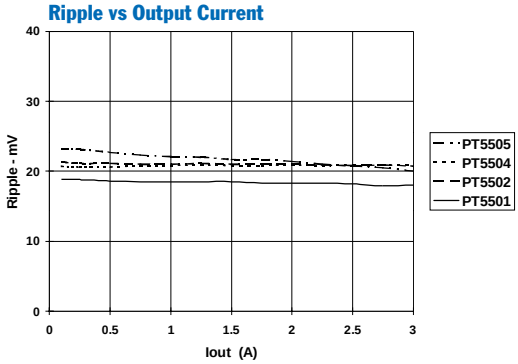
Typical Characteristics

Performance Data; V_{in} =5.0V (See Note A)

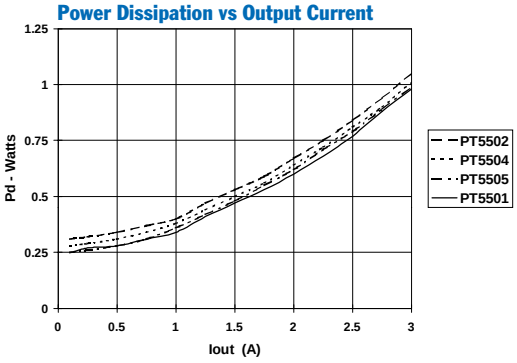
Efficiency vs Output Current



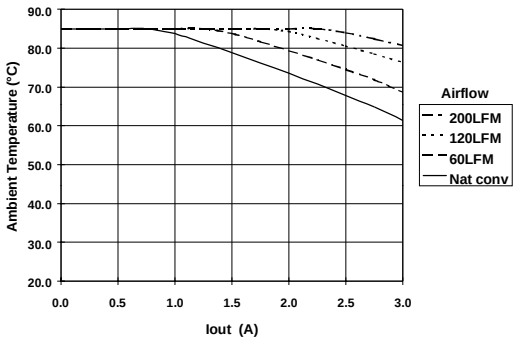
Ripple vs Output Current



Power Dissipation vs Output Current

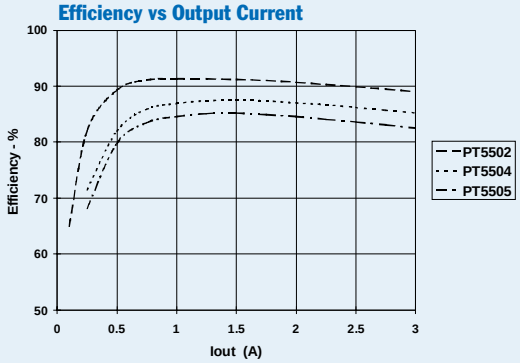


Safe Operating Area; V_{in} =5.0V (See Note B)

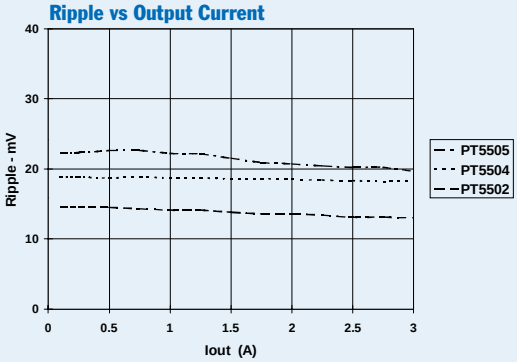


Performance Data; V_{in} =3.3V (See Note A)

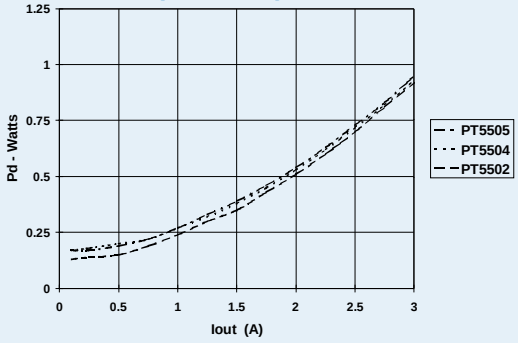
Efficiency vs Output Current



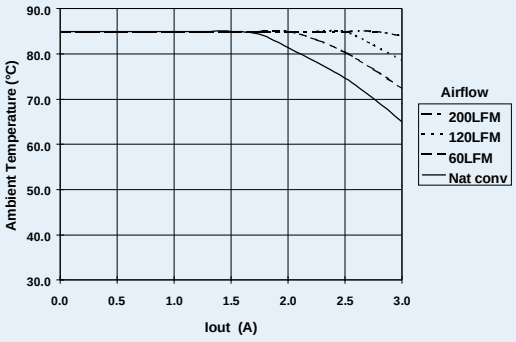
Ripple vs Output Current



Power Dissipation vs Output Current



Safe Operating Area; V_{in} =3.3V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

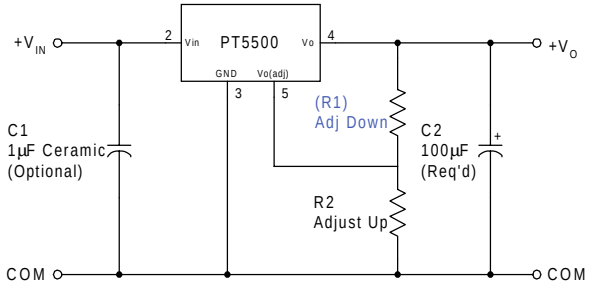
Adjusting the Output Voltage of the PT5500/20 Series of Excalibur™ Step-Down ISRs

The output voltage of both the PT5500 and PT5520 series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 1 accordingly gives the allowable adjustment range for each model for either series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R_2, between pin 5 (V_o adj) and pin 3 (GND).

Adjust Down: Add a resistor (R_1), between pin 5 (V_o adj) and pin 4 (V_{out}).

Figure 1



The values of (R_1) [adjust down], and R_2 [adjust up], can also be calculated using the following formulas. Refer to Figure 1 and Table 2 for both the placement and value of the required resistor; either (R_1) or R_2 as appropriate.

$$(R_1) = \frac{R_o\,(V_a - 0.9)}{V_o - V_a} - R_s \quad k\Omega$$

$$R_2 = \frac{0.9\,R_o}{V_a - V_o} - R_s \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_o = The resistance value from Table 1
R_s = The series resistance from Table 1

Notes:

1. Use only a single 1% resistor in either the (R_1) or R_2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o adj to either GND or V_{out}. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. For each model, adjustments to the output voltage may place additional limits on the minimum input voltage. The revised minimum input voltage must comply with the following requirement.

   V_{in}(min) = (V_a + 0.5)V or as specified in the data sheet, whichever is greater.

Table 1

ISR ADJUSTMENT RANGE AND FORMULA PARAMETERS

3.0 Adc Rated	PT5501	PT5502	PT5503	PT5504	PT5505	PT5506	PT5507
1.5 Adc Rated	PT5521	PT5522	PT5523	PT5524	PT5525	PT5526	PT5527
V_o (nom)	3.3	2.5	2.0	1.8	1.5	1.2	1.0
V_a (min)	2.88	1.97	1.64	1.5	1.3	1.08	0.97
V_a (max)	3.5	2.95	2.45	2.25	1.95	1.65	1.45
R_o (kΩ)	10.0	10.0	10.0	10.0	10.0	10.0	10.2
R_s (kΩ)	49.9	20.0	20.0	20.0	20.0	20.0	20.0

Table 2

ISR ADJUSTMENT RESISTOR VALUES							
3.0 Adc Rated	**PT5501**	**PT5502**	**PT5503**	**PT5504**	**PT5505**	**PT5506**	**PT5507**
1.5 Adc Rated	**PT5521**	**PT5522**	**PT5523**	**PT5524**	**PT5525**	**PT5526**	**PT5527**
V_o (nom)	**3.3**	**2.5**	**2.0**	**1.8**	**1.5**	**1.2**	**1.0**
V_a (req.d)							
0.97							(0.0)kΩ
1.0							
1.05							164.0kΩ
1.1						(0.0)kΩ	72.8kΩ
1.15						(30.0)kΩ	41.2kΩ
1.2							25.9kΩ
1.25						160.0kΩ	16.7kΩ
1.3					(0.0)kΩ	70.0kΩ	10.6kΩ
1.35					(10.0)kΩ	40.0kΩ	6.2kΩ
1.4					(30.0)kΩ	25.0kΩ	3.0kΩ
1.45					(90.0)kΩ	16.0kΩ	0.4kΩ
1.5				(0.0)kΩ		10.0kΩ	
1.55				(6.0)kΩ	160.0kΩ	5.7kΩ	
1.6				(15.0)kΩ	70.0kΩ	2.5kΩ	
1.65			(1.4)kΩ	(30.0)kΩ	40.0kΩ	0.0kΩ	
1.7			(6.7)kΩ	(60.0)kΩ	25.0kΩ		
1.75			(14.0)kΩ	(150.0)kΩ	16.0kΩ		
1.8			(25.0)kΩ		10.0kΩ		
1.85			(43.3)kΩ	160.0kΩ	5.7kΩ		
1.9			(80.0)kΩ	70.0kΩ	2.5kΩ		
1.95			(190.0)kΩ	40.0kΩ	0.0kΩ		
2.0		(2.0)kΩ		25.0kΩ			
2.05		(5.6)kΩ	160.0kΩ	16.0kΩ			
2.1		(10.0)kΩ	70.0kΩ	10.0kΩ			
2.15		(15.7)kΩ	0.0kΩ	5.7kΩ			
2.2		(23.3)kΩ	25.0kΩ	2.5kΩ			
2.25		(34.0)kΩ	16.0kΩ	0.0kΩ			
2.3		(50.0)kΩ	10.0kΩ				
2.35		(76.7)kΩ	5.7kΩ				
2.4		(130.0)kΩ	2.5kΩ				
2.45		(284.0)kΩ	0.0kΩ				
2.5							
2.55		160.0kΩ					
2.6		70.0kΩ					
2.65		40.0kΩ					
2.7		25.0kΩ					
2.75		16.0kΩ					
2.8		10.0kΩ					
2.85		5.7kΩ					
2.9	(0.0kΩ	2.5kΩ					
2.95	(8.5)kΩ	0.0kΩ					
3.0	(20.1)kΩ						
3.05	(36.1)kΩ						
3.1	(60.1)kΩ						
3.15	(100.0)kΩ						
3.2	(180.0)kΩ						
3.25	(420.0)kΩ						
3.3							
3.35	130.0kΩ						
3.4	40.1kΩ						
3.45	10.1kΩ						
3.48	0.0kΩ						

R1 = (Blue) R2 = Black

Using the Inhibit Control on the PT5500/PT5520 Series of Excalibur™ Step-Down ISRs

For applications requiring output voltage On/Off control, both the PT5500 and PT5520 series of power modules incorporate an inhibit function. This function can be used for power-up sequencing or wherever there is a requirement for the module to be switched off. The On/Off function is provided by the *Inhibit* (pin 1) control.

The ISR functions normally with Pin 1 open-circuit, providing a regulated output whenever a valid source voltage is applied to V_{in}, (pin 2). When a low-level[2] ground signal is applied to pin 1, the regulator output will be disabled.

Figure 1 shows an application schematic, which details the typical use of the Inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pull-up to $+V_{in}$ potential. An open-collector or open-drain device is required to control this pin.

The Inhibit pin control thresholds are given in Table 1. Equation 1 may be used to determine the approximate current drawn from the input source, and by Q_1 when the regulator is in the inhibit state.

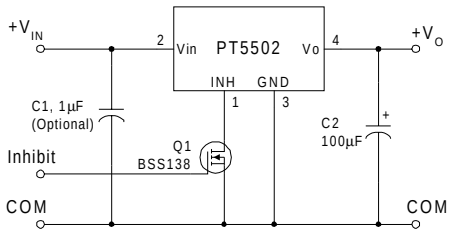
Table 1; Inhibit Control Requirements

Parameter	Min	Max
Enable (VIH)	Vin – 0.5	Open
Disable (VIL)	–0.2V	+0.5V

Equation 1

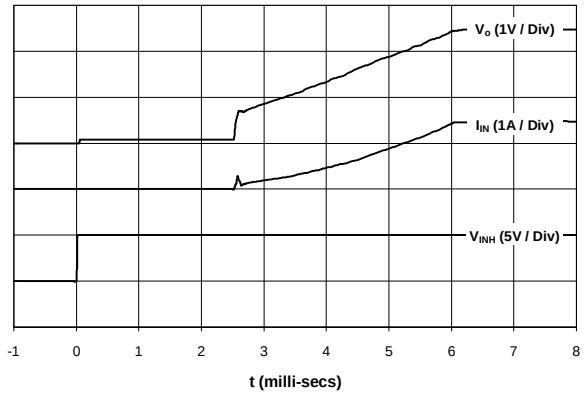
$$I_{inh} = V_{in} \div 10k\Omega \pm 20\%$$

Figure 1



Turn-On Time: In the circuit of Figure 1, turning Q_1 on applies a low-voltage to the Inhibit control (pin 1) and disables the regulator output. Correspondingly, turning Q_1 off allows the *Inhibit* control pin to be pulled high by its internal pull-up resistor. The ISR produces a fully regulated output voltage within 10-msec of the release of the Inhibit control pin. The actual turn-on time will vary with input voltage, output load, and the total amount of load capacitance. Figure 2 shows the typical rise in both output voltage and input current for a PT5502 (2.5V) following the turn-off of Q_1 at time t =0. The waveform was measured with a 5Vdc input voltage, and 2.5A resistive load.

Figure 2



Notes:

1. Use an open-collector device (preferably a discrete transistor) for the Inhibit input. A pull-up resistor is not necessary. To disable the output voltage, the control pin should be pulled low to less than +0.5VDC.
2. Do not control the Inhibit input with an external DC voltage. This will lead to erratic operation of the ISR and may over-stress the regulator.
5. Avoid capacitance greater than 500pF at the Inhibit control pin. Excessive capacitance at this pin will cause the ISR to produce a pulse on the output voltage bus at turn-on.
6. Keep the On/Off transition to less than 10µs. This prevents erratic operation of the ISR, which could cause a momentary high output voltage.

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