

# DAC1201D125

Dual 12-bit DAC, up to 125 Msps

Rev. 03 — 2 July 2012

Product data sheet

## 1. General description

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The DAC1201D125 is a dual-port, high-speed, 2-channel CMOS Digital-to-Analog Converter (DAC), optimized for high dynamic performance with low power dissipation. Supporting an update rate of up to 125 Msps, the DAC1201D125 is suitable for Direct IF applications.

Separate write inputs allow data to be written to the two DAC ports independently of one another. Two separate clocks control the update rate of each DAC port.

The DAC1201D125 can interface two separate data ports or one single interleaved high-speed data port. In Interleaved mode, the input data stream is demultiplexed into its original I and Q data and latched. The I and Q data is then converted by the two DACs and updated at half the input data rate.

Each DAC port has a high-impedance differential current output, suitable for both single-ended and differential analog output configurations.

The DAC1201D125 is pin compatible with the AD9765, DAC2902 and DAC5662.

## 2. Features and benefits

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- Dual 12-bit resolution
- 125 Msps update rate
- Single 3.3 V supply
- Dual-port or Interleaved data modes
- 1.8 V, 3.3 V and 5 V compatible digital inputs
- Internal and external reference
- 2 mA to 20 mA full-scale output current
- Typical 185 mW power dissipation
- 16 mW power-down
- SFDR: 81 dBc;  $f_o = 1$  MHz;  $f_s = 52$  Msps
- SFDR: 78 dBc;  $f_o = 10.4$  MHz;  $f_s = 78$  Msps
- SFDR: 74 dBc;  $f_o = 1$  MHz;  $f_s = 52$  Msps;  $-12$  dBFS
- LQFP48 package
- Industrial temperature range of  $-40$  °C to  $+85$  °C

## 3. Applications

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- Quadrature modulation
- Medical/test instrumentation
- Direct IF applications
- Direct digital frequency synthesis
- Arbitrary waveform generator



## 4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
DAC1201D125HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

## 5. Block diagram

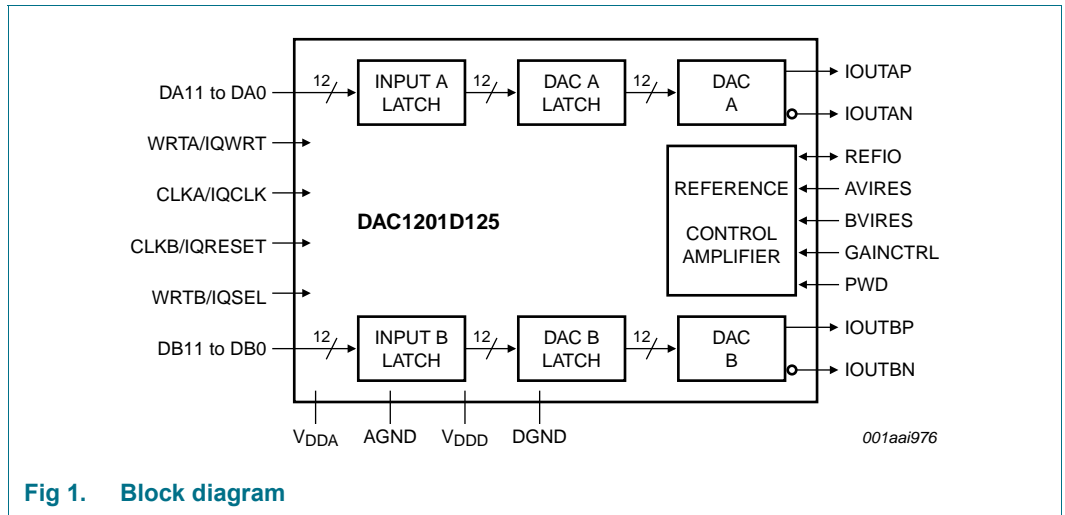


Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning

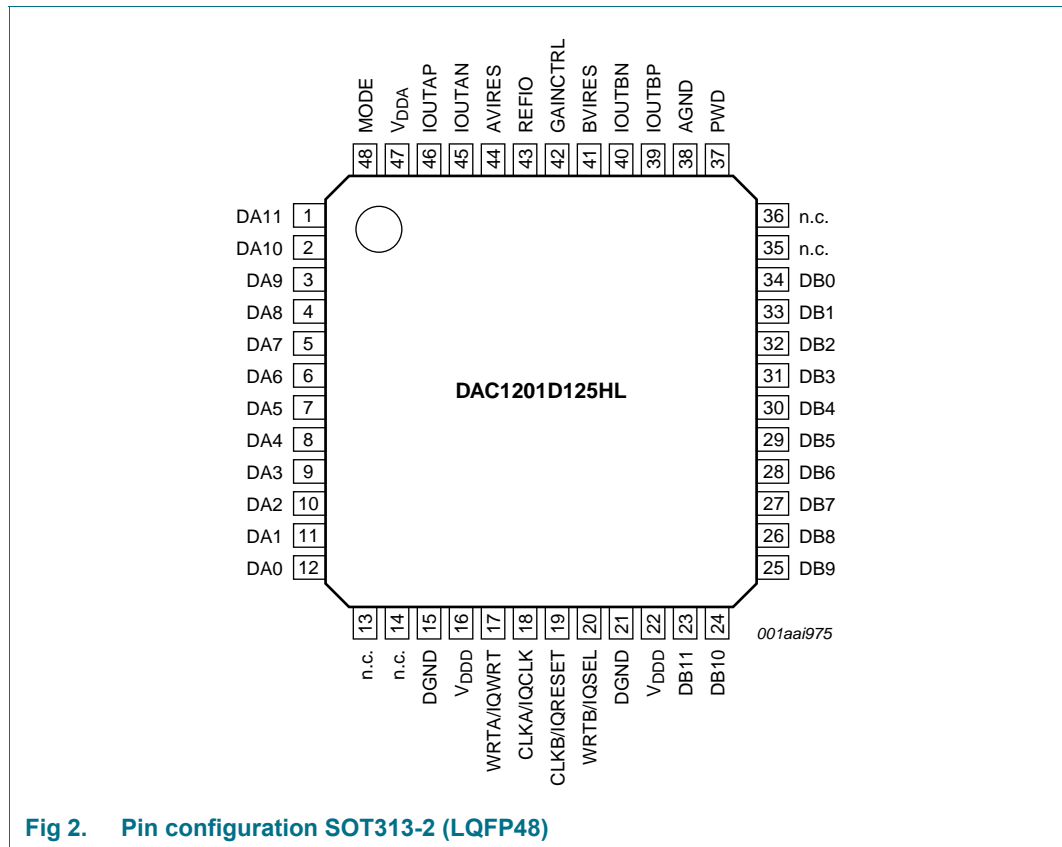


Fig 2. Pin configuration SOT313-2 (LQFP48)

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type <sup>[1]</sup>	Description
DA11	1	I	DAC A, data input bit 11 (MSB)
DA10	2	I	DAC A, data input bit 10
DA9	3	I	DAC A, data input bit 9
DA8	4	I	DAC A, data input bit 8
DA7	5	I	DAC A, data input bit 7
DA6	6	I	DAC A, data input bit 6
DA5	7	I	DAC A, data input bit 5
DA4	8	I	DAC A, data input bit 4
DA3	9	I	DAC A, data input bit 3
DA2	10	I	DAC A, data input bit 2
DA1	11	I	DAC A, data input bit 1
DA0	12	I	DAC A, data input bit 0 (LSB)
n.c.	13		not connected

Table 2. Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
n.c.	14		not connected
DGND	15	G	digital ground
V <sub>DD</sub>	16	S	digital supply voltage
WRTA/IQWRT	17	I	input write port A/input write IQ in Interleaved mode
CLKA/IQCLK	18	I	input clock port A/input clock IQ in Interleaved mode
CLKB/IQRESET	19	I	input clock port B/reset IQ in Interleaved mode
WRTB/IQSEL	20	I	input write port B/select IQ in Interleaved mode
DGND	21	G	digital ground
V <sub>DD</sub>	22	S	digital supply voltage
DB11	23	I	DAC B, data input bit 11 (MSB)
DB10	24	I	DAC B, data input bit 10
DB9	25	I	DAC B, data input bit 9
DB8	26	I	DAC B, data input bit 8
DB7	27	I	DAC B, data input bit 7
DB6	28	I	DAC B, data input bit 6
DB5	29	I	DAC B, data input bit 5
DB4	30	I	DAC B, data input bit 4
DB3	31	I	DAC B, data input bit 3
DB2	32	I	DAC B, data input bit 2
DB1	33	I	DAC B, data input bit 1
DB0	34	I	DAC B, data input bit 0 (LSB)
n.c.	35		not connected
n.c.	36		not connected
PWD	37	I	Power-down mode enable input
AGND	38	S	analog ground
IOUTBP	39	O	DAC B current output
IOUTBN	40	O	complementary DAC B current output
BVIRE	41	I	adjust DAC B for full-scale output current
GAINCTRL	42	I	gain control mode enable input
REFIO	43	I/O	reference voltage input/output
AVIRE	44	I	adjust DAC A for full-scale output current
IOUTAN	45	O	complementary DAC A current output
IOUTAP	46	O	DAC A current output
V <sub>DDA</sub>	47	S	analog supply voltage
MODE	48	I	select between Dual-port or Interleaved mode

[1] Type description: S = Supply; G = Ground; I = Input; O = Output; I/O = Input/Output.

## 7. Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDD}$	digital supply voltage		[1] -0.3	+5.0	V
$V_{DDA}$	analog supply voltage		[1] -0.3	+5.0	V
$\Delta V_{DD}$	supply voltage difference	between analog and digital supply voltage	-150	+150	mV
$V_I$	input voltage	digital inputs referenced to DGND	-0.3	+5.5	V
		pins REFIO, AVIRES, BVIRES referenced to AGND	-0.3	+5.5	V
$V_O$	output voltage	pins IOUTAP, IOUTAN, IOUTBP and IOUTBN referenced to AGND	-0.3	$V_{DDA} + 0.3$	V
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$T_j$	junction temperature		-	125	°C

[1] All supplies are connected together.

## 8. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	89.3	K/W
$R_{th(c-a)}$	thermal resistance from case to ambient	in free air	60.6	K/W

## 9. Characteristics

**Table 5. Characteristics**

$V_{DDD} = V_{DDA} = 3.3$  V; AGND and DGND connected together;  $I_{O(fs)} = 20$  mA and  $T_{amb} = -40$  °C to +85 °C; typical values measured at  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DDD}$	digital supply voltage		3.0	3.3	3.65	V
$V_{DDA}$	analog supply voltage		3.0	3.3	3.65	V
$I_{DDD}$	digital supply current	$f_s = 65$ Msps, $f_o = 1$ MHz, $V_{DD} = 3.0$ V to 3.6 V	-	6	7	mA
$I_{DDA}$	analog supply current	$f_s = 65$ Msps, $f_o = 1$ MHz, $V_{DD} = 3.0$ V to 3.6 V	-	50	65	mA
$P_{tot}$	total power dissipation	$f_s = 65$ Msps, $f_o = 1$ MHz, $V_{DD} = 3.0$ V to 3.6 V	-	185	260	mW
$P_{pd}$	power dissipation in power-down mode		-	16.5	-	mW

**Table 5. Characteristics ...continued**

$V_{DDD} = V_{DDA} = 3.3\text{ V}$ ; AGND and DGND connected together;  $I_{O(fs)} = 20\text{ mA}$  and  $T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$ ; typical values measured at  $T_{amb} = 25\text{ °C}$ .

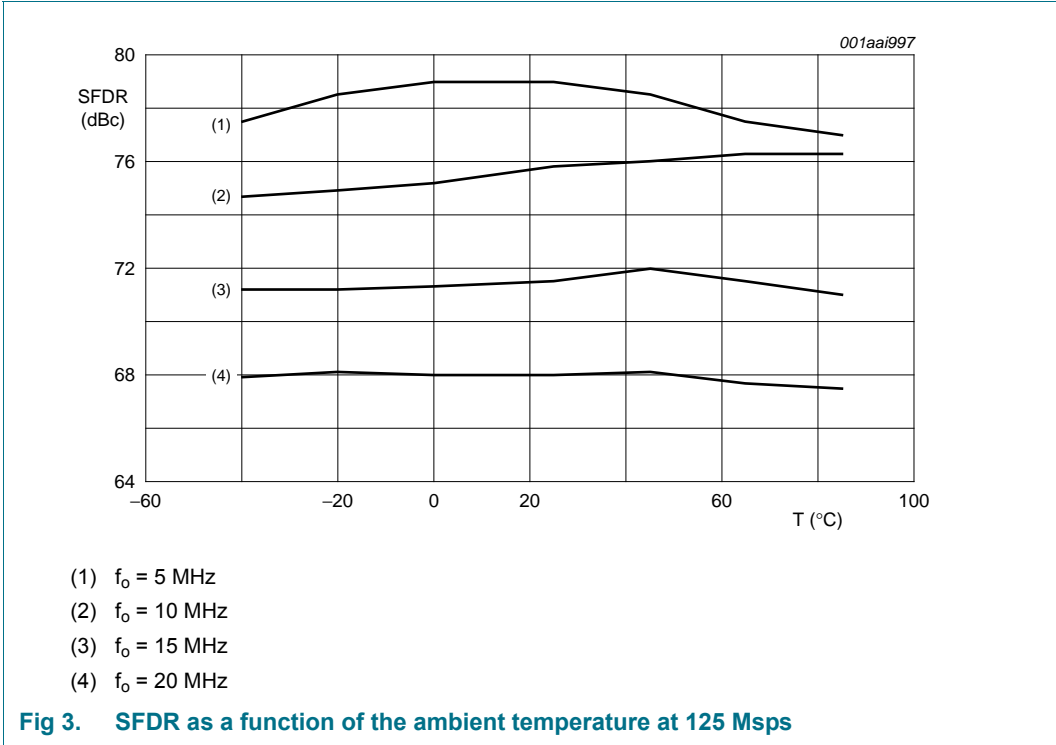
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Digital inputs</b>						
$V_{IL}$	LOW-level input voltage		DGND	-	0.9	V
$V_{IH}$	HIGH-level input voltage		1.3	-	$V_{DDD}$	V
$I_{IL}$	LOW-level input current	$V_{IL} = 0.9\text{ V}$	-	5	-	$\mu\text{A}$
$I_{IH}$	HIGH-level input current	$V_{IH} = 1.3\text{ V}$	-	5	-	$\mu\text{A}$
$C_i$	input capacitance		[1] -	5	-	pF
<b>Analog outputs (IOUTAP, IOUTAN, IOUTBP and IOUTBN)</b>						
$I_{O(fs)}$	full-scale output current	differential outputs	2	-	20	mA
$V_O$	output voltage	compliance range	[1] -1	-	+1.25	V
$R_O$	output resistance		[1] -	150	-	k $\Omega$
$C_O$	output capacitance		[1] -	3	-	pF
<b>Reference voltage input/output (REFIO)</b>						
$V_{O(ref)}$	reference output voltage		1.21	1.26	1.31	V
$I_{O(ref)}$	reference output current		[1] -	100	-	nA
$V_i$	input voltage	compliance range	1.0	-	1.26	V
$R_i$	input resistance		-	1	-	M $\Omega$
<b>Input timing, see Figure 18</b>						
$f_s$	sampling frequency		-	-	125	Msps
$t_{w(WRT)}$	WRT pulse width	pins WRTA, WRTB	2	-	-	ns
$t_{w(CLK)}$	CLK pulse width	pins CLKA, CLKB	2	-	-	ns
$t_{h(i)}$	input hold time		1	-	-	ns
$t_{su(i)}$	input set-up time		1.8	-	-	ns
<b>Output timing (IOUTAP, IOUTAN, IOUTBP and IOUTBN)</b>						
$t_d$	delay time		-	1	-	ns
$t_t$	transition time	rising or falling transition (10 % to 90 % or 90 % to 10 %)	[1] -	0.6	-	ns
$t_s$	settling time	$\pm 1\text{ LSB}$	[1] -	40	-	ns
<b>Static linearity</b>						
INL	integral non-linearity	25 °C	$\pm 0.4$	$\pm 0.55$	$\pm 0.70$	LSB
		-40 °C to +85 °C	$\pm 0.3$	-	$\pm 0.75$	LSB
DNL	differential non-linearity	-40 °C to +85 °C	$\pm 0.15$	$\pm 0.2$	$\pm 0.3$	LSB
<b>Static accuracy (relative to full-scale) with GAINCTRL = 0</b>						
$E_{offset}$	offset error		-0.02	-	+0.02	%
$E_G$	gain error	with external reference	-1.9	$\pm 1.5$	+2.5	%
		with internal reference	-2.9	$\pm 2.1$	+2.9	%
$\Delta G$	gain mismatch	between DAC A and DAC B	-0.5	$\pm 0.05$	+0.5	%

**Table 5. Characteristics ...continued**

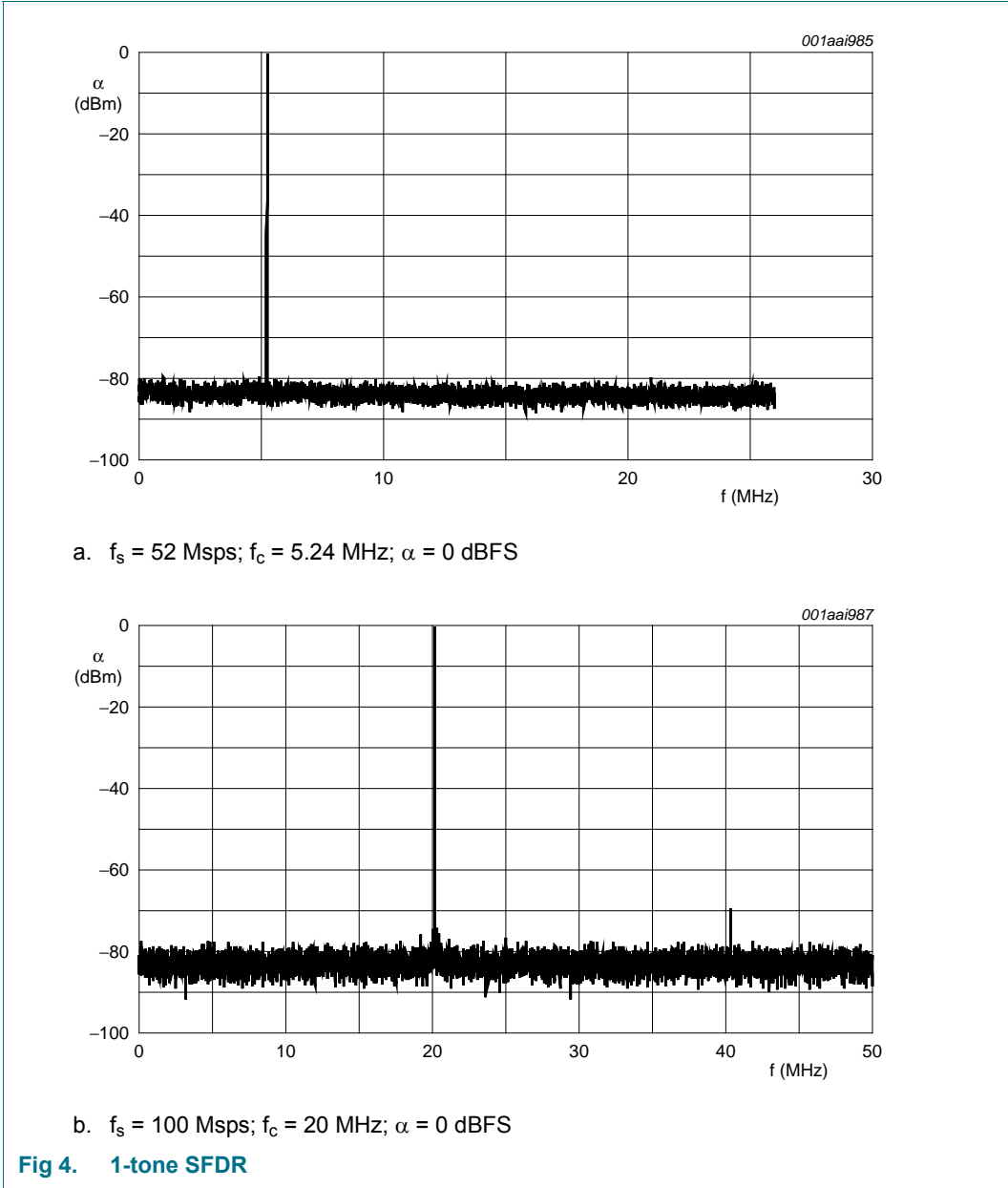
$V_{DD} = V_{DDA} = 3.3$  V; AGND and DGND connected together;  $I_{O(fs)} = 20$  mA and  $T_{amb} = -40$  °C to  $+85$  °C; typical values measured at  $T_{amb} = 25$  °C.

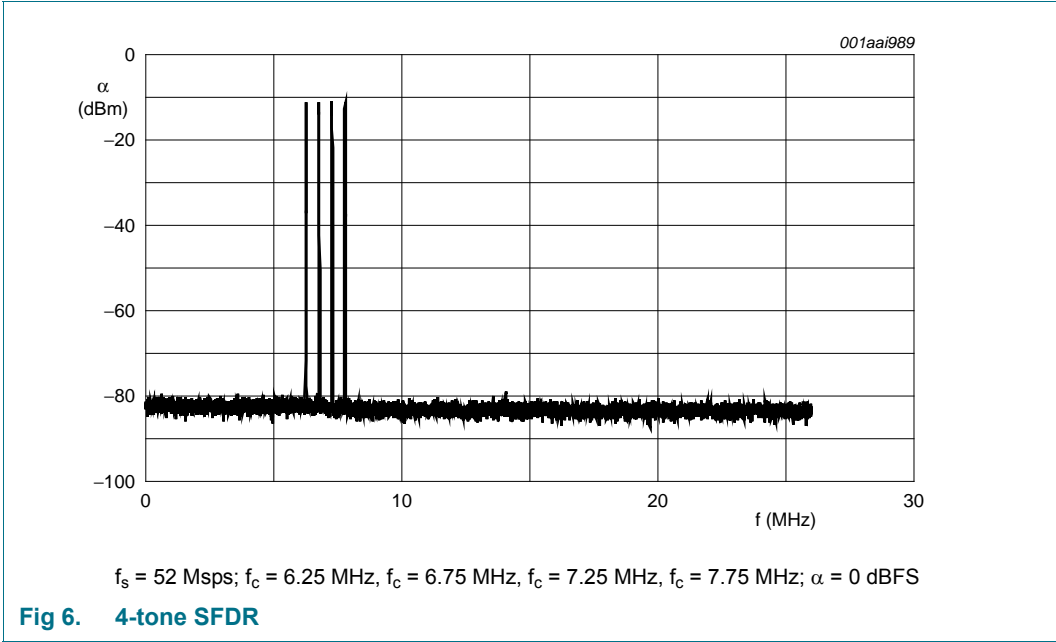
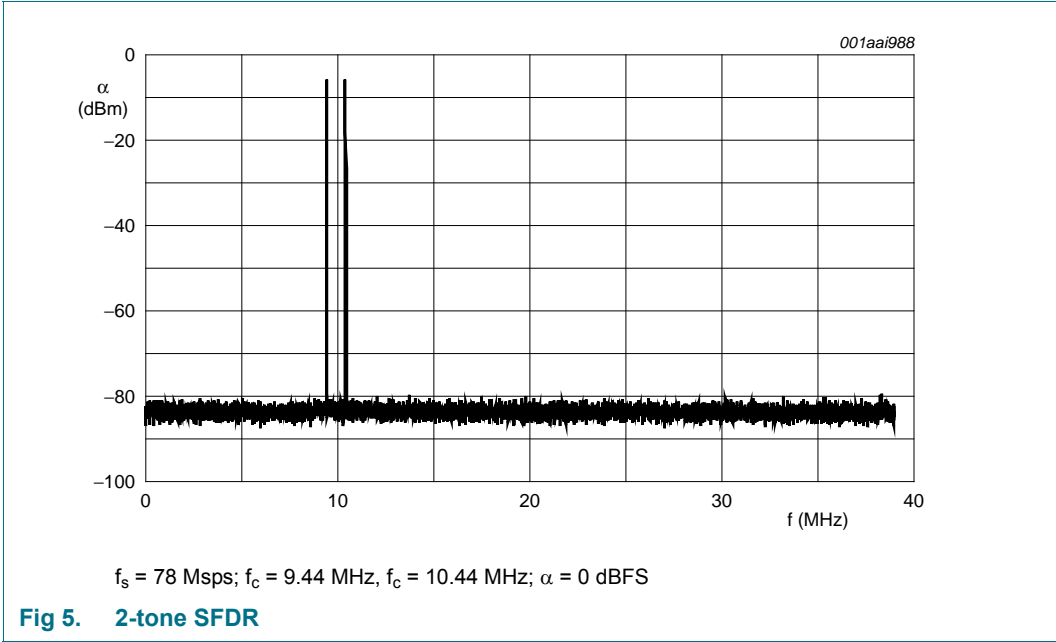
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic performance</b>						
SFDR	spurious free dynamic range	B = Nyquist				
		$f_s = 52$ Msps; $f_o = 1$ MHz				
		0 dBFS	-	81	-	dBc
		-6 dBFS	-	80	-	dBc
		-12 dBFS	-	74	-	dBc
		$f_s = 52$ Msps; 0 dBFS				
		$f_o = 5.24$ MHz	-	79	-	dBc
		$f_s = 78$ Msps; 0 dBFS				
		$f_o = 10.4$ MHz	-	78	-	dBc
		$f_o = 15.7$ MHz	-	71	-	dBc
		$f_s = 100$ Msps; 0 dBFS				
		$f_o = 5.04$ MHz	-	77	-	dBc
		$f_o = 20.2$ MHz	60	69	-	dBc
		$f_s = 125$ Msps; 0 dBFS				
		$f_o = 20.1$ MHz	-	68	-	dBc
within a window						
$f_s = 52$ Msps; $f_o = 1$ MHz; 2 MHz span	-	89	-	dBc		
$f_s = 52$ Msps; $f_o = 5.24$ MHz; 10 MHz span	-	87	-	dBc		
$f_s = 78$ Msps; $f_o = 5.26$ MHz; 2 MHz span	-	90	-	dBc		
$f_s = 125$ Msps; $f_o = 5.04$ MHz; 10 MHz span	79	90	-	dBc		
THD	total harmonic distortion	$f_s = 52$ Msps; $f_o = 1$ MHz	-	-78	-	dBc
		$f_s = 78$ Msps; $f_o = 5.26$ MHz	-	-76	-	dBc
		$f_s = 100$ Msps; $f_o = 5.04$ MHz	-	-74	-	dBc
		$f_s = 125$ Msps; $f_o = 20.1$ MHz	-	-64	-60	dBc
MTPR	multitone power ratio	$f_s = 65$ Msps; 2 MHz < $f_o$ < 2.99 MHz; 8 tones at 110 kHz spacing at 0 dB full-scale	-	80	-	dBc
NSD	noise spectral density	$f_s = 100$ Msps; $f_o = 5.04$ MHz	-	-148.7	-	dBm/Hz
$\alpha_{CS}$	channel separation	$f_s = 78$ Msps; $f_o = 10.4$ MHz	-	88.0	-	dBc
		$f_s = 125$ Msps; $f_o = 20.1$ MHz	-	83.5	-	dBc

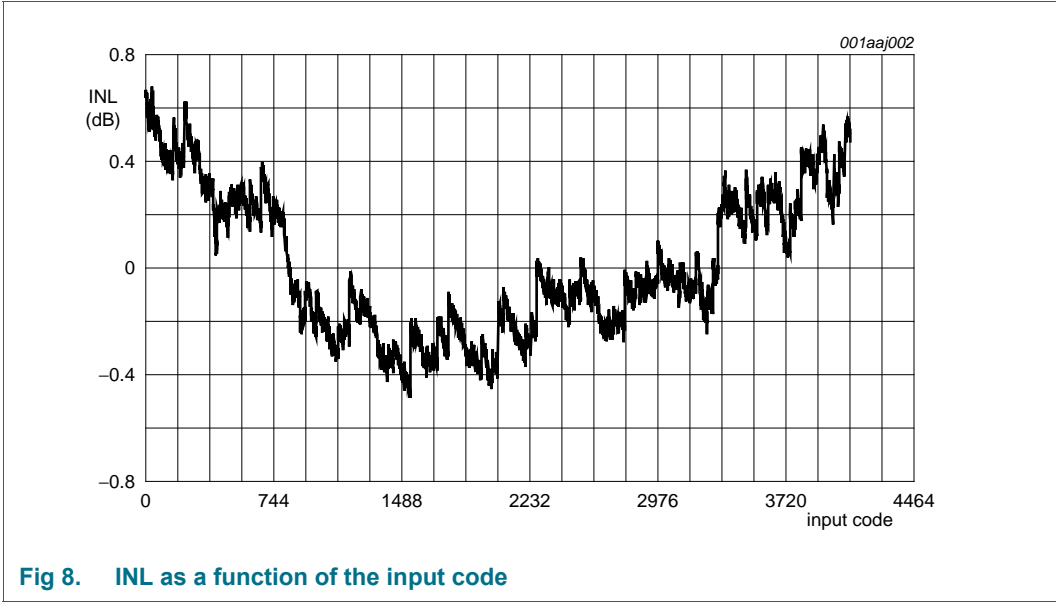
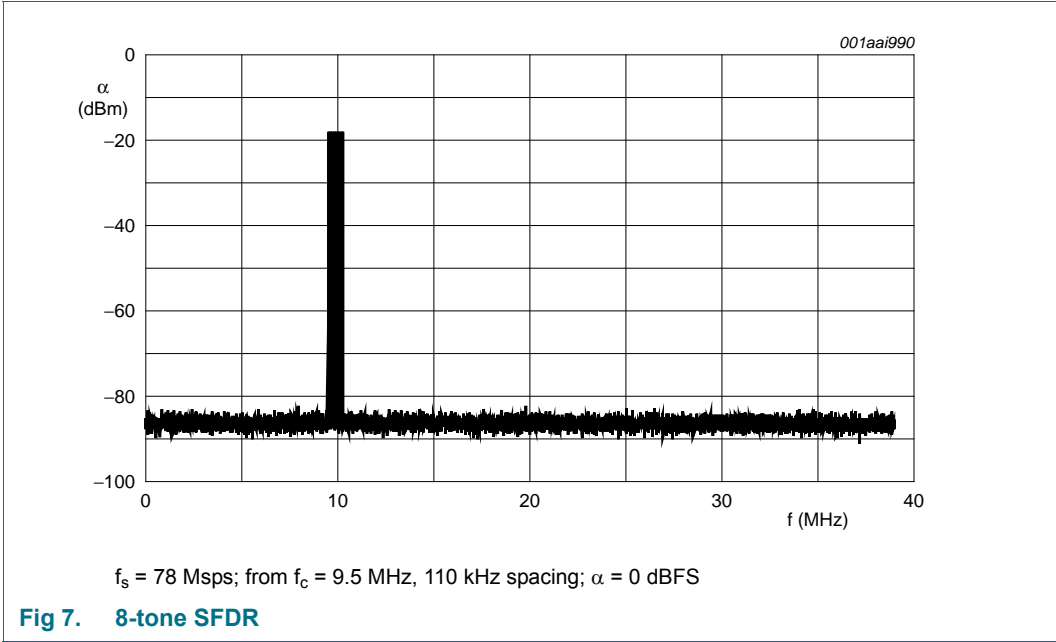
[1] Guaranteed by design.

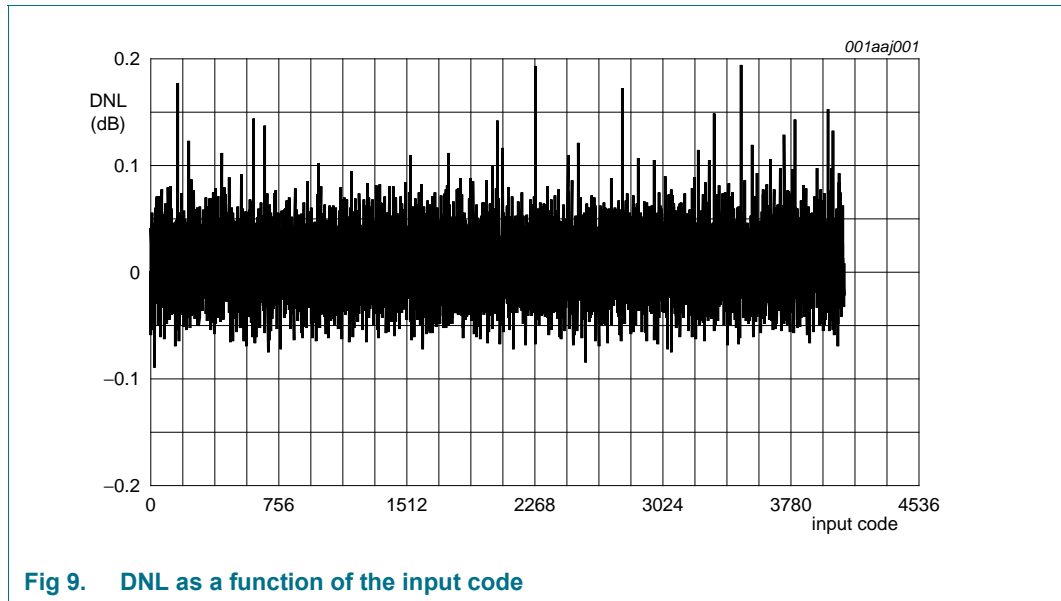




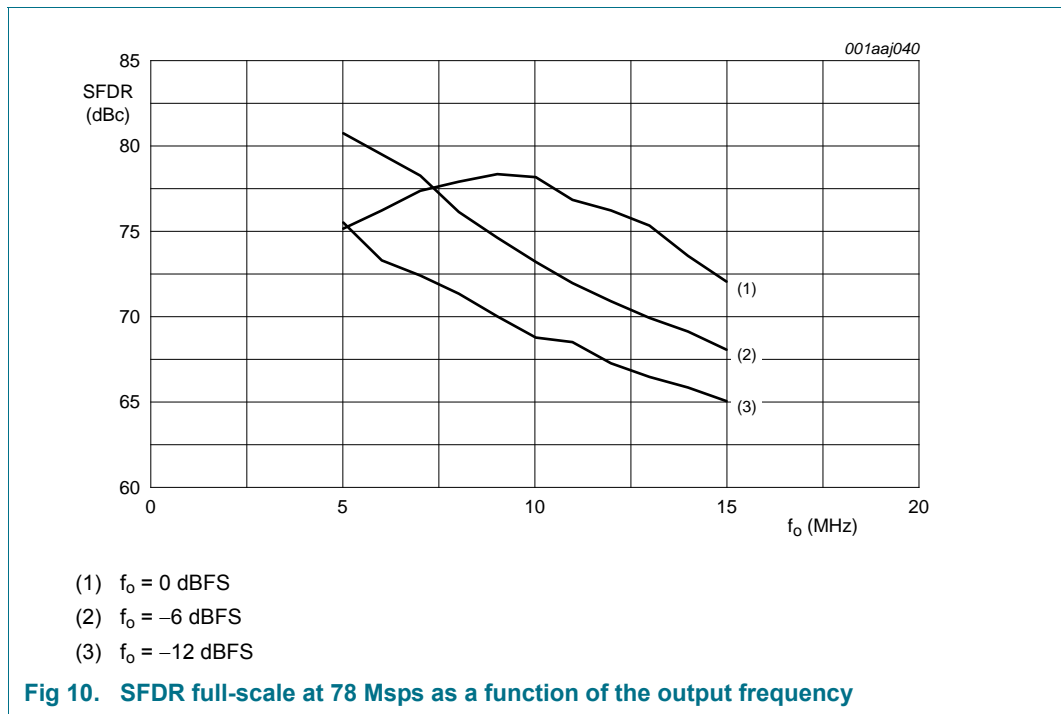




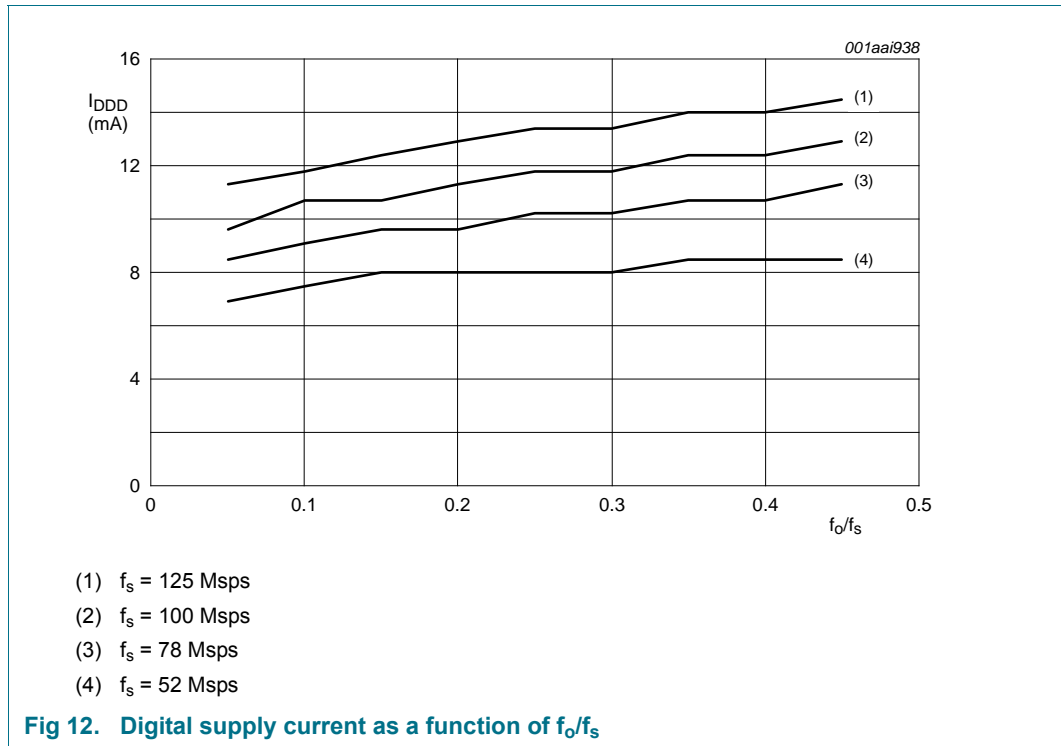
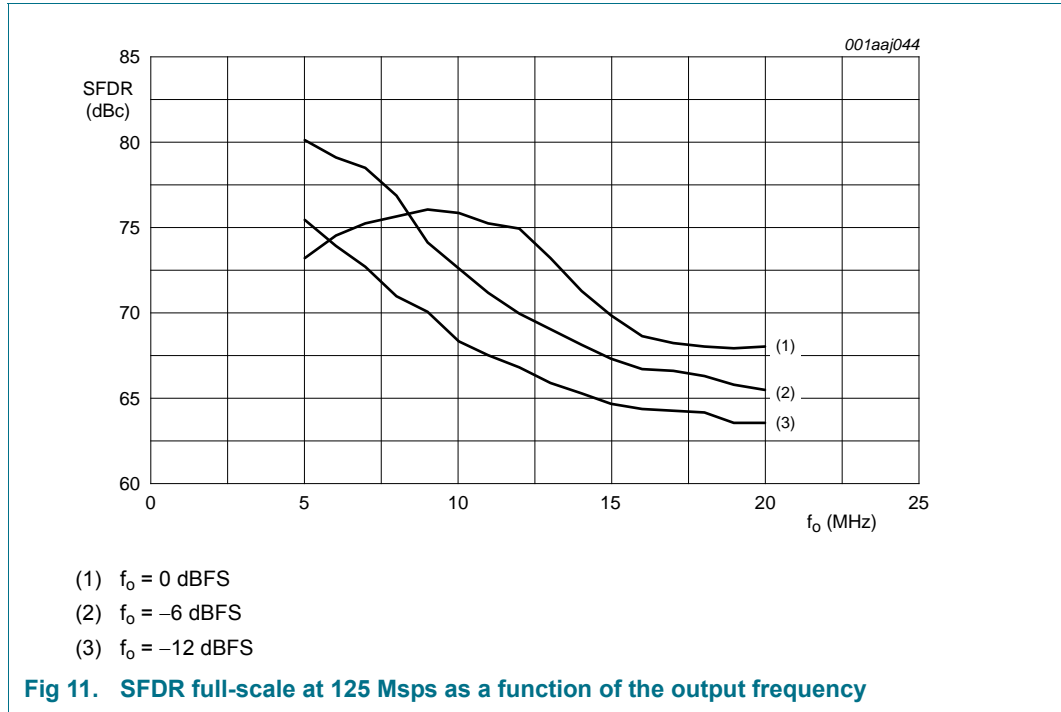


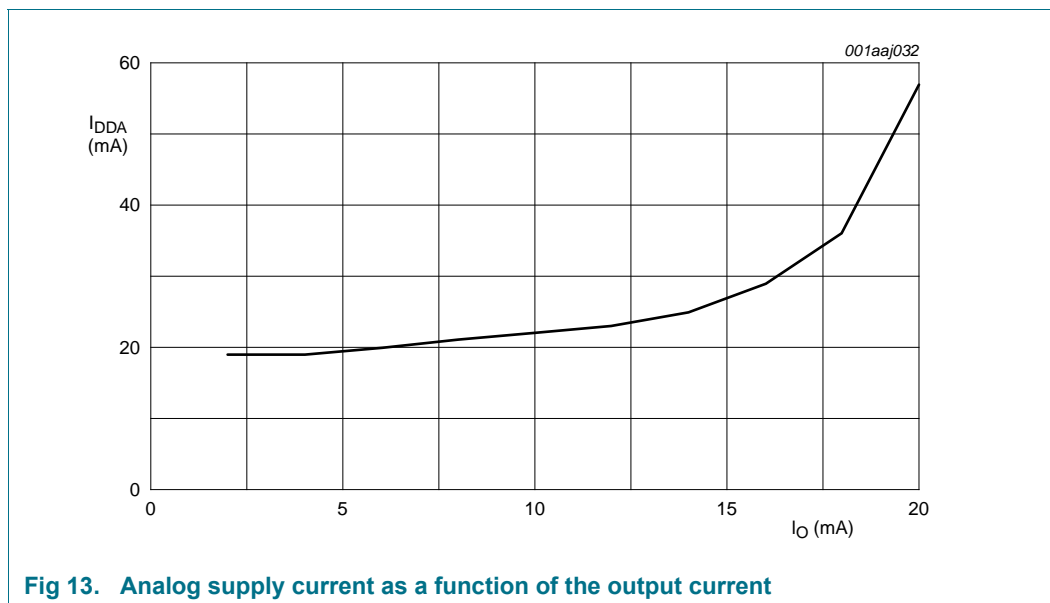


**Fig 9. DNL as a function of the input code**



**Fig 10. SFDR full-scale at 78 Mps as a function of the output frequency**





## 10. Application information

### 10.1 General description

The DAC1201D125 is a dual 12-bit DAC operating up to 125 Msps. Each DAC consists of a segmented architecture, comprising a 7-bit thermometer sub-DAC and a 5-bit binary weighted sub-DAC.

Two modes are available for the digital input depending on the status of pin MODE. In Dual-port mode, each DAC uses its own data input line at the same frequency as the update rate. In Interleaved mode, both DACs use the same data input line at twice the update rate.

Each DAC generates on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN two complementary current outputs. This provides a full-scale output current ( $I_{O(fs)}$ ), up to 20 mA. A single common or two independent full-scale current controls can be selected for both channels using pin GAINCTRL. An internal reference voltage is available for the reference current which is externally adjustable using pin REFIO.

The DAC1201D125 operates at 3.3 V and has separate digital and analog power supplies. Pin PWD is used to power-down the device. The digital input is 1.8 V compliant, 3.3 V compliant and 5 V tolerant.

### 10.2 Input data

The DAC1201D125 input follows a straight binary coding where DA11 and DB11 are the Most Significant Bits (MSB) and DA0 and DB0 are the Least Significant Bits (LSB).

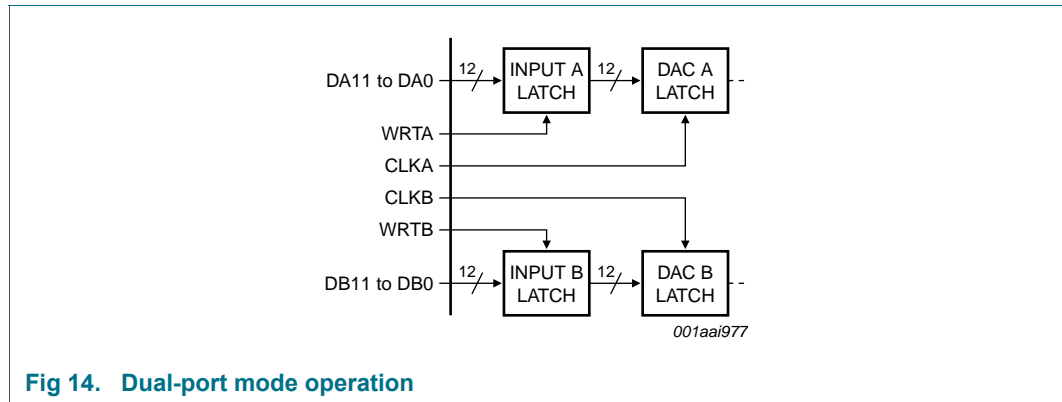
The setting applied to pin MODE defines whether the DAC1201D125 operates in Dual-port mode or in Interleaved mode (see Table 6).

**Table 6. Mode selection**

Mode	Function	DA11 to DA0	DB11 to DB0	Pin 17	Pin 18	Pin 19	Pin 20
LOW	Interleaved mode	active	off	IQWRT	IQCLK	IQRESET	IQSEL
HIGH	Dual-port mode	active	active	WRTA	CLKA	CLKB	WRTB

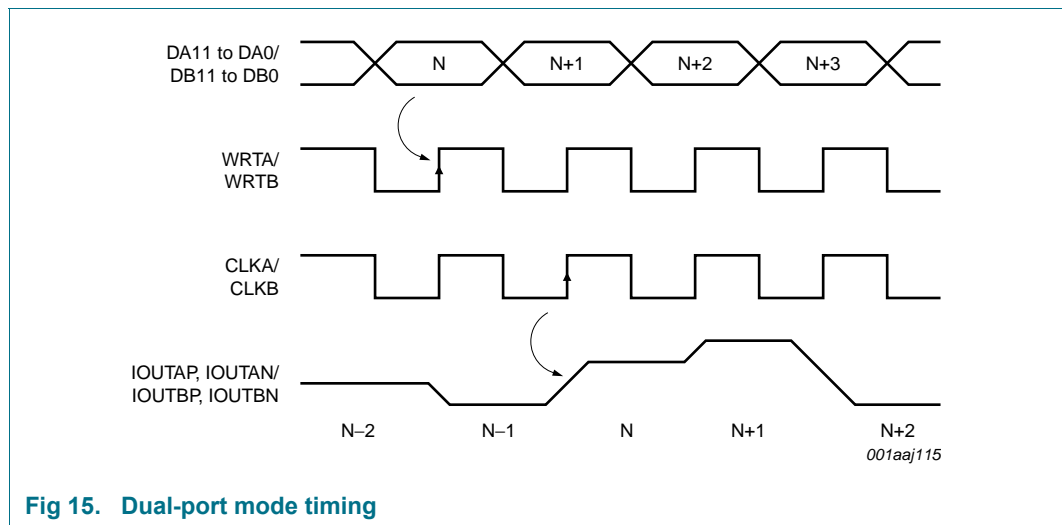
### 10.2.1 Dual-port mode

The data and clock circuit for Dual-port mode operation is shown in Figure 14.



**Fig 14. Dual-port mode operation**

Each DAC has its own independent data and clock inputs. The data enters the input latch on the rising edge of the WRTA/WRTB signal and is transferred to the DAC latch. The output is updated on the rising edge of the CLKA/CLKB signal.



**Fig 15. Dual-port mode timing**

10.2.2 Interleaved mode

The data and clock circuit for Interleaved mode operation is illustrated in Figure 16.

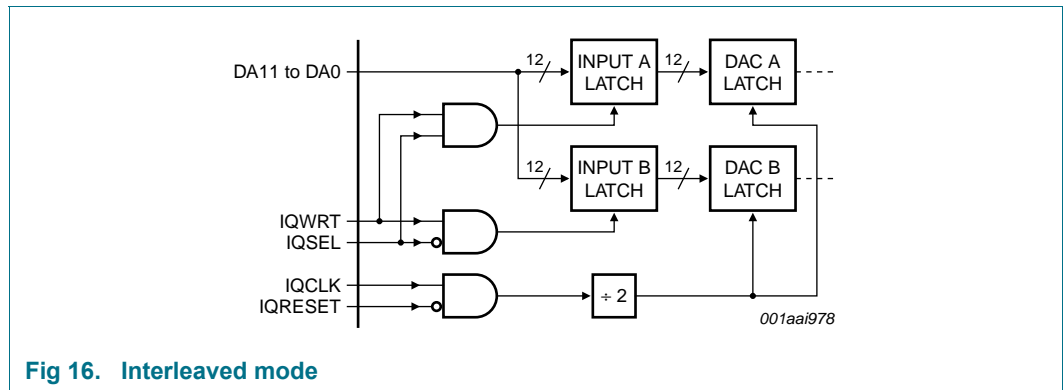


Fig 16. Interleaved mode

In Interleaved mode, both DACs use the same data and clock inputs at twice the update rate. Data enters the latch on the rising edge of IQWRT. The data is sent to either latch A or latch B, depending on the value of IQSEL. The IQSEL transition must occur when IQWRT and IQCLK are LOW.

The IQCLK is divided by 2 internally and the data is transferred to the DAC latch. It is updated on its rising edge. When IQRESET is HIGH, IQCLK is disabled, see Figure 17.

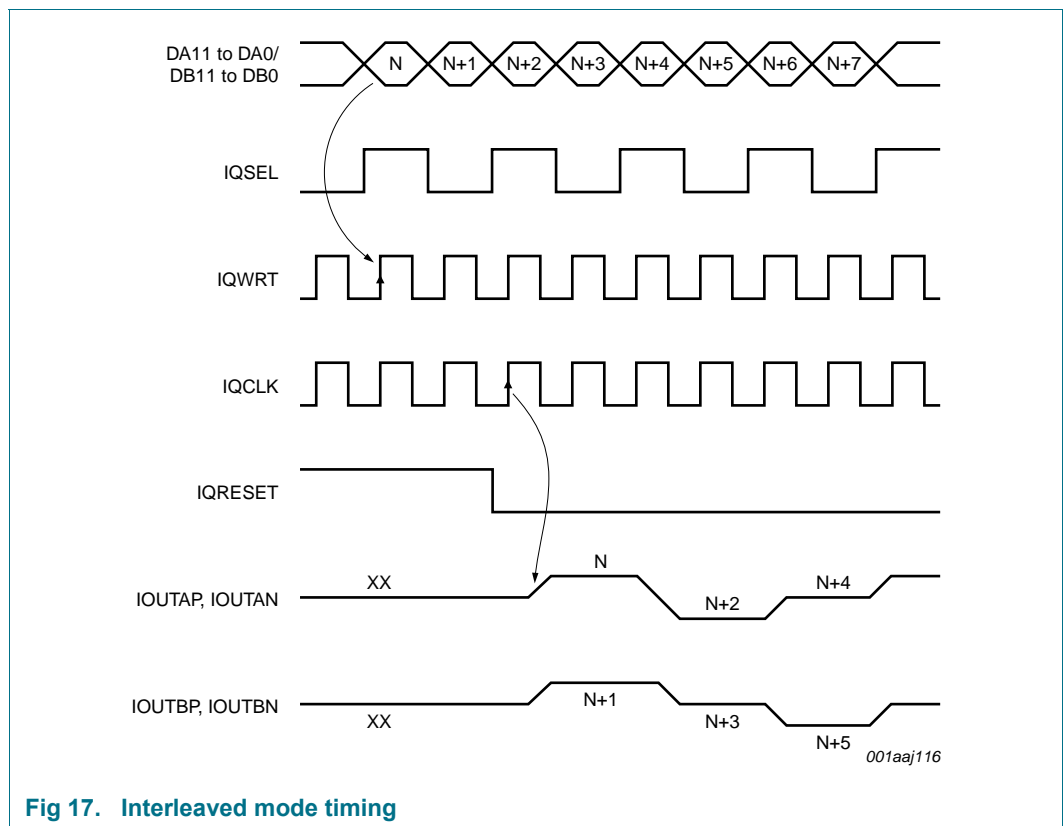


Fig 17. Interleaved mode timing



### 10.3 Timing

The DAC1201D125 can operate at an update rate up to 125 Msp/s. This generates an input data rate of 125 MHz in Dual-port mode and 250 MHz in Interleaved mode. The timing of the DAC1201D125 is shown in Figure 18.

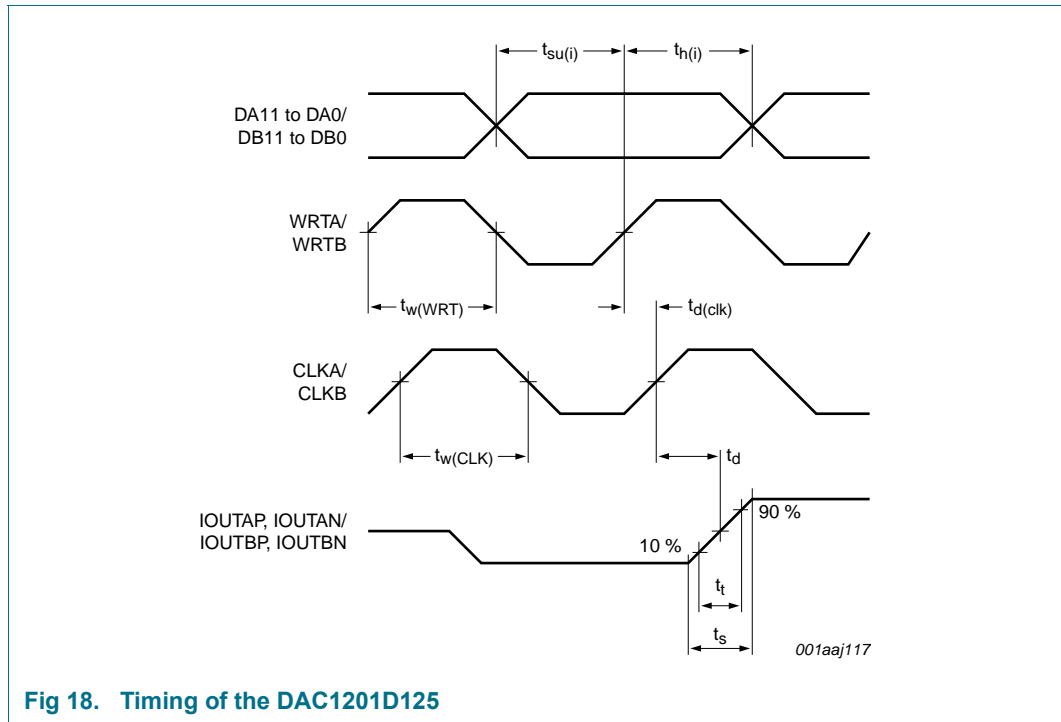


Fig 18. Timing of the DAC1201D125

The typical performances are measured at 50 % duty cycle but any timing within the limits of the characteristics will not alter the performance.

- A configuration resulting in the same timing for the signals WRTA/WRTB and CLKA/CLKB, can be achieved either by synchronizing them or by connecting them together.
- The rising edge of the CLKA/CLKB signal can also be placed in a range from half a period in front of the rising edge of the WRTA/WRTB signal to half a period minus 1 ns after the rising edge of the WRTA/WRTB signal.

A typical set-up time of 0 ns and a hold time of 0.6 ns enables the DAC1201D125 to be easily integrated into any application.

### 10.4 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{O(fs)} = I_{IOUTP} + I_{IOUTN} \tag{1}$$

The output current depends on the digital input data:

$$I_{IOUTP} = I_{O(fs)} \times \left( \frac{DATA}{4096} \right) \quad I_{IOUTN} = I_{O(fs)} \times \left( \frac{(4095 - DATA)}{4096} \right)$$

Table 7 shows the output current as a function of the input data, when  $I_{O(fs)} = 20 \text{ mA}$ .

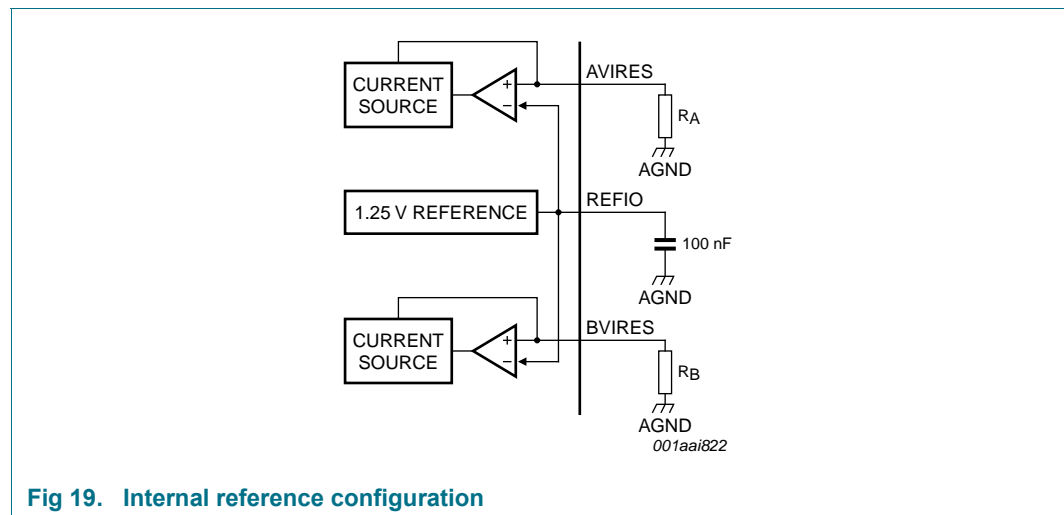
**Table 7. DAC transfer function**

Data	DA11/DB11 to DA0/DB0	IOUTAP/IOUTBP	IOUTAN/IOUTBN
0	0000 0000 0000	0 mA	20 mA
...	...	...	...
2047	1000 0000 0000	10 mA	10 mA
...	...	...	...
4095	1111 1111 1111	20 mA	0 mA

### 10.5 Full-scale current adjustment

The DAC1201D125 integrates one 1.25 V reference and two current sources to adjust the full-scale current in both DACs.

The internal reference configuration is shown in Figure 19.



**Fig 19. Internal reference configuration**

The bias current is generated by the output of the internal regulator connected to the inverting input of the internal operational amplifiers. The external resistors  $R_A$  and  $R_B$  are connected to pins AVIRES and BVIRES, respectively. This configuration is optimal for temperature drift compensation because the band gap can be matched with the voltage on the feedback resistors.

The relationship between full-scale output current ( $I_{O(fs)}$ ) at the output of channel A or channel B and the resistor is:

$$I_{O(fs)} = \frac{24V_{REFIO}}{R_A} \tag{2}$$

The output current of the two DACs is typically fixed at 20 mA when both resistors  $R_A$  and  $R_B$  are set to 1.5 kΩ. The operational range of DAC1201D125 is from 2 mA to 20 mA.

It is recommended to decouple pin REFIO using a 100 nF capacitor.

An external reference can also be used for applications requiring higher accuracy or precise current adjustment. Due to the high input impedance of pin REFIO, applying an external source disables the band gap.

### 10.6 Gain control

Table 8 shows how to select the different gain control modes.

**Table 8. Gain control**

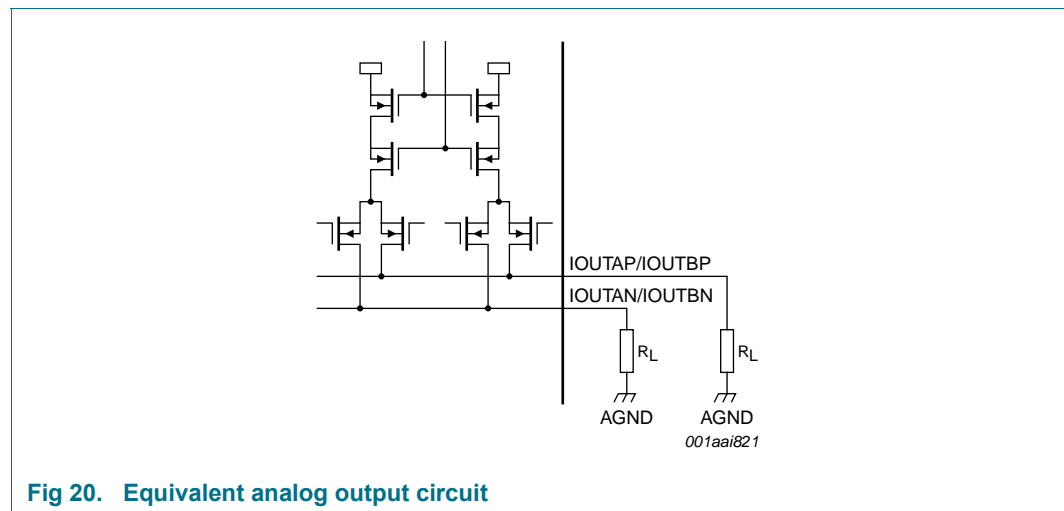
<b>GAINCTRL</b>	<b>Mode</b>	<b>DAC A full-scale control</b>	<b>DAC B full-scale control</b>
LOW	independent gain control	AVIRES	BVIRES
HIGH	common gain control	AVIRES	AVIRES

In Independent gain mode, both full-scale currents can be adjusted independently using resistors  $R_A$  on pin AVIRES and  $R_B$  on pin BVIRES.

In Common gain mode, the full-scale current is adjusted with resistor  $R_A$  on pin AVIRES and divided by two in both DACs.

### 10.7 Analog outputs

See Figure 20 for the analog output circuit of one DAC. This circuit consists of a parallel combination of PMOS current sources and associated switches for each segment.



**Fig 20. Equivalent analog output circuit**

Cascode source configuration enables the output impedance of the source to be increased, thus improving the dynamic performance by reducing distortion.

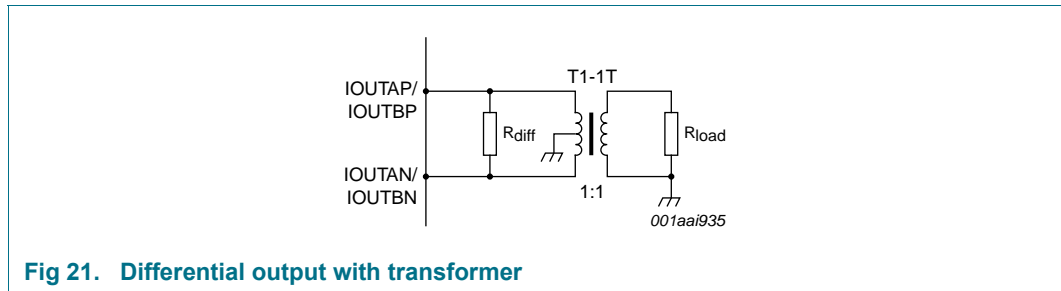
The DAC1201D125 can be used with either:

- a differential output, coupled to a transformer (or operational amplifier) to reduce even-order harmonics and noise
- a single-ended output for applications requiring unipolar voltage

A typical configuration is to use a 1 V p-p level on each output IOUTAP/IOUTBP and IOUTAN/IOUTBN. Several combinations can be used but they must respect the voltage compliance range.

**10.7.1 Differential output using transformer**

The use of a differential-coupled transformer output (see Figure 21) provides optimum distortion performance, and it helps to match the impedance and provides electrical isolation.

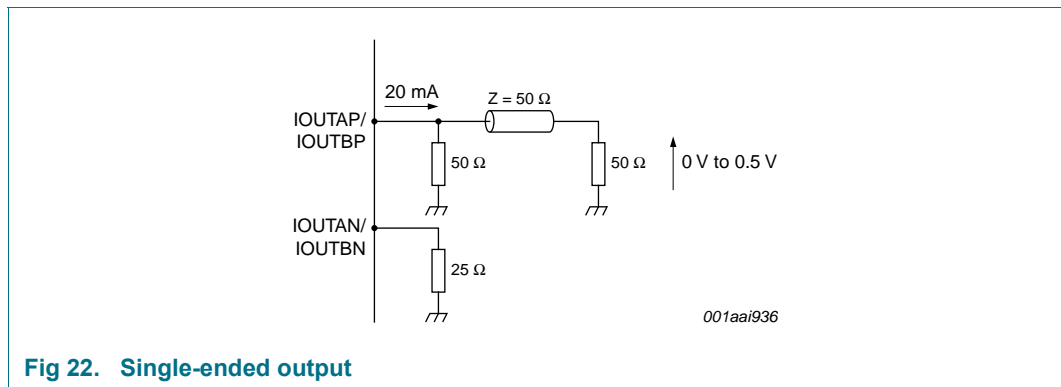


**Fig 21. Differential output with transformer**

The center tap is grounded to allow the DC current flow to/from both outputs. If the center tap is open, the differential resistor must be replaced by two resistors connected to ground.

**10.7.2 Single-ended output**

Using a single load resistor on one current output will provide a unipolar output range, typically from 0 V to 0.5 V with a 20 mA full-scale current at a 50 Ω load.



**Fig 22. Single-ended output**

The resistor on the other current output is 25 Ω.

**10.8 Power-down function**

The DAC1201D125 has a power-down function to reduce the power consumption when it is not active.

**Table 9. Power-down**

PWD	Device function	Power dissipation (typ)
LOW	active	185 mW
HIGH	not active	16.5 mW

## 10.9 Alternative devices

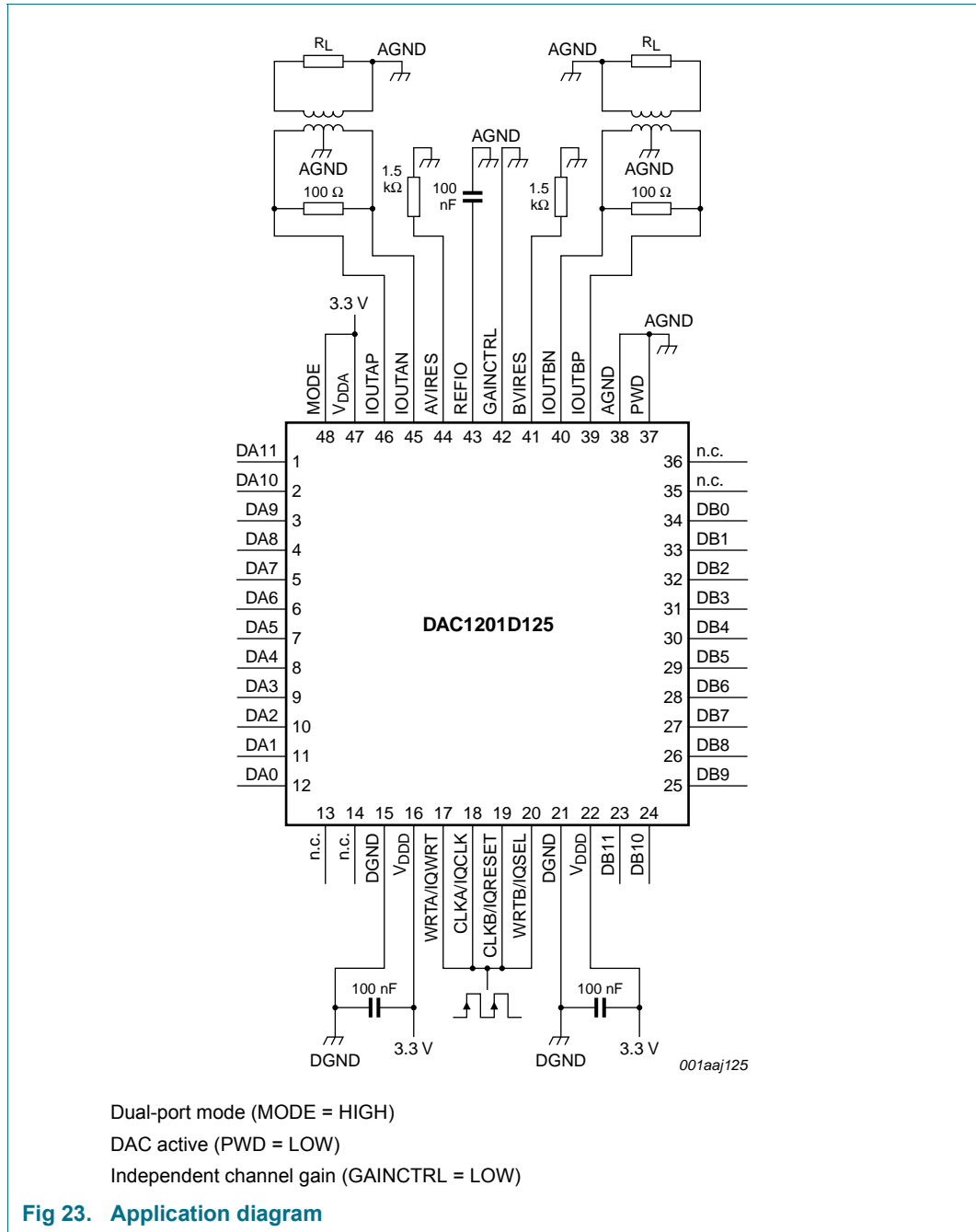
The following alternative devices are also available.

**Table 10. Alternative devices**

*Pin compatible*

Type number	Description	Sampling frequency
DAC1001D125	dual 10-bit DAC	up to 125 Msps
DAC1401D125	dual 14-bit DAC	up to 125 Msps

## 10.10 Application diagram



### 11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

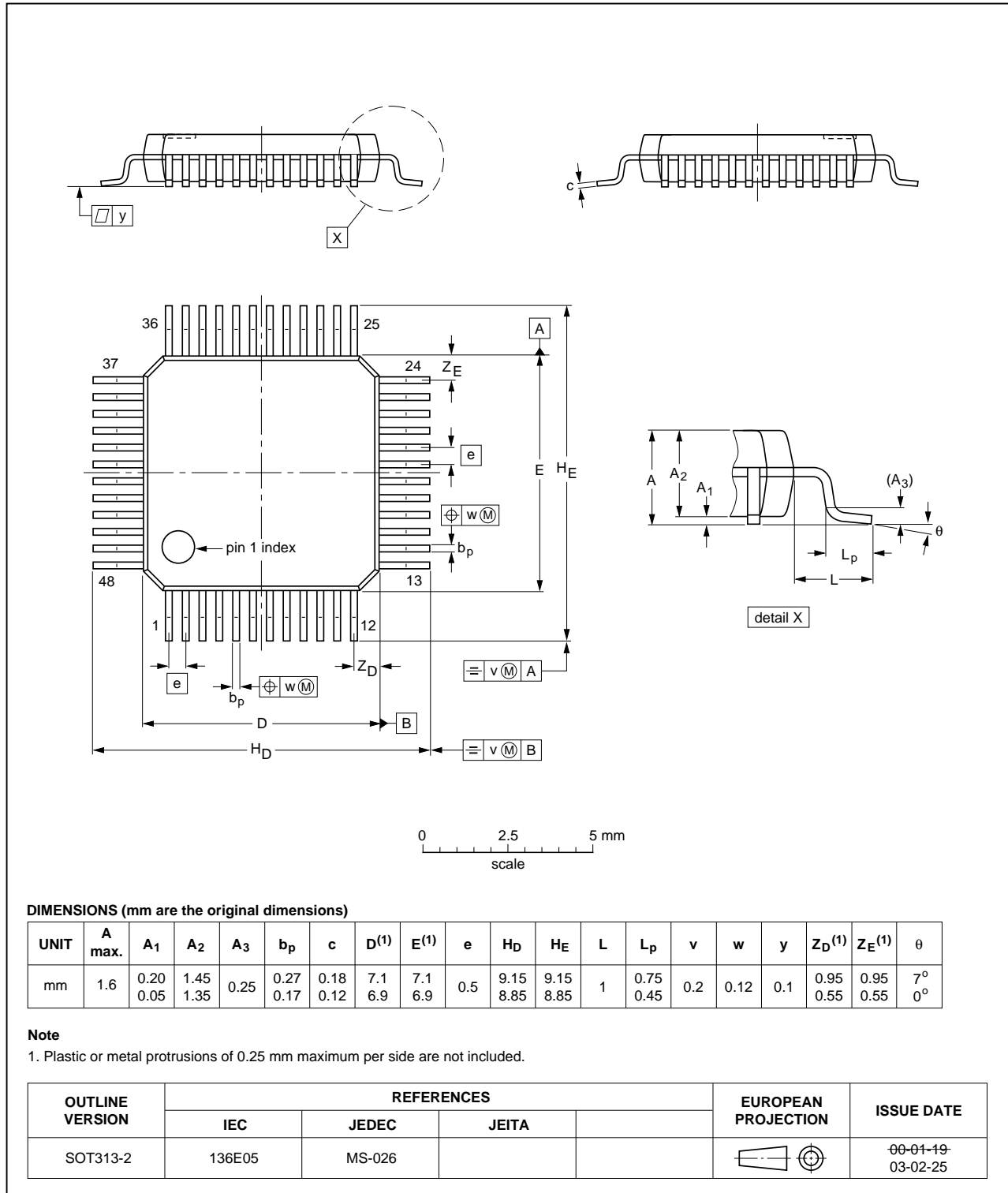


Fig 24. Package outline SOT313-2 (LQFP48)

## 12. Abbreviations

Table 11. Abbreviations

Acronym	Description
DNL	Differential Non-Linearity
dBFS	decibel Full-Scale
IF	Intermediate Frequency
INL	Integral Non-Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
PMOS	Positive-channel Metal-Oxide Semiconductor
SFDR	Spurious-Free Dynamic Range



## 13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1201D125 v.3	20120702	Product data sheet	-	DAC1201D125 v.2
DAC1201D125 v.2	20120127	Product data sheet	-	DAC1201D125 v.1
Modifications:	<ul style="list-style-type: none"><li>• Table 4 “Thermal characteristics” has been updated.</li><li>• Section 10.6 “Gain control” has been updated.</li></ul>			
DAC1201D125 v.1	20081127	Product data sheet	-	-

## 14. Contact information

For more information or sales office addresses, please visit: <http://www.idt.com>

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