

TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

## SSM3K35CT

○ High-Speed Switching Applications

○ Analog Switch Applications

- 1.2-V drive
- Low ON-resistance :  $R_{on} = 20 \Omega$  (max) (@ $V_{GS} = 1.2$  V)  
 $R_{on} = 8 \Omega$  (max) (@ $V_{GS} = 1.5$  V)  
 $R_{on} = 4 \Omega$  (max) (@ $V_{GS} = 2.5$  V)  
 $R_{on} = 3 \Omega$  (max) (@ $V_{GS} = 4.0$  V)

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

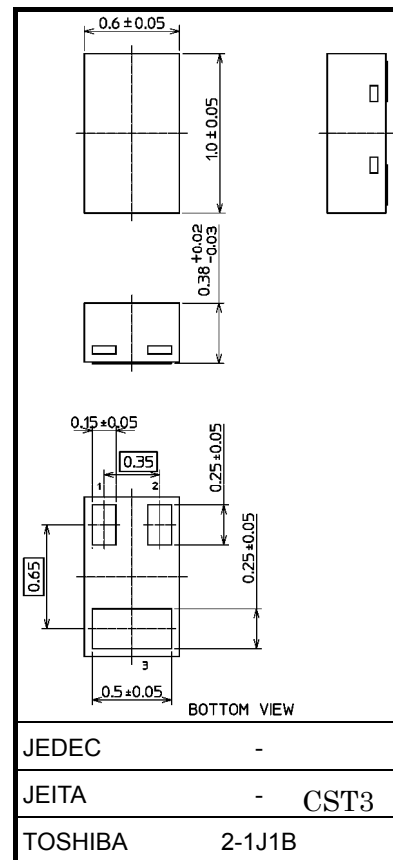
Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	20	V
Gate-source voltage		$V_{GSS}$	$\pm 10$	V
Drain current	DC	$I_D$	180	mA
	Pulse	$I_{DP}$	360	
Drain power dissipation		$P_D$ (Note 1)	100	mW
Channel temperature		$T_{ch}$	150	$^\circ\text{C}$
Storage temperature		$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

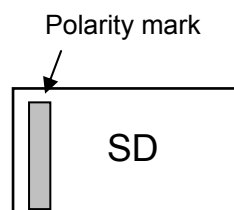
Note 1: Mounted on an FR4 board  
 (10 mm  $\times$  10 mm  $\times$  1.0 mm, Cu Pad: 100 mm<sup>2</sup>)

Unit: mm

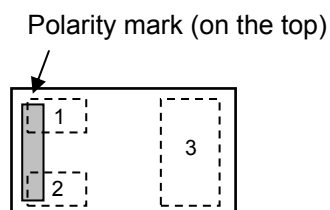


Weight: 0.75 mg (typ.)

### Marking (top view)

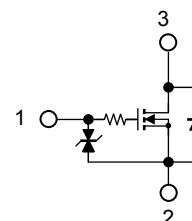


### Pin Condition (top view)



1. Gate
  2. Source
  3. Drain
- \*Electrodes: on the bottom

### Equivalent Circuit (top view)



Start of commercial production  
 2008-02

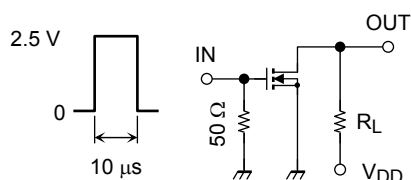
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1 \text{ mA}, V_{GS} = 0 \text{ V}$	20	—	—	V
Drain cutoff current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$	0.4	—	1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}, I_D = 50 \text{ mA}$ (Note 2)	115	—	—	mS
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = 50 \text{ mA}, V_{GS} = 4 \text{ V}$ (Note 2)	—	1.5	3	$\Omega$
		$I_D = 50 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note 2)	—	2	4	
		$I_D = 5 \text{ mA}, V_{GS} = 1.5 \text{ V}$ (Note 2)	—	3	8	
		$I_D = 5 \text{ mA}, V_{GS} = 1.2 \text{ V}$ (Note 2)	—	5	20	
Input capacitance	$C_{iss}$	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	9.5	—	pF
Reverse transfer capacitance	$C_{rss}$		—	4.1	—	
Output capacitance	$C_{oss}$		—	9.5	—	
Switching time	Turn-on time	$V_{DD} = 3 \text{ V}, I_D = 50 \text{ mA},$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}$	—	115	—	ns
	Turn-off time		—	300	—	
Drain-source forward voltage	$V_{DSF}$	$I_D = -180 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 2)	—	-0.9	-1.2	V

Note 2: Pulse test

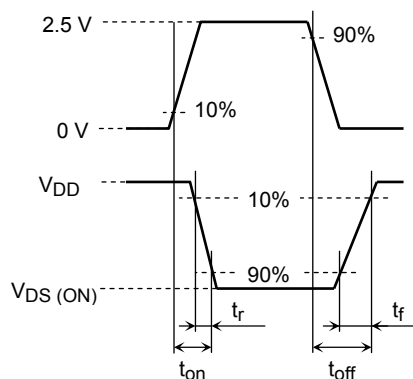
## Switching Time Test Circuit

### (a) Test Circuit



$V_{DD} = 3 \text{ V}$   
Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5 \text{ ns}$   
( $Z_{out} = 50 \Omega$ )  
Common Source  
 $T_a = 25^\circ\text{C}$

### (b) $V_{IN}$



### (c) $V_{OUT}$

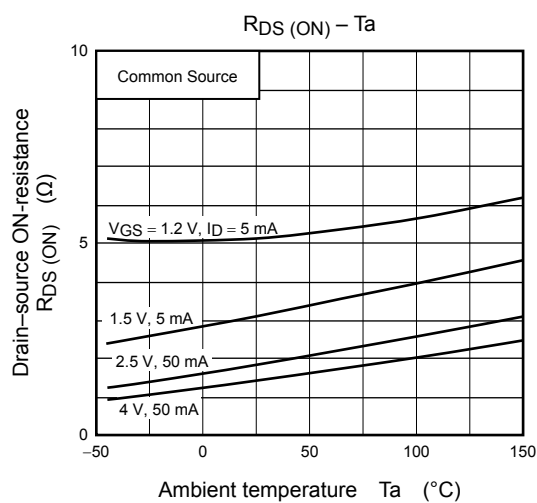
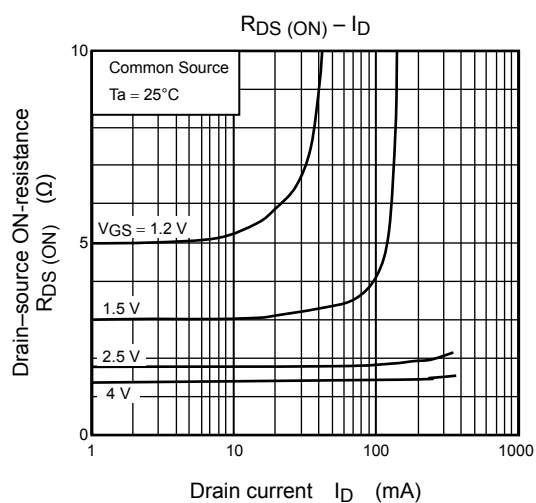
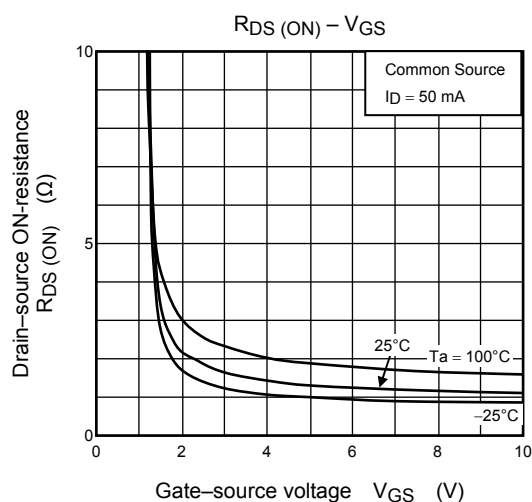
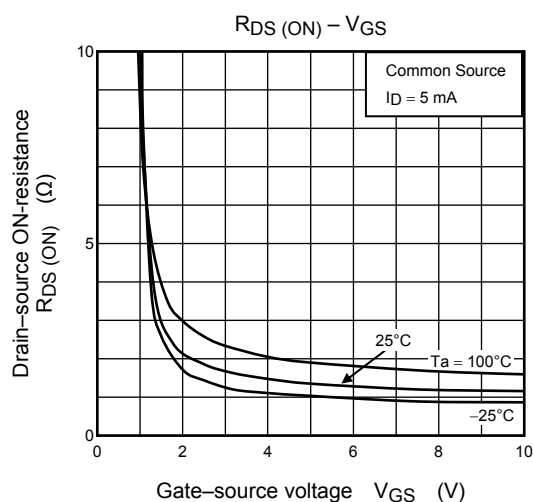
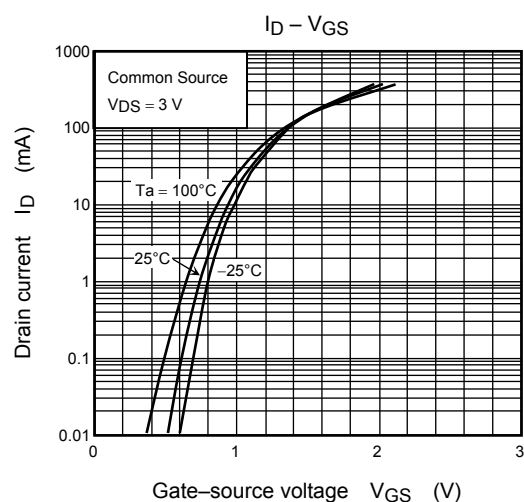
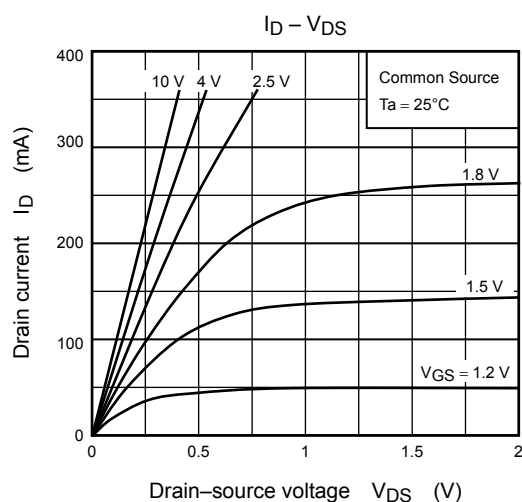
## Usage Considerations

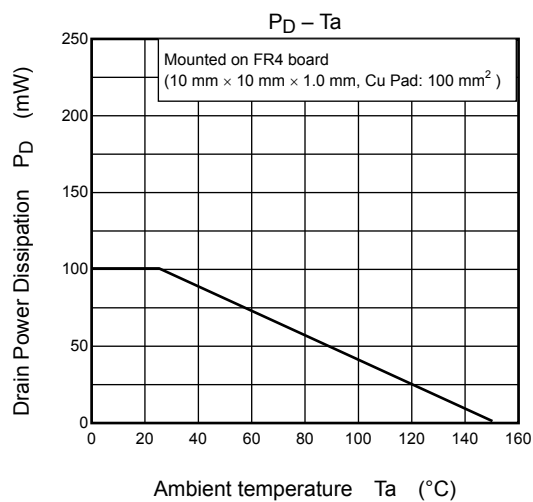
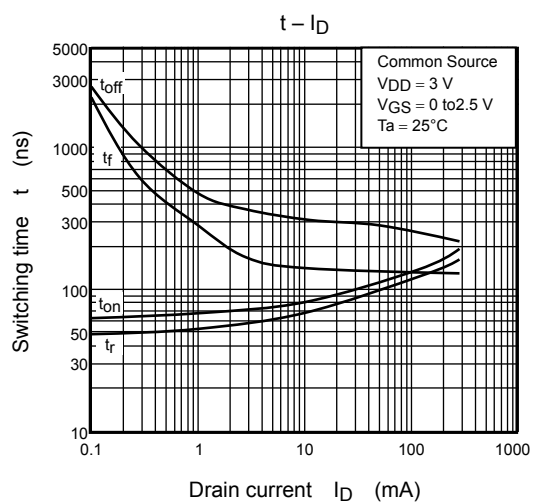
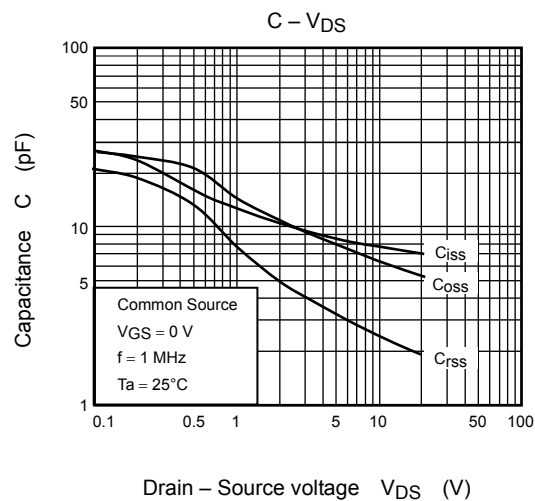
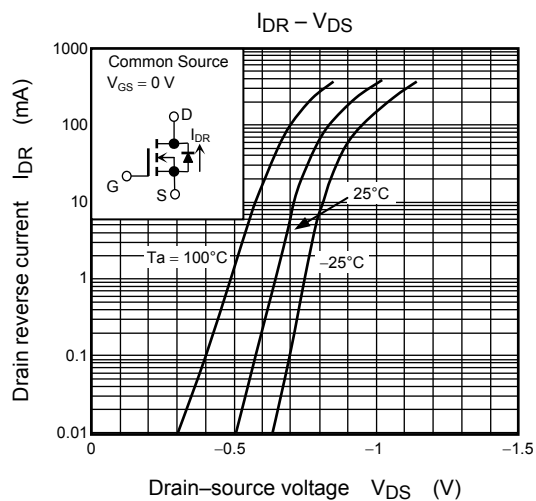
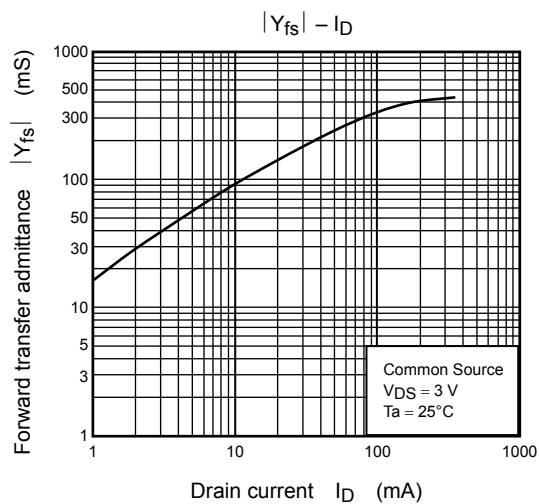
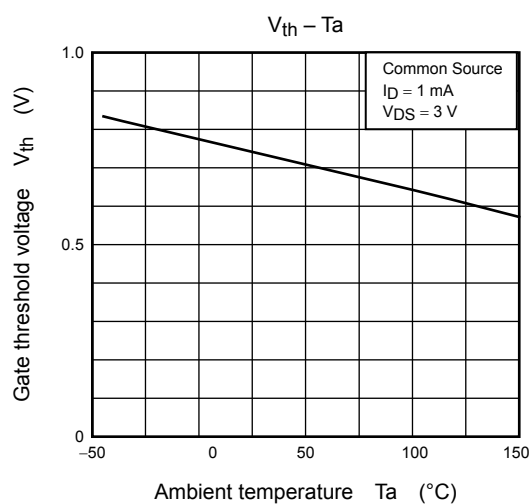
Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be below (1 mA for the SSM3K35CT). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

Take this into consideration when using the device.

## Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.





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