TEXAS INSTRUMENTS
TPS565242, TPS565247
SLUSEN1A – FEBRUARY 2022 – REVISED APRIL 2022

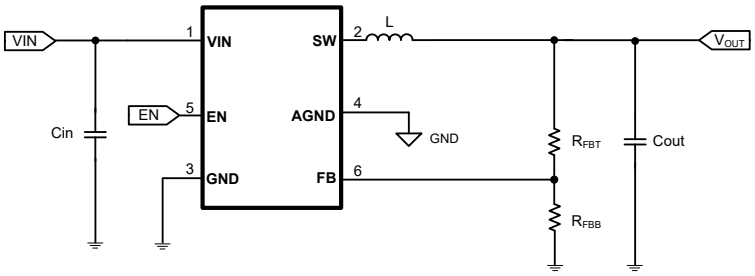
TPS56524x 3-V to 16-V Input Voltage, 5-A Synchronous Buck Converter in a SOT-563 Package

1 Features

- Configured for a wide range of applications
  - 3-V to 16-V input voltage range
  - 0.6-V to 7-V output voltage range
  - 0.6-V reference voltage
  - ±1% reference accuracy at 25°C
  - ±1.5% reference accuracy at –40°C to 125°C
  - Integrated 28.2-mΩ and 15.1-mΩ R_{DSON} FET
  - 120-µA low quiescent current
  - 600-kHz switching frequency
  - Supports maximum 98% duty cycle operation
  - Precision EN threshold voltage
  - 1.39-ms fixed typical soft-start time
- Ease of use and small solution size
  - Eco-mode (TPS565242) and FCCM mode at light loading (TPS565247)
  - Part of a full P2P family including solutions for 4 A, 5 A, and 6 A and FCCM/ECO operation
  - D-CAP3™ control topology
  - Support start-up with prebiased output
  - Non-latch for OV/OT/UVLO protection
  - Hiccup mode for UV protection
  - Cycle-by-cycle OC and NOC limit
  - 6-pin SOT-563 package
- Create a custom design using the TPS565242 with the WEBENCH® Power Designer
- Create a custom design using the TPS565247 with the WEBENCH® Power Designer

2 Applications

- LCD TV, STB and DVR, streaming media player
- IP network camera, video doorbell, building security gateway
- WLAN/Wi-Fi access point, small business router, rack server



Simplified Schematic

3 Description

The TPS56524x is simple, easy-to-use, high power density, high efficiency synchronous buck converter. The device supports input voltage ranging from 3 V to 16 V and up to 5-A continuous current with a SOT-563 package.

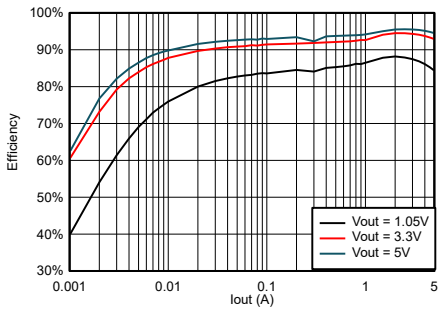
The TPS56524x uses D-CAP3 topology to provide a fast transient response and support low-ESR output capacitors with no requirement for external compensation. It has two grounds, GND and AGND, which should be connected together for optimal thermal performance. AGND also provides a good load and line regulation. The device can support up to 98% duty operation.

The TPS565242 operates in Eco-mode, which maintains high efficiency during light loading. The TPS565247 operates in FCCM mode, which keeps the same frequency and lower output ripple during all load conditions. It integrates complete protection through OVP, OCP, UVLO, OTP, and UVP with hiccup. The device is available in 1.6-mm × 1.6-mm SOT-563 package and has an optimized pinout for easy PCB layout. The junction temperature is specified from –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS565242	SOT-563 (6)	1.60 mm × 1.60 mm
TPS565247		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



TPS565242, Efficiency at V_{IN} = 12 V

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4 Revision History

Changes from Revision * (February 2022) to Revision A (April 2022)	Page
• Changed marketing status from Advance Information to initial release.	1

5 Pin Configuration and Functions

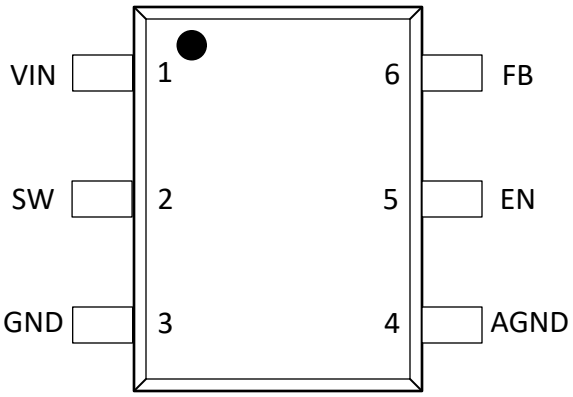


Figure 5-1. 6-Pin SOT-563 DRL Package (Top View)

Table 5-1. Pin Functions

Pin		Type[1]	Description
Name	No.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between the high-side NFET and low-side NFET
GND	3	—	Ground pin source terminal of the low-side power NFET as well as the ground terminal for controller circuit
AGND	4	—	Ground of internal analog circuitry. Connect AGND to the GND plane.
EN	5	I	Enable input to converter. Driving EN high enables the converter.
FB	6	I	Converter feedback input. Connect to the output voltage with a feedback resistor divider.

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	18	V
	FB, EN	–0.3	6	
	AGND, PGND	–0.3	0.3	
Output voltage	SW	–2	18	V
	SW (< 20 ns)	–6.5	20	
Operating junction temperature range, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP157 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	3		16	V
	FB, EN	–0.1		5.5	
	AGND, PGND	–0.1		0.1	
Output voltage	SW	–1		16	V
	SW (< 20 ns)	–6		18	
Output current	IO	0		6	A
T_J	Operating junction temperature	–40		125	°C
T_{stg}	Storage temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRL (SOT-563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	°C/W
$R_{\theta JA\_effective}$ (2)	Junction-to-ambient thermal resistance on EVM board	58	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	16.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) This $R_{\theta JA\_effective}$ is tested on TPS565242EVM board (2 layer, copper thickness of top and bottom layer are 2 oz) at V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 5A , T_A = 25°C.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input voltage range	V_{IN}	3		16	V
I_{VIN}	VIN supply current	No load, V_{EN} = 5 V, V_{FB} = 0.65 V, non-switching, ECO version		120		µA
		No load, V_{EN} = 5 V, V_{FB} = 0.65 V, non-switching, FCCM version		400		µA
I_{INSDN}	VIN shutdown current	No load, V_{EN} = 0 V		2		µA
UVLO						
UVLO	VIN undervoltage lockout	Wake-up VIN voltage	2.75	2.92	3	V
UVLO	VIN undervoltage lockout	Shutdown VIN voltage	2.6	2.72	2.9	V
UVLO	VIN undervoltage lockout	Hysteresis VIN voltage		200		mV
FEEDBACK VOLTAGE						
V_{REF}	FB voltage	T_J = 25°C	594	600	606	mV
V_{REF}	FB voltage	T_J = –40°C to 125°C	591	600	609	mV
MOSFET						
$R_{DS\ (ON)HI}$ (1)	High-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} ≥ 5 V		28.2		mΩ
	High-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} = 3 V		30.1		mΩ
$R_{DS\ (ON)LO}$	Low-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} ≥ 5 V		15.1		mΩ
$R_{DS\ (ON)LO}$	Low-side MOSFET $R_{DS(ON)}$	T_J = 25°C, V_{VIN} = 3 V		16.1		mΩ
I_{OCL_LS}	Overcurrent threshold	Valley current setpoint	5.3	6.9	8.5	A
I_{NOCL}	Negative overcurrent threshold		2	3.4	4.2	A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	T_J = 25°C, V_{VOUT} = 3.3 V		600		kHz
$T_{ON(MIN)}$ (1)	Minimum on time	T_J = 25°C		50		ns
$T_{OFF(MIN)}$ (1)	Minimum off time	V_{FB} = 0.5 V		100		ns
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN threshold high level		1.07	1.18	1.33	V
$V_{EN(OFF)}$	EN threshold low level		0.95	1	1.2	V
V_{ENHYS}	EN hystersis			180		mV
REN1	EN pulldown resistor			2		MΩ
SOFT START						
t_{SS}	Internal soft-start time			1.39		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold		115%	120%	125%	
t_{OVPDLY}	OVP prop deglitch	T_J = 25°C		24		µs
V_{UVP}	UVP trip threshold		55%	60%	65%	
t_{UVPDLY}	UVP prop deglitch			256		µs
t_{UVPDEL}	Output hiccup delay relative to SS time	UVP detect		256		µs
t_{UVPEN}	Output hiccup enable delay relative to SS time	UVP detect		13		ms
THERMAL PROTECTION						
T_{OTP} (2)	OTP trip threshold			155		°C

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{OTPHSY} (2)	OTP hysteresis			20		°C

(1) Specified by design
(2) Not production tested

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

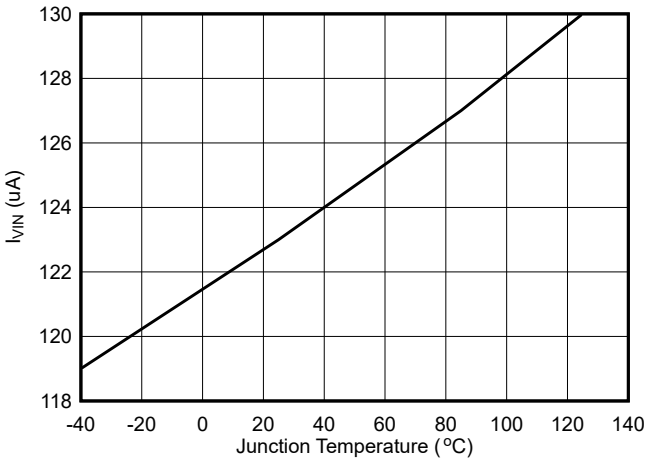


Figure 6-1. TPS565242 Quiescent Current

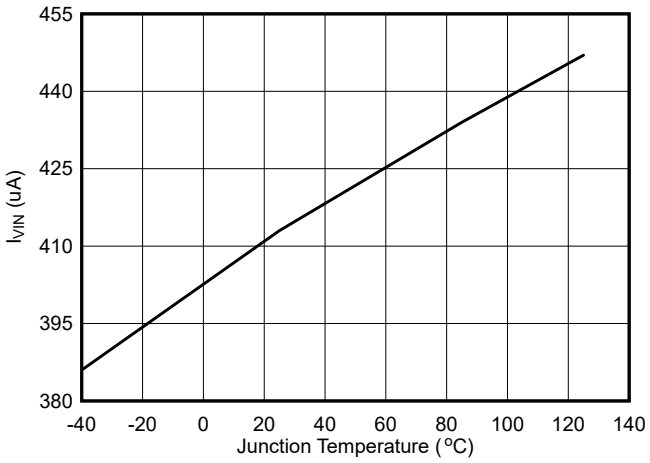


Figure 6-2. TPS565247 Quiescent Current

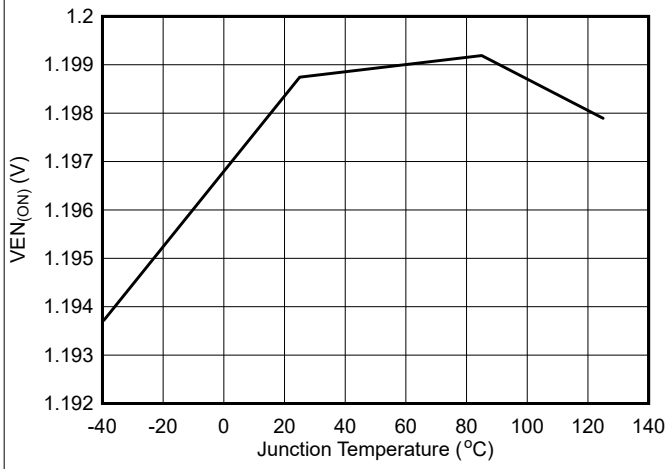


Figure 6-3. Enable On Threshold Voltage

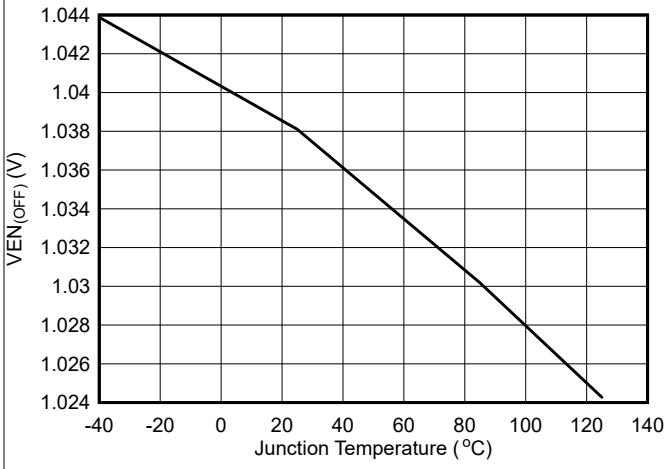


Figure 6-4. Enable Off Threshold Voltage

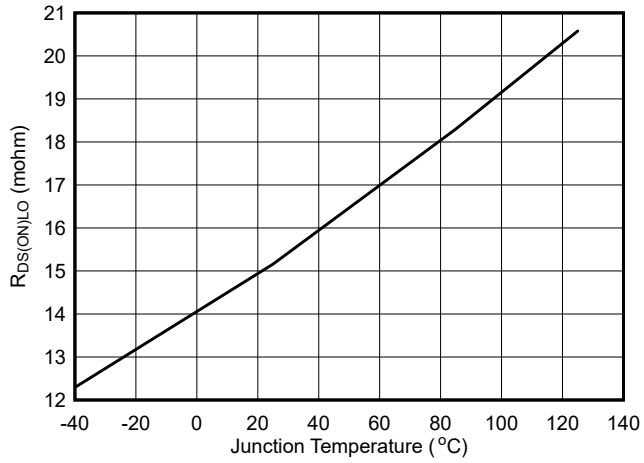


Figure 6-5. Low-Side $R_{DS(ON)}$

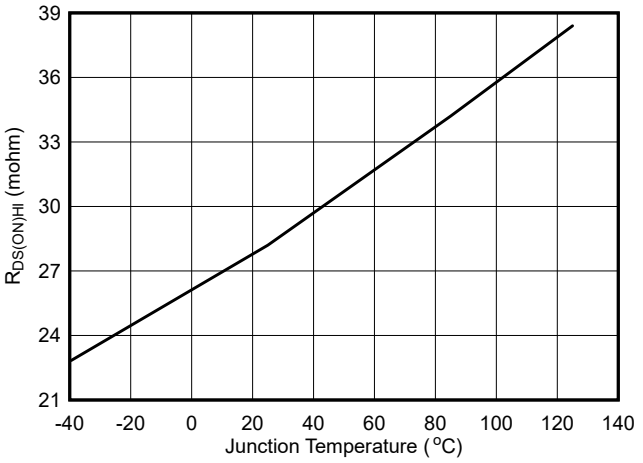


Figure 6-6. High-Side $R_{DS(ON)}$

6.6 Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

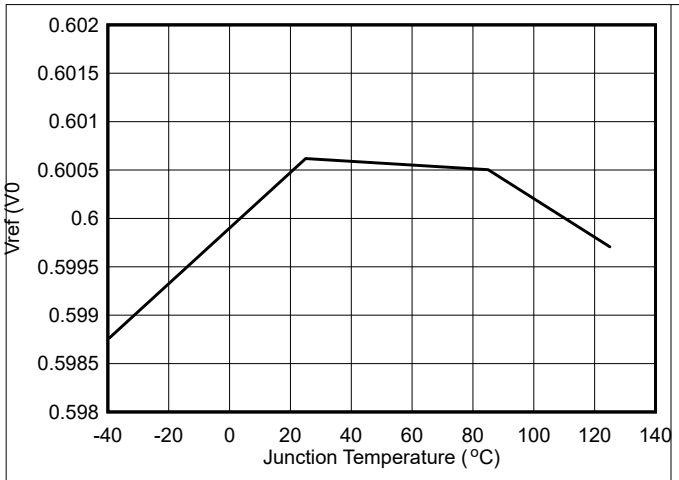


Figure 6-7. V_{REF} Voltage

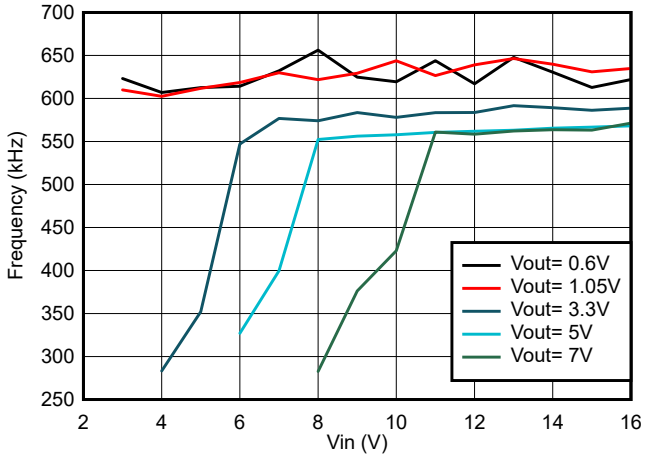


Figure 6-8. Frequency vs Input Voltage at 5-A Loading

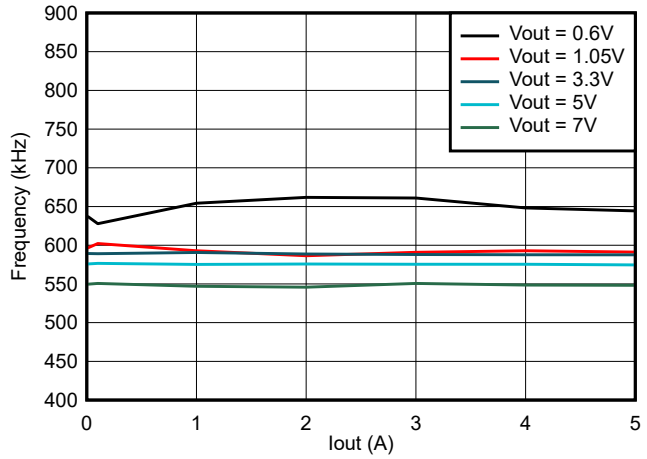


Figure 6-9. TPS565247 Frequency vs Loading

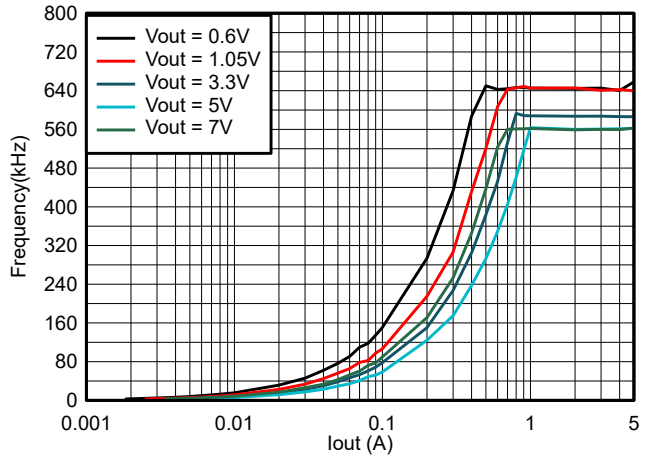


Figure 6-10. TPS565242 Frequency vs Loading

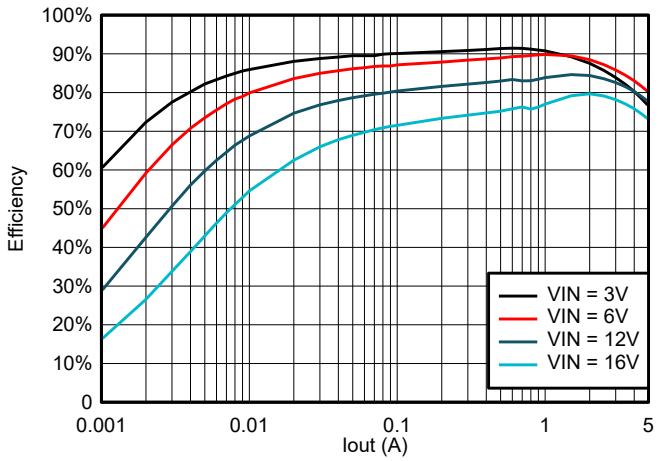


Figure 6-11. TPS565242 Efficiency at 0.6 V_{OUT} with a 0.82-µH Inductor

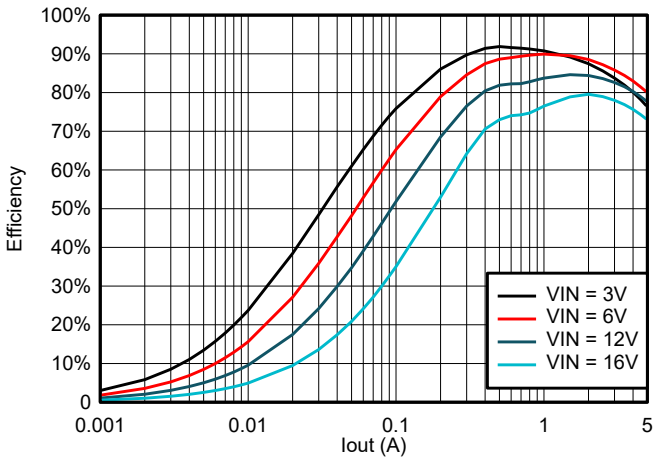


Figure 6-12. TPS565247 Efficiency at 0.6 V_{OUT} with a 0.82-µH Inductor

6.6 Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

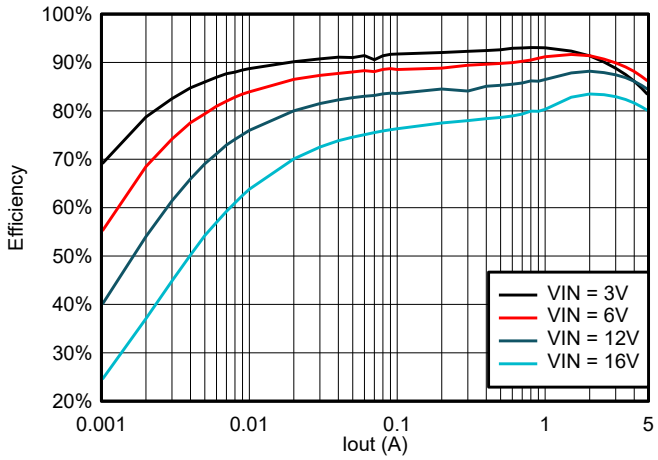


Figure 6-13. TPS565242 Efficiency at 1.05 V_{OUT} with a 1-µH Inductor

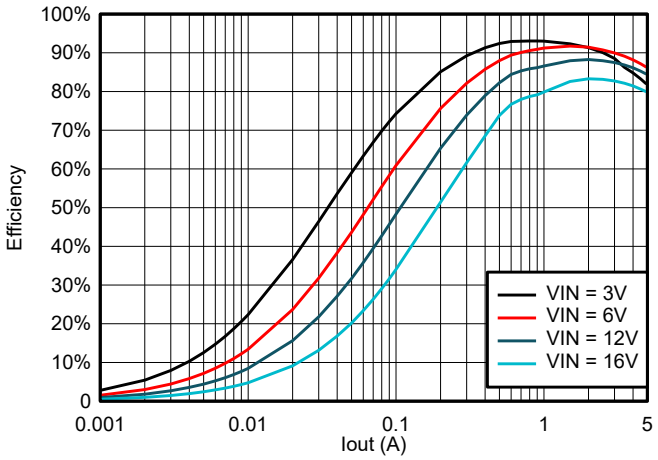


Figure 6-14. TPS565247 Efficiency at 1.05 V_{OUT} with a 1-µH Inductor

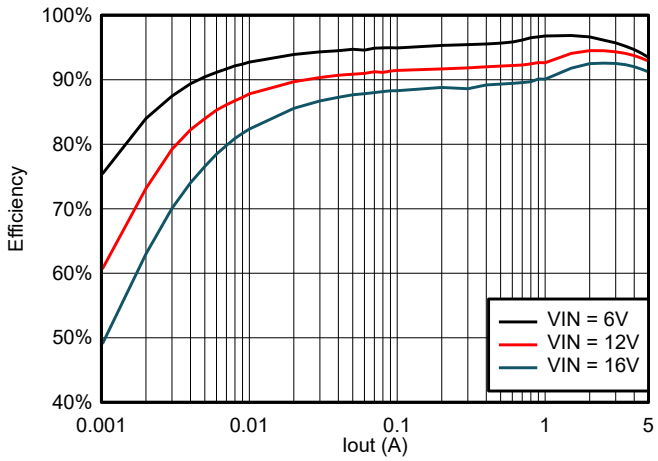


Figure 6-15. TPS565242 Efficiency at 3.3 V_{OUT} with a 2.2-µH Inductor

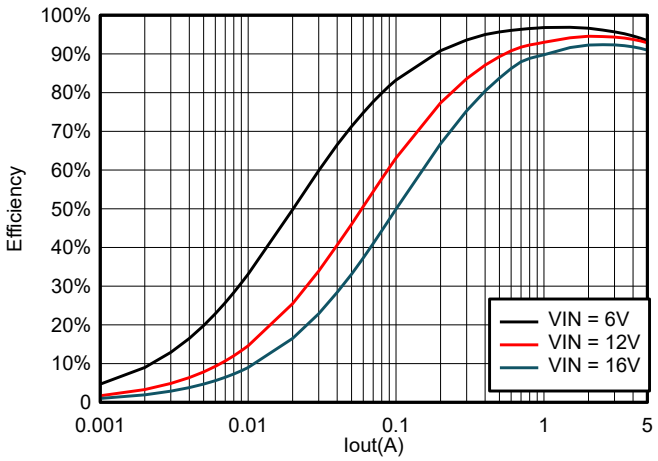


Figure 6-16. TPS565247 Efficiency at 3.3 V_{OUT} with a 2.2-µH Inductor

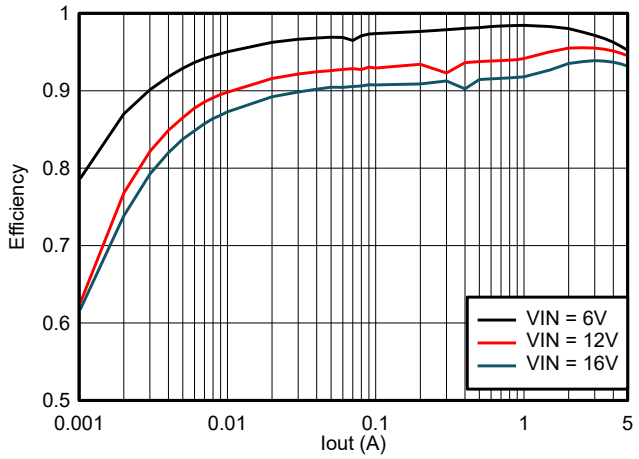


Figure 6-17. TPS565242 Efficiency at 5 V_{OUT} with a 2.2-µH Inductor

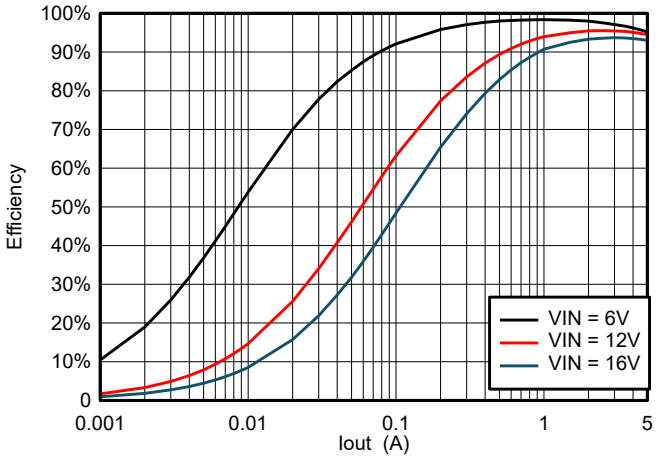


Figure 6-18. TPS565247 Efficiency at 5 V_{OUT} with a 2.2-µH Inductor

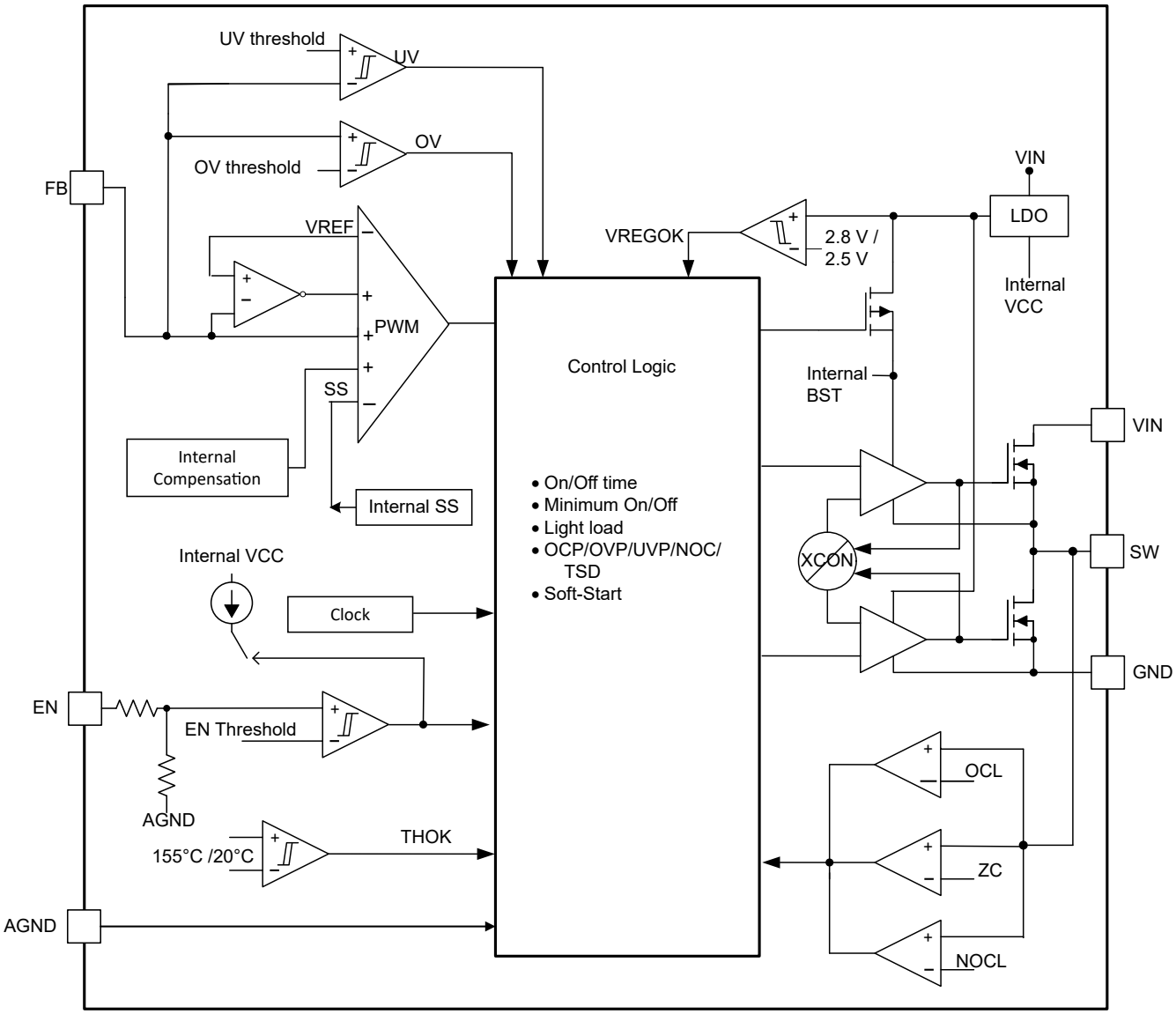
7 Detailed Description

7.1 Overview

The TPS56524x is a 5-A integrated FET and BST pin synchronous step-down buck converter that operates from 3-V to 16-V input voltage (V_{IN}) and 0.6-V to 7-V output voltage. This device also integrates the BST pin in an internal IC and adds one AGND pin. The device employs D-CAP3 topology that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition.

The Eco-mode version allows the TPS565242 to maintain high efficiency at light load. The FCCM version allows the TPS565247 to maintain a fixed switching frequency and lower output voltage ripple. The TPS56524x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3 Control

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3 mode control. The DCAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS56524x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multilayered ceramic capacitors (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

7.3.2 Eco-Mode Control

The TPS56524x is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current and keeps the light load efficiency high. The transition point to the light load operation, $I_{OUT(LL)}$ current, can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Prebiased Soft Start

The TPS56524x has an internal fixed soft start. The EN default status is low. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage, V_{FB}. This scheme makes sure that the converter ramps up smoothly into the regulation point.

7.3.4 Overvoltage Protection

The TPS56524x has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, OVP is triggered with a 24-µs deglitch time. Both the high-side MOSFET driver and the low-side MOSFET driver are turned off. When the overvoltage condition is removed, the device returns to switching.

7.3.5 Large Duty Operation

The TPS56524x can support large duty operations up to 98% by smoothly dropping down the switching frequency. When V_{IN} / V_{OUT} < 1.6 and V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make TON extended to implement the large duty operation and improve the performance of the load transient performance. Please refer frequency test waveform in Figure 6-18. The minimum switching frequency is limited to about 200 kHz.

7.3.6 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- On time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT}. If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it and the device shuts down after the UVP delay time (typically 256 µs) and restarts after the hiccup wait time (typically 13 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS565247 is a FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When the NOC condition is removed, the device returns to normal switching.

Because the TPS565247 is a FCCM mode port, if the inductance is so small that the device trigger NOC, it will cause output voltage to be higher than target value. The minimum inductance is identified as Equation 2.

$$L = \frac{V_{out} \times (1 - \frac{V_{out}}{V_{in}})}{2 \times Frequency \times NOC_{min}} \quad (2)$$

7.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.8 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Eco-Mode Operation

The TPS565242 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on

time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

7.4.2 FCCM Mode Control

The TPS565247 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (FSW) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is typical buck DC/DC converters. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 5 A. The following design procedure can be used to select component values for the TPS56524x. Alternately, the WEBENCH® software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in Figure 8-1 was developed to meet the requirements in Table 8-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

Figure 8-1 shows the TPS56524x 12-V input, 1.05-V output converter schematic.

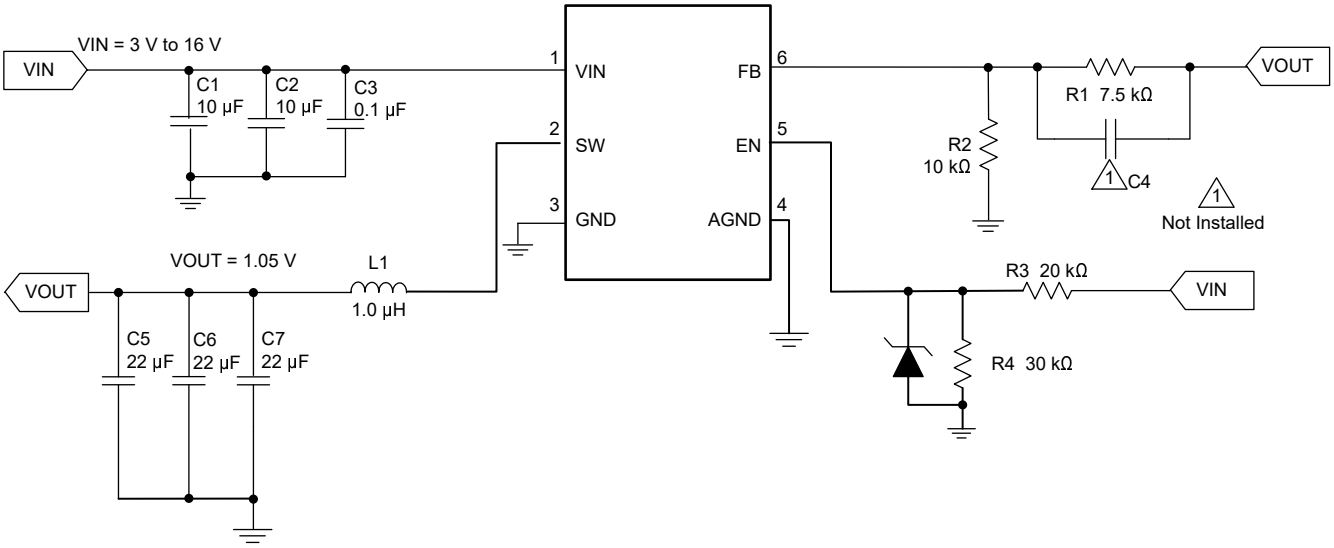


Figure 8-1. Schematic

8.2.1 Design Requirements

Table 8-1 shows the design parameters for this application.

Table 8-1. Design Parameters

Parameter	Example Value
Input voltage range	3 to 16 V
Output voltage	1.05 V
Transient response, 2.5-A load step	ΔVout = ±5%
Output ripple voltage	20 mV
Output current rating	5 A
Operating frequency	600 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS565242 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS565247 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 3 to calculate V_{OUT}.

To improve efficiency at very light loads, consider using larger value resistors because too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable. It is suggested to use a 10-kΩ resistor for R2 to start the design.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right) \tag{3}$$

8.2.2.3 Output Filter Selection

The LC filter used as the output filter has a double pole at Equation 4. In this equation, C_{OUT} should use its effective value after derating, not its nominal value.

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

For any control topology that is compensated internally, there is a range of the output filter it can support. At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops has a 180 degree drop. The internal ripple generation network introduces a

high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 66 kHz. The inductor and capacitor selected for the output filter is recommended that the double pole is located about 20 kHz, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (FSW).

Table 8-2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	Minimum L1 (µH)	Typical L1 (µH)	Maximum L1 (µH)	Minimum C_{OUT} (µF)	Typical C_{OUT} (µF)	Maximum C_{OUT} (µF)	CFF (pF)
0.6	0	10.0	0.42	0.82	2.2	44	88	220	—
1.05	7.5	10.0	0.68	1/1.5	2.2	44	66	220	—
1.8	20.0	10.0	1	1.5	2.2	44	66	220	10–470
2.5	95.0	30.0	1.2	2.2	4.7	44	66	220	10–470
3.3	135.0	30.0	1.5	2.2	4.7	44	66	220	10–470
5	220.0	30.0	2.2	2.2/3.3	6.8	44	66	220	10–470
7	320.0	30.0	2.2	3.3	6.8	44	66	220	10–470

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using Equation 5, Equation 6, and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (5)$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \quad (6)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \quad (7)$$

For this design example, the calculated peak current is 5.8 A and the calculated RMS current is 5.02 A. The inductor used is WE744311100 with 8-A saturation current and 15-A rated current.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56524x are intended for use with ceramic or other low-ESR capacitors. Use Equation 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (8)$$

For this design, four MuRata GRM21BR61A226ME44L 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.47 A and each output capacitor is rated for 4 A.

8.2.2.4 Input Capacitor Selection

The TPS56524x requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.3 Application Curves

The following data is tested with V_{IN} = 12 V, V_{OUT} = 1.05 V, T_A = 25°C, unless otherwise specified.

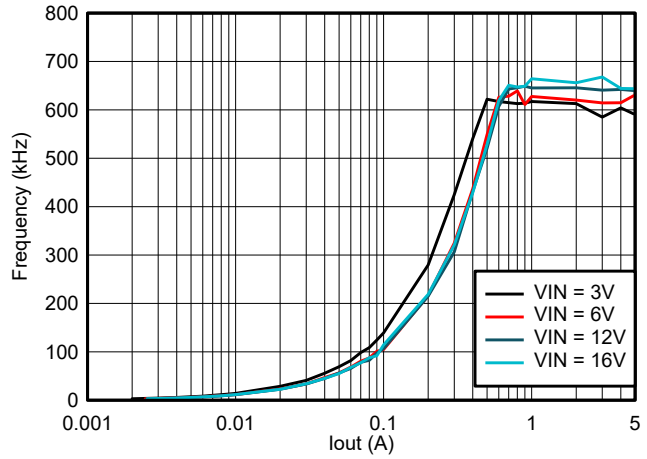


Figure 8-2. TPS565242 Frequency vs Loading

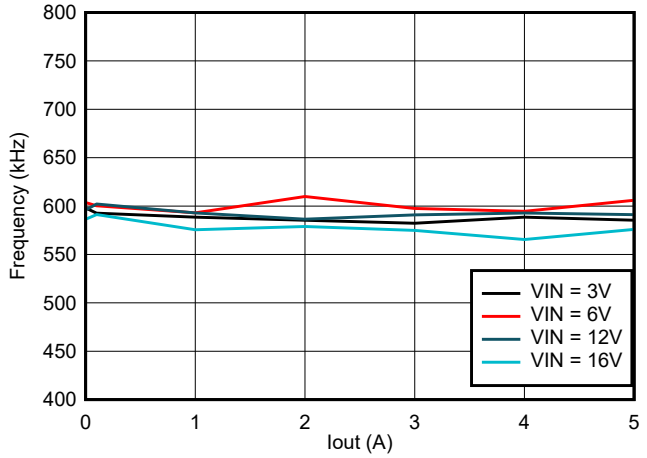


Figure 8-3. TPS565247 Frequency vs Loading

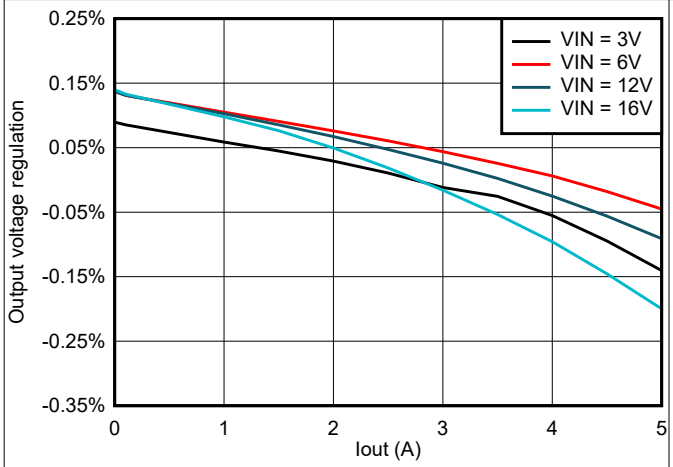


Figure 8-4. TPS565242 Load Regulation vs Loading

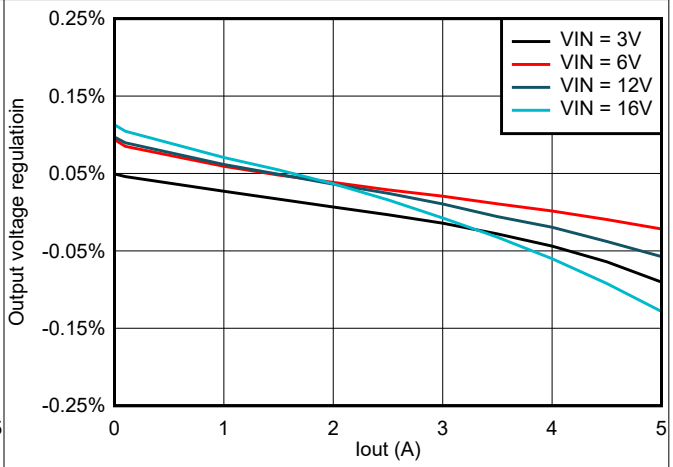


Figure 8-5. TPS565247 Load Regulation vs Loading

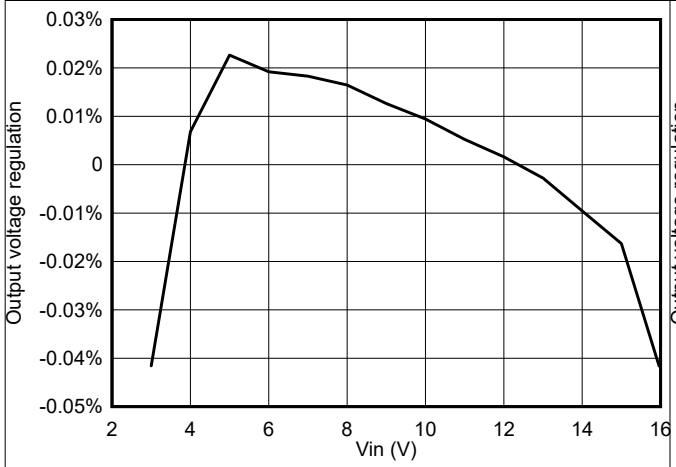


Figure 8-6. TPS565242 Line Regulation vs V_{IN} with 5-A Loading

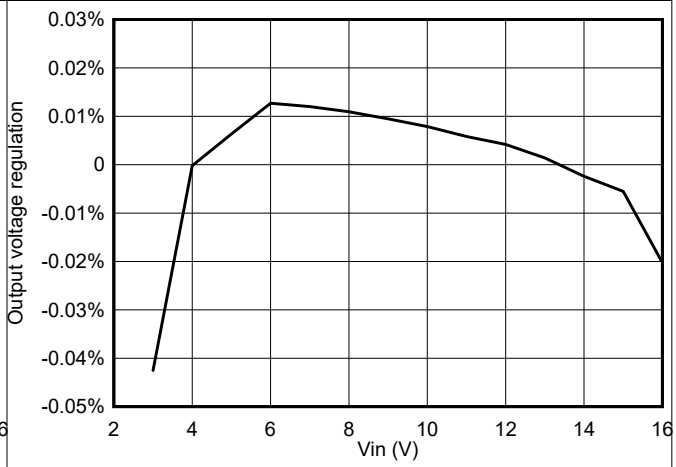


Figure 8-7. TPS565247 Line Regulation vs Loading with 5-A Loading

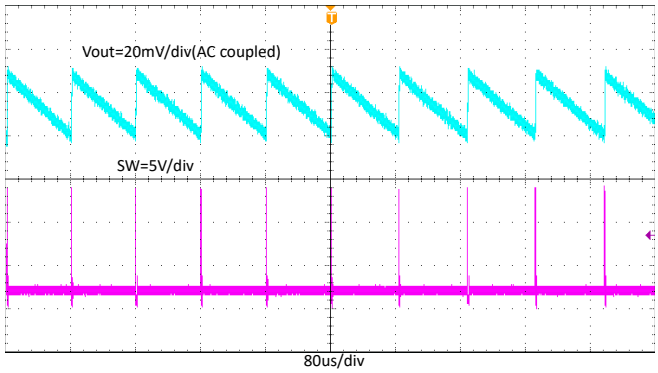


Figure 8-8. TPS565242 Output Voltage Ripple with 0.01-A Loading

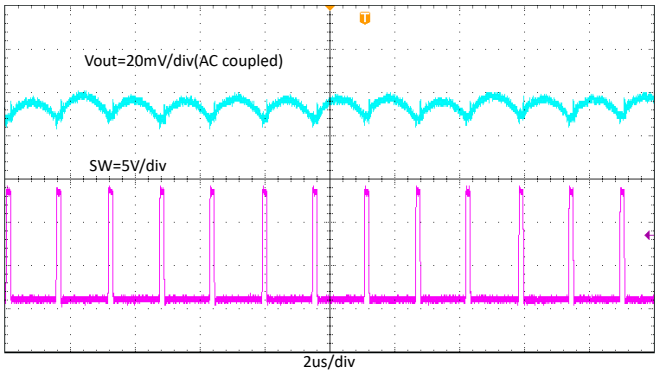


Figure 8-9. TPS565247 Output Voltage Ripple with 0.01-A Loading

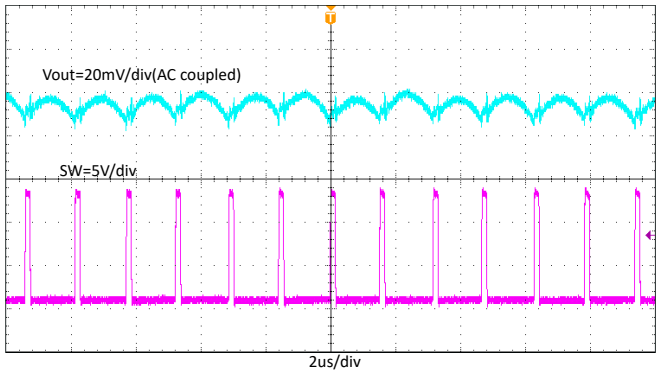


Figure 8-10. Output Voltage Ripple with 5-A Loading

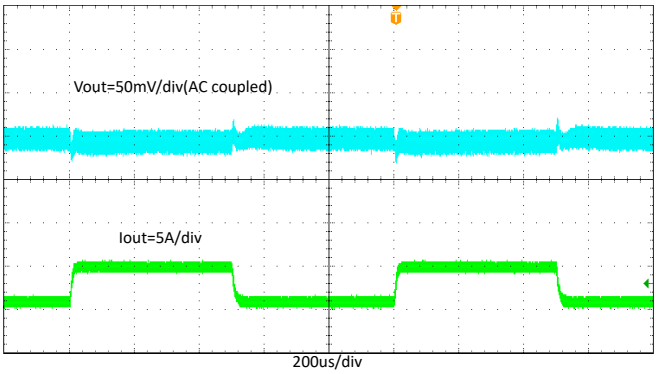


Figure 8-11. TPS565242 Transient Response with 0.5 A to 4.5 A by 2.5-A/µs Load Step

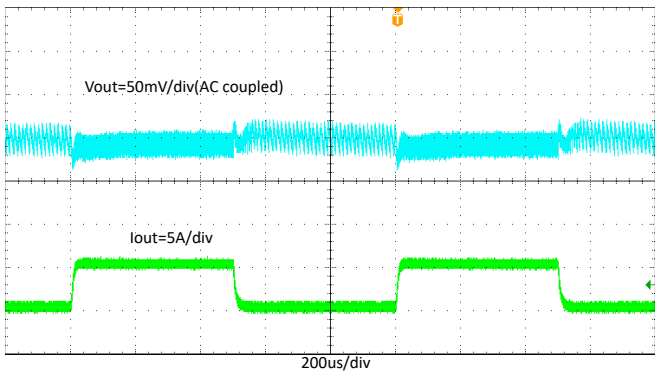


Figure 8-12. TPS565242 Transient Response with 0.1 A to 5 A by 2.5-A/µs Load Step

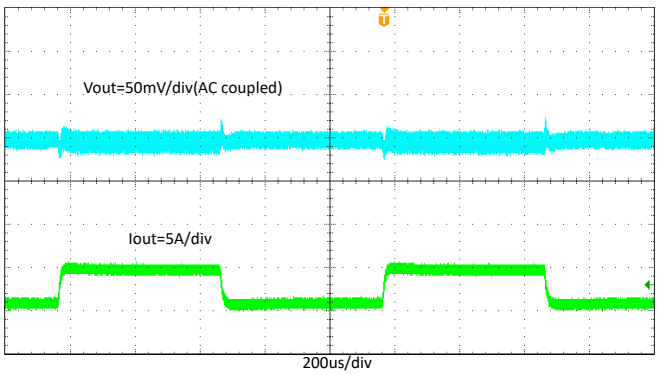


Figure 8-13. TPS565247 Transient Response with 0.5 A to 4.5 A by 2.5-A/µs Load Step

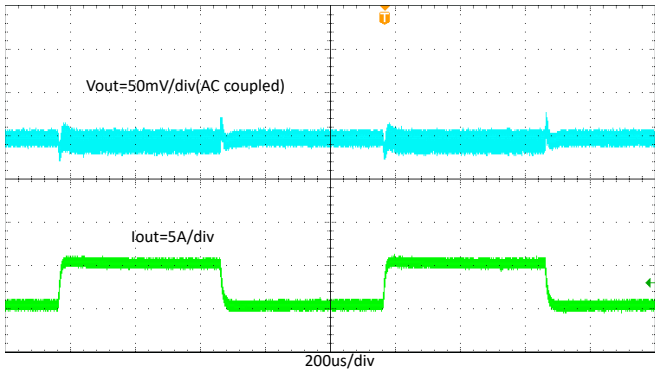


Figure 8-14. TPS565247 Transient Response with 0.1 A to 5 A by 2.5-A/µs Load Step

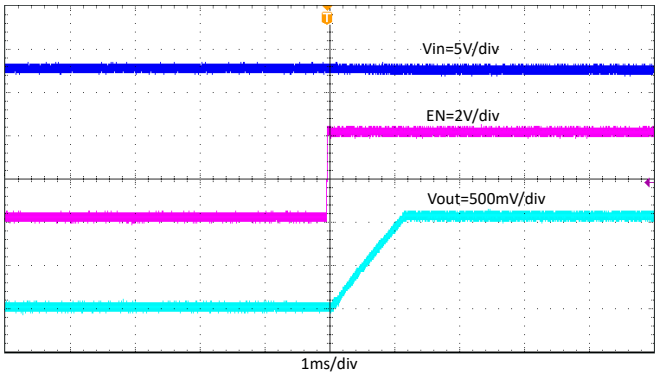


Figure 8-15. Start-Up Through EN, I_{OUT} = 5 A

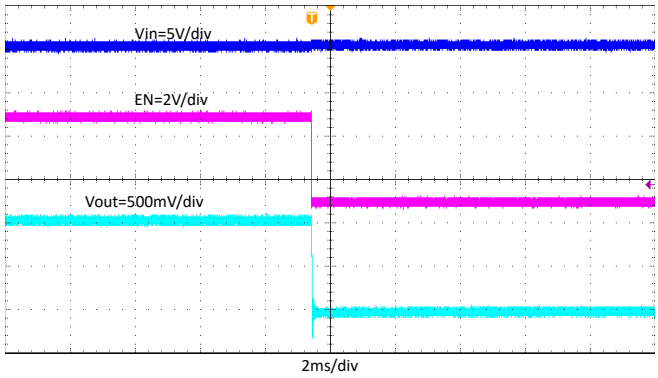


Figure 8-16. Shutdown Through EN, I_{OUT} = 5 A

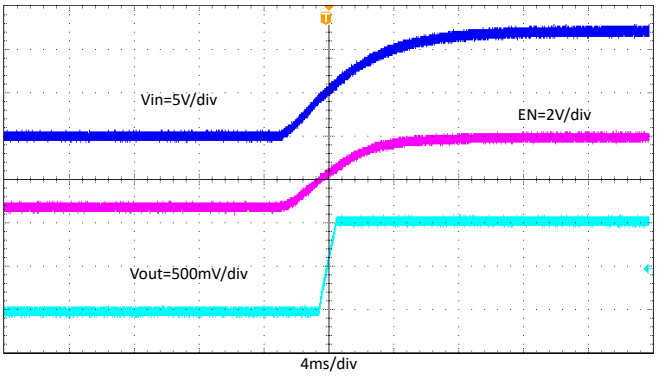


Figure 8-17. Start-Up with V_{IN} Rising, I_{OUT} = 5 A

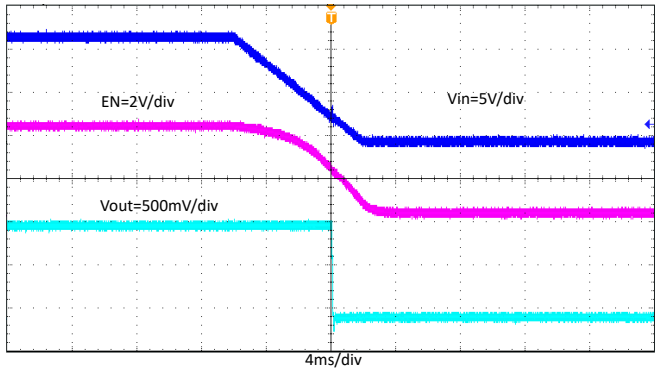


Figure 8-18. Start-Up with V_{IN} Falling, I_{OUT} = 5 A

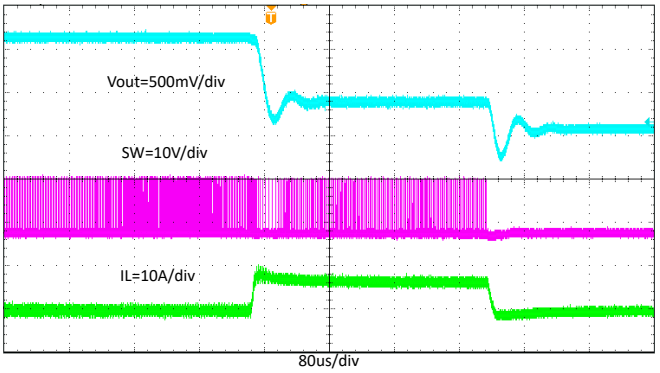


Figure 8-19. TPS565242 Normal Operation to Output Hard Short

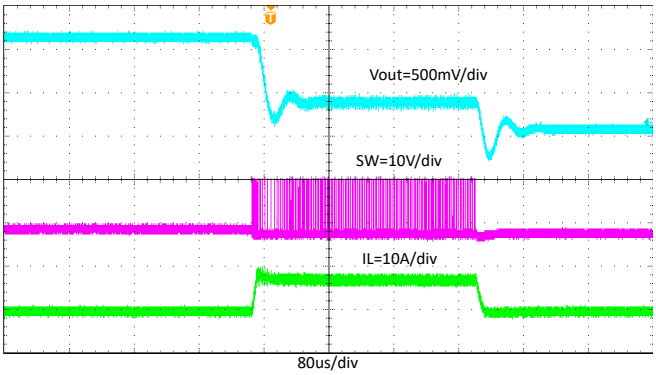


Figure 8-20. TPS565247 Normal Operation to Output Hard Short

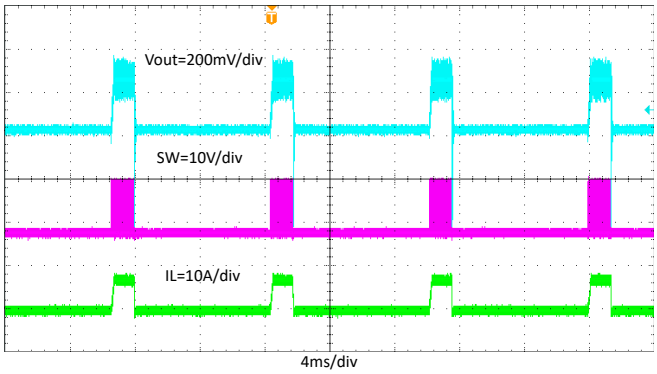


Figure 8-21. Output Hard Short Hiccup

9 Power Supply Recommendations

The TPS56524x are designed to operate from input supply voltages in the range of 3 V to 16 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

10 Layout

10.1 Layout Guidelines

- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate VOUT path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the FB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

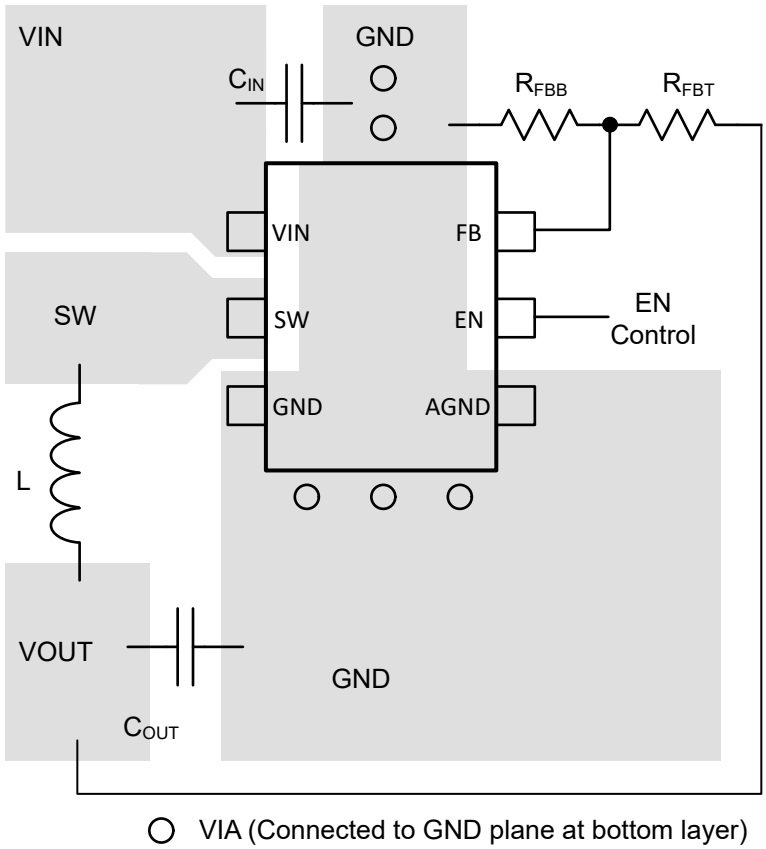


Figure 10-1. Suggested Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS565242 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS565247 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS565242DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	5242	Samples
TPS565247DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	5247	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

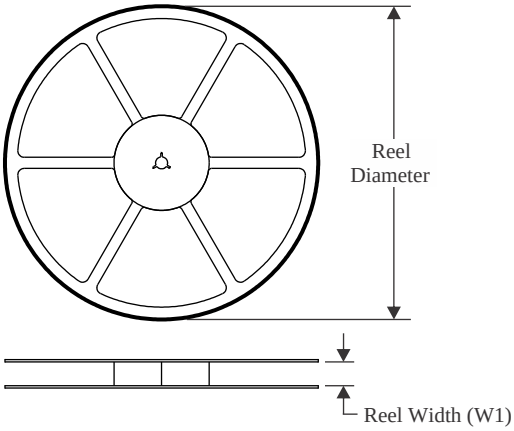
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

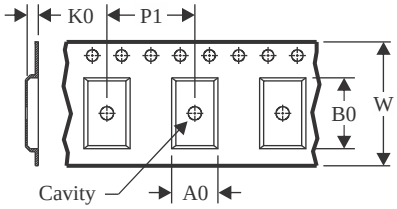
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

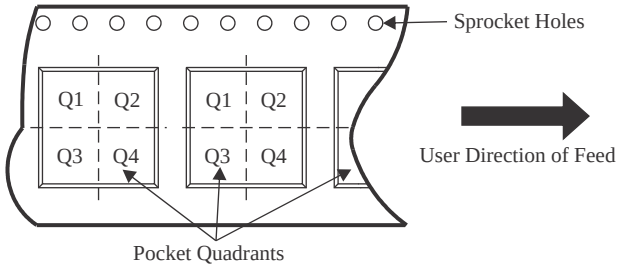


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

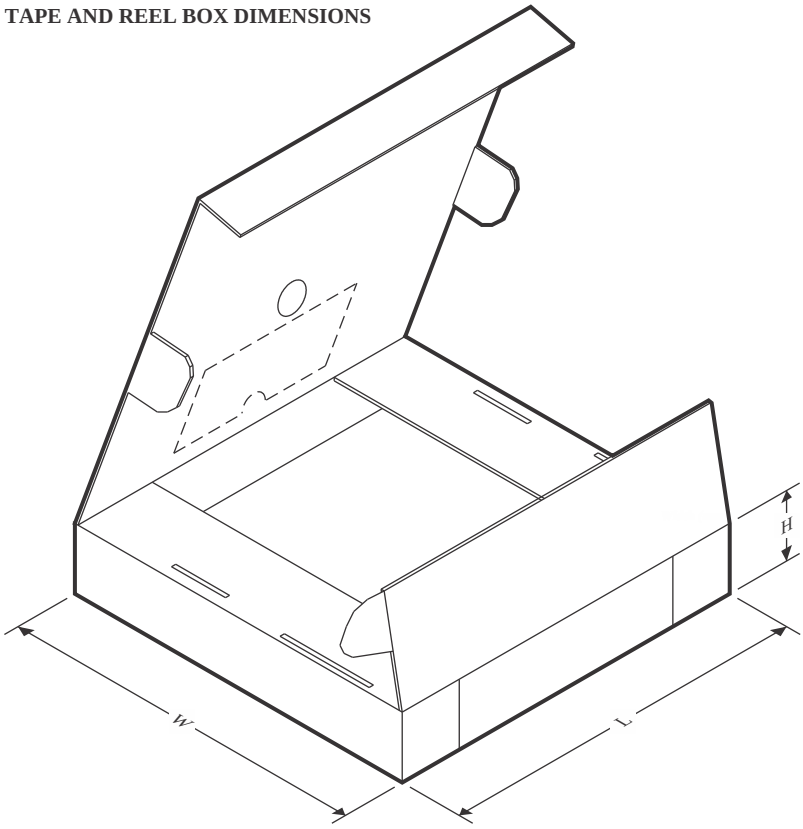
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS565242DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS565247DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

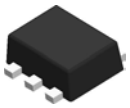
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS565242DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS565247DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

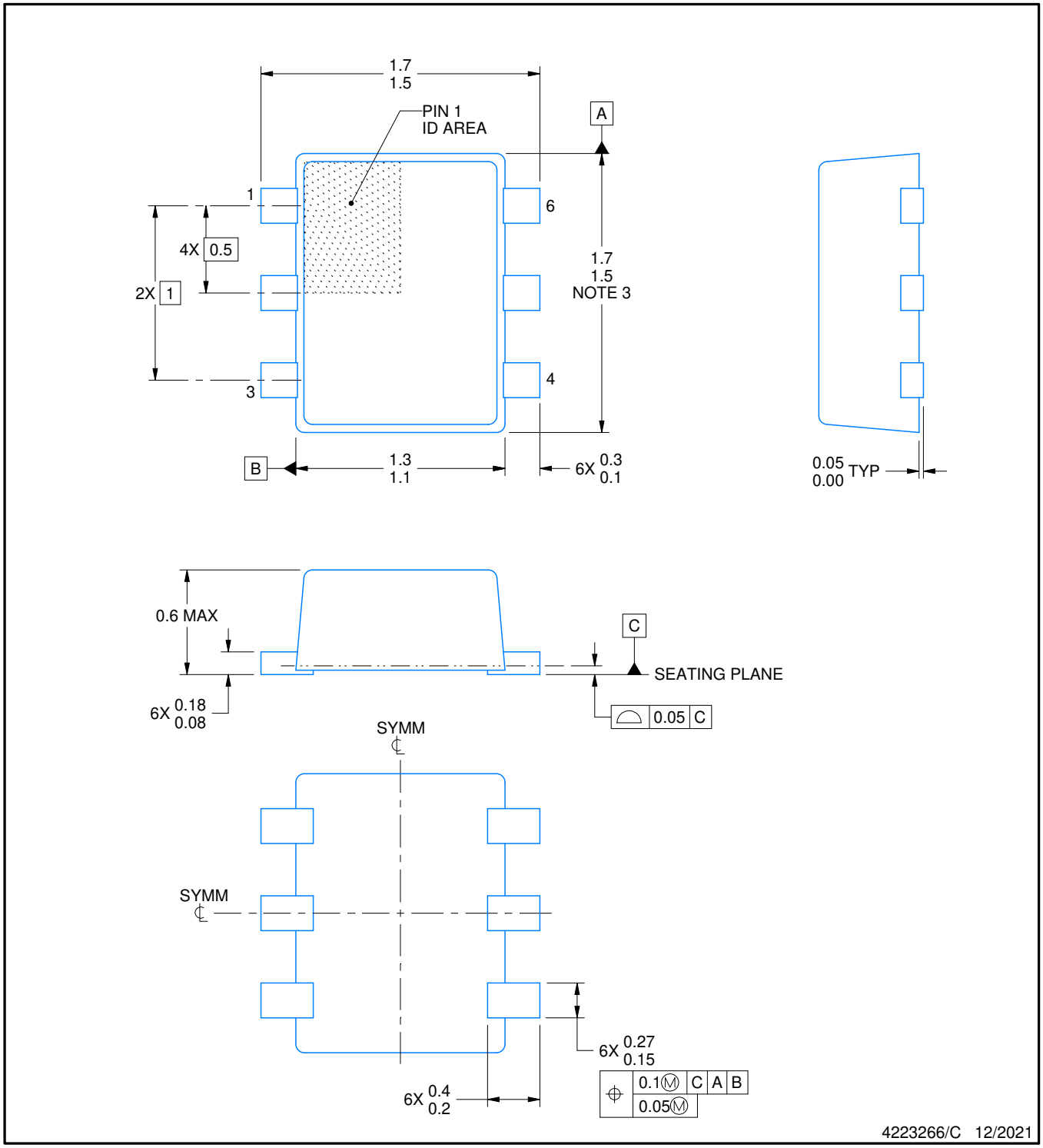
DRL0006A



PACKAGE OUTLINE

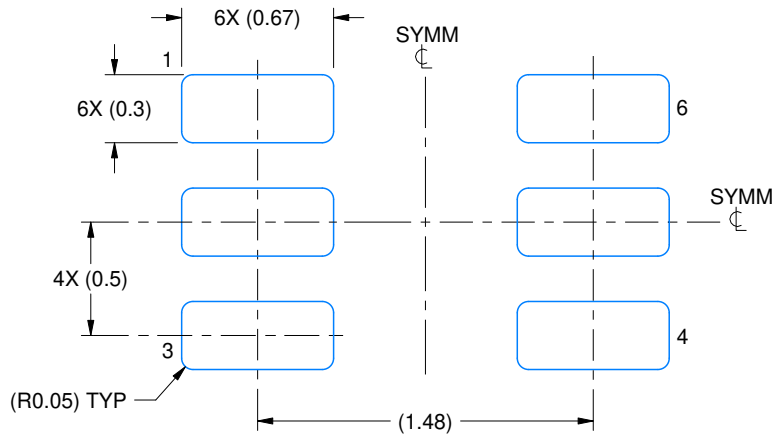
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

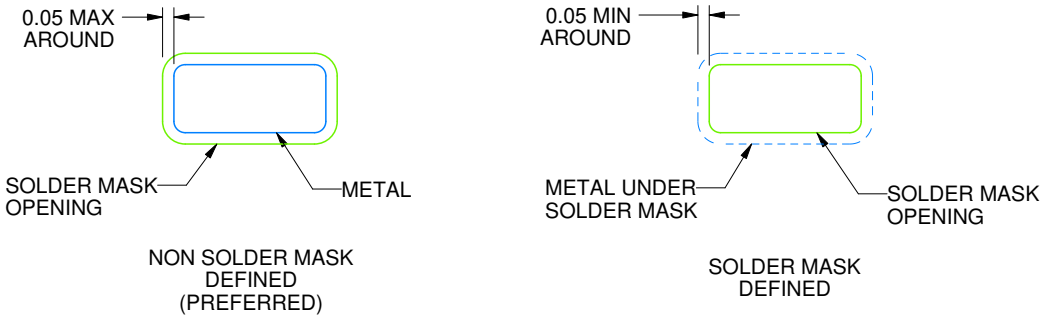


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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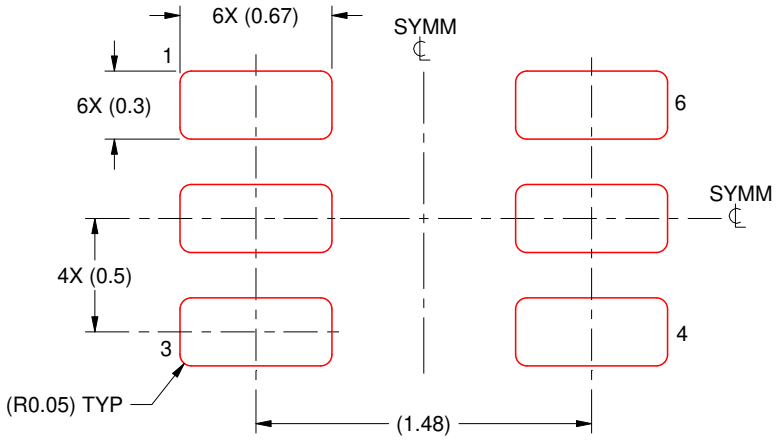
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265