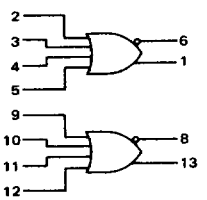
MC1023

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

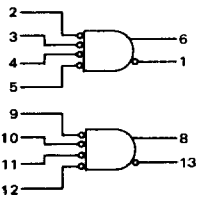
This circuit is designed to operate in high-speed digital computer applications as a clock driver or as a high-speed gate.

POSITIVE LOGIC



$6 = \overline{2 + 3 + 4 + 5}$
$1 = 2 + 3 + 4 + 5$

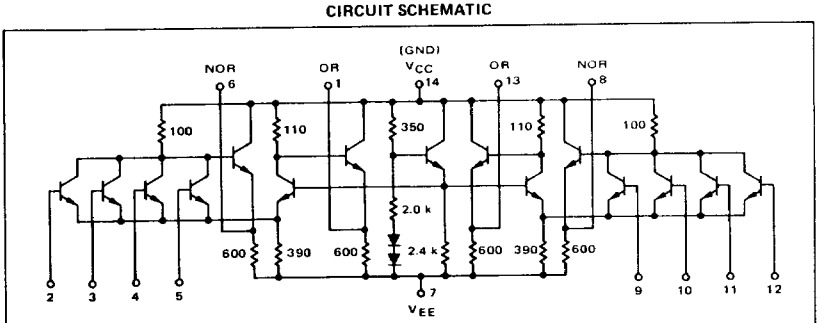
NEGATIVE LOGIC



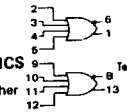
$6 = \overline{2 \cdot 3 \cdot 4 \cdot 5}$
$1 = 2 \cdot 3 \cdot 4 \cdot 5$

DC Input Loading Factor = 3
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test is shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature
0°C
+25°C
+75°C

Characteristic	Symbol	Pin Under Test	MC1023P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	61	-	-	mAdc
Input Current	I_{in}	2 3 4 5	-	-	-	300	-	-	μAdc
Input Leakage Current	I_R	2 3 4 5	-	-	-	1.0	-	5.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.930	-0.750	-0.850	-0.700	-0.790	-0.635	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	6	-2.050	-1.530	-2.000	-1.500	-1.940	-1.440	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.930	-0.750	-0.850	-0.700	-0.790	-0.635	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	1	-2.050	-1.530	-2.000	-1.500	-1.940	-1.440	Vdc
Switching Times*			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 2)*	t_{5+6-}	6	2.0	3.5	2.0	3.5	3.0	4.5	ns
	t_{5-6+}	6	2.0	3.0	2.0	3.0	3.0	4.0	
	t_{5+1-}	1	2.0	3.0	2.0	3.0	3.0	4.0	
	t_{5-1+}	1	2.0	3.5	2.0	3.5	3.0	4.5	
(Fan-Out = 10)*	t_{5+6-}	6	2.5	3.5	2.5	3.5	3.0	5.0	
	t_{5-6+}	6	2.0	3.5	2.0	3.5	3.0	5.0	
	t_{5-1+}	1	2.0	3.5	2.0	3.5	3.0	5.0	
	t_{5+1-}	1	2.5	3.5	2.5	3.5	3.0	5.0	
Rise Time (Fan-Out = 2)*	t_{6+}	6	2.0	4.0	2.0	4.0	3.5	5.0	
	t_{1+}	1	2.0	4.0	2.0	4.0	3.5	5.0	
(Fan-Out = 10)*	t_{6+}	6	3.0	5.5	3.0	5.5	5.0	7.5	
	t_{1+}	1	3.0	5.5	3.0	5.5	5.0	7.5	
Fall Time (Fan-Out = 2)*	t_{6-}	6	2.0	4.5	2.0	4.5	3.0	5.5	
	t_{1-}	1	2.0	4.5	2.0	4.5	3.0	5.5	
(Fan-Out = 10)*	t_{6-}	6	3.0	5.5	3.0	5.5	5.0	7.5	
	t_{1-}	1	3.0	5.5	3.0	5.5	5.0	7.5	

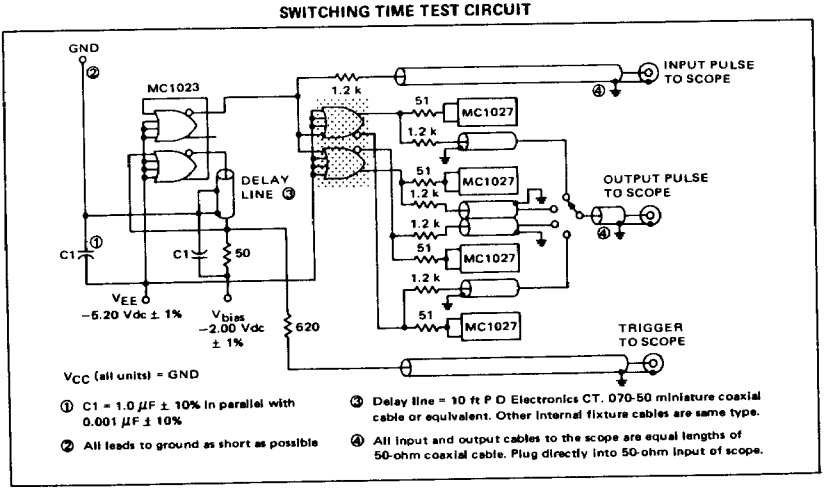
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ max}$	$V_{IH\ min}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
-1.530	-0.930	-0.750	-5.2	-2.5
-1.500	-0.850 min	-0.700	-5.2	-2.5
-1.440	-0.790	-0.635	-5.2	-3.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ max}$	$V_{IH\ min}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
-	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	14
-	-	2	3, 4, 5, 7, 9, 10, 11, 12	-	14
-	-	3	2, 4, 5, 7, 9, 10, 11, 12	-	
-	-	4	2, 3, 5, 7, 9, 10, 11, 12	-	
-	-	5	2, 3, 4, 7, 9, 10, 11, 12	-	
-	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	14
-	-	-		-	
-	-	-		-	
2	-	-	3, 4, 5, 7, 9, 10, 11, 12	6	14
3	-	-	2, 4, 5, 7, 9, 10, 11, 12		
4	-	-	2, 3, 5, 7, 9, 10, 11, 12		
5	-	-	2, 3, 4, 7, 9, 10, 11, 12		
-	3	-	2, 4, 5, 7, 9, 10, 11, 12	-	14
-	3	-	2, 4, 5, 7, 9, 10, 11, 12	-	
-	4	-	2, 3, 5, 7, 9, 10, 11, 12	-	
-	5	-	2, 3, 4, 7, 9, 10, 11, 12	-	
-	2	-	3, 4, 5, 7, 9, 10, 11, 12	1	14
-	3	-	2, 4, 5, 7, 9, 10, 11, 12		
-	4	-	2, 3, 5, 7, 9, 10, 11, 12		
-	5	-	2, 3, 4, 7, 9, 10, 11, 12		
2	-	-	3, 4, 5, 7, 9, 10, 11, 12	-	14
3	-	-	2, 4, 5, 7, 9, 10, 11, 12	-	
4	-	-	2, 3, 5, 7, 9, 10, 11, 12	-	
5	-	-	2, 3, 4, 7, 9, 10, 11, 12	-	
Pulse In	Pulse Out				
5	6	-	2, 3, 4, 7, 9, 10, 11, 12	-	14
	1	-		-	
	1	-		-	
	6	-		-	
	6	-		-	
	1	-		-	
	6	-		-	
	1	-		-	
	6	-		-	
	1	-		-	

* A fan-out is defined as one $\overline{3}$ or $\overline{E}$ input.

SWITCHING TIME TEST CIRCUIT

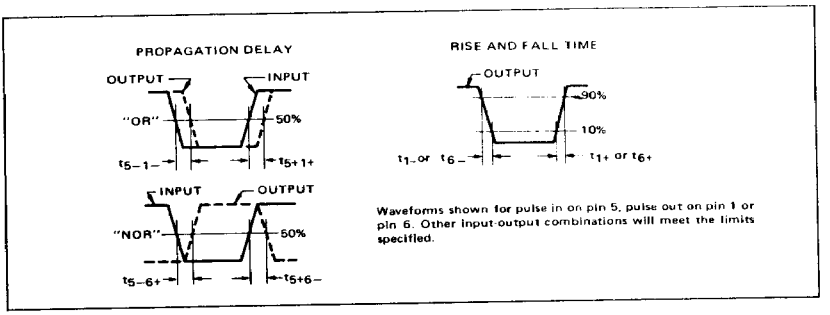


① C1 = 1.0 μF ± 10% in parallel with 0.001 μF ± 10%

② All leads to ground as short as possible

③ Delay line = 10 ft P D Electronics CT. 070-50 miniature coaxial cable or equivalent. Other internal fixture cables are same type.

④ All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Plug directly into 50-ohm input of scope.



APPLICATIONS INFORMATION

The MC1023 is a dual high-speed gate designed for use as a clock driver which allows the MECL II flip-flops to operate at their full speed capability. More advanced processing techniques than those used on standard MECL II are employed for the clock driver, resulting in an improved speed-power product. The dual gate exhibits typical propagation delay times of 2.0 ns. Due to this short propagation delay, the gate makes an ideal clock driver for long shift registers where the clock pulse may be distributed with minimal skew time over the entire register length.

Since rise and fall times may be as fast as 1.0 ns under light loading, the following precautions must be taken during layout. The MC1023 will not drive back-plane point-to-point wiring satisfactorily. Due to the fast logic transitions a maximum length of three inches for point-to-point wiring is recommended. Lower impedance printed wires allow longer line lengths. Due to the low output impedance (5.0 ohms) of the MC1023, additional terminating resistance to −5.2 V may be employed. This reduces fall time for capacitive loads and propagation delay to negative-going outputs. Figure 1 shows typical curves for output voltage versus load current. Figures 2 through 7 show curves for rise, fall, and propagation delay times versus loading for a typical gate. Capacitance of 5.0 pF per fan-out was used during the tests. This is conservative, since stray and input capacitance is closer to 4.0 pF per fan-out when driving flip-flops in high-speed designs.

The MC1023 is also very useful for providing the additional levels of gating required for some counting configurations such as divide-by-seven and divide-by-thirteen counters. The maximum frequency of operation of such a counter depends upon the flip-flop and gating delay which determines the minimum "up time" of the clock waveforms. Due to its short propagation delay the MC1023 when used with an MC1027 allows a divide-by-seven counter to operate up to 100 MHz.

Due to the 5.0-ohm output impedance the clock driver will also drive low impedance lines. When driving a 50-ohm termination to −2.0 V the output "1" level will be reduced by a maximum of 0.100 V. The minimum "1" level is approximately −0.950 V with a load current of 21 mA, reducing voltage noise immunity by 0.100 V. Noise power or energy noise immunity is still good due to the very low gate output impedance and low line impedance.

Two additional applications of the MC1023 are shown in Figures 8 and 9.

FIGURE 1 - TYPICAL OUTPUT CHARACTERISTICS

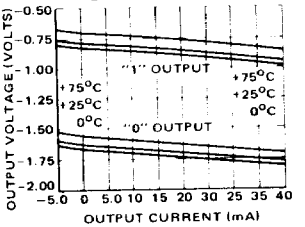


FIGURE 2 - RISE TIME

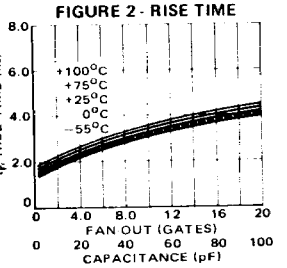
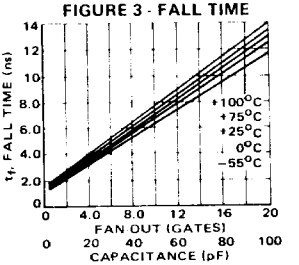


FIGURE 3 - FALL TIME



APPLICATIONS INFORMATION (continued)

FIGURE 4 - t_{pd+-}

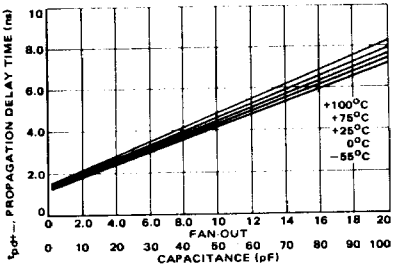


FIGURE 5 - t_{pd-+}

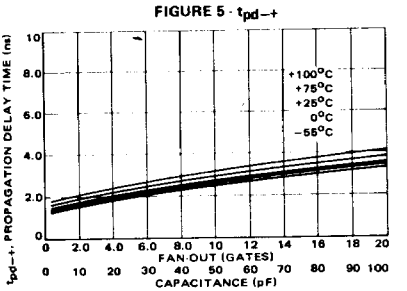


FIGURE 6 - t_{pd++}

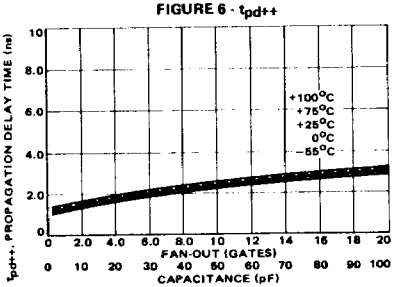


FIGURE 7 - t_{pd--}

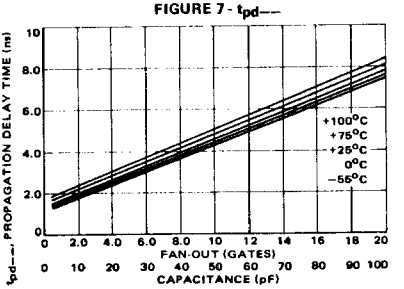
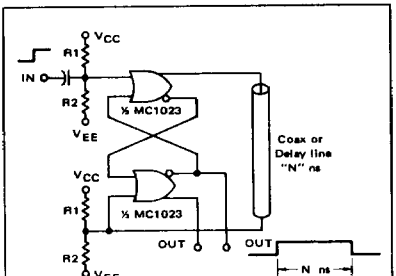


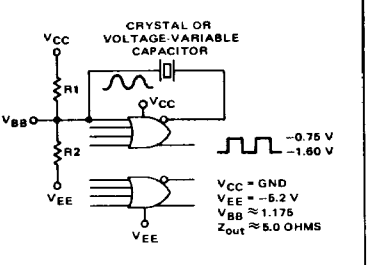
FIGURE 8 - MC1023 AS A ONE SHOT AND CLOCK SHAPER



Uniform pulse determined only by delay "N". The circuit is very useful for generating accurate and stable pulse widths or reshaping clock pulse width. Pulse widths down to 3.0 ns are obtainable.

Circuit courtesy of Mr. O. Gene Gabbard, Member of Technical staff, Communications Satellite Corporation.

FIGURE 9 - MC1023 AS A CRYSTAL OSCILLATOR



Power Dissipation = ¼ Watt
The Gate is Useful to 150+ MHz

For specific frequencies of operation, the crystal feedback may be obtained from the OR output. For further information see Application Note AN-417.