# HARRIS SEMICONDUCTOR

# CDP68HC68T3

## ADVANCE INFORMATION

October 17 1995

## Serial (SPI) Counter CMOS IC

### Features

- SPI Bus Compatible
- Time-out with Automatic Shutdown or Continuous Mode Countdown
- Programmable Countdown - from 1 Second to 72 hours with 1 Second Resolution
- Low Power Drain
  - Oscillator/Counter Active:..... 50µA Max.
  - Standby Mode:..... 10µA Max.
- Operating Voltage Range ..... 3V to 6V
- POR at $V_{DD}$ Power-up w/o External Components
- Available in an 8 Lead SOIC or PDIP Package
- Operating Temperature Range ..... -40°C to +85°C

### Applications

- µP/Logic Countdown Timer
- Automotive Engine Time-Off Internal Timer
- Delayed Event Timer
- Single Event Timer
- Repetitive Cycling Timer (Wake-up)
- Pulse Generator
- Interval Timer

### Description

The CDP68HC68T3 is a Programmable CMOS Counter IC with a Serial Peripheral Interface (SPI). The T3 provides a low power real time counter function with one second resolution programmable to a maximum count of 72 hours. The IC can function as either a counter or pulse generator. In the counter mode it can provide a method of determining the real time between events. The T3 will begin counting down from the programmed starting value, and can be queried to determine the elapsed time from start. In order to minimize power, the counter will enter a standby mode when the counter reaches zero. In the pulse generator mode the counter can be programmed to provide a repetitive square wave output with a period determined by the count in its 3 byte SPI register. In this mode of operation the IC can provide a "wake-up" signal at programmable time intervals of up to 72 hours. Read/write access is provided via 3 byte data transfers over the SPI bus.

The block diagram shows the internal functions of the T3. The 32kHz crystal oscillator determines the accuracy of the counter. The SPI clock (SCK) provides data transfer control when CE is active. An internal power on reset (POR) occurs when $V_{DD}$ is switched ON. No external components are required.

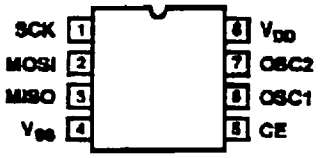
Very little power is consumed in normal operation, allowing an ambient operating temperature range up to 125°C. In the standby mode, the quiescent supply current drain is less than 10µA.

### Ordering Information

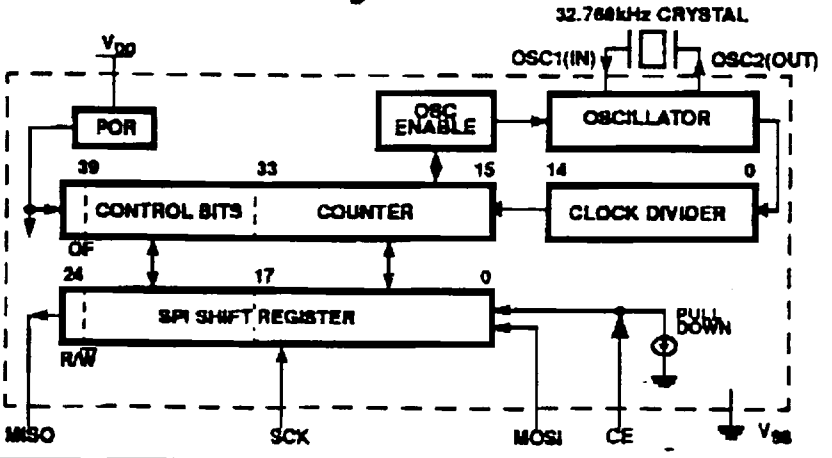
| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| CDP68HC68T3M | -40°C to +85°C | 8 Lead Plastic SOIC |
| CDP68HC68T3E | -40°C to +85°C | 8 Lead PlasticDIP |

### Pinout

SOIC
TOP VIEW




### Functional Block Diagram




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Copyright © Harris Corporation 1995

File Number TBD



*HRISS056*

## Absolute Maximum Ratings

Supply Voltage, $V_{DD}$ ..... -0.5V to +7V
All Inputs and Outputs, Max. Voltage Range .$V_{SS}$ 0.3V to $V_{DD}$+0.3V
Operating Ambient Temperature Range..... -40°C to +125°C
Storage Temperature Range, TSTG..... -55°C to +150°C
Lead Temperature (Soldering 10s)..... +265°C

Thermal Resistance $\theta_{JA}$
Plastic SOIC Package, ..... 165°C/W
Maximum Dissipation, $P_D$
At +125°C ..... 152mW
Above +125°C, derate at ..... 6.1mW/°C
Maximum Junction Temperature..... +150°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications $V_{DD}$ = +4.75V to +5.25V, $T_A$ = -40°C to +85°C, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Active Supply Current | $I_{DDQ}$ | Oscillator and Counter Running | | | 50 | µA |
| Low Power Mode Supply Current | $I_{DDQ}$ | $V_{CE}$=$V_{MISO}$ =$V_{MOSI}$=$V_{SCK}$=0.0V | | | 10 | µA |
| Power On Reset Trip Point, $V_{DD}$ | $V_{POR}$ | | | | 1.5 | V |
| Input Resistance, CE | $R_{IN}$ | | 10 | | 25 | KΩ |
| Input Voltage Low, SCK, MOSI, CE, OSC1 | $V_{IL}$ | | $V_{SS}$ - 0.3 | | $V_{DD}$ x 0.2 | V |
| Input Voltage High, SCK, MOSI, CE, OSC1 | $V_{IH}$ | | $V_{DD}$ x 0.7 | | $V_{SS}$ +0.3 | V |
| Input Leakage Current, SCK, MOSI, OSC1 | $I_{LK}$ | | -1 | | +1 | µA |
| Output Voltage Low, MISO | $V_{OL}$ | $I_{OUT}$ = 1.6mA | | | 0.4 | V |
| Output Voltage High, MISO | $V_{OH}$ | $I_{OUT}$ = -0.8mA | $V_{DD}$ - 0.8 | | | V |
| High Z Leakage Current, MISO | $I_Z$ | $V_{MOSI}$ = $V_{DD}$ or $V_{SS}$ | -1 | | +1 | µA |

## AC Characteristics $V_{DD}$ = +4.75V to +5.25V, $T_A$ = -40°C to +85°C, $C_{L(MISO)}$ = 200pF Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Internal Oscillator Timer Characteristics | | | | | | |
| Oscillator Timer Accuracy | $f_{OSC}$ | | 32.44 | 32.768 | 33.096 | KHz |
| Interval Accuracy | | | 0.5 | | 0.5 | s |
| Oscillator Stabilization Time | $t_{STAB}$ | | | | 1 | s |
| SPI Characteristics | | | | | | |
| Serial Clock Frequency | $f_{SCK}$ | | | | 2.72 | MHz |
| Serial Clock High Time | $t_{SCKH}$ | $f_{SCK}$ = Maximum Frequency | 150 | | | ns |
| Serial Clock Low Time | $t_{SCKL}$ | $f_{SCK}$ = Maximum Frequency | 150 | | | ns |
| Serial Clock Period | $t_{SCKP}$ | $f_{SCK}$ = Maximum Frequency | 367 | | | ns |
| Serial Clock Rise Time | $t_{SCKR}$ | | | | 30 | ns |
| Serial Clock Fall Time | $t_{SCKL}$ | | | | 30 | ns |
| Access Time | $t_{ACC}$ | CE Rising Edge to MISO Data Valid | | | 466 | ns |
| CE Setup Time | $t_{CE}$ | CE Rising Edge to SCK Rising Edge | 500 | | | ns |
| MISO Disable Time | $t_{DOZ}$ | CE Falling Edge to MISO High Z | | | 200 | ns |

**AC Characteristics** $V_{DD}$ = +4.75V to +5.25V, $T_A$ = -40°C to +85°C, $C_{L(MISO)}$ = 200pF Unless Otherwise Specified (Continued)

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| MOSI Hold Time | $t_{DIH}$ | SCK Rising Edge to MOSI Invalid | 150 | | | ns |
| MOSI Setup Time | $t_{DIS}$ | SDI Valid to SCK Rising Edge | 100 | | | ns |
| MISO Valid Time | $t_{DOV}$ | SCK Falling Edge to MISO Valid | | | 120 | ns |
| MISO Hold Time | $t_{DOH}$ | SCK Falling Edge to MISO Invalid | 0 | | | ns |
| Enable Low Time | $t_{CEA}$ | Minimum Time Between Consecutive CE Assertions | 200 | | | ns |
| Enable Lag Time | $t_{LAG}$ | SCK Falling Edge to CE Falling Edge | 150 | | | ns |
| Oscillator Response Time | $t_{RESP}$ | $C_L$ = 4pF, $V_{IH}$ = 3.32V, $V_{IL}$ = 1.42V, $V_{OH}$ > 2.9V, $V_{OL}$ < 1.8V, $V_{DD}$ = 4.75V | | | 14 | µs |

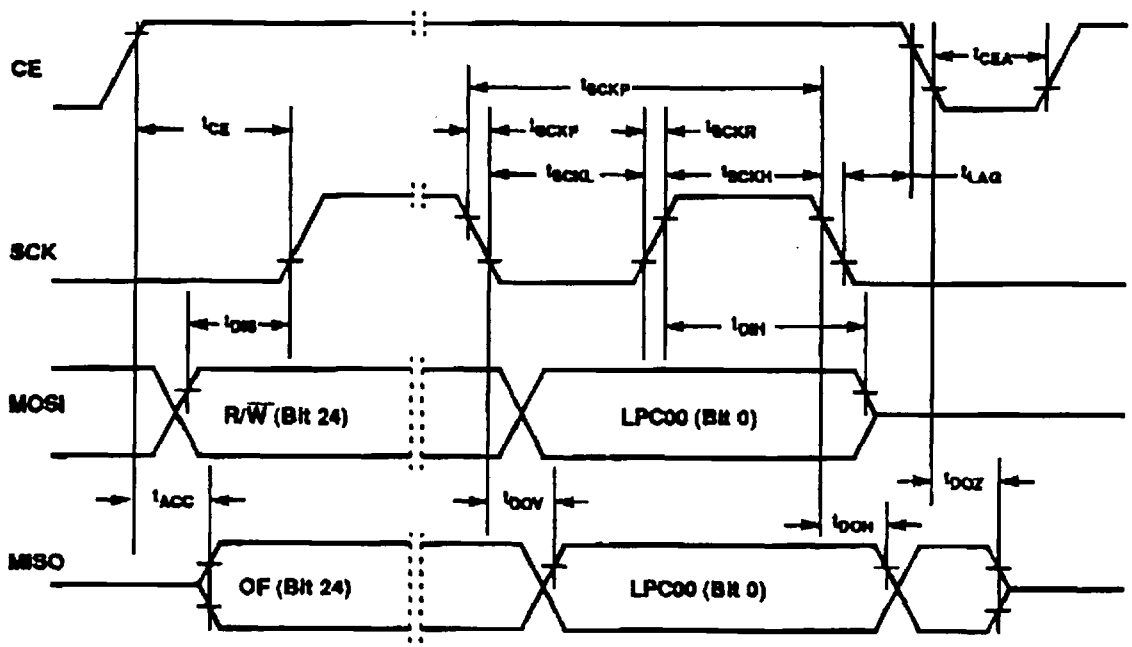



FIGURE 1. TIMING DIAGRAM FOR SPECIFICATION REFERENCE. WHILE CE IS HIGH, EACH SCK CLOCK SHIFTS ONE BIT OF DATA INTO MOSI AND ONE BIT OUT OF MISO. REFER TO TABLE 1 FOR A DESCRIPTION OF EACH BIT IN THE 3 BYTE (24 BIT) SPI INPUT SHIFT REGISTER

## Pin Description

**SCK (1) Serial Clock (Input)**

Serial data is shifted out on MISO, synchronously, with each leading edge of SCK. Input data from the MOSI pin is latched, synchronously, with each trailing edge of SCK.

**MOSI (2) Master-Out-Slave-In (Input)**

Data bytes are shifted in at this pin most significant bit first.

**MISO (3) Master-IN-Slave-Out (Output)**

Serial data is shifted out on this pin most significant bit first. When the chip enable signal is high, this pin is HI-Z. In continuous mode operation the pin is enabled and an output transition occurs at every programmed time out.

**VSS (4)**

Negative power supply line.

**CE (5) Chip Enable (Input)**

A positive chip enable input. Following a transition from low to high on CE the CDP68HC68T3 interprets the first 6 bits transferred as control information and the least significant two bits of the first byte and the following two bytes (18 bits) as data. CE must remain enabled throughout the three byte data transfer. An active pull-down is provided at the input pin.

**OSC1 (6) OSC2 (7) Oscillator (Input & Output)**

Normally connected to a crystal. The crystal and components should be mounted as close as possible to the oscillator terminals to minimize output distortion and start-up stabilization time.

**VDD (8)**

Positive power supply line.

## Applications

### SPI BUS CONTROL

Serial communication with the CDP68HC68T3 is via the SPI bus and a host CPU or µP such as the CDP68HC05. The SPI port pins are the MOSI input, MISO output, CE chip enable and the SCK system clock input.

On power up, the counter and clock divide register is set to all zero's and the T3 remains in a low power mode until a write operation. All commands are initiated from the SPI bus lines when 24 bits of data are written into the SPI Shift Register of the LPC. A SPI write will trigger the oscillator to start-up, clear the divide register to insure an accurate 1 second interval. The T3 will then begin counting down from the value loaded into the counter via the SPI.

The LPC is selected and data transfers are enabled when the CE input goes high. When CE goes high MISO output changes from a high Z to an active mode (the state of MISO output corresponds to the status of the overflow bit), internal data transfer from the LPC Counter and Control Registers to the SPI Shift Register are disabled, and the MOSI input is enabled; the SCK input should be in the low state.

Data bits are transferred to the LPC on high-low transitions of the SCK signal. Each serial bit is latched into the SPI Shift Register on the rising edge of the SCK, followed by data shifted out to the MISO line on the falling edge of the SCK. The timing diagram is shown in Figure 1. The 24 bit SPI Data Configuration is shown in Table 1. Each Read/Write operation must be a continuous 3 byte data sequence (Chip Enable remains in the high state throughout the 3 byte transfer. Read data (MISO output) consists of the counter status and the last written control bit information. Read data starts with the OF (Over Flow) bit as the first bit shifted out.

On the trailing edge of CE (high-to-low transition) the data in the SPI Shift Register will be transferred to the LPC Counter and Control Registers. A low on the CE line returns the MISO three-state output to a three-state high Z mode. The

**TABLE 1. LPC SPI SHIFT REGISTER BIT DESCRIPTION**

| BYTE | BIT NO. | 24 BIT SHIFT REGISTER | BIT FUNCTION |
|---|---|---|---|
| | | ↑ DATA OUT, MISO | |
| 1 | 7 | R/W /OF | Defines Write mode where R/W=0. When writing data, all 24 data bits must be written on the same assertion of CE. For Read only mode, R/$\overline{W}$=1. When Reading, the OF (Over Flow) bit is 1st bit read at MISO. (OF bit may be read immediately after CE goes high) |
| | 6 | Control 4 | Enable/Disable Bit. When High, a Write will Disable the oscillator. This bit is active low to enable the oscillator. (The Function Bit must also be high) |
| | 5 | Control 3 | Square Wave Bit. When High, this bit forces a square wave repetitive mode at the MISO output (The Function Bit must also be high) |
| | 4 | Control 2 | Test Bit. Used by mfr to expedite chip test time. Normal operation requires this bit to be set low. |
| | 3 | Control 1 | Function Bit. This bit must be set high with other control bits to force activation of that function. |
| | 2 | Control 0 | Test Bit. Used by mfr to expedite chip test time. Normal operation requires this bit to be set low. |
| | 1 | LPC17 | MSB |
| | 0 | LPC16 | |
| 2 | 7 | LPC15 | |
| | 6 | LPC14 | |
| | 5 | LPC13 | |
| | 4 | LPC12 | |
| | 3 | LPC11 | The LPC00 to LPC17 bits specify the SPI data input/output for the counter |
| | 2 | LPC10 | WRITE Mode, R/$\overline{W}$ = 0: LPCxx bits are written from the SPI Shift Register to the counter when CE goes low. |
| | 1 | LPC09 | |
| | 0 | LPC08 | READ Mode, R/$\overline{W}$ = 1: No data is written, the LPC bits are shifted out of MISO on the falling edge of SCK. The first bit shifted out is the MSB. When reading, the LPC bits define the countdown status of the counter. |
| 3 | 7 | LPC07 | |
| | 6 | LPC06 | |
| | 5 | LPC05 | |
| | 4 | LPC04 | |
| | 3 | LPC03 | |
| | 2 | LPC02 | |
| | 1 | LPC01 | |
| | 0 | LPC00 | LSB (Represents a count of 1 second) |
| | | ↑ DATA IN, MOSI | |

CE input has an internal pull-down to keep the LPC serial interface inactive when the input line is open or the CPU is in reset.

### DEFINITION OF DATA BITS

As shown in Table 1, 24 bits of data are transferred into the SPI Shift Register. The 18 data bit sequence LPC00 to LPC17 is used to write a countdown value to the internal counter. If the R/$\overline{W}$ value of bit 24 is set to zero, the data in the SPI Shift Register is written to the Counter data register. A read only command requires the R/$\overline{W}$ bit to be set to 1. When reading the data stream from the SPI Shift Register, the first bit shifted out to the MISO line is the counter Over Flow status (OF bit 24). Data follows in the sequence shown in Table 1 as control bits followed by the 18 bit LPCxx group with the timer countdown status. Control bit values shifted out will be the values previously written to the SPI Shift Register

The control bits are used to set command and control functions with the defined action as shown in Table 1.

### WRITE OPERATION

When CE goes low and the R/$\overline{W}$ bit in the SPI shifted data is set to zero, the data Write mode is initiated. An R/$\overline{W}$ bit set to zero forces the SPI Shift Register data to be latched into the Counter and Control Register. The Write command resets the Clock Divider, clears the OF bit and starts the oscillator. Start-up of the Oscillator may inherently produce an error in the count value. Initialization should be done with two SPI Write commands. The second Write must occur after the $t_{STAB}$ time interval.

### READ OPERATION

If the R/$\overline{W}$ bit is set to one the counter register will not be altered. The data in the SPI Shift Register consists of the updated Counter countdown status and the Control bits last written to the Control Register. The SPI shift register is updated with the latest counter value at one second intervals. Data is shifted out to the MISO line starting with the OF bit. In order to avoid a change in operating mode Control Bit 1 should be in the low state.

### POR

An Internal Power-On-Reset (POR) is active only in response to the $V_{DD}$ level. Reset occurs when power is applied to $V_{DD}$. Reset action occurs when $V_{DD}$ is no greater than 1.5V. (No external components are required.) Reset at power on initializes the Counter, Clock Divider and Data Register to all zeros, stops the internal 32.768kHz clock and sets the LPC into a low power mode.

### OSCILLATOR & CLOCK DIVIDER

The Clock Divider functions as a prescaler for the 32.768kHz oscillator with a $2^{15}$ divide count. This provides crystal oscillator accuracy for the 1 second timing pulse delivered to the Counter. A SPI write command resets the Clock Divider to all zero's and clears the OF bit to initialize the start of timing.

The oscillator may be disabled by writing a 1 to Control Bits 1 and 4. A data write operation is required in order to restart the oscillator.

### COUNTER OPERATION

The LPC is a low power counter with 1 second of resolution and 1% interval accuracy. The maximum timer duration is 72.8 hours which results from an 18 bit countdown of the Counter register when clocked by the 1 second Clock Divider pulse. Count data loaded from a host CPU via the SPI Bus sets the timer.

Countdown begins from the value loaded into the counter and will continue until the counter overflows bits (i.e all ones). At 1 second intervals, 0.5 seconds after the Counter LSB changes, the SPI Shift Register is updated with the current Counter value. A read operation may be used to determine the Counter value. Counting continues until all Counter bits and the OF bit are 1. After the all 1's state is reached, the counter and OF bits are cleared to 0's and the LPC goes to the Low Power mode with the Oscillator disabled.

### SQUARE WAVE, REPETITIVE CYCLE MODE

To initiate operation in the Square Wave mode, the Square Wave Bit and the Function Bit are set High. This forces a square wave output at the MISO pin. The initial state of the MISO output after a POR is low. After POR a write to the timer with the square wave bit set (high) will force MISO into a high state. MISO's state will change on all subsequent time outs (OF=1).

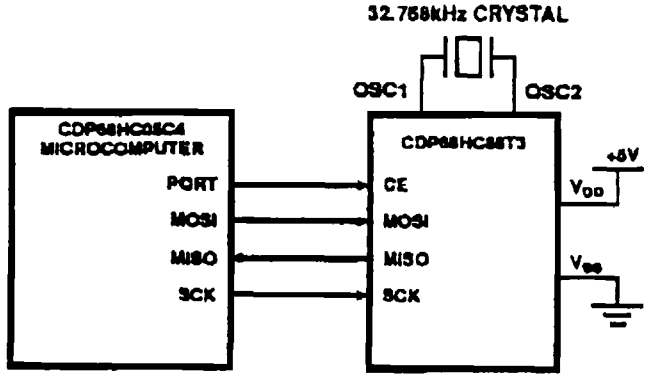
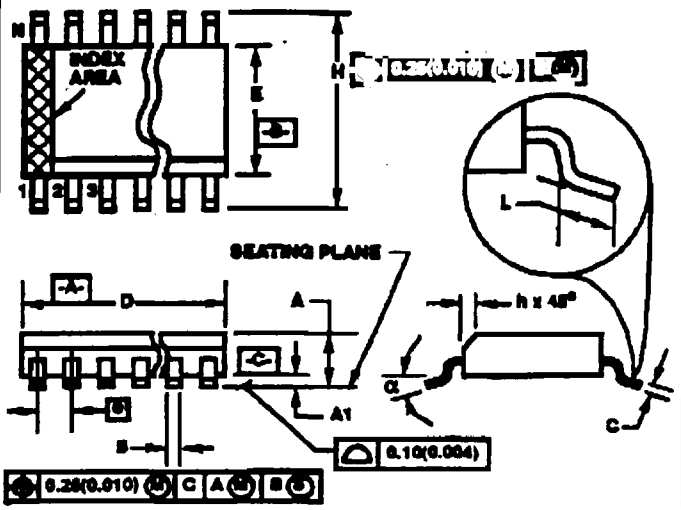



FIGURE 2. TYPICAL MICROCONTROLLER INTERFACE WITH THE CDP68HC68T3 LOW POWER COUNTER

## Packaging

**M8.15** (JEDEC MS-012-AA)
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**




| SYMBOL | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | NOTES |
|---|---|---|---|---|---|
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

*Harris Semiconductor products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Harris is believed to be accurate and reliable. However, no responsibility is assumed by Harris or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Harris or its subsidiaries.*

## Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call 1-800-4-HARRIS

**UNITED STATES**
Harris Semiconductor
P.O. Box 883, Mail Stop 53-210
Melbourne, Florida 32902
TEL: 1-800-442-7747
(407) 729 4984
FAX: (407) 729 5321

**EUROPE**
Harris Semiconductor
Mercure Centre
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2-724-2111

**SOUTH ASIA**
Harris Semiconductor H.K. Ltd.
13/F Foursseas Building
208-212 Nathan Road
Tsimshatsui, Kowloon
Hong Kong
TEL: (852) 723-6339

**NORTH ASIA**
Harris K.K.
Kojimachi-Nakata Bldg. 4F
5-3-5 Kojimachi
Chiyoda-ku, Tokyo 102 Japan
TEL: (81) 3-3265-7572 (Sales)

HARRIS SEMICONDUCTOR