# BQ298xyz Voltage, Current, Temperature Protectors with an Integrated High-Side NFET Driver for Fast/Flash Charging Single-Cell Li-Ion and Li-Polymer Batteries

## 1 Features

- Voltage protection:
  - Overvoltage (OV): ±10 mV
  - Undervoltage (UV): ±20 mV
- Current protection:
  - Overcurrent in charge (OCC): ±1 mV
  - Overcurrent in discharge (OCD): ±1 mV
  - Short circuit in discharge (SCD): ±5 mV
- Temperature protection:
  - Overtemperature (OT)
- Additional features:
  - Supports as low as a 1-mΩ sense resistor ($R_{SNS}$)
  - High-side protection
  - High Vgs FET drive
  - 0-V charging (only BQ2980)
  - CTR pin for FET override control for system reset/shutdown
  - Configure CTR for second OT protection through an external PTC thermistor
- Current consumption:
  - NORMAL mode: 4 µA
  - SHUTDOWN mode: 0.1-µA maximum
- Package:
  - 8-pin X2QFN: 1.50 × 1.50 × 0.37 mm

## 2 Applications

- Smartphones
- Tablets
- Power bank
- Wearables

## 3 Description

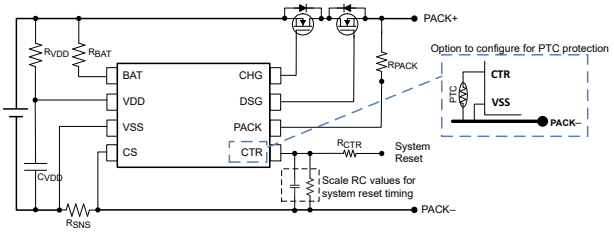
The BQ298xyz family of devices, featuring integrated charge-pump FET drivers, provides high-side primary battery cell protection for 1-series Li-ion and Li-polymer batteries, enabling consistent Rdson across cell voltages. For better system thermal performance, the BQ298x device's accuracy enables the use of a sense resistor as low as 1 mΩ.

The CTR pin in the BQ298x device can be configured to override the FET driver by host control to create a system reset or shutdown function. Alternatively, the CTR pin can be configured to connect an external Positive Temperature Coefficient (PTC) thermistor for FET OT protection in addition to the internal die temperature sensor. The BQ2980xy devices support zero-volt (0-V) charging, while the BQ2982xy devices have this disabled.

**Device Information**

| PART NUMBER(1) | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| BQ2980xy | X2QFN | 1.50 mm × 1.50 mm × 0.37 mm |
| BQ2982xy | X2QFN | 1.50 mm × 1.50 mm × 0.37 mm |

(1) For all available packages, see the orderable addendum and *Device Comparison Table*.




**Simplified Schematic**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision I (November 2021) to Revision J (December 2022)** **Page**

- Added the BQ298217 device to the *Device Comparison Table* ....3

**Changes from Revision H (July 2021) to Revision I (November 2021)** **Page**

- Changed the *Device Comparison Table* ....3

**Changes from Revision G (May 2021) to Revision H (July 2021)** **Page**

- Changed the BQ298019 device from PRODUCT PREVIEW to Production Data in the *Device Comparison Table* ....3

**Changes from Revision F (December 2020) to Revision G (May 2021)** **Page**

- Removed "Product Preview" footnote from BQ2982 in *Description* ....1
- Changed the *Device Comparison Table* ....3
- Removed PRODUCT PREVIEW footnote from BQ2982xy in *Thermal Information* ....4
- Clarified CHG driver at low VDD in *Electrical Characteristics* ....5
- Clarified VDD condition in *Charge and Discharge Driver* ....11
- Clarified ZVCHG in *ZVCHG (0-V Charging)* ....13

## 5 Device Comparison Table

| BQ298xyz Device Family (BQ2980xy with ZVCHG [0-V Charging] Enabled, BQ2982xy with ZVCHG Disabled) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PART NUMBER | OVP (V) | OVP DELAY (s) | UVP (V) | UVP DELAY (ms) | OCC (mV) | OCC DELAY (ms) | OCD (mV) | OCD DELAY (ms) | SCD (mV) | SCD DELAY (µs) | OT (°C) | CTR/ PTC Config | UV_Shut |
| BQ298000 | 4.475 | 1.25 | 2.600 | 144 | –8 | 8 | 8 | 8 | 20 | 250 Fixed | 85 | CTR | Enabled |
| BQ298006 | 4.475 | 1.00 | 2.500 | 20 | –12 | 16 | 14 | 16 | 40 | 250 Fixed | 75 | CTR | Enabled |
| BQ298009 | 4.500 | 1.00 | 2.900 | 20 | –18 | 8 | 30 | 16 | 40 | 250 Fixed | Disable | CTR | Enabled |
| BQ298010 | 4.500 | 1.00 | 2.900 | 20 | –10 | 8 | 20 | 16 | 30 | 250 Fixed | Disable | CTR | Enabled |
| BQ298012 | 4.300 | 1.00 | 2.750 | 144 | –4 | 8 | 14 | 20 | 30 | 250 Fixed | Disable | CTR | Enabled |
| BQ298015 | 4.440 | 1.25 | 2.800 | 144 | –8 | 8 | 8 | 8 | 20 | 250 Fixed | 85 | CTR | Enabled |
| BQ298018 | 4.400 | 1.00 | 2.700 | 144 | –8 | 8 | 20 | 48 | 60 | 250 Fixed | 85 | CTR | Enabled |
| BQ298019 | 4.425 | 1.25 | 2.800 | 144 | –30 | 48 | 8 | 48 | 40 | 250 Fixed | 85 | CTR | Enabled |
| BQ298215 | 4.440 | 1.25 | 2.800 | 144 | –8 | 8 | 8 | 8 | 20 | 250 Fixed | 85 | CTR | Enabled |
| BQ298216 | 4.300 | 1.00 | 2.500 | 144 | –4 | 8 | 14 | 20 | 30 | 250 Fixed | Disabled | CTR | Enabled |
| BQ298217 | 4.250 | 1.25 | 2.600 | 125 | -36 | 8 | 60 | 16 | 200 | 250 Fixed | Disabled | CTR | Enabled |

## 6 Pin Configuration and Functions

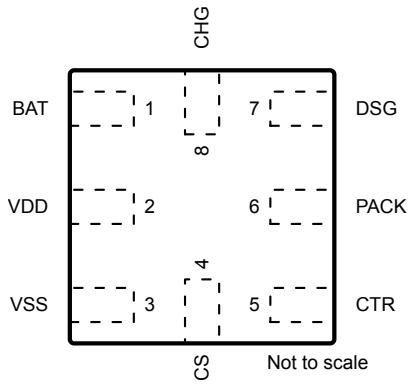



**Figure 6-1. RUG Package 8-Pin X2QFN Top View**

**Table 6-1. Pin Functions**

| NUMBER | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | BAT | I(1) | BAT voltage sensing input (connected to the battery side) |
| 2 | VDD | P | Supply voltage |
| 3 | VSS | — | Device ground |
| 4 | CS | I | Current sensing input (connect to PACK– side of the sense resistor) |
| 5 | CTR | I | Active high control pin to open FET drivers and shut down the device. It can be configured to enable an internal pull-up and connect the CTR pin to an external PTC for OT protection. |
| 6 | PACK | I | Pack voltage sensing pin (connected to the charger side, typically referred to as PACK+ and PACK–) |
| 7 | DSG | O | DSG FET driver |
| 8 | CHG | O | CHG FET driver |

(1) I = input, O = output, P = power

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | VDD | –0.3 | 6 | V |
| Input voltage | PACK | –0.3 | 24 | V |
| | BAT | –0.3 | 6 | |
| | CS | –0.3 | 0.3 | |
| | CTR | –0.3 | 5 | |
| Output voltage | CHG | –0.3 | 20 | V |
| | DSG | –0.3 | 20 | |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | VDD | 1.5 | 5.5 | V |
| Input voltage | PACK | 0 | 20 | V |
| | BAT | 1.5 | 5.5 | |
| | CS | –0.25 | 0.25 | |
| | CTR | 0 | 5 | |
| Output voltage | CHG | $V_{SS}$ | VDD + VDD × $A_{FETON}$ | V |
| | DSG | $V_{SS}$ | VDD + VDD × $A_{FETON}$ | |
| Operating temperature, $T_A$ | | –40 | 85 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | BQ2980xy/BQ2982xy RUG (X2QFN) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 171.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 75 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 94.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 94.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

Typical values stated at $T_A$ = 25°C and VDD = 3.6 V. MIN/MAX values stated with $T_A$ = –40°C to +85°C and VDD = 3 to 5 V unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT CONSUMPTION** | | | | | | |
| $I_{NORMAL}$ | Normal mode supply current | $V_{CHG}$ and $V_{DSG}$ > 5 V, $C_{LOAD}$ = 8 nF (typical 20 nA[1]), VDD > 4.0 V | | 5 | 8 | µA |
| | | $V_{CHG}$ and $V_{DSG}$ > 5 V, $C_{LOAD}$ = 8 nF (typical 20 nA[1]), UVP < VDD < 3.9 V | | 4 | 6 | µA |
| $I_{FETOFF}$ | Supply current with both FET drivers off | $V_{CHG}$ = $V_{DSG}$ ≤ 0.2 V | | 2 | 4 | µA |
| $I_{SHUT}$ | Shutdown current | $V_{PACK}$ < VBAT, VDD = 1.5 V | | | 0.1 | µA |
| **N-CH FET DRIVER, CHG and DSG** | | | | | | |
| $A_{FETON}$ | FET driver gain factor, the Vgs voltage to FET | $V_{CHG}$ or $V_{DSG}$ = VDD + VDD × $A_{FETON}$<br>UVP < VDD < 3.9 V<br>$C_{LOAD}$ = 8 nF | 1.65 | 1.75 | 1.81 | V/V |
| | | $V_{CHG}$ or $V_{DSG}$ = VDD + VDD × $A_{FETON}$<br>VDD > 4.0 V<br>$C_{LOAD}$ = 8 nF | 1.45 | 1.55 | 1.68 | V/V |
| $V_{FETOFF}$ | FET driver off output voltage | $V_{FETOFF}$ = $V_{CHG}$ – VSS or $V_{DSG}$ – VSS<br>$C_{LOAD}$ = 8 nF | | | 0.2 | V |
| $V_{DRIVER\_SHUT}$ | FET driver charge pump shut down voltage | Charge pump enabled when VDD rises to $V_{DRIVER\_SHUT}$ | 1.95 | 2 | 2.1 | V |
| $V_{DRIVER\_SHUT\_HYS}$ | FET driver charge pump shut down voltage hysteresis | Charge pump disabled when VDD falls to $V_{DRIVER\_SHUT}$ – $V_{DRIVER\_SHUT\_HYS}$ | | 50 | | mV |
| $t_{rise}$ [2] | FET driver rise time | $C_{LOAD}$ = 8 nF,<br>$V_{CHG}$ or $V_{DSG}$ rises from VDD to (2 × VDD) | | 400 | 800 | µs |
| $t_{fall}$ | FET driver fall time | $C_{LOAD}$ = 8 nF,<br>$V_{CHG}$ or $V_{DSG}$ fall to $V_{FETOFF}$ | | 50 | 200 | µs |
| $I_{LOAD}$ | FET driver maximum loading | | | | 10 | µA |
| **VOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | Overvoltage detection range | Factory configured, 50-mV step | 3750 | | 5200 | mV |
| $V_{OVP\_ACC}$ | Overvoltage detection accuracy | $T_A$ = 25°C, CHG/DSG $C_{LOAD}$ < 1 µA | –10 | | 10 | mV |
| | | $T_A$ = 0°C to 60°C, CHG/DSG $C_{LOAD}$ < 1 µA | –15 | | 15 | |
| | | $T_A$ = –40°C to +85°C, CHG/DSG $C_{LOAD}$ < 1 µA | –25 | | 25 | |
| $V_{OVP\_HYS}$ | Overvoltage release hysteresis voltage | Fixed at 200 mV | 150 | 200 | 250 | mV |
| $V_{UVP}$ | Undervoltage detection range | Factory configured, 50-mV step | 2200 | | 3000 | mV |
| $V_{UVP\_ACC}$ | Undervoltage detection accuracy | $T_A$ = 25°C | –20 | | 20 | mV |
| | | $T_A$ = 0°C to 60°C | –30 | | 30 | mV |
| | | $T_A$ = –40°C to +85°C | –50 | | 50 | mV |
| $V_{UVP\_HYS}$ | Undervoltage release hysteresis voltage | Fixed at 200 mV | 150 | 200 | 250 | mV |
| $R_{PACK-VSS}$ | Resistance between PACK and VSS during UV fault | | 100 | 300 | 550 | kΩ |
| **CURRENT PROTECTION** | | | | | | |
| $V_{OC}$ | Overcurrent in charge (OCC) and discharge (OCD) range | Factory configured, 2-mV step. For OCC, the range is negative (min = –64, max = –4). | 4 | | 64 | mV |

## 7.5 Electrical Characteristics (continued)

Typical values stated at $T_A$ = 25°C and VDD = 3.6 V. MIN/MAX values stated with $T_A$ = –40°C to +85°C and VDD = 3 to 5 V unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SCD}$ | Short circuit in discharge threshold | Factory configured | | 10 | | mV |
| | | | | 20 | | |
| | | | | 30 | | |
| | | | | 40 | | |
| | | | | 60 | | |
| | | | | 120 | | |
| | | | | 200 | | |
| $V_{OC\_ACC}$ | Overcurrent (OCC, OCD1, OCD2, SCD) detection accuracy | < 20 mV | –1 | | 1 | mV |
| | | 20 to approximately 55 mV | –3 | 2 | 3 | |
| | | 56 to approximately 100 mV | –5 | | 5 | |
| | | > 100 mV | –12 | | 12 | |
| $I_{PACK-VDD}$ | Current sink between PACK and VDD during current fault. Used for load removal detection | | 8 | | 24 | µA |
| $I_{OCD\_REC}$ | OCD, SCD recovery detection current | Sum of current from VDD and BAT during OCD or SCD fault | | | 55 | µA |
| $V_{OC\_REL}$ | OCC fault release threshold | ($V_{BAT}$ – $V_{PACK}$) | | 100 | | mV |
| | OCD, SCD fault release threshold | ($V_{PACK}$ – $V_{BAT}$) | | –400 | | mV |
| **OVERTEMPERATURE PROTECTION**[2] | | | | | | |
| $T_{OT}$ | Internal overtemperature threshold | Factory configured | | 75 | | °C |
| | | | | 85 | | |
| $T_{OT\_ACC}$ | Internal overtemperature detection accuracy | | –10 | | 10 | °C |
| $T_{OT\_HYS}$ | Internal overtemperature hysteresis | | 8 | 15 | 22 | °C |
| **PROTECTION DELAY**[2] | | | | | | |
| $t_{OVP}$ | Overvoltage detection delay | Factory configured | 0.2 | 0.25 | 0.3 | s |
| | | | 0.8 | 1 | 1.2 | |
| | | | 1 | 1.25 | 1.5 | |
| | | | 3.6 | 4.5 | 5.4 | |
| $t_{UVP}$ | Undervoltage detection delay | Factory configured | 16 | 20 | 24 | ms |
| | | | 76.8 | 96 | 115.2 | |
| | | | 100 | 125 | 150 | |
| | | | 115.2 | 144 | 172.8 | |
| $t_{OC}$ | Overcurrent (OCC, OCD) detection delay | Factory configured | 5.6 | 8 | 10.5 | ms |
| | | | 12.4 | 16 | 19.6 | |
| | | | 16 | 20 | 24 | |
| | | | 38.4 | 48 | 57.6 | |
| $t_{SCD}$ | Short circuit discharge detection delay | Fixed configuration | 125 | 250 | 375 | µs |
| $t_{OT}$ | Overtemperature detection delay | Fixed configuration | 3.6 | 4.5 | 5.4 | s |
| **FET OVERRIDE/DEVICE SHUTDOWN CONTROL, CTR** | | | | | | |
| $V_{IH}$ | High-level input | | 1 | | | V |

## 7.5 Electrical Characteristics (continued)

Typical values stated at $T_A$ = 25°C and VDD = 3.6 V. MIN/MAX values stated with $T_A$ = –40°C to +85°C and VDD = 3 to 5 V unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input | | | | 0.4 | V |
| $V_{HYS}$ | Hysteresis for $V_{IH}$ and $V_{IL}$ | | 200 | | | mV |
| $R_{PULL\_UP}$ | Effective Internal pull-up resistance (to use with external PTC) | Factory configured if enabled | | 1.5 | | MΩ |
| | | | | 5 | | |
| | | | | 8 | | |
| **ZVCHG (0-V Charging)** | | | | | | |
| $V_{0CHGR}$ | Charger voltage requires to start 0-V charging | BQ2980xy only (ZVCHG is disabled in BQ2982xy). The CHG driver becomes high impedance when VDD < $V_{0INH}$. | 2 | | | V |
| $V_{0INH}$ | Battery voltage that inhibits 0-V charging | | | | 1 | V |

(1) $I_{NORMAL}$ is impacted by the efficiency of the charge pump driving the CHG and DSG FETs. An ultra-low-gate-leakage FET may be required. $I_{NORMAL}$ can be significantly higher with FETs with typical $I_{GSS}$ values of 10 µA. See *Selection of Power FET* for more details.
(2) Specified by design.

## 7.6 Typical Characteristics

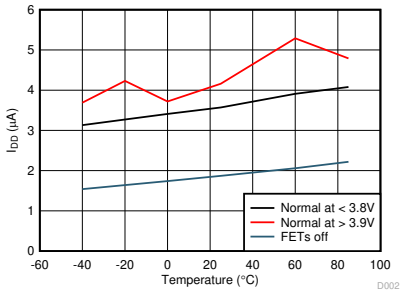



**Figure 7-1. Normal and FET Off Current Across Temperature**

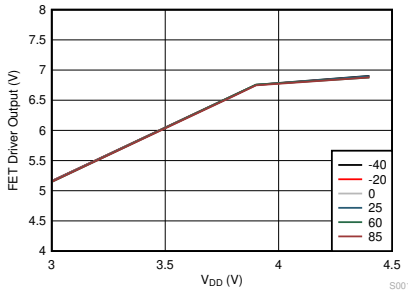



**Figure 7-2. CHG and DSG Output (Loading with an 8-nF Capacitor on CHG and DSG) Across VDD**

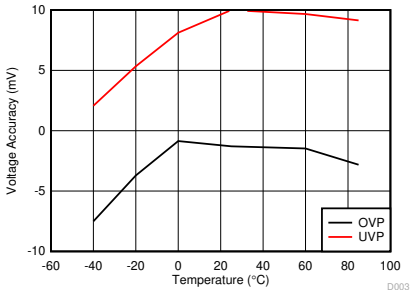



**Figure 7-3. Overvoltage and Undervoltage Accuracy Across Temperature**

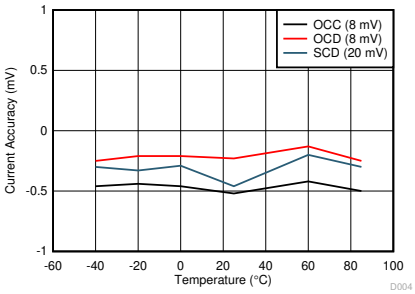



**Figure 7-4. Overcurrent Accuracy Across Temperature**

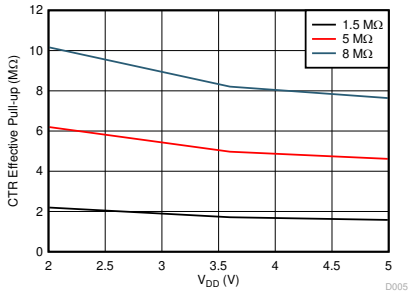



**Figure 7-5. CTR Internal Pull-Up Resistor (if Configured) Across VDD**

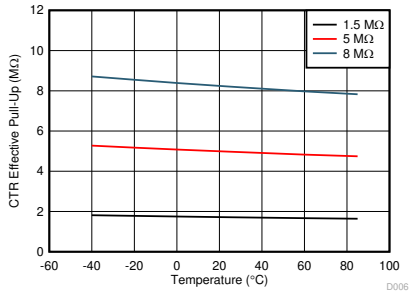



**Figure 7-6. CTR Internal Pull-Up Resistor (if Configured) Across Temperature (VDD at 3.6 V)**

# 8 Detailed Description

## 8.1 Overview

The BQ298xyz devices are high-side single-cell protectors designed to improve thermal performance by reducing power dissipation across the protection FETs. This is achieved with high-side protection with a built-in charge pump to provide higher Vgs to the FET gate voltage to reduce FET Rdson. Additionally, the device supports as low as a 1-mΩ sense resistor with ±1-mV accuracy, resulting in lower heat dissipation at the sense resistor without compromising current accuracy.

The BQ298x device implements a CTR pin that allows external control to open the power FETs, as well as shut down the device for low power storage. Optionally, the CTR pin can be configured to connect to a PTC and be used for overtemperature protection.

### 8.1.1 Device Configurability

Table 8-1 provides guidance on possible configurations of the BQ2980 and BQ2982 devices.

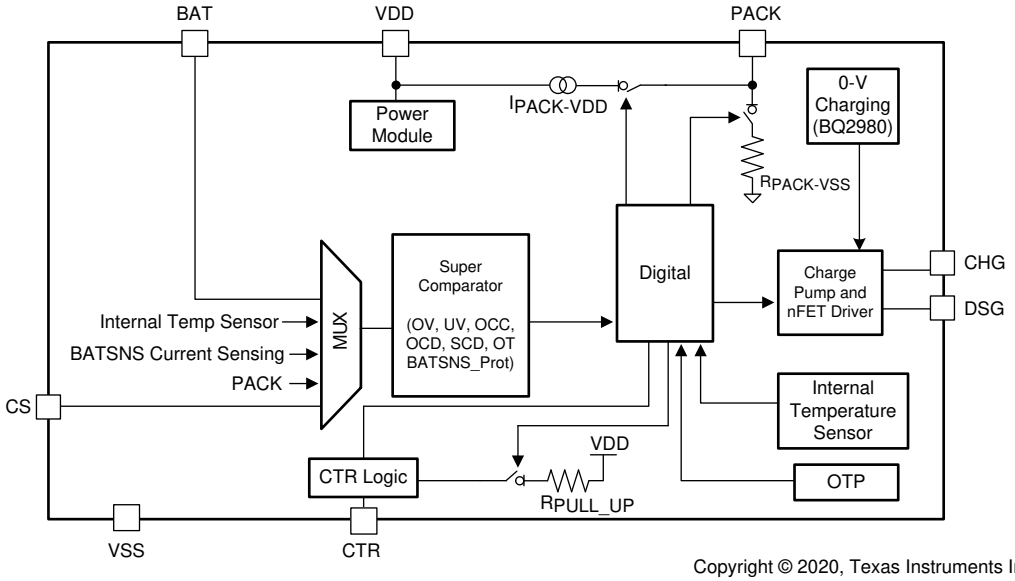
**Note**

Texas Instruments preprograms devices: Devices are not intended to be further customized by the customer.

**Table 8-1. Device Configuration Range**

| FAULT | | RANGE | STEP SIZE | UNIT | DELAY SELECTION | CHG, DSG STATUS | RECOVERY DESCRIPTION (Non-Configurable) |
|---|---|---|---|---|---|---|---|
| OV | Overvoltage | 3750 – 5200 | 50 | mV | 0.25, 1, 1.25, 4.5 s | CHG OFF | (200-mV hysteresis AND charger removal) OR (below OV threshold AND discharge load is detected) |
| UV | Undervoltage | 2200 – 3000 | 50 | mV | 20, 96, 125, 144 ms | Option 1: UV_SHUT enable The device goes into SHUTDOWN. | (200-mV hysteresis AND discharge load is removed before device shuts down) OR (above UV threshold AND charger connection) |
| | | | | | | Option 2: UV_SHUT disable DSG off, power consumption drops to $I_{FETOFF}$, and the device does not shut down. | (200-mV hysteresis) OR (above UV threshold AND charger connection) |
| OCC | Overcurrent in Charge | –64 – –4 | 2 | mV | 8, 16, 20, 48 ms | CHG OFF | Detect a charger removal ($V_{BAT}$ – $V_{PACK}$) > 100-mV typical |
| OCD | Overcurrent in Discharge | 4 – 64 | 2 | mV | | DSG OFF | Detect a discharge load removal ($V_{BAT}$ – $V_{PACK}$) < 400-mV typical |
| SCD | Short circuit in discharge | 10, 20, 30, 40, 60, 120, 200 | — | mV | Fixed 250 µs | | |
| OT | Overtemperature (through internal temperature sensor) | 75, 85 | — | °C | Fixed 4.5 s | CHG and DSG OFF | Fixed 15°C hysteresis |
| OT (PTC) | Internal pull-up resistor for OT with PTC (through external PTC on CTR pin) | 1.5, 5, 8 | — | MΩ | — | CHG and DSG OFF | Voltage on CTR pin drops below CTR $V_{IL}$ level |

## 8.2 Functional Block Diagram






## 8.3 Feature Description

### 8.3.1 Overvoltage (OV) Status

The device detects an OV fault when $V_{BAT}$ > $V_{OVP}$ (OV threshold) during charging. If this condition exists for longer than the OV delay ($t_{OVP}$), the CHG output is driven to $V_{FETOFF}$ to turn off the CHG FET.

The OV status is released and the CHG output rises to HIGH, that is, $V_{CHG}$ = VDD × (1 + $A_{FETON}$), if one of the following conditions occurs:

- When $V_{BAT}$ is < ($V_{OVP}$ – $V_{OVP\_HYS}$) and the charger is removed or
- When $V_{BAT}$ is < $V_{OVP}$ and a discharge load is detected.

The device detects the charger is removed if ($V_{PACK}$ – $V_{BAT}$) < 100-mv typical. To detect if a load is attached, the device checks if ($V_{BAT}$ – $V_{PACK}$) > 400-mv typical.

### 8.3.2 Undervoltage (UV) Status

The device detects a UV fault when the battery voltage measured is below the UV threshold ($V_{UVP}$). If this condition exists for longer than the UV delay ($t_{UVP}$), the DSG output is driven to $V_{FETOFF}$ to turn off the DSG FET.

The device includes a UV_SHUT option which may be enabled during factory configuration. If this option is enabled, during the UV fault state the device goes into SHUTDOWN mode to preserve the battery. In SHUTDOWN mode, the BQ2980 will drive the CHG output to the PACK voltage, putting the device into ZVCHG mode (the BQ2982 does not enable this ZVCHG mode). That means, the CHG FET can be turned on if a charger is connected and both VDD and PACK meet the ZVCHG turn-on conditions (see *Section 8.3.9* for more details). The PACK pin is internally pulled to VSS through $R_{PACK-VSS}$. This is to determine if the charger is disconnected on the PACK+ terminal before shutting down the device. It is also to ensure the device does not falsely wake up from SHUTDOWN mode due to noise.

The UV status is released and the DSG output rises to HIGH, that is, $V_{DSG}$ = VDD × (1 + $A_{FETON}$), if one of the following conditions occurs:

- When $V_{BAT}$ is > ($V_{UVP}$ + $V_{UVP\_HYS}$) and the discharge load is removed or
- When $V_{BAT}$ is > $V_{UVP}$ and a charger is connected.

The device detects that the charger is attached if ($V_{PACK}$ – $V_{BAT}$) > 700-mV typical. To detect for load removal, the device checks if ($V_{BAT}$ – $V_{PACK}$) < 400-mV typical.

If the UV_SHUT option is disabled, during a UV fault DSG is turned off and the device does not go into SHUTDOWN. The power consumption is reduced to $I_{FETOFF}$. The PACK pin is still internally pulled to VSS through $R_{PACK-VSS}$. To recover UV with this option, one of the following conditions must occur:

- When $V_{BAT}$ is > ($V_{UVP}$ + $V_{UVP\_HYS}$) or
- When $V_{BAT}$ is > $V_{UVP}$ and a charger is connected.

### 8.3.3 Overcurrent in Charge (OCC) Status

The BQ298xyz device detects a current fault by monitoring the voltage drop across an external sense resistor ($R_{SNS}$) between the CS and VSS pins. The device detects an OCC fault when ($V_{CS}$ – VSS) < OCC threshold (–$V_{OC}$). If this condition exists for longer than the OCC delay ($t_{OC}$), the CHG output is driven to $V_{FETOFF}$ to turn off the CHG FET.

The OCC status is released and the CHG output rises to HIGH, that is $V_{CHG}$ = VDD × (1 + $A_{FETON}$), if ($V_{BAT}$ – $V_{PACK}$) > 100 mV, indicating a charger is removed.

### 8.3.4 Overcurrent in Discharge (OCD) and Short Circuit in Discharge (SCD) Status

The BQ298xyz device detects a current fault by monitoring the voltage drop across an external sense resistor ($R_{SNS}$) between the CS and VSS pins. The device applies the same method to detect OCD and SCD faults and applies the same recovery scheme to release the OCD and SCD faults.

The device detects an OCD fault when ($V_{CS}$ – VSS) > OCD threshold (+$V_{OC}$). If this condition exists for longer than the OCD delay ($t_{OC}$), the DSG output is driven to $V_{FETOFF}$ to turn off the DSG FET. The SCD detection is similar to OCD, but uses the SCD threshold ($V_{SCD}$) and SCD delay ($t_{SCD}$) time.

During an OCD or SCD state, the device turns on the recovery detection circuit. An internal current sink ($I_{PACK\ –\ VDD}$) is connected between the PACK and VDD pins, and the device consumes $I_{OC\_REC}$ during the OCD and SCD fault until recovery is detected.

The OCD or SCD status is released and the DSG output rises to HIGH, that is $V_{DSG}$ = VDD × (1 + $A_{FETON}$), if ($V_{BAT}$ – $V_{PACK}$) < 400 mV, indicating a discharge load is removed.

### 8.3.5 Overtemperature (OT) Status

The device has a built-in internal temperature sensor for OT protection. The sensor detects OT when the internal temperature measurement is above the internal overtemperature threshold ($T_{OT}$). If this condition exists for longer than the OT delay ($t_{OT}$), both CHG and DSG outputs are driven to $V_{FETOFF}$ to turn off the CHG and DSG FETs.

The OT state is released and the CHG and DSG outputs rise to HIGH, that is $V_{CHG}$ and $V_{DSG}$ = VDD × (1 + $A_{FETON}$), if the internal temperature measurement falls below ($T_{OT}$ – $T_{OT\_HYS}$).

### 8.3.6 Charge and Discharge Driver

The device has a built-in charge pump to support high-side protection using an NFET. When the drivers are on, the CHG and DSG pins are driven to the VDD × (1 + $A_{FETON}$) voltage level. This means the Vgs across the CHG or DSG FET is about (VDD × $A_{FETON}$). When the drivers are turned off and VDD ≥ $V_{0INH}$ , the CHG and/or DSG output is driven to $V_{FETOFF}$.

The charge pump requires VDD > $V_{DRIVER\_SHUT}$ to operate. When VDD falls below $V_{DRIVER\_SHUT}$-$V_{DRIVER\_SHUT\_HYS}$, the DSG output is off. The CHG output can be turned on in BQ2980 if the ZVCHG charging condition is met. See *Section 8.3.9* for more details.

### 8.3.7 CTR for FET Override and Device Shutdown

The CTR pin is an active-high input pin, which can be controlled by the host system to turn off both CHG and DSG outputs momentarily to reset the system, shut down the system for low-power storage, or as a necessary shutdown if the host detects a critical system error.

The CTR pin uses a 4.5-s timer (same specification tolerance as the $t_{OVP}$ delay 4.5-s option) to differentiate a reset and shutdown signal. CHG and DSG are off when $V_{CTR}$ > CTR $V_{IH}$ for > 200 µs. Counting from the start of

$V_{CTR}$ > $V_{IH}$, if $V_{CTR}$ drops below $V_{IL}$ within 3.6 s, CHG and DSG simply turn back on. If CTR remains HIGH for > 5.4 s, the device enters SHUTDOWN mode.

With this timing control, the system designer can use an RC circuit to implement either a host-controlled power-on-reset or a system shutdown.

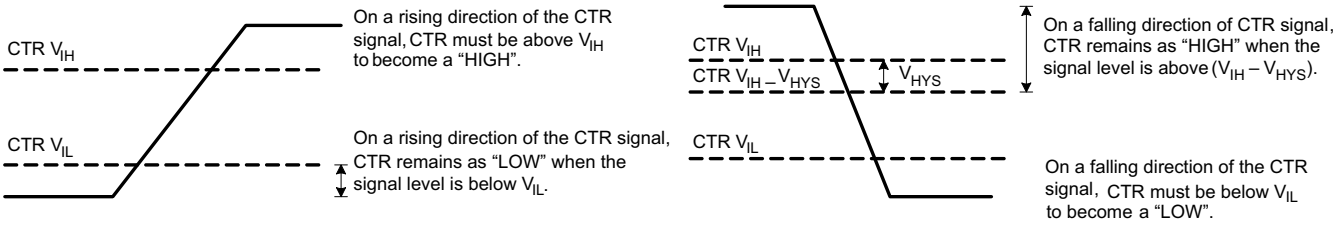



**Figure 8-1. CTR Level in Rising and Falling Direction**

**Note**

- CTR shuts down the device only when $V_{CTR}$ is HIGH for > 5.4 s AND when there is no OV or OT fault present.
- The CTR $V_{IH}$ level is the voltage level at which the CTR pin is considered HIGH in the positive direction as voltage increases. There is a minimum hysteresis designed into the logic level; therefore, as voltage decreases, CTR is considered HIGH at the ($V_{IH}$ – $V_{HYS}$) level.
- The FET override and the shutdown functions are not available if the CTR pull-up is enabled. See *Section 8.3.8* for details.

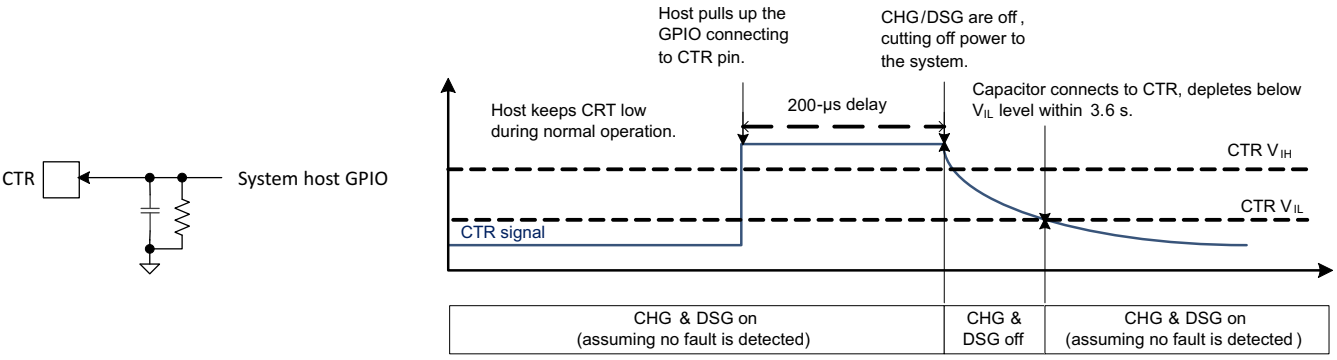



**Figure 8-2. System Reset Function Implementation**

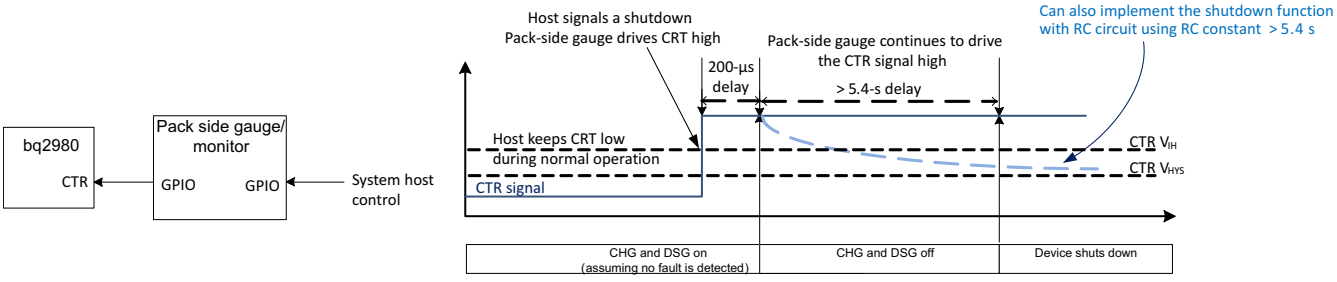



**Figure 8-3. Potential System- Controlled Shutdown Implementation**

### 8.3.8 CTR for PTC Connection

If any of the CTR pull-up resistors are selected, the device assumes a PTC is connected to the CTR pin. There are three internal pull-up options: 1.5 MΩ, 5 MΩ, or 8 MΩ. The internal pull-up allows a PTC to be connected between the CTR pin and VSS. This turns the CTR pin to detect an overtemperature fault through an external PTC, as shown in Figure 8-4.

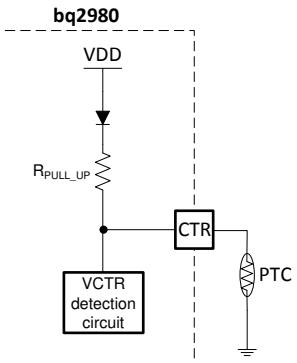





**Figure 8-4. Connecting PTC to CTR Pin for Overtemperature Protection**

When any of the CTR internal pull-up resistors are selected (factory configured), an active-high signal ($V_{CTR}$ > CTR $V_{IH}$) on CTR turns off both CHG and DSG outputs, but it does not shut down the device.

As temperature goes up, the PTC resistance increases and when the voltage divided by the internal $R_{PULL\_UP}$ and the $R_{PTC}$ is > CTR $V_{IH}$, the CHG and DSG outputs are turned off. As temperature falls and the PTC resistance decreases, the CHG and DSG outputs turn back on when ($V_{CTR}$ < CTR $V_{IL}$).

### 8.3.9 ZVCHG (0-V Charging)

ZVCHG (0-V charging) is a special function that allows charging a severely depleted battery that is below the FET driver charge pump shutdown voltage ($V_{DRIVER\_SHUT}$). The BQ2980 has ZVCHG enabled, while the BQ2982 device has it disabled.

In BQ2980, if $V_{BAT}$ > $V_{0INH}$ and VDD < $V_{DRIVER\_SHUT}$-$V_{DRIVER\_SHUT\_HYS}$ and the charger voltage at PACK+ is > $V_{0CHGR}$, then the CHG output will be driven to the voltage of the PACK pin, allowing charging. ZVCHG mode in the BQ2980 is exited when $V_{BAT}$ > $V_{DRIVER\_SHUT}$, at which point the charge pump is enabled, and CHG transitions to being driven by the charge pump. In the BQ2982, ZVCHG is entirely disabled, so charging is disabled whenever VDD < $V_{DRIVER\_SHUT}$ –$V_{DRIVER\_SHUT\_HYS}$.

For BQ2980 and BQ2982, when the voltage on VDD is below $V_{0INH}$, the CHG output becomes high impedance, and any leakage current flowing through the CHG FET may cause this voltage to rise and reenable charging. If this is undesired, a high impedance resistor can be included between the CHG FET gate and source to overcome any leakage and ensure the FET remains disabled in this case. This resistance should be as high as possible while still ensuring the FET is disabled, since it will increase the device operating current when the CHG driver is enabled. Because gate leakage is typically extremely low, a gate-source resistance of 50 MΩ to 100 MΩ may be sufficient to overcome the leakage.

## 8.4 Device Functional Modes

### 8.4.1 Power Modes

#### *8.4.1.1 Power-On-Reset (POR)*

The device powers up in SHUTDOWN mode, assuming a UV fault. To enter NORMAL mode, both $V_{BAT}$ and $V_{PACK}$ must meet the UV recovery requirement. In summary, if UV_SHUT is enabled, ($V_{BAT}$ > $V_{UVP}$) and $V_{PACK}$ detecting a charger connection are required to enter NORMAL mode. If UV_SHUT is disabled, ($V_{BAT}$ > $V_{UVP}$) and ($V_{PACK}$ > the minimum value of VDD) are required to enter NORMAL mode. See *Section 8.4.1.4* for more details.

During the ZVCHG operation mode (only available in BQ2980), the CHG pin is internally connected to PACK when the device is in SHUTDOWN mode. If both $V_{BAT}$ and $V_{PACK}$ meet the ZVCHG condition (see *Section 8.3.9* for details), CHG is on, even if UV recovery conditions are not met.

#### 8.4.1.2 NORMAL Mode

In NORMAL mode, all configured protections are active. No fault is detected, and both CHG and DSG drivers are enabled. For the BQ298x device, if none of the internal CTR pull-up resistor options is selected, $V_{CTR}$ must be < CTR $V_{IL}$ for CHG and DSG to be on.

#### 8.4.1.3 FAULT Mode

If a protection fault is detected, the device enters FAULT mode. In this mode, the CHG or DSG driver is pulled to $V_{FETOFF}$ to turn off the CHG or DSG FETs.

#### 8.4.1.4 SHUTDOWN Mode

This mode is the lowest power-consumption state of the device, with both CHG and DSG turned off.

The two conditions to enter SHUTDOWN mode are as follows:

- Undervoltage (UV): If the device is configured with UV_SHUT enabled, when UV protection is triggered, the device enters SHUTDOWN mode. See *Section 8.3.2* for details.
- CTR control: When CTR is HIGH for > 5.4 s, the device enters SHUTDOWN mode. See *Section 8.3.7* for details.

**Note**

If the internal CTR pull-up is enabled, a HIGH at CTR does not activate the shutdown process. This is because when the internal pull-up is enabled, the CTR pin is configured for use with an external PTC for overtemperature protection, and the CTR functionality is disabled.

# 9 Application and Implementation

**Application Information Disclaimer**

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Test Circuits for Device Evaluation

1. *Test Power Consumption (Test Circuit 1)*

   This setup is suitable to test for device power consumption at different power modes. VS1 is a voltage source that simulates a battery cell. VS2 is used to simulate a charger and load under different power mode conditions.

   I1 is a current meter that monitors the device power consumption at different modes. I2 is a current meter that monitors the PACK pin current. The $I_{PACK}$ current is insignificant in most operation modes. If a charger is connected (VS2 has a positive voltage), but the device is still in SHUTDOWN mode, I2 reflects the $I_{PACK}$ current drawing from the charger due to the internal $R_{PACK-VSS}$ resistor.
2. *Test CHG and DSG Voltage and Status (Test Circuit 2)*

   This setup is suitable to test $V_{CHG}$ and $V_{DSG}$ levels or monitor the CHG and DSG status at different operation modes. It is not suitable to measure power consumption of the device, because the meters (or scope probes) connected to CHG and/or DSG increase the charge pump loading beyond the normal application condition. Therefore, the current consumption of the device under this setup is greatly increased.
3. *Test for Fault Protection (Test Circuit 3)*

   This setup is suitable to test OV, UV, OCD, OCD, and SCD protections.

Voltage protection:

Adjust VS1 to simulation OV and UV. TI recommends having 0 V on VS3 during the voltage test to avoid generating multiple faults. Adjust VS2 to simulate the charger/load connection or disconnection. Combine with test circuit 1 to monitor power consumption, or combine with test circuit 2 to monitor CHG and DSG status.

Test example for OV fault and OV recovery by charger removal:

a. Adjust both VS1 and VS2 > OVP threshold.
b. As the device triggers for OVP and CHG is open, VS2 can be set to a maximum expected charger voltage as if in an actual application when CHG is open, and charger voltage may regulate to the maximum setting.
c. To test for OV recovery, adjust VS1 below ($V_{OVP}$ – $V_{OVP\_Hys}$). Reduce the VS2 voltage so that (VS2 – VS1) < 100 mV (to emulate removal of a charger).

Current protection:

Similar to the voltage protection test, adjust VS3 to simulate OCC, OCD, and SCD thresholds. Use VS2 to simulate a charger/load status. TI recommends setting VS1 to the normal level to avoid triggering multiple faults.

**Note**

It is normal to observe CHG or DSG flipping on and off if VS2 is not set up properly to simulate a charger or load connection/disconnection, especially when the voltage source is used to simulate fault conditions. It is because an improper VS2 setting may mislead the device to sense a recovery condition immediately after a fault protection is triggered.

4. *Test for CTR Control (Test Circuit 4)*

This setup is suitable to test for CTR control. Adjust VS4 above or below the CTR $V_{IH}$ or $V_{IL}$ level. Combine with test circuit 1 to observe the power consumption, or combine with test circuit 2 to observe the CHG and DSG status.

### 9.1.2 Test Circuit Diagrams

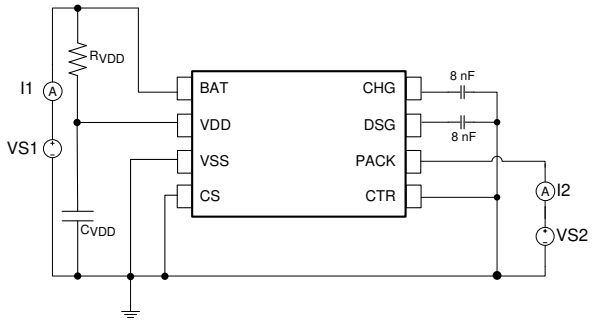



**Figure 9-1. Test Circuit 1**

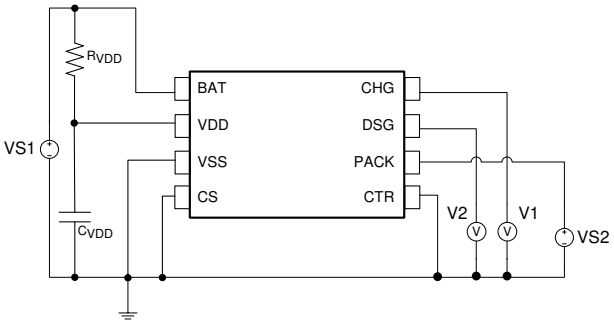



**Figure 9-2. Test Circuit 2**

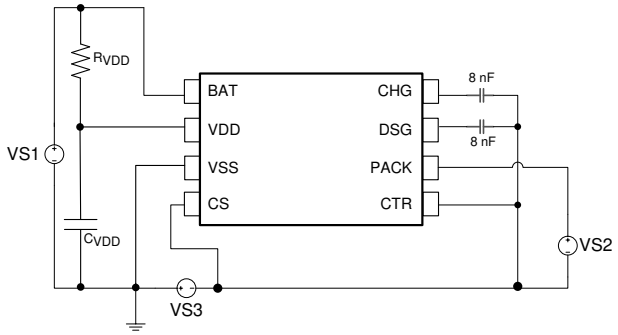





**Figure 9-3. Test Circuit 3**

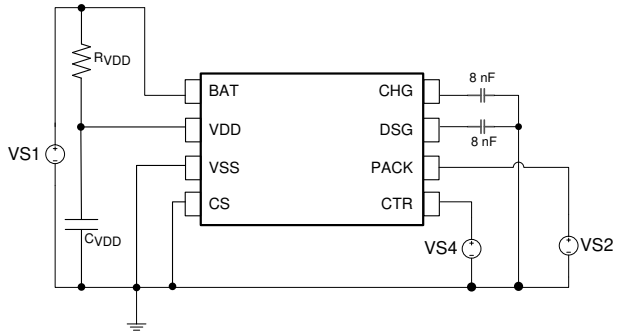





**Figure 9-4. Test Circuit 4**

### 9.1.3 Using CTR as FET Driver On/Off Control

Normally, CTR is not designed as a purely on/off control of the FET drivers, because there is a timing constriction on the pin. The following is a list of workarounds to implement the CTR as an on/off switch to the FET drivers.

1. *Switching CTR from high to low with less than 3.6 s:*

   If the application only requires turning off the FET drivers in < 3.6 s, then the CTR pin can simply be viewed as an on/off switch of the FET drivers. That means, after the CTR pin is pulled high, the application will pull the CTR pin back low in < 3.6 s.
2. *Applying a voltage on PACK to prevent the device from entering SHUTDOWN mode:*

   When the CTR pin is be pulled high for > 3.6 s, there is a chance the device may go into SHUTDOWN mode. If the CTR pin is high for > 5.4 s, the device will be in SHUTDOWN mode. For applications that may use the CTR to keep the FET drivers off for > 3.6 s, the workaround is to keep $V_{PACK}$ within the VDD recommended operating range while the CTR is pulled high to prevent the device from entering SHUTDOWN mode. The device is forced to stay in NORMAL mode with this method.

   Because the PACK pin is also connected to the PACK terminal, the system designer should have a blocking diode to protect the GPIO (that controls the CTR pin) from high voltage.

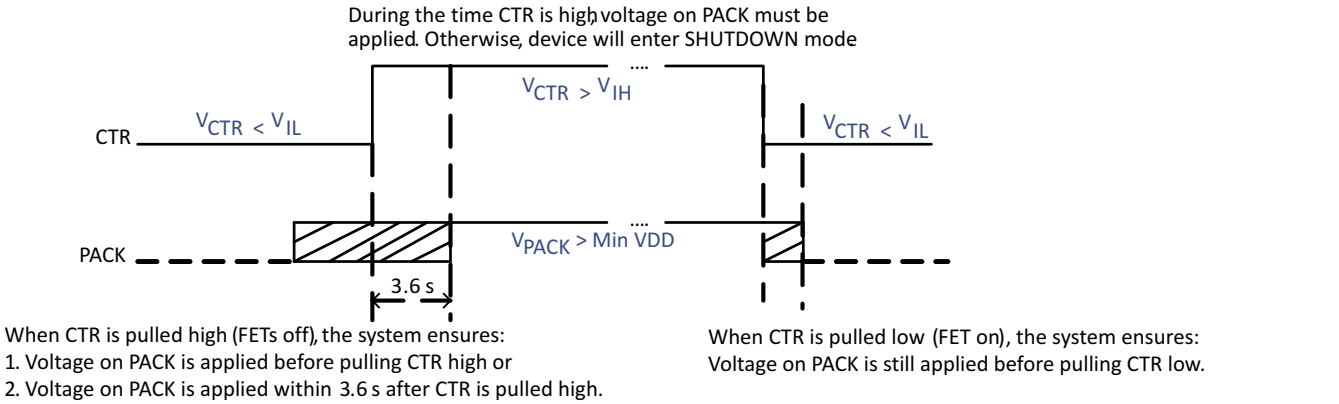





**Figure 9-5. PACK Voltage Timing with Switching CTR as On/Off Control of FET Drivers**

## 9.2 Typical Applications

### 9.2.1 BQ298x Configuration 1: System-Controlled Reset/Shutdown Function

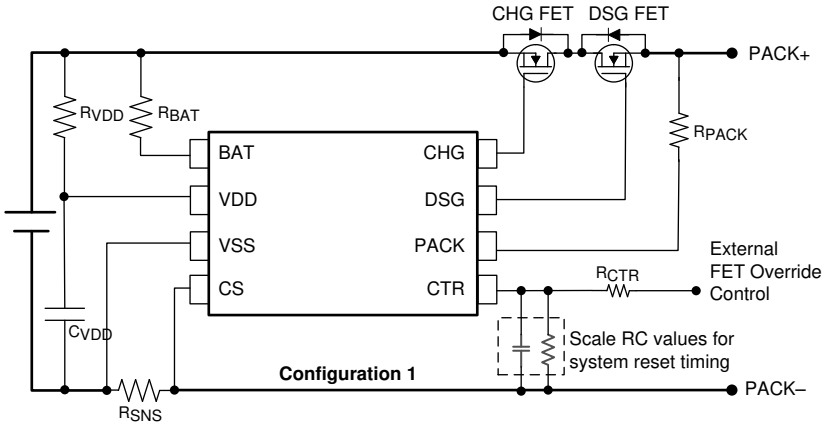



**Figure 9-6. BQ298x Reference Schematic Configuration 1**

#### *9.2.1.1 Design Requirements*

For this design example, use the parameters listed Table 9-1.

**Table 9-1. Recommended Component Selection**

| PARAMETER | | TYP | MAX | UNIT | COMMENT |
|---|---|---|---|---|---|
| $R_{PACK}$ | PACK resistor | — | 2 | kΩ | This resistor is used to protect the PACK pin from a reserve charging current condition. |
| $R_{VDD}$ | VDD filter resistor | — | 300 | Ω | |
| $C_{VDD}$ | VDD filter capacitor | 0.1 | 1 | μF | |
| $R_{BAT}$ | BAT resistor (for safety. To limit current if BAT pin is shorted internally) | 20 | — | Ω | This resistor limits current if the BAT pin is shorted to ground internally. BAT is used for voltage measurement for OV and UV. A larger resistor value can impact the voltage measurement accuracy. |
| $R_{CTR}$ | CTR resistor (optional for ESD) | 100 | — | Ω | This is optional for ESD protection and is highly dependent on the PCB layout. |

#### *9.2.1.2 Detailed Design Procedure*

- Determine if a CTR for FET override or an improved voltage measurement function is required in the battery pack design.
- See Figure 9-6 for the schematic design.
- Check the cell specification and system requirement to determine OV and UV levels.
- Define the sense resistor value and system requirement to determine OCC, OCD, and SCD levels. For example, with a 1-mΩ sense resistor and OCC, OCD, and SCD, the requirement is 6 A, 8 A, and 20 A, respectively. The OCC threshold should be set to 6 mV, the OCD threshold should be at 8 mV, and the SCD threshold should be at 20 mV.
- Determine the required OT protection threshold. The OT fault turns off the CHG and the DSG, so the threshold must account for the highest allowable charge and discharge temperature range.
- When a decision is made on the various thresholds, search for whether a device configuration is available or contact the local sales office for more information.

#### *9.2.1.3 Selection of Power FET*

The high-side driver of the BQ298x device limits the Vgs below 8 V with a 4.4-V battery cell. This means the device can work with a power FET with an absolute maximum rating as low as ±8 V Vgs, which is common in smartphone applications.

Additionally, TI highly recommends using a low gate leakage FET around 6-V to 7-V Vgs range. The power FET on the BQ298x evaluation module has the following typical gate leakage. TI recommends selecting a similar gate leakage FET for the design.

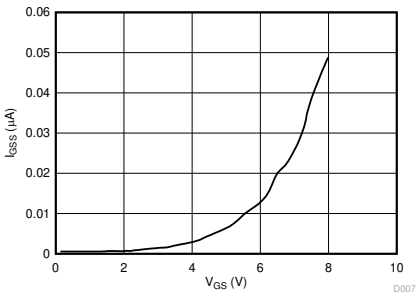



**Figure 9-7. Power FET (on BQ2980 EVM) Gate Leakage Versus Vgs**

### *9.2.1.4 Application Curves*

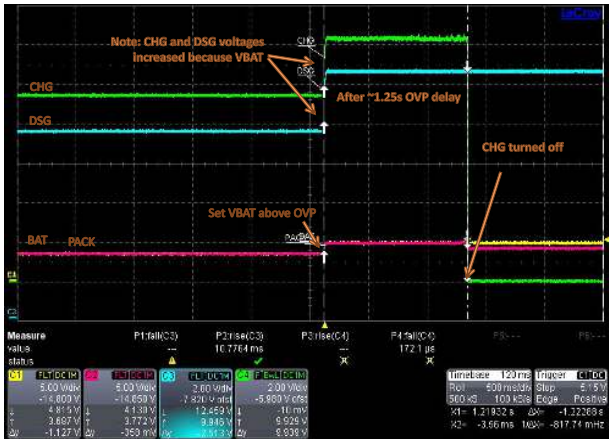



**Figure 9-8. Overvoltage (OV) Protection**

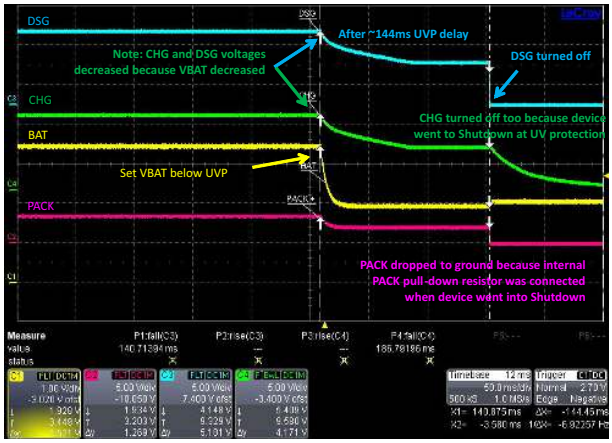



**Figure 9-9. Undervoltage (UV) Protection**

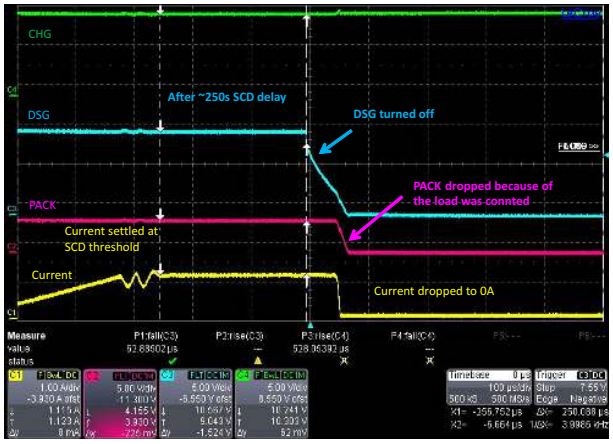
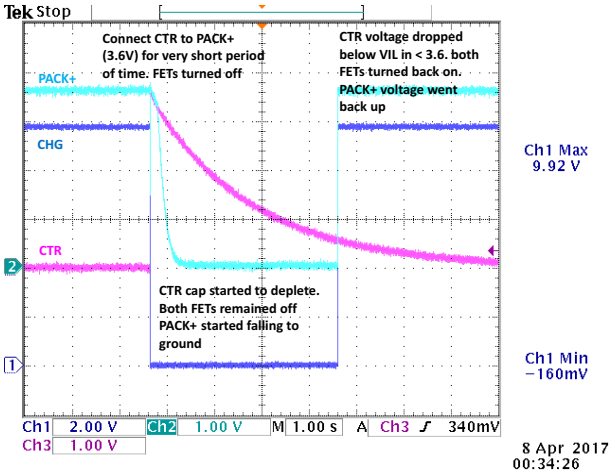
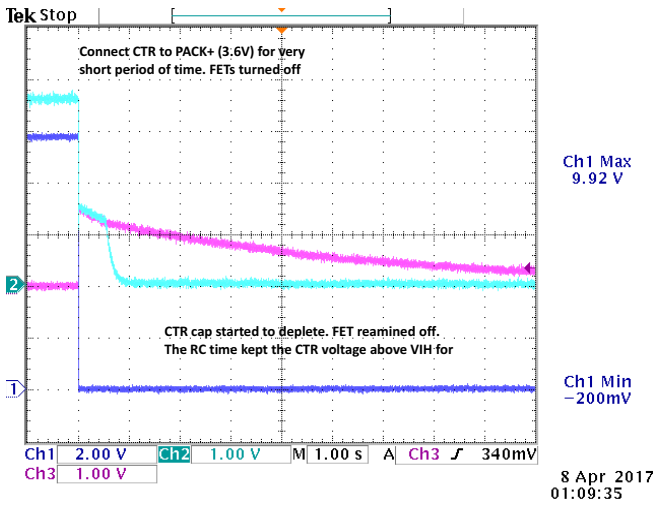



**Figure 9-10. Short Circuit (SCD) Protection**




The RC values used in this example are for reference only. System designers should depend on their pull-up voltage and RC tolerance to add any additional margin. TI also recommends users keep the delay time below 3.6 s, if possible, for the reset function.

**Figure 9-11. Setup CTR for System Reset (Using 5 MΩ and 1 µF RC)**




The RC values used in this example are for reference only. System designers should depend on their pull-up voltage and RC tolerance to add any additional margin. TI also recommends users keep the delay time below 5.4 s, if possible, for the shutdown function.

**Figure 9-12. Setup CTR for System Shutdown (Using 5 MΩ and 1 µF RC)**

### 9.2.2 BQ298x Configuration 2: CTR Function Disabled

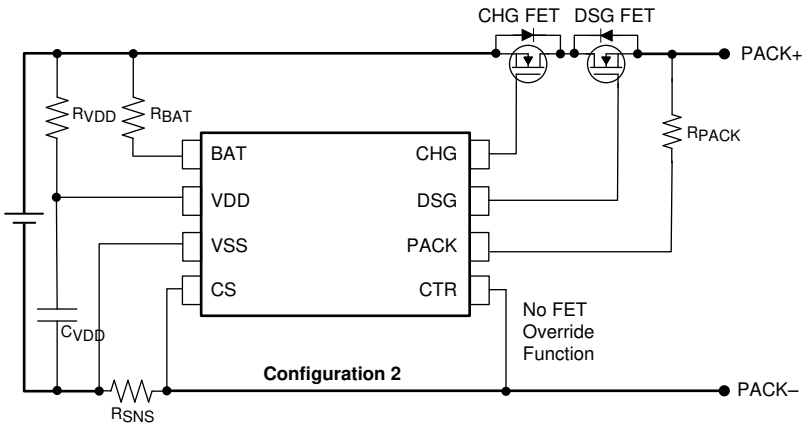



**Figure 9-13. BQ298x Reference Schematic Configuration 2**

### 9.2.3 BQ298x Configuration 3: PTC Thermistor Protection

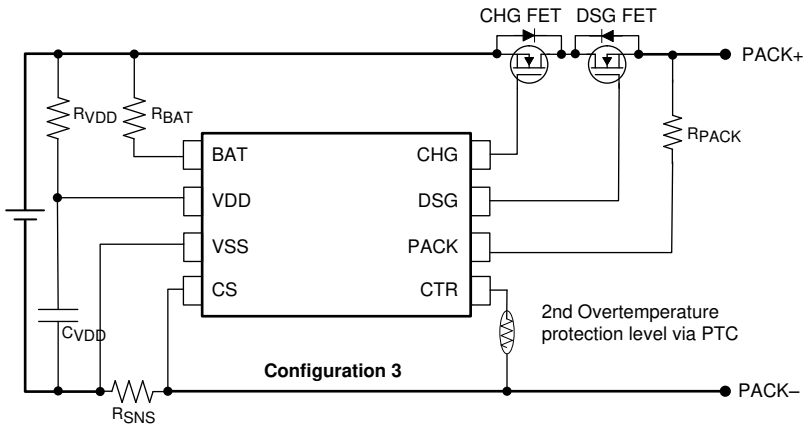



**Figure 9-14. BQ298x Reference Schematic Configuration 3**

## 10 Power Supply Recommendations

The device supports single-cell li-ion and li-polymer batteries of various chemistries with a maximum VDD below 5.5 V.

## 11 Layout

### 11.1 Layout Guidelines

1. Place the components to optimize the layout. For example, group the high-power components like cell pads, PACK+ and PACK– pads, power FETs, and $R_{SNS}$ together, allowing the layout to optimize the power traces for the best thermal heat spreading.
2. Separate the device's VSS and low-power components to a low-current ground plane. Both grounds can meet at $R_{SNS}$.
3. Place the VDD RC filter close to the device's VDD pin.

### 11.2 Layout Example

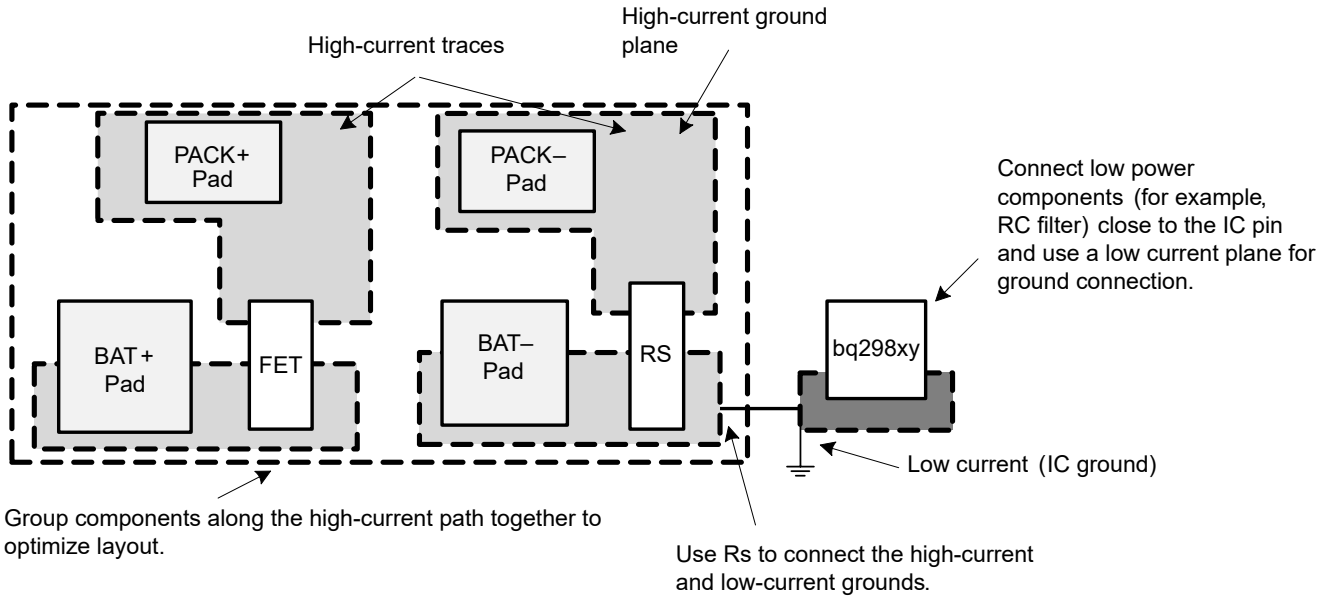



**Figure 11-1. Component Placement and Grounding Pattern Example**

# 12 Device and Documentation Support

## 12.1 Third-Party Products Disclaimer

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## 12.4 Trademarks

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## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ298000RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I | Samples |
| BQ298000RUGT | ACTIVE | X2QFN | RUG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I | Samples |
| BQ298006RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 06 | Samples |
| BQ298006RUGT | ACTIVE | X2QFN | RUG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 06 | Samples |
| BQ298009RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 09 | Samples |
| BQ298009RUGT | ACTIVE | X2QFN | RUG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 09 | Samples |
| BQ298010RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 10 | Samples |
| BQ298010RUGT | ACTIVE | X2QFN | RUG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 10 | Samples |
| BQ298012RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 12 | Samples |
| BQ298012RUGT | ACTIVE | X2QFN | RUG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 12 | Samples |
| BQ298015RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 15 | Samples |
| BQ298015RUGT | ACTIVE | X2QFN | RUG | 8 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 15 | Samples |
| BQ298018RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 18 | Samples |
| BQ298019RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 5I 19 | Samples |
| BQ298215RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 82 15 | Samples |
| BQ298216RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 82 16 | Samples |
| BQ298217RUGR | ACTIVE | X2QFN | RUG | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 82 17 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

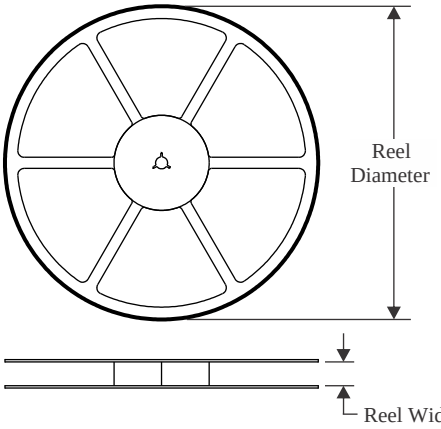
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

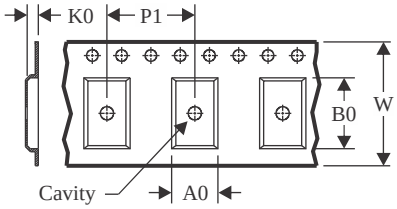
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

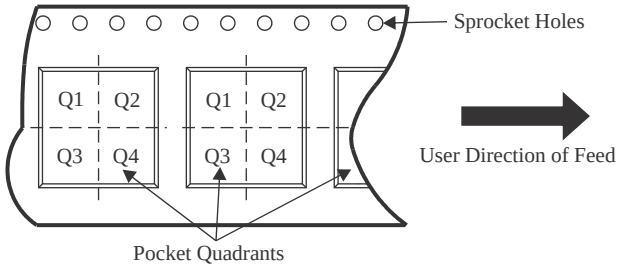



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

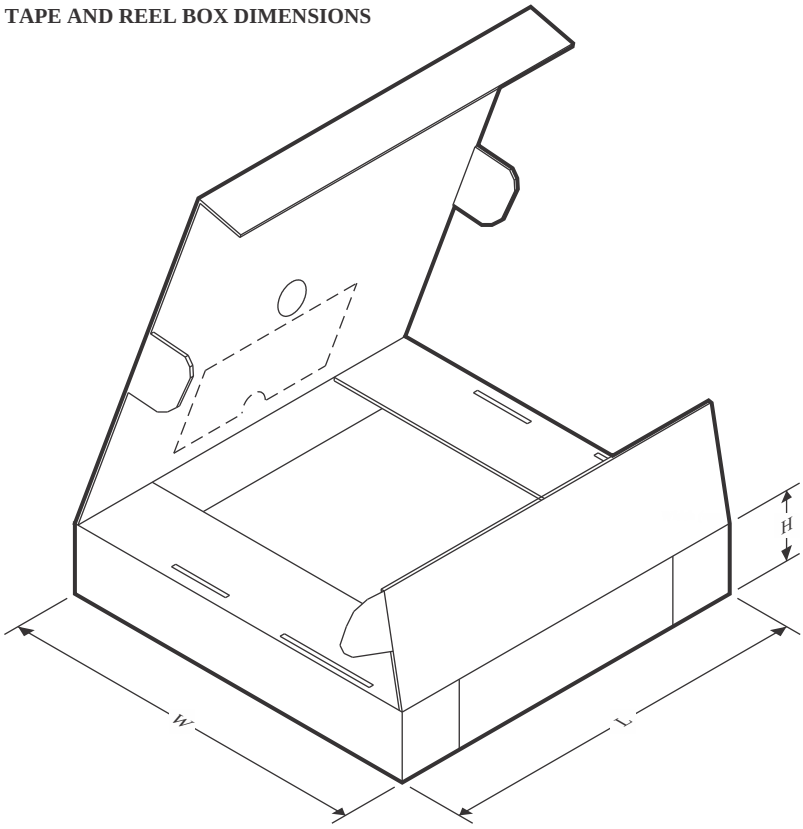



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ298000RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298000RUGT | X2QFN | RUG | 8 | 250 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298006RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298006RUGT | X2QFN | RUG | 8 | 250 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298009RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298009RUGT | X2QFN | RUG | 8 | 250 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298010RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298010RUGT | X2QFN | RUG | 8 | 250 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298012RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298012RUGT | X2QFN | RUG | 8 | 250 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298015RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298015RUGT | X2QFN | RUG | 8 | 250 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298018RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298019RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298215RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |
| BQ298216RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ298217RUGR | X2QFN | RUG | 8 | 3000 | 180.0 | 9.5 | 1.69 | 1.69 | 0.63 | 4.0 | 8.0 | Q2 |

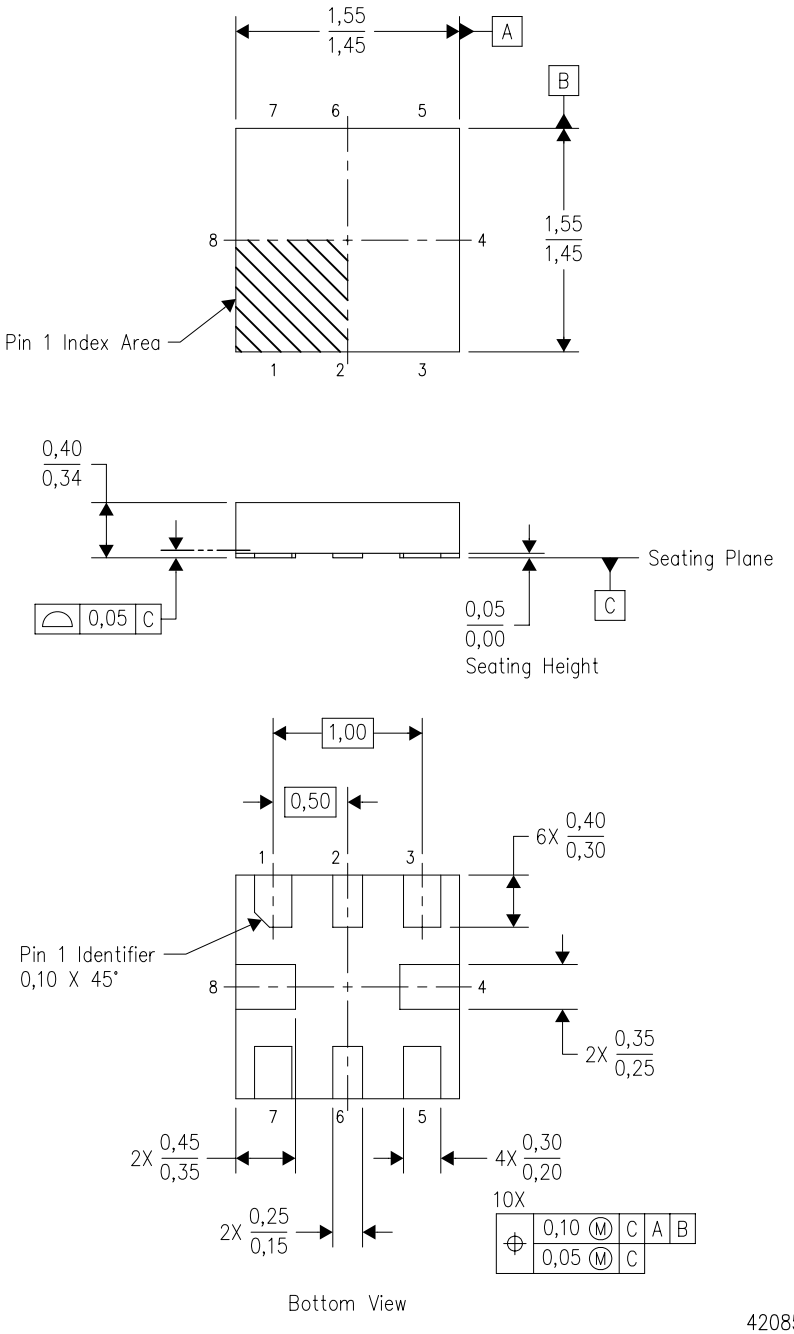
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ298000RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298000RUGT | X2QFN | RUG | 8 | 250 | 189.0 | 185.0 | 36.0 |
| BQ298006RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298006RUGT | X2QFN | RUG | 8 | 250 | 189.0 | 185.0 | 36.0 |
| BQ298009RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298009RUGT | X2QFN | RUG | 8 | 250 | 189.0 | 185.0 | 36.0 |
| BQ298010RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298010RUGT | X2QFN | RUG | 8 | 250 | 189.0 | 185.0 | 36.0 |
| BQ298012RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298012RUGT | X2QFN | RUG | 8 | 250 | 189.0 | 185.0 | 36.0 |
| BQ298015RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298015RUGT | X2QFN | RUG | 8 | 250 | 189.0 | 185.0 | 36.0 |
| BQ298018RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298019RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298215RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298216RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |
| BQ298217RUGR | X2QFN | RUG | 8 | 3000 | 189.0 | 185.0 | 36.0 |

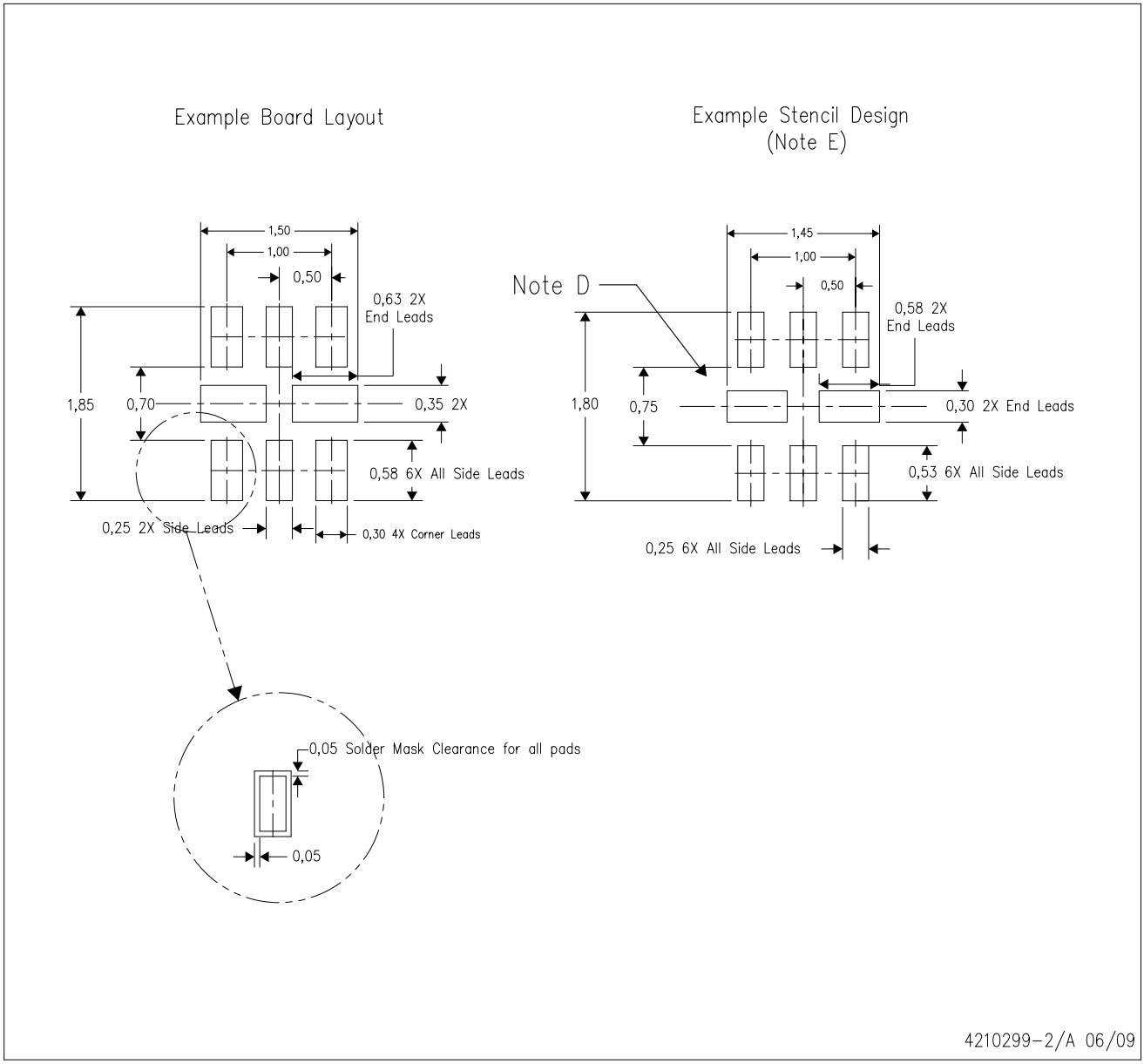
RUG (S–PQFP–N8) PLASTIC QUAD FLATPACK




4208528–2/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2ECD.

RUG (R–PQFP–N8)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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