



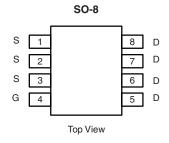
N-Channel 30-V MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
30	0.0045 at V _{GS} = 10 V	20	24			
	0.006 at $V_{GS} = 4.5 \text{ V}$	17	24			

FEATURES

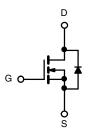
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- 100 % R_g Tested





Ordering Information: Si4430BDY-T1-E3 (Lead (Pb)-free)

Si4430BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_A = 25$ °C, unles	ss otherwise r	noted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Dunin Courset /T 150 °C\	T _A = 25 °C	- I _D	20	14	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		16	11	
Pulsed Drain Current		I _{DM}	± 60		Α
Continuous Source Current (Diode Conduction) ^a		I _S	2.7	1.40	
Avalanche Current	L = 0.1 mH	I _{AS}	40 80		
Single Pulse Avalanche Energy	L=0.1 IIII	E _{AS}			mJ
M	T _A = 25 °C	P _D	3.0	1.6	W
Maximum Power Dissipation ^a	T _A = 70 °C] ' D	2.0	1.0	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55	i to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana la matica to Ambient (MOCFET)	t ≤ 10 s	R _{thJA}	34	41	1
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State	' ¹thJA	67	80	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	19	

Notes

a. Surface Mounted on 1" x 1" FR4 board.

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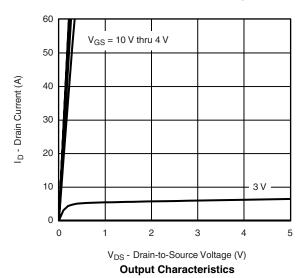
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		3.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Cuvvant		V _{DS} = 30 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 70 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
		V _{GS} = 10 V, I _D = 20 A		0.0037	0.0045	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$		0.0048	0.006	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		80		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 2.7 A, V _{GS} = 0 V		0.72	1.1	V	
Dynamic ^b	•			•			
Total Gate Charge	Q_g			24	36		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$		10.5		nC	
Gate-Drain Charge	Q_{gd}			7.5			
Gate Resistance	R_g		0.5	1.1	1.7	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		14	22		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		60	90	ns	
Fall Time	t _f			18	30		
Course Ducin Double Double Time	t _{rr}	L = 2.7 A dl/dt = 100 A/···		35	50		
Source-Drain Reverse Recovery Time	Q _{rr}	$I_F = 2.7 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$	1/αι = 100 Ανμδ		50	nC	

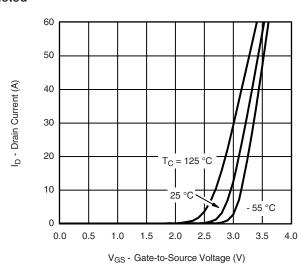
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

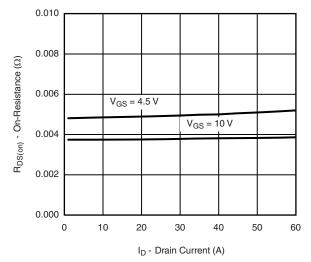




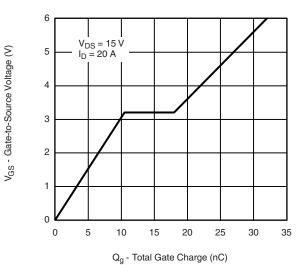




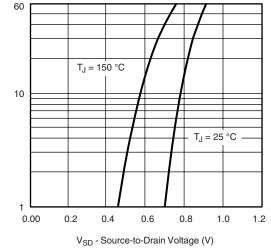
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



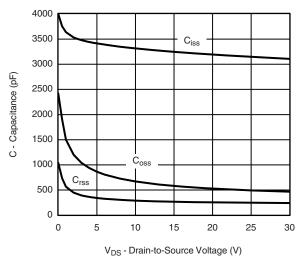
On-Resistance vs. Drain Current



Gate Charge

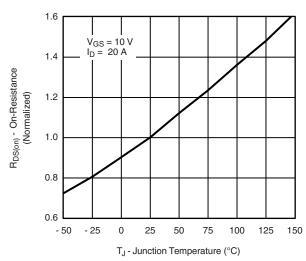


Source-Drain Diode Forward Voltage

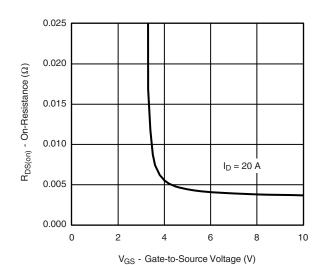


VDS Brain to Godice Voltage (V





On-Resistance vs. Junction Temperature



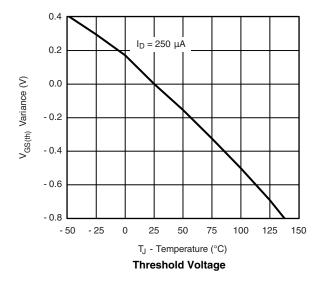
On-Resistance vs. Gate-to-Source Voltage

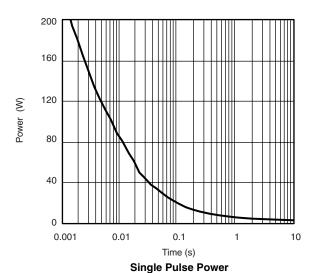
Is - Source Current (A)

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





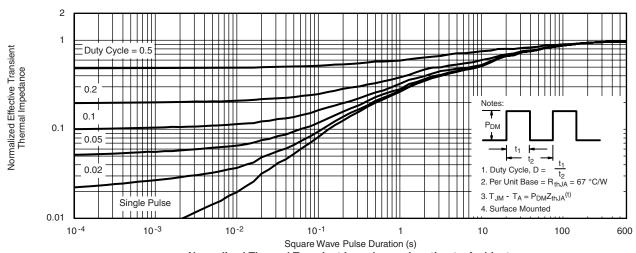
 $\label{eq:VDS} V_{DS} - Drain-to-Source Voltage (V) $$^*V_{GS} > minimum V_{GS} \ at \ which \ R_{DS(on)} \ is \ specified$

DC

100



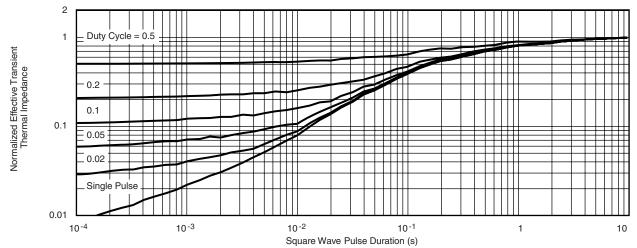
0.01 **L**



Normalized Thermal Transient Impedance, Junction-to-Ambient



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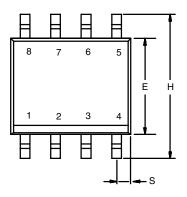


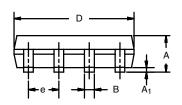
Normalized Thermal Transient Impedance, Junction-to-Foot

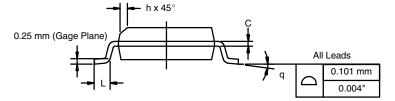
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

APPLICATION NOTE



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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