



Phase-Locked Loop Clock Driver with 4 Clock Outputs

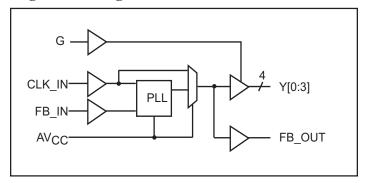
Product Features

- High-Performance Phase-Locked-Loop Clock Distribution for Networking
- Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Wide range of Clock Frequencies up to 80 MHz
- Package: Plastic 16-pin QSOP Package (Q)

Product Description

The PI6C2504 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM and server applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero.

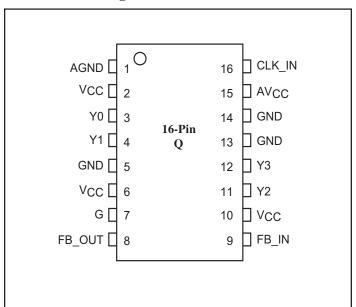
Logic Block Diagram



Functional Table

Inputs	Outputs		
G	Y[0:3]	FB_OUT	
L	L	CLK_IN	
Н	CLK_IN	CLK_IN	

Product Pin Configuration





Pin Functions

Pin Name	Pin No.	Type	Description
CLK_IN	16	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
FB_IN	9	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
G	7	I	Output bank enable. When G is LOW, outputs Y[0:3] are disabled to a logic low state.
FB_OUT	8	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs Yx.
Y[0:3]	3,4,11,12	O	Clock outputs. These outputs provide low-skew copies of CLK_IN Each output has an embedded series-damping resistor.
AV _{CC}	15	Power	Analog power supply. For test purposes, AV_{CC} can be also used to bypass the PLL. When AV_{CC} is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V _{CC}	2, 6, 10	Power	Power supply.
GND	5, 13, 14	Ground	Ground

DC Specifications (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
$V_{\rm I}$	Input voltage range	0.5	V	V
V_{O}	Output voltage range	-0.5	V _{CC} +0.5	V
I _{O_DC}	DC output current		100	mA
Power	Maximum power dissipation at $T_A = 55^{\circ}C$ in still air		1.0	W
T _{STG}	Storage temperature	-65	150	°C

Note: Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Parameter	Test Conditions	V_{CC}	Min.	Тур.	Max.	Units
I_{CC}	$V_{\rm I} = V_{\rm CC}$ or GND; $I_{\rm O} = 0^{(1)}$	3.6V			10	μΑ
C_{I}	$V_{\rm I} = V_{\rm CC}$ or GND	3.3V		4		nΕ
Co	V _O =V _{CC} or GND	3.3 V		6		pF

Note: 1. Continuous Output Current

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply voltage	3.0	3.6	
V_{IH}	High level input voltage	2.0		W
V_{IL}	Low level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	
T _A	Operating free-air temperature	0	70	°C



Electrical Characteristics

(Over recommended operating free-air temperature range Pull Up/Down Currents, $V_{CC} = 3.0V$)

Symbol	Parameter	Condition	Min.	Max.	Units	
І _{ОН}	Pull-up current	$V_{OUT} = 2.4V$		-18		
		$V_{OUT} = 2.0V$		-30		
I_{OL}	Pull-down current	$V_{OUT} = 0.8V$	25		mA	
		$V_{OUT} = 0.55V$	17			

AC Specifications

Timing requirements over recommended ranges of supply voltage and operating free-air temperature

Symbol	Parameter	Min.	Max.	Units
F_{CLK}	Clock frequency	25	80	MHz
Dcyi	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

Switching Characteristics

(Over recommended ranges of supply voltage and operating free-air temperature, CL=30pF)

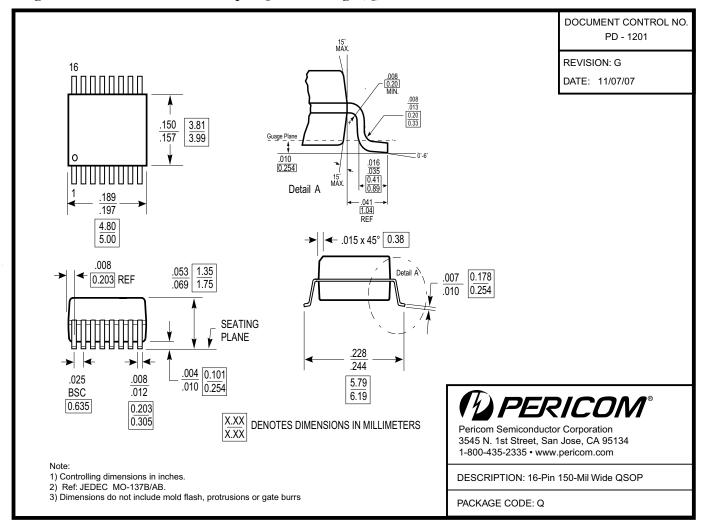
Downson	Every (Instruct)	To (Output)	$V_{\rm CC}$ = 3.3V ±0.3V, 0-70 °C			T I *4
Parameter	From (Input)		Min.	Тур.	Max.	Units
tphase error without jitter	CLK_IN ↑ at 100MHz and 66MHz	FB_IN↑	-150		+150	
Jitter, cycle-to-cycle	At 100 MHz and 66 MHz	Any Y or FB_OUT	-100		+100	ps
Skew, at 100 MHz and 66 MHz	Any Y or FB_OUT				200	
Duty cycle			45		55	%
tr, rise-time, 0.4V to 2.0V				1.0		
tf, fall-time, 2.0V to 0.4V				1.1		ns

Note: These switching parameters are guaranteed by design.

08-0298 PS8380A 11/13/08 3



Package Mechanical Information: 16-pin QSOP Package (Q).



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2504QE	Q16	Pb-Free & Green 16-pin QSOP	Commercial

Notes:

- 1. Thermal characteristics and package top marking information can be found at http://www.pericom.com/packaging/
- 2. E = Pb-free and Green
- 3. X suffix = tape/reel

Pericom Semiconductor Corporation • 1-800-435-2336 • http://www.pericom.com

08-0298 4 PS8380A 11/13/08