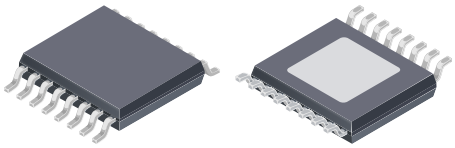
Wide Input Voltage Range, High-Efficiency, Fault-Tolerant LED Driver

FEATURES AND BENEFITS

- Automotive AEC-100 qualified
- Fully integrated 42 V MOSFET for boost converter
- Fully integrated LED current sinks
- Withstands surge input to 40 V_{IN} for load dump
- Operates down to 3.9 V_{IN} (max) for idle stop
- Drives two strings of LEDs
- Maximum output voltage 40 V
  - □ Up to 11 white LEDs in series
- Drive current for each string is 200 mA
- Fixed 2.15 MHz boost switching frequency
- Dithering of boost switching frequency to reduce EMI (A8518 only)
- Extremely high LED contrast ratio
  - □ 10,000:1 using PWM dimming alone
  - □ 100,000:1 when combining PWM and analog dimming
- Excellent input voltage transient response at lowest PWM duty cycle
- Gate driver for optional P-channel MOSFET input disconnect switch

Continued on the next page…

PACKAGE: 16-Pin TSSOP with Exposed Thermal Pad (suffix LP)



Not to scale

DESCRIPTION

The A8518 is a multi-output LED driver for small-size LCD backlighting. It integrates a current-mode boost converter with internal power switch and two current sinks. The boost converter can drive up to 22 white LEDs, 11 LEDs per string, at 200 mA. The LED sinks can be paralleled together to achieve higher LED currents up to 400 mA. The A8518 operates from a single power supply from 4.5 to 40 V, which allows the part to withstand load dump conditions encountered in automotive systems.

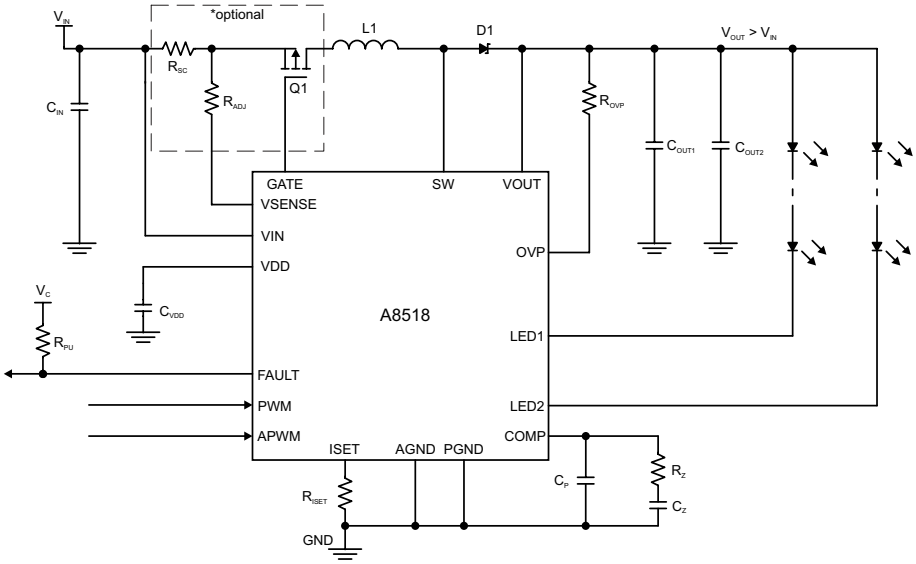
The A8518 can control LED brightness through a digital (PWM) signal. An LED brightness contrast ratio of 10,000:1 can be achieved using PWM dimming at 100 Hz; a higher ratio of 100,000:1 is possible when using a combination of PWM and analog dimming.

If required, the A8518 can drive an external P-channel MOSFET to disconnect input supply from the system in the event of a fault. The A8518 provides protection against output short, overvoltage, open or shorted diode, open or shorted LED pin, and overtemperature. A cycle-by-cycle current limit protects the internal boost switch against high-current overloads.

Continued on the next page…

APPLICATIONS:

- Automotive infotainment backlighting
- Automotive cluster
- Automotive center stack



Typical Application Circuit Showing VOUT-to-Ground Short Protection Using Optional P-Channel MOSFET

FEATURES AND BENEFITS (continued)

- LED current accuracy 0.7%
- LED string current-matching accuracy 0.8%
- Protection against:
  - □ Shorted boost switch, inductor or output capacitor
  - □ Shorted I_{SET} resistor
  - □ Open or shorted LED pins and LED strings
  - □ Open boost diode
  - □ Overtemperature

DESCRIPTION (continued)

The A8518 has a fixed boost switching frequencies of 2.15 MHz. The high switching frequency allows the converter to operate above the AM radio band.

The A8518 offers dithering of boost switching frequency, which helps reduce EMI (electromagnetic interference). The A8518-1 is identical to the A8518, but without the dithering feature.

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A, (°C)	Frequency Dithering	Package	Packaging	Leadframe Plating
A8518KLPTR-T	–40 to 125	Yes	16-Pin TSSOP with exposed thermal pad	4000 pieces per reel	100% matte tin
A8518KLPTR-T-1	–40 to 125	No	16-Pin TSSOP with exposed thermal pad	Contact Factory	100% matte tin

Contact Allegro for additional packing options.

Pb

Table of Contents

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SPECIFICATIONS

Absolute Maximum Ratings [1]

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pins	V_{LEDx}	x = 1 and 2	–0.3 to 40	V
OVP Pin	V_{OVP}		–0.3 to 40	V
VIN, VOUT Pins	V_{IN}, V_{OUT}		–0.3 to 40	V
VSENSE, GATE Pins	V_{SENSE}, V_{GATE}		V_{IN} –7.4 to V_{IN} + 0.4	V
SW Pin [2]	V_{SW}	Continuous	–0.6 to 42	V
		t < 50 ns	–1 to 48	V
FAULT Pin	V_{FAULT}		–0.3 to 40	V
APWM, PWM, COMP, ISET, VDD Pins			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the electrical characteristics table is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
[2] SW DMOS is self-protecting and will conduct when V_{SW} exceeds 48 V.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer 3 in^2 PCB	48.5	°C/W
		On 4-layer PCB based on JEDEC standards	34	°C/W

[3] Additional thermal information available on the Allegro website.

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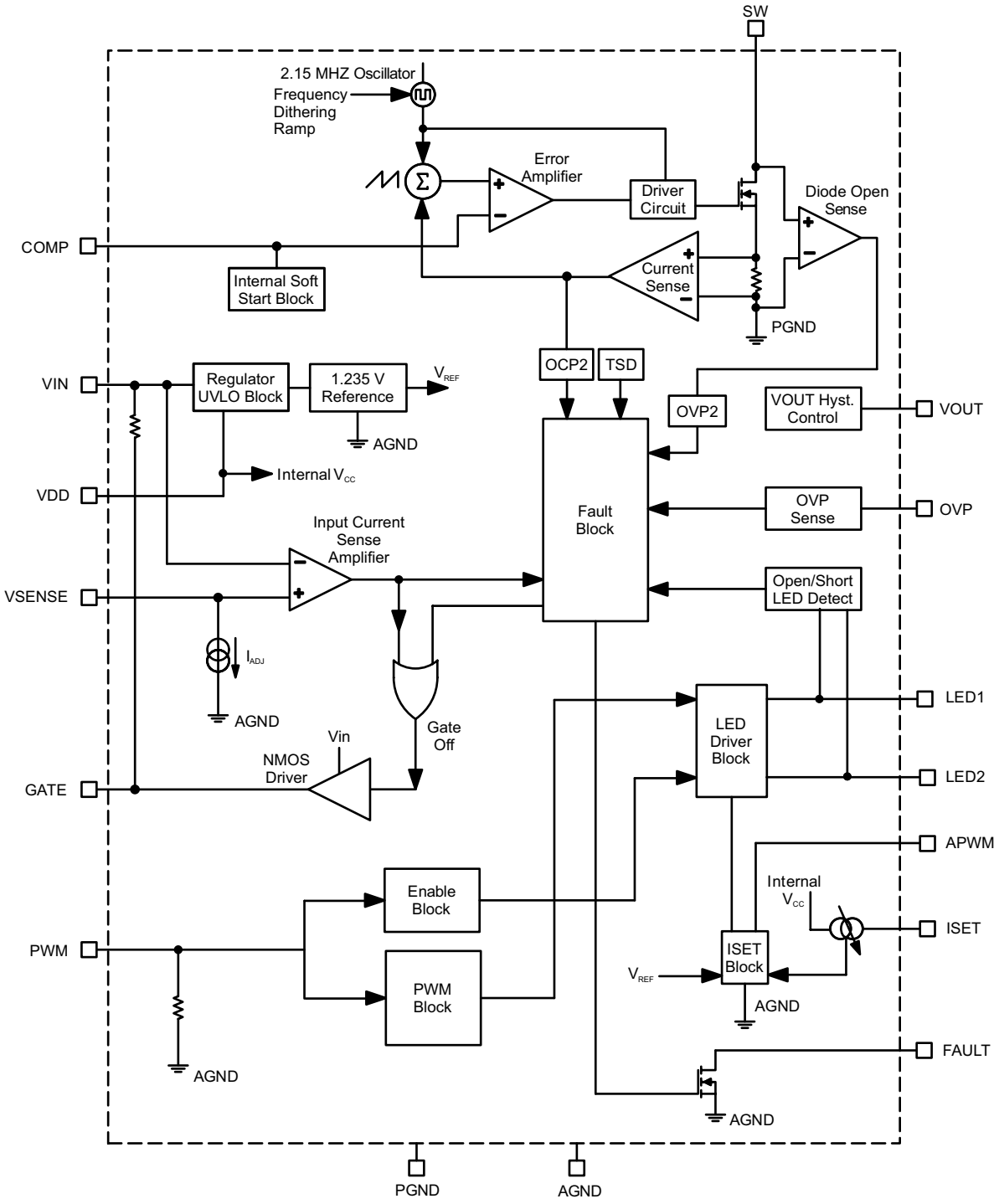

Functional Block Diagram

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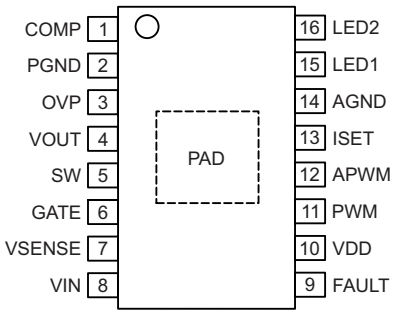
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 16-Pin TSSOP Pinout Diagram

Terminal List Table

Name	Number	Function
1	COMP	Output of the error amplifier and compensation node. Connect a series R_Z-C_Z-C_P network from this pin to GND for control loop compensation.
2	PGND	Power ground for internal N-channel MOSFET switching device.
3	OVP	Overvoltage protection. Connect external resistor from VOUT to this pin to adjust the overvoltage protection level.
4	VOUT	Connect directly to boost output voltage.
5	SW	The drain of the internal N-channel MOSFET switching device of the boost converter.
6	GATE	Output gate driver pin for external P-channel MOSFET control.
7	VSENSE	Connect this pin to the negative sense side of the current sense resistor R_{SC}. The threshold voltage is measured as V_{IN}-V_{SENSE}. There is also fixed current sink to allow for trip threshold adjustment.
8	VIN	Input power to the IC, as well as the positive input used for current sense resistor.
9	FAULT	The pin is an open-drain type configuration that will be pulled low when a fault occurs. Connect a 100 kΩ resistor between this pin and desired logic level voltage.
10	VDD	Output of internal LDO (bias regulator). Connect a 1 µF decoupling capacitor between this pin and GND.
11	PWM	Enables the IC when this pin is pulled high. Also serves to control the LED intensity by using pulse-width modulation. Typical PWM dimming frequency is in the range of 100 to 400 Hz.
12	APWM	Analog trimming option or dimming. Applying a digital PWM signal to this pin adjusts the internal ISET current.
13	ISET	Connect R_{ISET} resistor between this pin and GND to set the desired LED current setting.
14	AGND	LED current ground. Connect to PCB ground plane.
15	LED1	LED current sink #1. Connect the cathode of LED string to associated pin. Unused LEDx pin must be terminated to GND through a 1.54 kΩ resistor.
16	LED2	LED current sink #2. Connect the cathode of LED string to associated pin. Unused LEDx pin must be terminated to GND through a 1.54 kΩ resistor.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the pad.

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ELECTRICAL CHARACTERISTICS [1]: Unless otherwise noted, specifications are valid at V_{IN} = 16 V, T_A = 25°C, • indicates specifications guaranteed over the full operating temperature range with $T_A = T_J$ = –40°C to 125°C, typical specifications are at T_A = 25°C

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE							
Input Voltage Range [3]	V_{IN}		•	4.5	–	40	V
UVLO Start Threshold	$V_{UVLOrise}$	V_{IN} rising	•	–	–	4.35	V
UVLO Stop Threshold	$V_{UVLOfall}$	V_{IN} falling	•	–	–	3.9	V
UVLO Hysteresis	$V_{UVLOHYS}$			300	450	600	mV
INPUT SUPPLY CURRENT							
Input Quiescent Current	I_Q	$V_{PWM} = V_{IH}$, f_{SW} = 2 MHz	•	–	8	15	mA
Input Sleep Supply Current	I_{SLEEP}	V_{IN} = 16 V, V_{PWM} = 0 V	•	–	2	10	µA
INPUT LOGIC LEVELS (PWM, APWM)							
Input Logic Level Low	V_{IL}		•	–	–	0.4	V
Input Logic Level High	V_{IH}		•	1.5	–	–	V
PWM Input Pull-Down Resistor	R_{EN}	V_{PWM} = 5 V		60	100	140	kΩ
APWM Input Pull-Down Resistor	R_{APWM}	$V_{PWM} = V_{IH}$		60	100	140	kΩ
APWM							
APWM Frequency [2]	f_{APWM}		•	40	–	1000	kHz
ERROR AMPLIFIER							
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V		–	–600	–	µA
Sink Current	$I_{EA(SINK)}$	V_{COMP} = 1.5 V		–	+600	–	µA
COMP Pin Pull-Down Resistance	R_{COMP}	FAULT = 0, V_{COMP} = 1.5V		–	1.4	–	kΩ
OVERVOLTAGE PROTECTION							
OVP Pin Voltage Threshold	$V_{OVP(th)}$	OVP pin connected to VOUT	•	7	8.3	9.5	V
OVP Pin Sense Current Threshold	$I_{OVP(th)}$	Current into OVP pin	•	190	200	210	µA
OVP Pin Leakage Current	$I_{OVP(LKG)}$	V_{IN} = 16 V, PWM = L	•	–	0.1	1	µA
OVP Accuracy				–	–	5	%
Undervoltage Protection Threshold	$V_{UVP(th)}$	Measured at VOUT pin when R_{OVP} = 160 kΩ [2]		–	3	–	V
		Measured at VOUT pin when R_{OVP} = 0		–	0.55	0.7	V
Secondary Overvoltage Protection	$V_{OVP(sec)}$	Measured at SW pin	•	42	45	48	V
BOOST SWITCH							
Switch On-Resistance	R_{SW}	I_{SW} = 0.750 A, V_{IN} = 16 V	•	100	250	500	mΩ
Switch Leakage Current	$I_{SW(LKG)}$	V_{SW} = 16 V, $V_{PWM} = V_{IL}$	•	–	0.1	1	µA
Switch Current Limit	$I_{SW(LIM)}$		•	3	3.65	4.5	A
Secondary Switch Current Limit [2]	$I_{SW(LIM2)}$	Higher than max $I_{SW(LIM)}$ under all conditions part latches when detected		~	4.9	–	A
Minimum Switch On-Time	$t_{SW(on)}$		•	45	65	85	ns
Minimum Switch Off-Time	$t_{SW(off)}$		•	–	65	85	ns

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Minimum V_{IN} = 4.5 V is only required at startup. After startup is completed, IC can continue to operate down to V_{IN} = 3.9 V.
[4] LED current is trimmed to cancel variations in both Gain and ISET voltage.

Continued on the next page…

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	f_{SW} measurements were taken with dithering function disabled	•	1.95	2.15	2.35	MHz
LED CURRENT SINKS							
LEDx Accuracy [4]	Err_{LED}	R_{ISET} = 8.33 kΩ	•	–	0.7	3	%
LEDx Matching	Δ_{LEDx}	ISET = 120 µA	•	–	0.8	2	%
LEDx Regulation Voltage	V_{LED}	$V_{LED1} = V_{LED2}$, ISET = 120 µA	•	750	850	975	mV
ISET to ILEDx Current Gain	A_{ISET}	ISET = 120 µA	•	1391	1419	1453	A/A
ISET Pin Voltage	V_{ISET}			0.987	1.017	1.047	V
Allowable ISET Current	I_{ISET}		•	20	–	144	µA
V_{LEDx} Short Detect	$V_{LEDx(SC)}$	While LED sinks are in regulation; sensed from V_{LEDx} to AGND	•	4.7	5.2	5.7	V
LED Startup Ramp Time [2]	t_{SS}	Maximum time duration before all LED channels come into regulation, or OVP is tripped		–	20	–	ms
Maximum PWM Dimming Until Off-Time [2]	t_{PWML}	Measured while PWM = low, during dimming control and internal references are powered on (exceeding t_{PWML} results in shutdown)		–	16	–	ms
Minimum PWM On-Time	$t_{PWMH(min1)}$	First cycle when powering up IC (PWM = 0 to 3.3 V)	•	–	0.75	2	µs
		Subsequent PWM pulses	•	–	0.5	1	µs
PWM High to LED On Delay	$t_{dPWM(on)}$	Time between PWM going high and when LED current reaches 90% of maximum (V_{PWM} = 0 to 3.3 V)	•	–	0.2	0.5	µs
PWM Low to LED Off Delay	$t_{dPWM(off)}$	Time between PWM going low and when LED current reaches 10% of maximum (V_{PWM} = 3.3 to 0 V)	•	–	0.36	0.5	µs
GATE PIN							
Gate Pin Sink Current	I_{GSINK}	$V_{GS} = V_{IN}$, no input OCP fault		–	–113	–	µA
Gate Pin Source Current	$I_{GSOURCE}$	$V_{GS} = V_{IN}$ – 6 V, input OCP fault tripped		–	6	–	mA
Gate Shutdown Delay When Overcurrent Fault Is Tripped [2]	t_{FAULT}	$V_{IN} – V_{SENSE}$ = 200 mV. Monitored at FAULT pin		–	–	3	µs
Gate Voltage	V_{GS}	Measured between GATE and VIN when gate is on		–	–6.7	–	V
VSENSE PIN							
VSENSE Pin Sink Current	I_{adj}		•	17.2	21.5	25.8	µA
VSENSE Trip Point	$V_{SENSE(trip)}$	Measured between VIN and VSENSE, R_{ADJ} = 0	•	95	110	125	mV

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Minimum V_{IN} = 4.5 V is only required at startup. After startup is completed, IC can continue to operate down to V_{IN} = 3.9 V.
[4] LED current is trimmed to cancel variations in both Gain and ISET voltage.

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Fault Pin							
FAULT Pull-Down Voltage	V_{FAULT}	I_{FAULT} = 1 mA		–	–	0.5	V
FAULT Pin Leakage Current	$I_{FAULT(lkg)}$	V_{FAULT} = 5 V		–	–	1	µA
Thermal Protection (TSD)							
Thermal Shutdown Threshold [2]	T_{SD}	Temperature rising		155	170	–	°C
Thermal Shutdown Hysteresis [2]	T_{SDHYS}			–	20	–	°C

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[3] Minimum V_{IN} = 4.5 V is only required at startup. After startup is completed, IC can continue to operate down to V_{IN} = 3.9 V.
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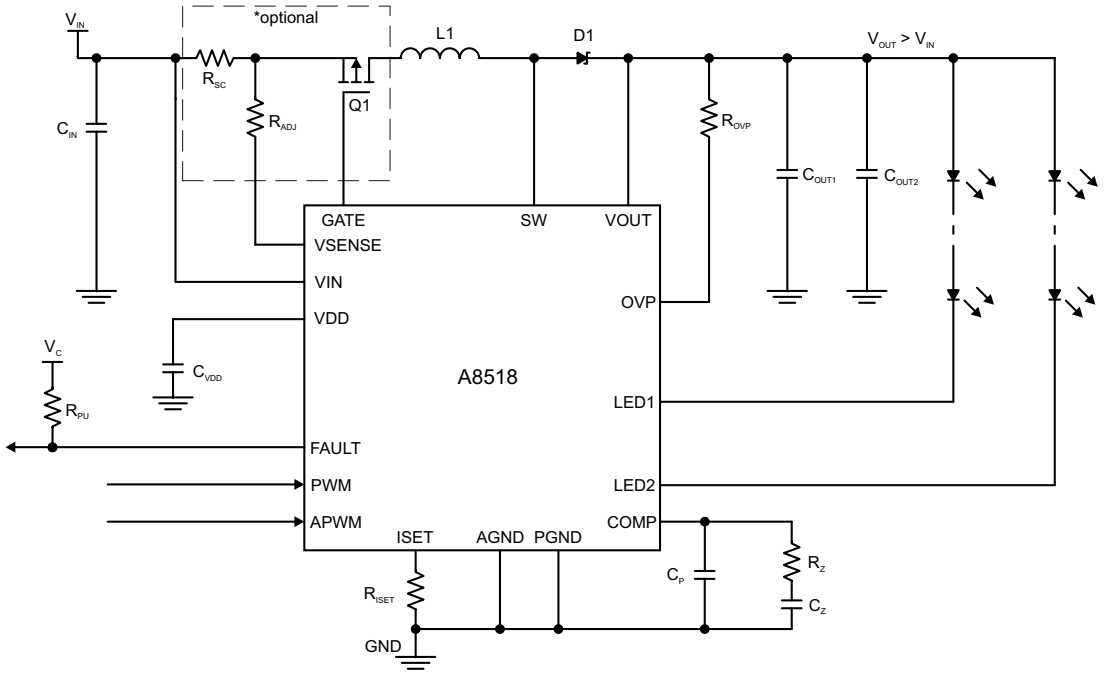
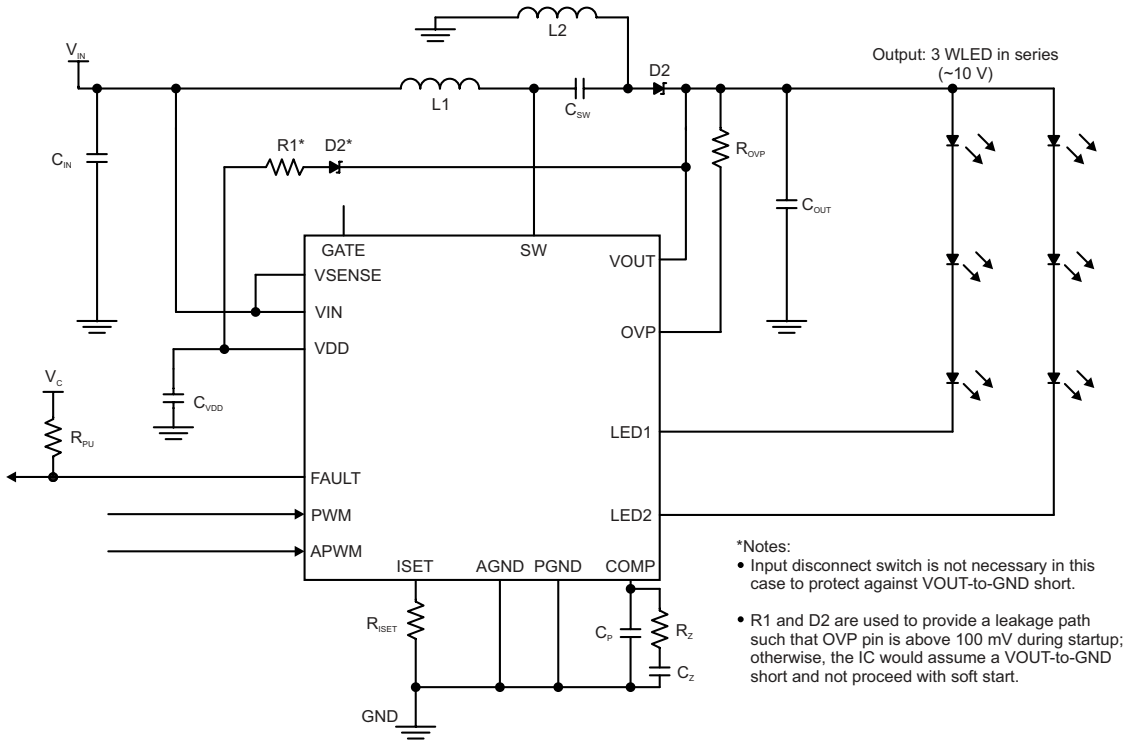


Typical Application Showing Boost Configuration with Input Switch to Protect Against VOUT-to-GND Short



Typical Application Showing SEPIC Configuration for Flexible Input/Output Voltage Ratio

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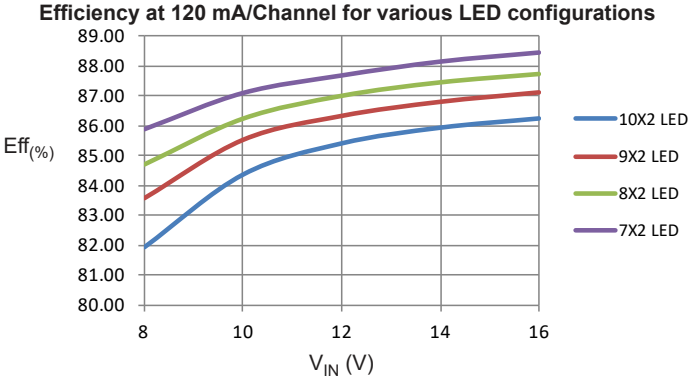
CHARACTERISTIC PERFORMANCE

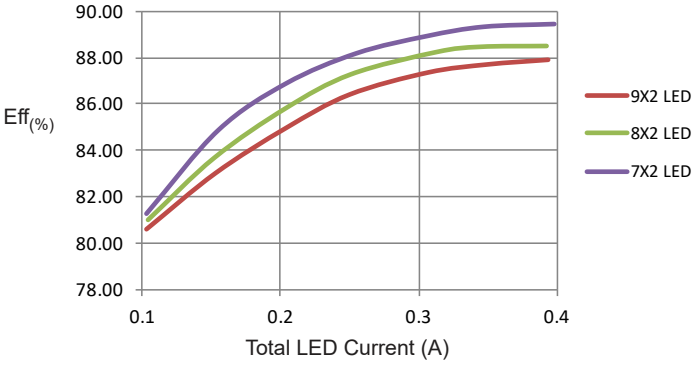
Efficiency Measurement

Efficiency at 120 mA/Channel for various LED configurations



A8518 Evaluation Board Efficiency versus Input Voltage while Disconnect Switch and Snubber Circuit are Used

Efficiency at V_{IN} = 12 V for various LED configurations

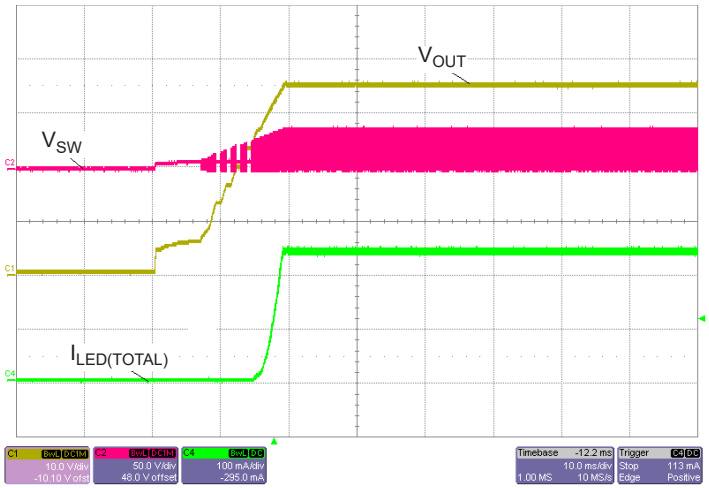


A8518 Evaluation Board Efficiency versus Total LED Current while Disconnect Switch and Snubber Circuit are Used

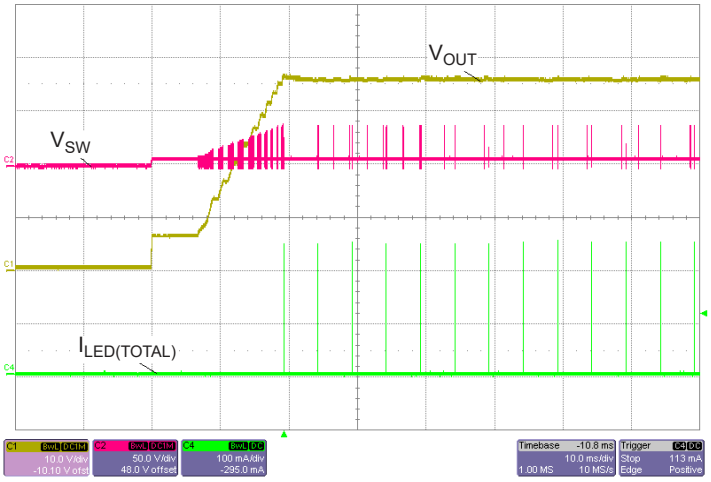
Higher efficiency can be achieved by:

- Using an inductor with a low DCR.
- Using lower forward voltage drop and a smaller junction capacitance Schottky diode.
- Removal of snubber circuit; however, this might compromise the EMI performance.
- Shorting out the disconnect switch and the input current sense resistor; however, this will eliminate the output short-to-GND protection feature.

Startup Waveforms



Start up at 100% PWM Dimming, V_{IN} = 7 V, 2 Channels, 10 LEDs/Channels, 120 mA/Channels; Time base = 10 ms/Div



Start up at 0.02% PWM Dimming at 200 Hz, V_{IN} = 7 V, 2 Channels, 10 LEDs/Channel, 120 mA/Channel; Time base = 10 ms/Div

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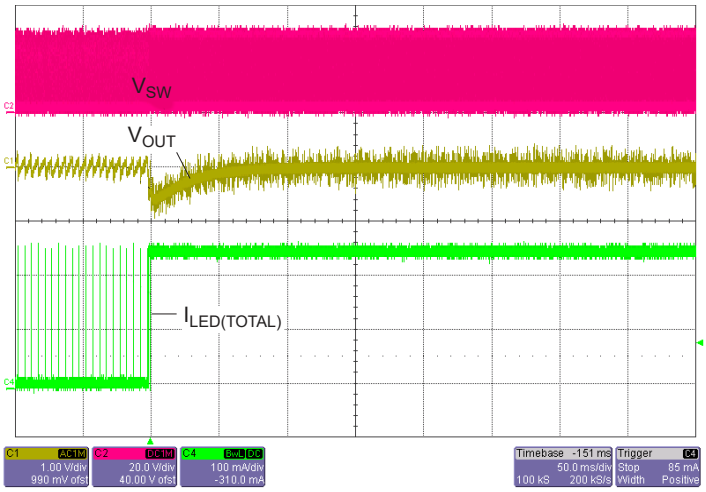
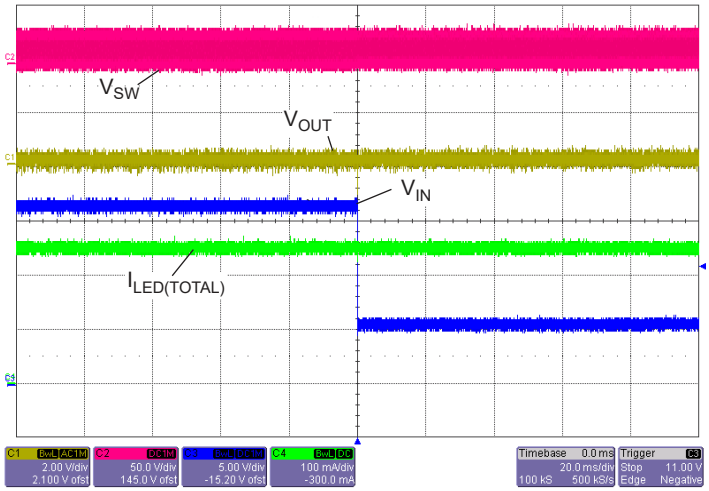
Transient Response to Step Change in PWM Dimming

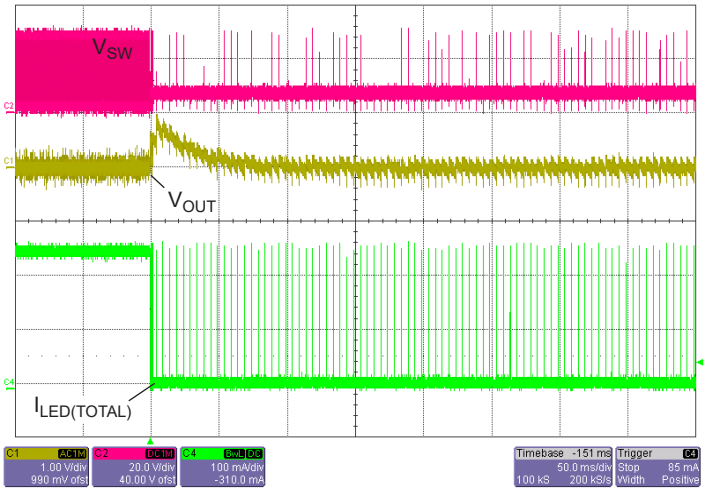


From PWM = 0.1% to PWM = 100% at 120 mA/Channel, V_{IN} = 12 V; Time base = 50 ms/Div

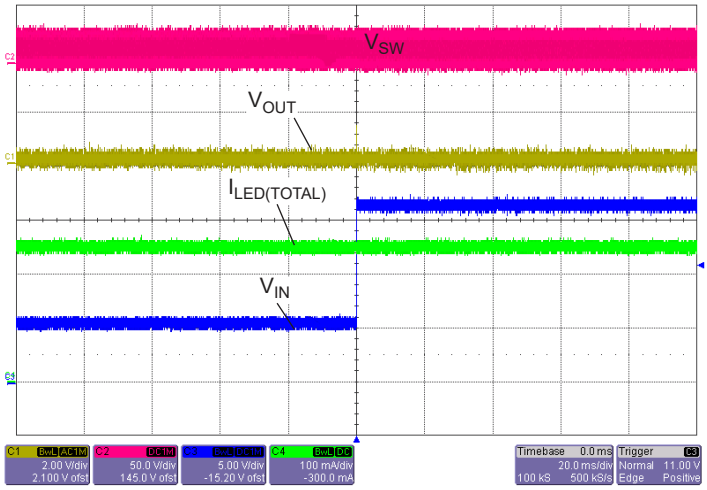
Transient Response to Step Change in V_{IN} Voltage



From V_{IN} = 16 V to V_{IN} = 5.5 V, 2 Ch, 120 mA/Channel, PWM = 100%; Time base = 20 ms/Div



From PWM = 100% to PWM = 0.01% at 120 mA/Channel, V_{IN} = 12 V; Time base = 50 ms/Div



From V_{IN} = 5.5 V to V_{IN} = 16 V, 2 Ch, 120 mA/Channel, PWM = 100%; Time base = 20 ms/Div

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FUNCTIONAL DESCRIPTION

Enabling the IC

The IC turns on when a logic high signal is applied on the PWM pin with a minimum duration of $t_{PWMH(min1)}$ for the first clock cycle, and the input voltage present on the VIN pin is greater than 4.35 V to clear the UVLO threshold. Before the LEDs are enabled, the A8518 driver goes through a system check to see if there are any possible fault conditions that might prevent the system from functioning correctly.

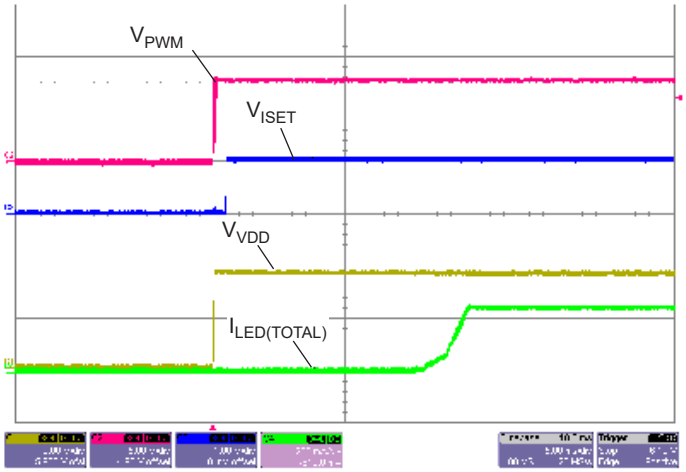

Figure 1: Power-Up Diagram Showing PWM, ISET, VDD Voltages, and LED Current

Once the IC is enabled, there are only two ways to shut down the IC into low-power mode:

1. Pull PWM pin to low for at least 32,750 clock cycles (approximately 16 ms at 2 MHz).
2. Cut off the supply and allow V_{IN} to drop below UVLO falling threshold (less than 3.9 V).

Powering Up: LED Pin Check

Once VIN pin goes above UVLO and a high signal is present on the PWM pin, the IC proceeds to power up. The A8518 then enables the disconnect switch (GATE) and checks to see if the LED pins are shorted to ground and/or are not used. The LED detect phase starts when the GATE voltage of the disconnect switch is equal to V_{IN} – 3.3 V.

Figure 2 shows the relation of LEDx pins with respect to the gate voltage of the disconnect switch (if used) during LED detect phase.

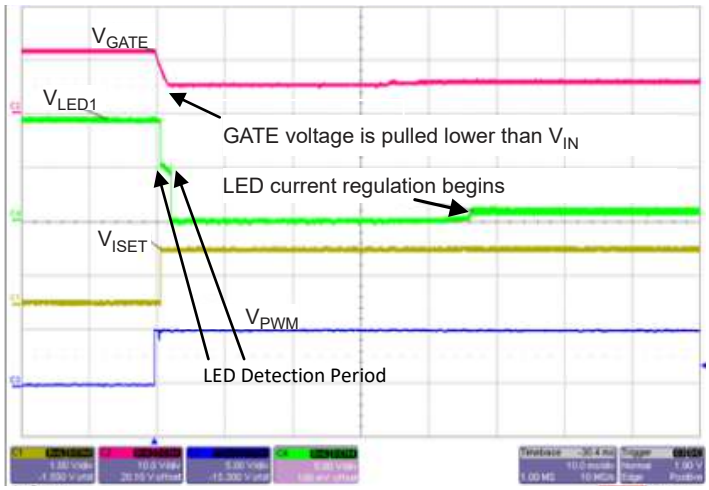

Figure 2: Power Up Diagram Showing Disconnect, V_{GATE}, V_{LED1}, V_{ISET}, and V_{PWM} During LED Pins Detect and Regulation Period

When the voltage on the LEDx pins exceeds 120 mV, a delay between 3000 and 4000 clock cycles (1.5 to 2 ms) is used to determine the status of the pins.

All unused LED pins should be connected with a 1.54 kΩ resistor to GND. The unused pin, with the pull-down resistor, will be taken out of regulation at this point and will not contribute to the boost regulation loop.

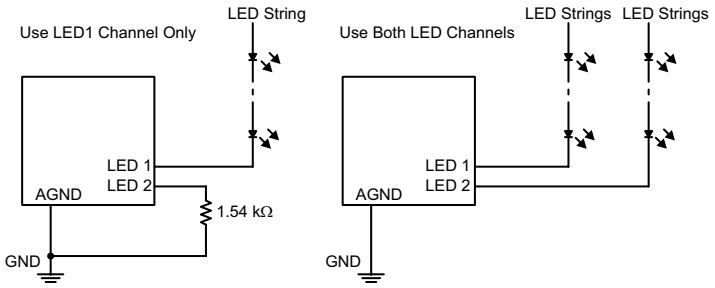

Figure 3: Channel Select Setup

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Table 1: LED Detection Voltage Thresholds

LED Pin Voltage Level	LED Pin	Action
Less than 70 mV	Indicates a short to PCB GND	A8518 will not proceed with power up
150 mV	Not used	LED string connected with the unused LED pin is removed from operation
325 mV	LED pin in use	None

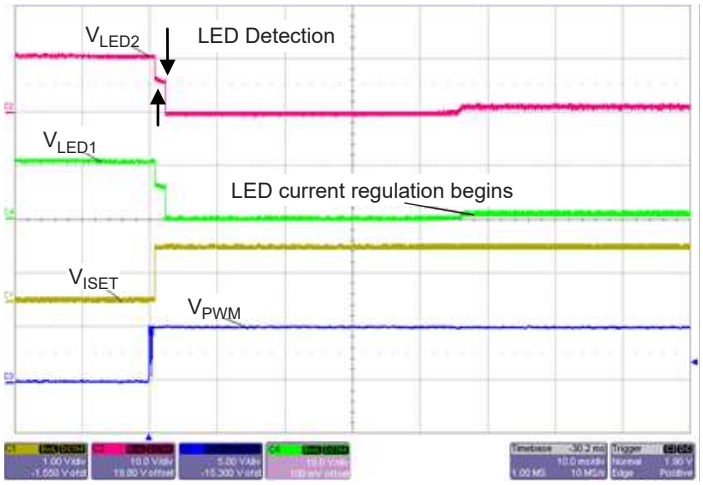

Figure 4: LED String Detect Occurs when Both LEDs are Selected to be Used

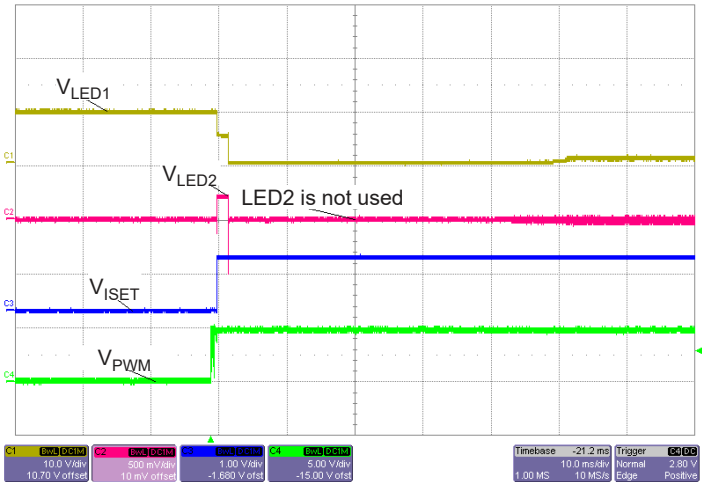

Figure 5: Detect Voltage is about 150 mV when LED Pin 2 is Not Used

If an LED pin is shorted to ground, the A8518 will not proceed with soft-start until the short is removed from the LED pin. This prevents the A8518 from powering up and putting an uncontrolled amount of current through the LEDs.

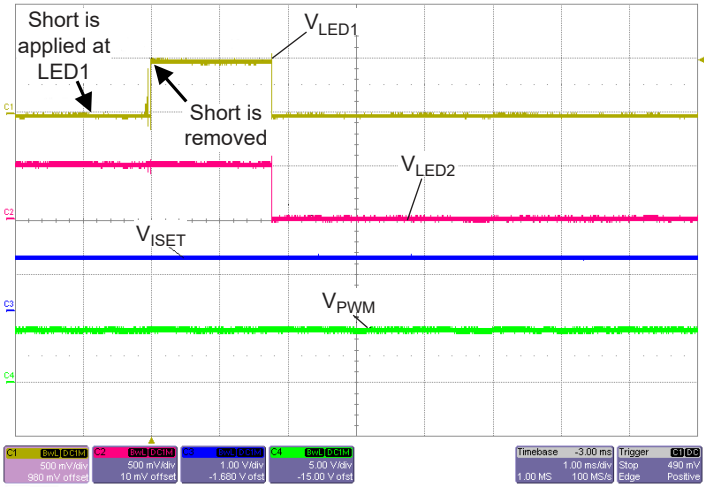

Figure 6: One LED is Shorted to GND.
The IC will not proceed with power up until LED pin is released, at which point the LED is checked to see if it used.

Powering Up: Boost Output Undervoltage Protection

During startup, after the input disconnect switch has been enabled, the output voltage is checked through the OVP pin. If the sensed voltage does not rise above $V_{UVP(th)}$, the output is assumed to be at fault and the IC will not proceed with soft-start.

Undervoltage protection may be caused by one of the following faults:

- Output capacitor shorted to GND
- Boost inductor or diode open
- OVP sense resistor open

After an Output UVP fault has been detected, the A8518 immediately shuts down but does not latch off. It will retry as soon as the UVP fault is removed.

In case of output capacitor shorted to GND fault, however, the high inrush current will also trip the Input OCP fault. This causes the IC to shut down and latch off. To enable the IC again, the PWM pin must be pulled low for at least 32,750 clock cycles (about 16 ms at 2 MHz), then pulled high again.

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Soft-Start Function

During startup, the A8518 ramps up its boost output voltage following a fixed ramp function. This technique limits the input inrush current and ensures the same startup time regardless of PWM duty cycle.

The soft-start process is completed when any one of the following conditions is met:

1. All LED currents have reached regulation target,
2. Output voltage has reached 93% of its OVP threshold, or
3. Soft-start ramp time (t_{SS}) has expired.

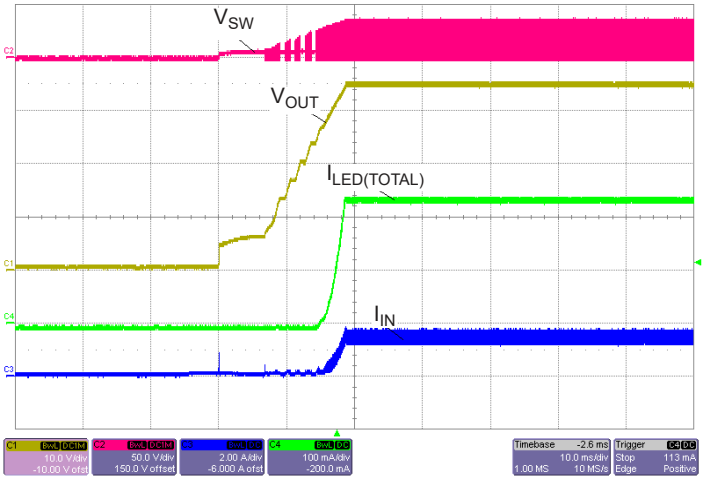

Figure 7: Startup Diagram Showing the Input Current, Output Voltage, Total LED Current, and Switch Node Voltage

LED Current Setting and LED Dimming

The maximum LED current can be up to 200 mA per channel and is set through the ISET pin. To set I_{LED}, calculate R_{ISET} as follows:

$$I_{LED} = I_{ISET} \times A_{ISET}$$

$$I_{ISET} = \frac{V_{ISET}}{R_{ISET}}$$

$$R_{ISET} = \frac{(V_{ISET} \times A_{ISET})}{I_{LED}}$$

where I_{LED} is in A and R_{ISET} is in Ω.

This sets the maximum current through the LEDs, referred to as the 100% current.

Table 2: LED Current Setting Resistors (Values Rounded to the Nearest Standard Resistor Value)

Standard Closest R_{ISET} Resistor Values	LED Current I_{LED}
7.15 kΩ	200 mA per LED
8.87 kΩ	160 mA per LED
11.8 kΩ	120 mA per LED
14.3 kΩ	100 mA per LED
17.8 kΩ	80 mA per LED

PWM Dimming

The LED current can be reduced from the 100% current level by PWM dimming using the PWM pin. When the PWM pin is pulled high, the A8518 turns on and all enabled LEDs sink 100% current. When PWM is pulled low, the boost converter and LED sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active. The typical PWM dimming frequencies fall between 200 Hz and 1 kHz.

The A8518 is designed to deliver a maximum dimming ratio of 10,000:1 at PWM frequency of 100 Hz. That means a minimum PWM duty cycle of 0.01%, or an on-time of just 1 µs out of a period of 10 ms.

High-PWM dimming ratio is achieved by regulating the output voltage during PWM off-time. The VOUT pin samples the output voltage during PWM on-time and regulates it during off-time. A hysteresis control loop brings VOUT higher by approximately 350 mV whenever it drops below the target voltage. In a highly noisy switching environment, it is necessary to insert an RC filter at the VOUT pin. A typical value of R = 10 kΩ and C = 47 pF is recommended.

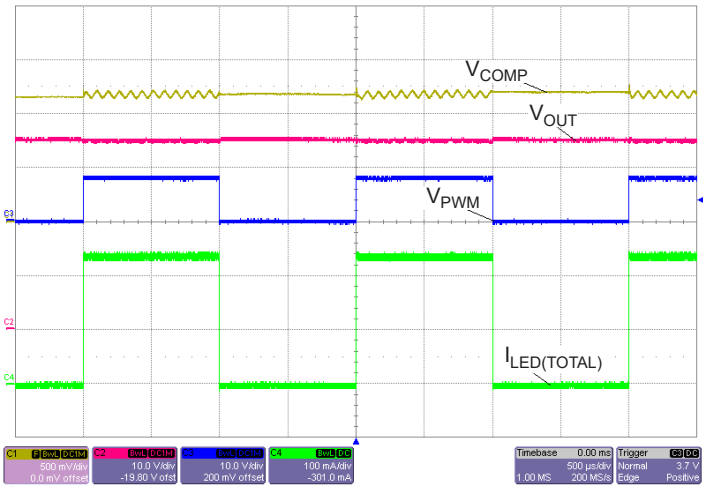

Figure 8: Typical PWM Diagram Showing V_{OUT}, I_{LED}, and COMP Pins, as well as the PWM Signal. (PWM dimming Frequency is 500 Hz 50% duty cycle.)

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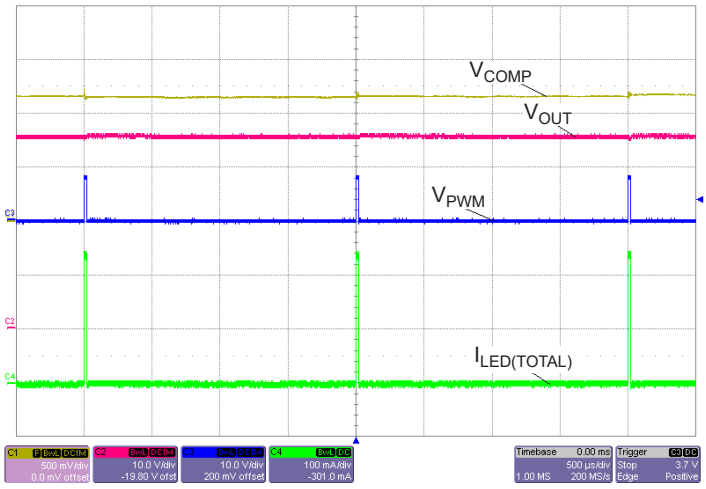

Figure 9: Typical PWM Diagram Showing V_{OUT}, I_{LED}, and COMP Pins, as well as the PWM Signal. (PWM dimming frequency is 500 Hz 1% duty cycle.)

Another important feature of the A8518 is the PWM signal to LED current delay. This delay is typically less than 500 ns, which allows for greater LED current accuracy at low-PWM dimming duty cycles.

The error introduced by LED turn-on delay is partially offset by LED turn-off delay. Therefore, a PWM pulse width of under 1 µs is still feasible, but the percentage error of LED current will increase with narrower pulse width.

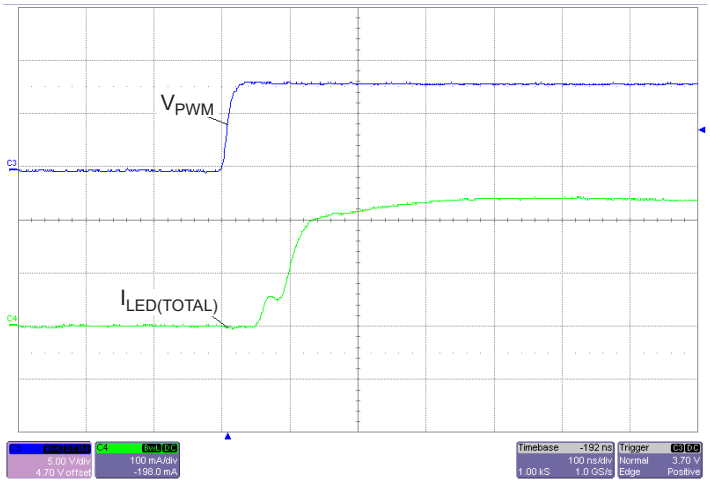

Figure 10: Rising Edge PWM Signal to Total LED Current $I_{LED(TOTAL)}$ Turn-On Delay. Time base = 100 ns

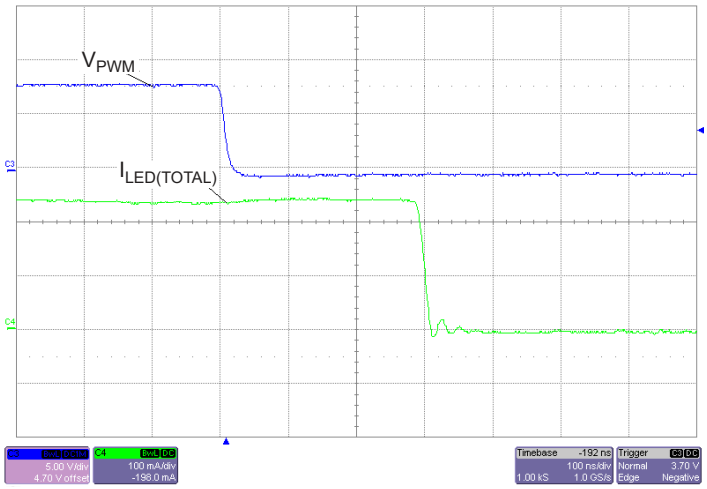

Figure 11: Falling Edge PWM Signal to Total LED Current $I_{LED(TOTAL)}$ Turn-Off Delay. Time base = 100 ns

APWM Pin

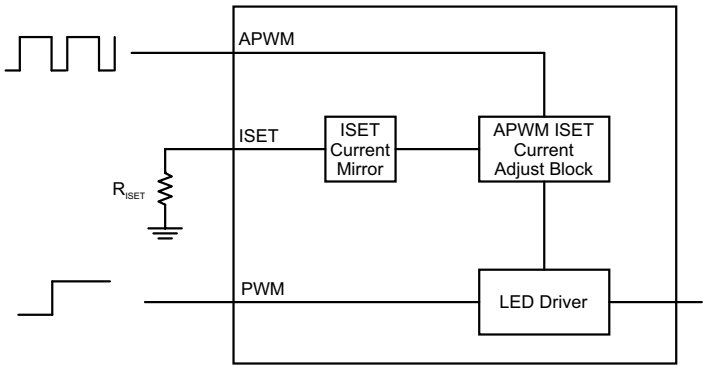

Figure 12: Simplified Block Diagram of APWM ISET Block

The APWM pin is used in conjunction with the ISET pin (see Figure 12). This is a digital signal pin that internally adjusts the I_{ISET} current. The typical input signal frequency is between 40 kHz and 1 MHz. The duty cycle of this signal is inversely proportional to the percentage of current that is delivered to the LED (see Figure 13). As an example, a system that delivers $I_{ILED(TOTAL)}$ = 240 mA would deliver $I_{ILED(TOTAL)}$ = 180 mA when an APWM signal with a duty cycle of 25% is applied. When this pin is not used it should be tied to AGND.

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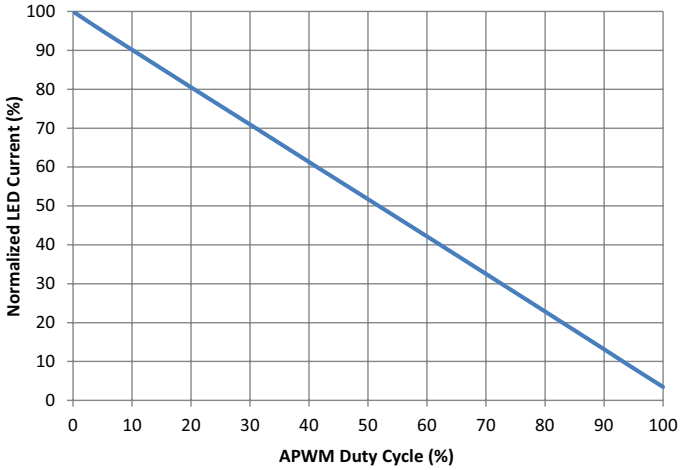

Figure 13: Normalized LED Current vs. APWM Duty Cycle
V_{IN} = 9 V, V_{OUT} = ~22 V, R_{ISET} = 24 kΩ, APWM = 200 kHz

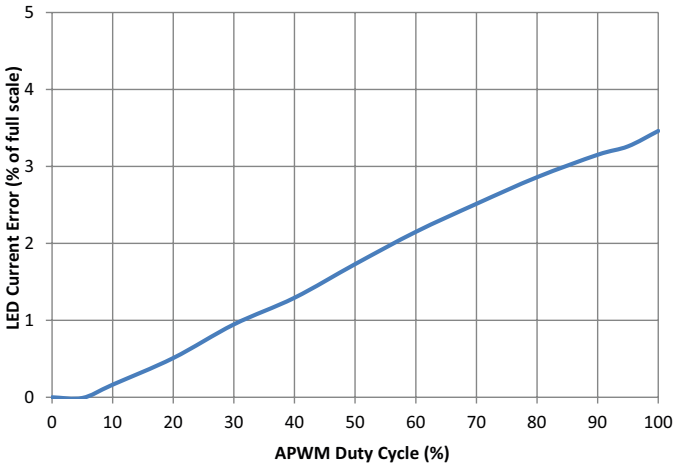

Figure 14: Error in LED Current vs. APWM Duty Cycle
V_{IN} = 9 V, V_{OUT} = ~22 V, R_{ISET} = 24 kΩ, APWM = 200 kHz

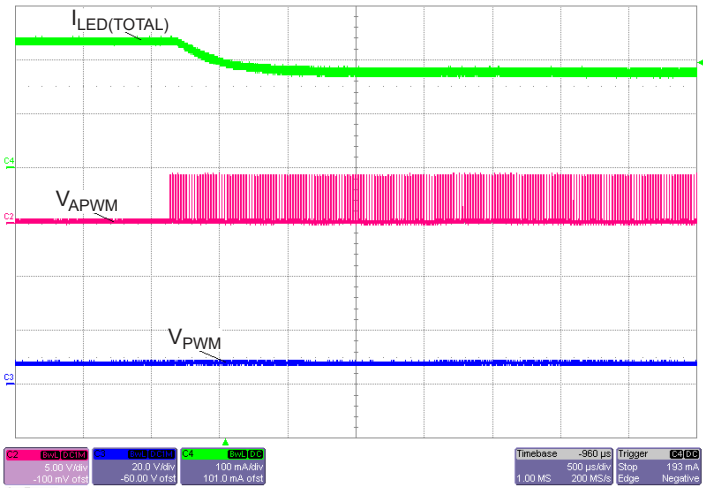

Figure 15: Transition of total LED current from 240 mA to 180 mA, when a 50 kHz 25% APWM signal is applied to the APWM pin. (Dimming PWM = 100%)

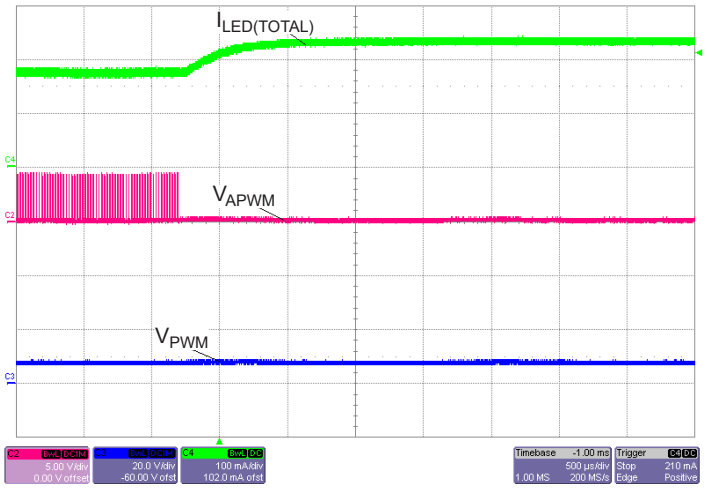

Figure 16: Transition of total LED current from 180 mA to 240 mA, when a 50 kHz 25% APWM stops being applied to the APWM pin. (Dimming PWM = 100%)

To use the APWM pin as a trim function, the user should set the maximum output current to a value higher than the desired current by at least 5%. The LED I_{ISET} current is then trimmed down to the appropriate desired value. Another consideration is the limitation of the APWM signal's duty cycle. In some cases, it might be more desirable to set the maximum I_{ISET} current to be 25% to 50% higher, thus allowing the APWM signal to have duty cycles that are between 25% and 50%.

Although the APWM dimming function has a wide frequency range, if used strictly as an analog dimming function, it is recommended to use frequency ranges between 50 and 500 kHz for best accuracy. The frequency range needs to be considered only if the user is not using APWM as a closed-loop trim function. It takes about 1 millisecond to change the actual LED current due to propagation delay between the APWM signal and $I_{LED(TOTAL)}$.

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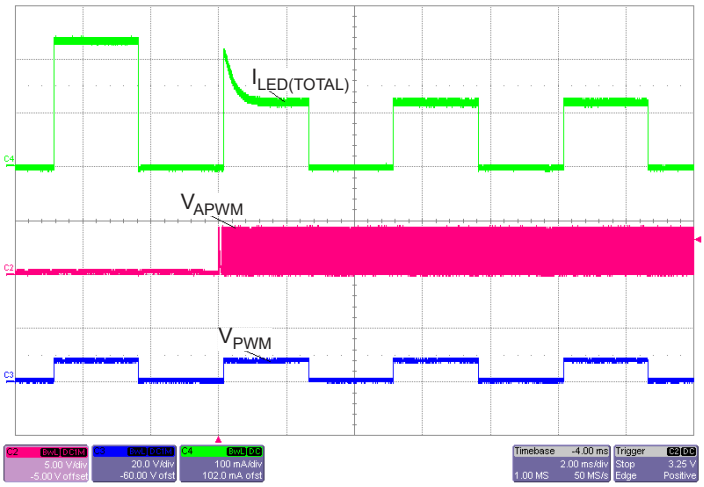

Figure 17: Transition of output current level when a 50 kHz 50% duty cycle APWM signal is applied to the APWM pin, in conjunction with 50% duty cycle applied to the PWM pin.

Extending LED Dimming Ratio

The dynamic range of LED brightness can be further extended by using a combination of PWM duty cycle, APWM duty cycle, and analog dimming method.

For example, the following approach can be used to achieve a 50,000:1 dimming ratio at 200 Hz PWM frequency:

- Vary PWM duty cycle from 100% down to 0.02% to give 5,000:1 dimming.
- With PWM duty cycle at 0.02%, vary APWM duty from 0% to 90% to reduce LED current down to 10%. This gives a net effect of 50,000:1 dimming.

Analog Dimming

Besides using APWM signal, the LED current can also be reduced by using an external DAC or another voltage source. Connect R_{ISET} between the DAC output and the ISET pin. The limit of this type of dimming is dependent of the range of the ISET pin. In the case of the A8518, the limit is 20 to 144 µA.

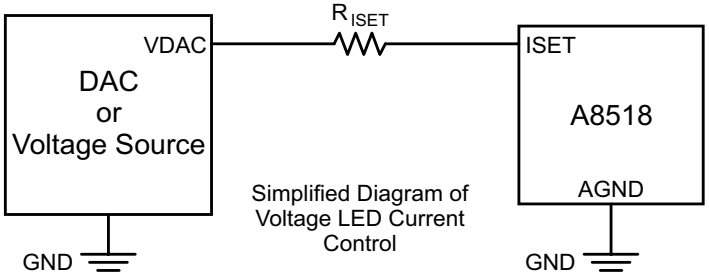

Figure 18: Typical Application Circuit Using a DAC to Control the LED Current in the A8518

The LED current is controlled by the following formula:

$$I_{ISET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET}}$$

where V_{ISET} is the ISET pin voltage and V_{DAC} is the DAC output voltage.

When the DAC voltage is 0 V, the LED current will be at its maximum. To keep the internal gain amplifier stable, do not decrease the current through the R_{ISET} resistor to less than 20 µA.

Figure 19 shows a typical application circuit using a DAC to control the LED current using a two-resistor configuration. The advantage of this circuit is that the DAC voltage can be higher or lower, thus adjusting the LED current to a higher or lower value of the preset LED current set by the R_{ISET} resistor.

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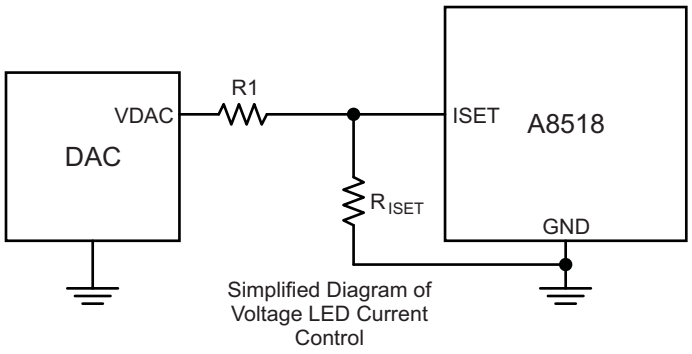

Figure 19: Typical Application Circuit Using a DAC and R_{ISET} Resistor to Control the LED Current in the A8518

The LED current can be adjusted using the following formula:

$$I_{ISET} = \frac{V_{ISET}}{R_{ISET}} - \left[\frac{V_{DAC} - V_{ISET}}{R1}\right]$$

where V_{ISET} is the ISET pin voltage and V_{DAC} is the DAC output voltage.

When V_{DAC} is equal to 1 V, the output is strictly controlled by the R_{ISET} resistor. When V_{DAC} is higher than 1 V, the LED current is reduced. When V_{DAC} is lower than 1 V, the LED current is increased.

LED String Short Detect

All LEDx pins are capable of handling the maximum V_{OUT} that the converter can deliver, thus allowing for LEDx pin to V_{OUT} protection in case of a connector short.

In case some of the LEDs in an LED string are shorted, the voltage at the corresponding LEDx pin will increase. Any LEDx pin that has a voltage exceeding $V_{LEDx(SC)}$ will be removed from operation. This will prevent the IC from dissipating too much power by having a large voltage present on an LEDx pin.

At least one LED must be in regulation for the LED string short-detect protection to activate. In case all of the LED pins are above regulation voltage (this could happen when the input voltage rises too high for the LED strings), they will continue to operate normally.

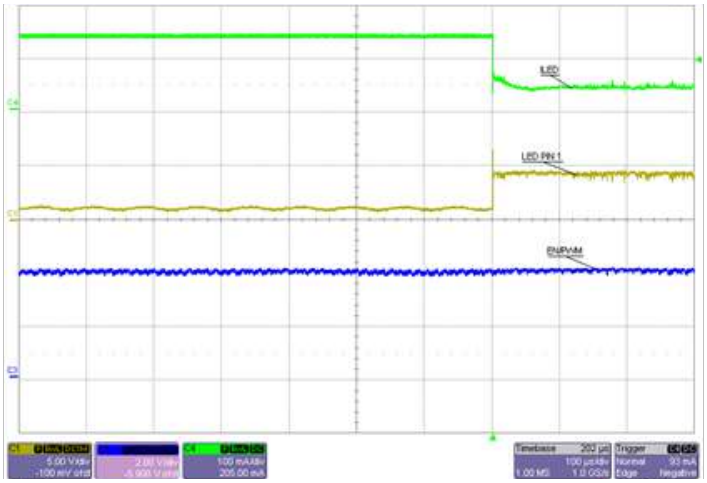

Figure 20: Disabling of LED1 String when the LED1 Pin Voltage is Increased Above 4.6 V

While the IC is being PWM dimmed, the IC will recheck the disabled LED every time the PWM signal goes high to prevent false tripping of LED short. This also allows for some self-correction if an intermittent LED pin short-to-VOUT is present.

Overvoltage Protection

The A8518 has output overvoltage protection (OVP) and open Schottky diode protection (secondary OVP). The OVP pin has a threshold level of 8.3 V. A resistor can be used to set the output overvoltage protection threshold up to approximately 40 V. This is sufficient for driving 11 white LED in series.

The formula for calculating the OVP resistor is shown below:

$$R_{OVP} = \frac{(V_{OVP} - V_{OVP(th)})}{I_{OVP(th)}}$$

where $V_{OVP(th)}$ = 8.3 V typical and $I_{OVP(th)}$ = 200 µA typical.

The OVP function is not inherently a latched fault. If the OVP condition occurs during a load dump, the IC will stop switching but not shut down.

There are several possibilities why an OVP condition is encountered during operation, the two most common being an open LED string and a disconnected output condition.

Figure 21 illustrates when the output of the A8518 is disconnected from load during normal operation. The output voltage instantly increases up to OVP voltage level, and then the boost stops switching to prevent damage to the IC. When the output

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voltage decreases to a low value, the boost converter will begin switching. If the condition that caused the OV event still exists, OVP will be triggered again.

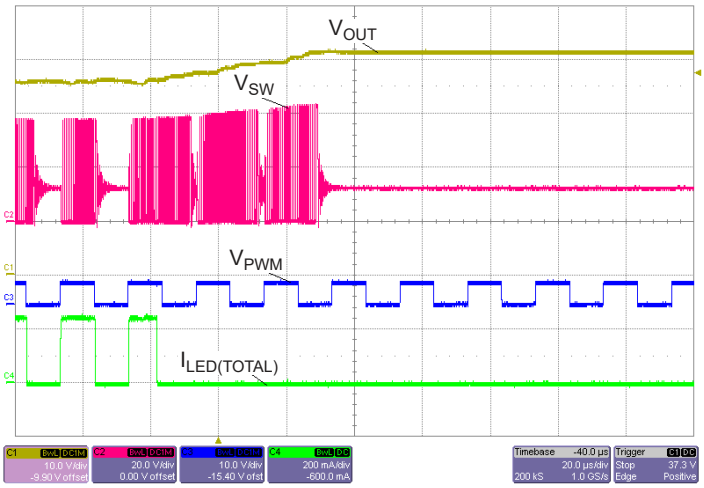

Figure 21: Output of A8518 when Disconnected from Load During Normal Operation

Figure 22 illustrates a typical OVP condition caused by an open LED string. Once the OVP is detected, the boost stops switching, and the open LED string is removed from operation. Afterwards, V_{OUT} is allowed to fall, the boost will resume switching, and the A8518 will resume normal operation.

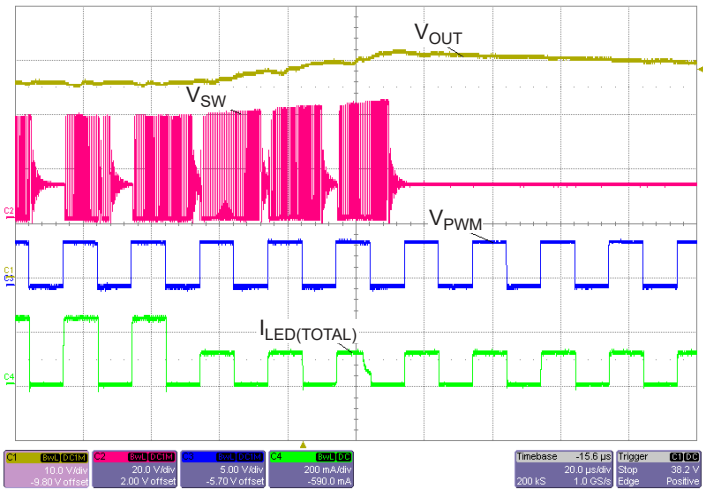

Figure 22: Typical OVP Condition Caused by an Open LED String

The A8518 also has built-in secondary overvoltage protection to protect the internal switch in the event of an open-diode condition. Open Schottky diode detection is implemented by detecting overvoltage on the SW pin of the device. If voltage on the SW pin exceeds the device's safe operating voltage rating, the A8518 disables and remains latched. To clear this fault, the IC must be shut down by either using the PWM signal or by going below the UVLO threshold on the VIN pin.

Figure 23 illustrates open Schottky diode protection while the IC is in normal operation. As soon as the switch node voltage (SW) exceeds 48 V, the IC will shut down. Due to small delays in the detection circuit, as well as there being no load present, the switch node voltage (V_{SW}) will rise above the trip point voltage.

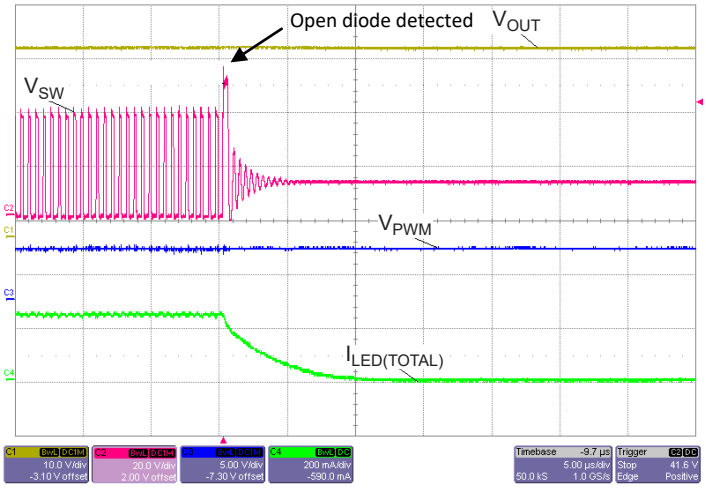

Figure 23: Open Schottky Diode Protection

When enabling the A8518 into an open-diode condition, the IC will first go through all of its initial LED detection and will then check the boost output voltage. At that point, the open diode is detected.

Boost Switch Overcurrent Protection

The boost switch is protected with cycle-by-cycle current limiting set at a minimum of 3 A. Figure 24 illustrates the normal operation of the switch node (V_{SW}), inductor current, and output voltage (V_{OUT}) for an 11×2 LED configuration.

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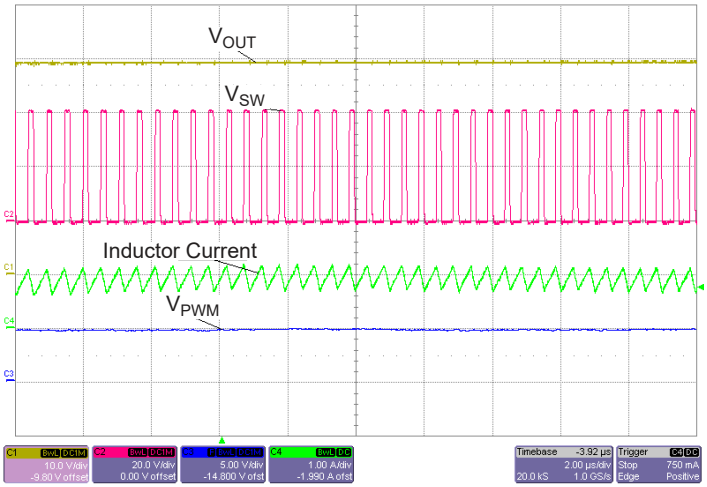

Figure 24: Normal Operation of Switch Node (V_{SW}), Inductor Current and Output Voltage (V_{OUT})

Figure 25 illustrates the cycle-by-cycle current limit showing the inductor current as a green trace. Note that the inductor current is truncated and as a result the output voltage is reduced compared to normal operation shown for the 11×2 LED configuration.

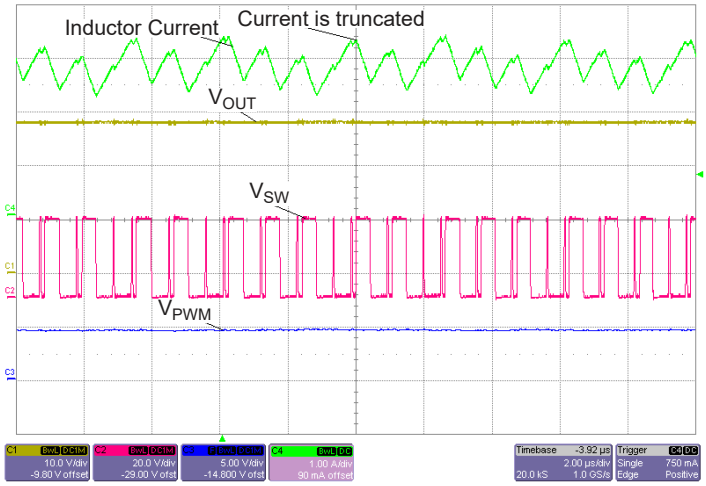

Figure 25: Cycle-by-Cycle Current Limit

There is also a secondary current limit ($I_{SW(LIM2)}$) that is sensed through the boost switch. This current limit, once detected, immediately shuts down the A8518. The level of this current limit is set above the cycle-by-cycle current limit to protect the switch from destructive currents when the boost inductor is shorted. Figure 26 shows the secondary boost switch OCP. Once this limit is reached, the A8518 will immediately shut down.

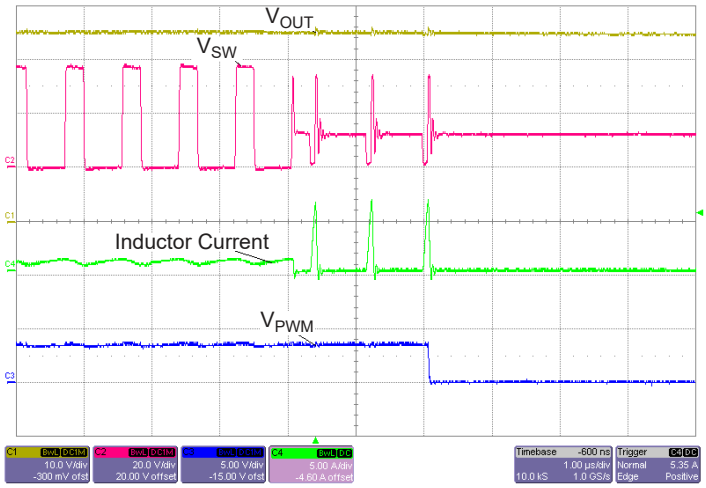

Figure 26: Secondary Boost Switch OCP

Input Overcurrent Protection and Disconnect Switch

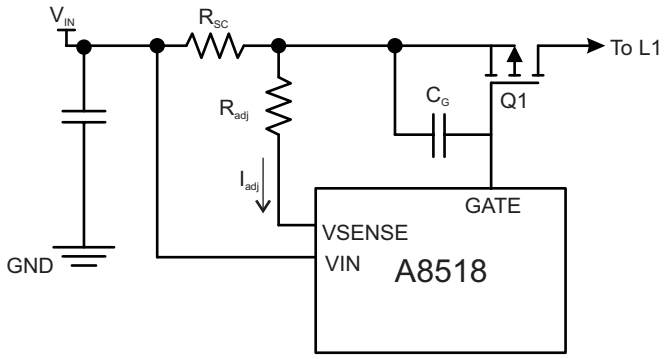

Figure 27: Typical Circuit Showing Implementation of Input Disconnect Feature

The primary function of the input disconnect switch is to protect the system and the device from catastrophic input currents during a fault condition.

If the input current level goes above the preset current limit threshold, the part will be shut down in less than 3 µs—this is a latched condition. The fault flag is also set low to indicate a fault. This protection feature prevents catastrophic failure in the system due to a short of the inductor, inductor short to GND, or short at the output to GND. Figure 28 illustrates the typical input overcurrent fault condition. As soon as input OCP limit is reached, the part disables the gate of the disconnect switch Q1.

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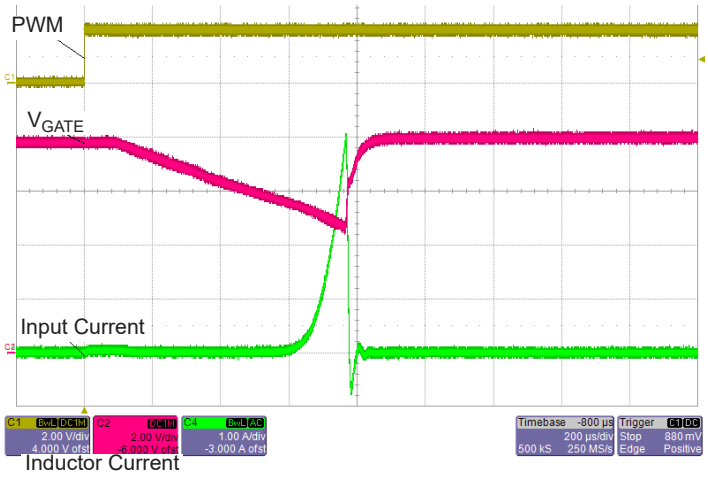

Figure 28: Startup into Output Shorted to GND Fault. Input OCP tripped at 4 A (R_{SC} = 0.024 Ω, R_{adj} = 383 Ω)

During startup when Q1 first turns on, an inrush current flows through Q1 into the output capacitance. If Q1 turns on too fast (due to its low gate capacitance), the inrush current may trip input OCP limit. In this case, an external gate capacitance C_G is added to slow down the turn-on transition. Typical value for C_G is around 4.7 to 22 nF. Do not make C_G too large, since it also slows down the turn-off transient during a real input OCP fault.

Setting the Current Sense Resistor

As shown in Figure 27:

$$V_{IN} - V_{SENSE} = V_{SC} + I_{adj} \times R_{adj}$$

or

$$I_{SC} = ((V_{IN} - V_{SENSE}) - I_{adj} \times R_{adj})/R_{SC}$$

where V_{SC} = the voltage drop across R_{SC}. The typical threshold for the current sense is $V_{IN} - V_{SENSE}$ = 110 mV when R_{adj} is 0 Ω. The A8518 can have this voltage trimmed using the R_{adj} resistor. It is recommended to set the trip point to be above 3.65 A to avoid conflicts with the cycle-by-cycle current limit typical threshold. A sample calculation is done below for 4.25 A of input current.

The calculated max value of sense resistor R_{SC} = 0.11 V/4.25 A = 0.0259 Ω.

The R_{sc} chosen is 0.024 Ω, a standard value. Therefore, the voltage drop across R_{SC} is:

$$V_{SC} = 4.25\ A \times 0.024\ \Omega = 0.102\ V$$

$$R_{adj} = \frac{V_{SENSE(trip)} - V_{SC}}{I_{adj}}$$

$$R_{adj} = \frac{0.11\ V - 0.102\ V}{21.5\ \mu A} = 372\ \Omega$$

Input UVLO

When V_{IN} and V_{SENSE} rise above $V_{UVLOrise}$ threshold, the A8518 is enabled. The A8518 is disabled when V_{IN} falls below $V_{UVLOfall}$ threshold for more than 50 µs. This small delay is used to avoid shutting down because of momentary glitches in the input power supply.

Figure 29 illustrates a shutdown showing a falling input voltage (V_{IN}). When V_{IN} falls below 3.90 V, the IC will shut down.

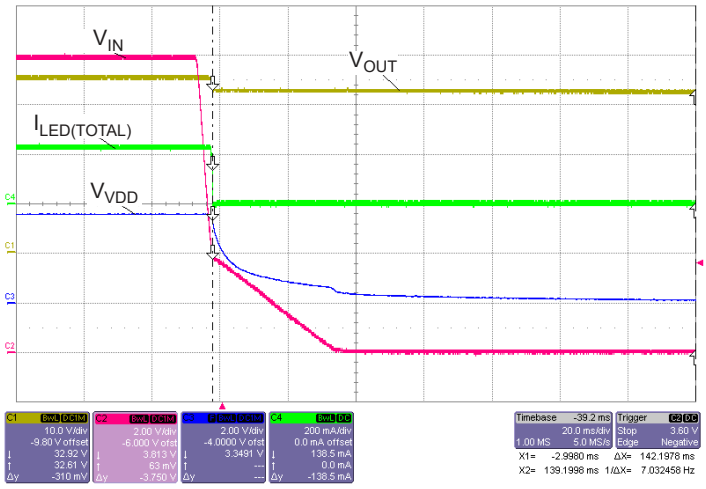

Figure 29: Shutdown with Falling Input Voltage

VDD

The VDD pin provides regulated bias supply for internal circuits. Connect a C_{VDD} capacitor with a value of 1 µF or greater to this pin. The internal LDO can deliver no more than 2 mA of current with a typical VDD voltage of about 3.5 V, enabling this pin to serve as the pull-up voltage for the fault pin.

Shutdown

If PWM pin is pulled low for more than t_{PWML} (16 ms), the device enters shutdown mode and clears all internal fault registers. When shut down, the IC will disable all current sources and wait until the PWM goes high to re-enable the IC.

Figure 30 depicts the shutdown using the PWM, showing the 16 ms delay between PWM signal and when the VDD and GATE of disconnect switch turn off.

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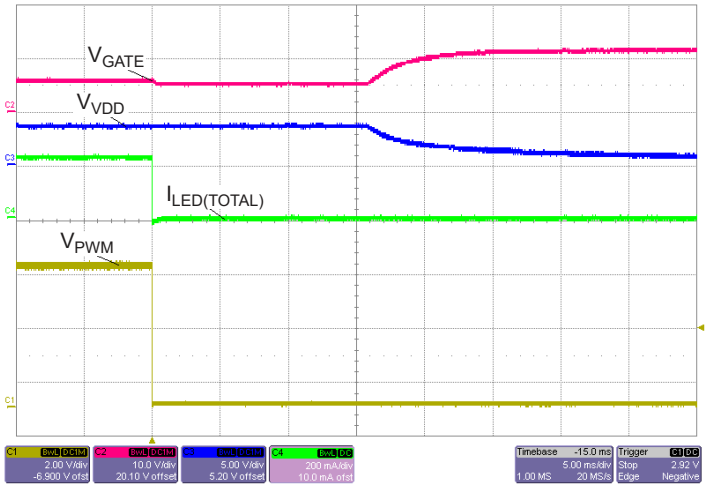

Figure 30: Shutdown Using the Enable

Dithering Feature (A8518 only)

To minimize the switching frequency harmonics, a dithering feature is implemented in A8518. This feature simplifies the input filters needed to meet the automotive CISPR 25 conducted and radiated emission limits. The dithering sweep is internally set at ±5%. The switching frequency will ramp from 0.95 times the programmed frequency to 1.05 times the programmed frequency. The rate or modulation at which the frequency sweeps is governed by an internal 12.5 kHz triangle pattern.

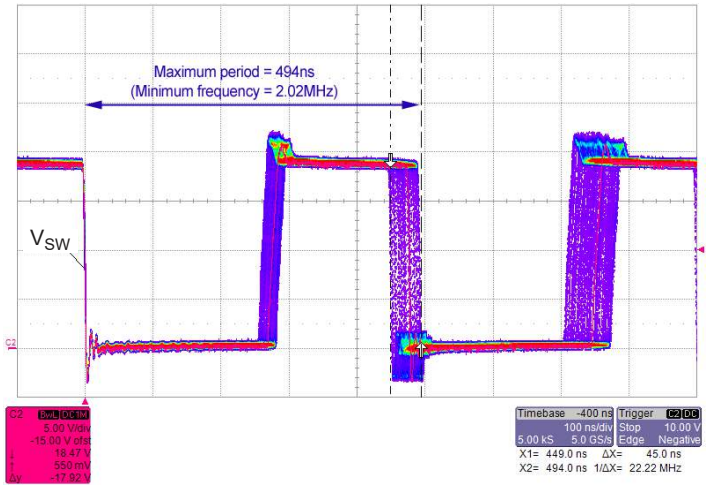

Figure 31: Minimum Dithering Switching Frequency = 2.02 MHz at V_{IN} = 12 V, and PWM Ratio = 100%

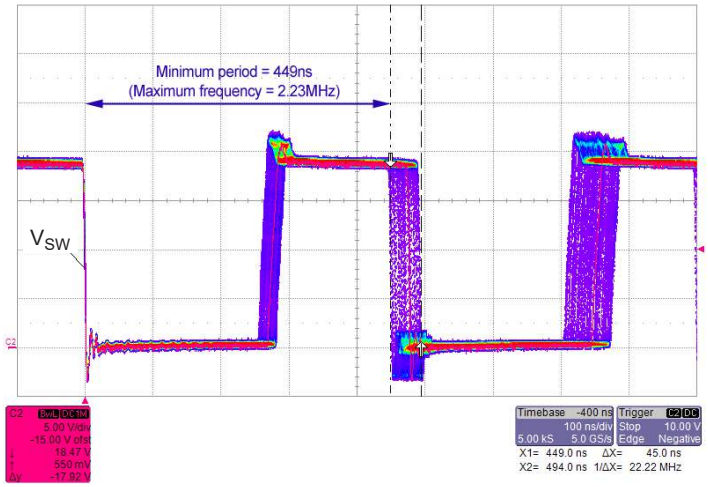

Figure 32: Maximum Dithering Switching Frequency = 2.23 MHz at V_{IN} = 12 V, and PWM Ratio = 100%

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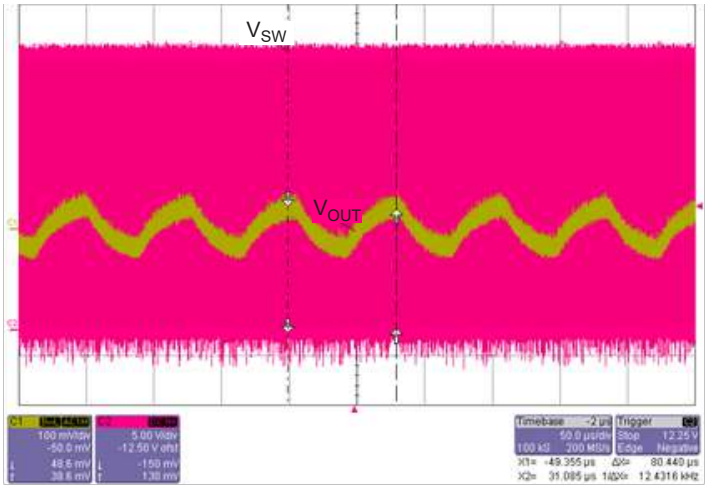

Figure 33: Output Voltage Ripple Frequency Due to Dithering = 12.4 kHz at V_{IN} = 12 V, and PWM Ratio = 100%

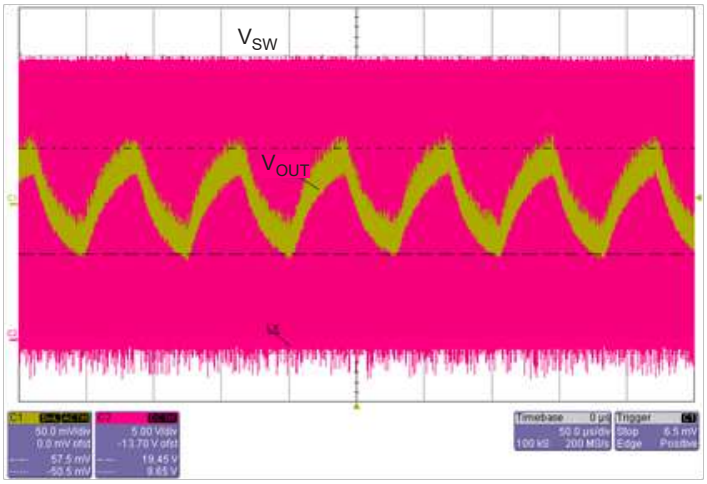

Figure 34: Output Voltage Ripple Amplitude Due to Dithering = 100 mV at V_{IN} = 12 V, and PWM Ratio = 100%

Fault Protection During Operation

The A8518 constantly monitors the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in Table 3. There are several points at which the A8518 monitors for faults during operation. The locations are input current, switch current, output voltage, and LED pins.

Note:
Some protection features might not be active during startup to prevent false triggering of fault conditions.

The detectable faults are:

- Open LED pin
- Shorted LED pin to GND
- Open or shorted inductor
- Open or shorted boost diode
- VOUT pin shorted to GND
- SW pin shorted to GND
- ISET pin shorted to GND

Note:
Some faults will not be protected if the input disconnect switch is not used. An example of this is VOUT pin shorted to GND.

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Table 3: Fault Mode Table

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Disconnect Switch	LED Sink Drivers
Primary Switch Overcurrent Protection (cycle-by-cycle current limit)	Auto-restart	Always	NO	This fault condition is triggered when the SW current exceeds the cycle-by-cycle current limit, $I_{SW(LIM)}$.The present SW on-time is truncated immediately to limit the current. Next switching cycle starts normally.	Off for a single cycle	ON	ON
Secondary Switch Current Limit	Latched	Always	YES	When current through boost switch exceeds secondary SW current limit ($I_{SW(LIM2)}$), the device immediately shuts down the disconnect switch, LED drivers and boost. The Fault flag is set. To re-enable the part, the PWM pin needs to be pulled low for 32,750 clock cycles.	OFF	OFF	OFF
Input Disconnect Current Limit	Latched	Always	YES	The device is immediately shut off if the voltage across the input sense resistor is above the $V_{SENSE(trip)}$ threshold. To re-enable the device, the PWM pin must be pulled low for 32,750 clock cycles.	OFF	OFF	OFF
Secondary OVP	Latched	Always	YES	Secondary overvoltage protection is used for open-diode detection. When diode D1 opens, the SW pin voltage will increase until $V_{OVP(sec)}$ is reached. This fault latches the IC. The input disconnect switch is disabled as well as the LED drivers. To re-enable the part, the PWM pin needs to be pulled low for 32,750 clock cycles.	OFF	OFF	OFF
LEDx Pin Short Protection	Auto-restart	Startup	NO	This fault prevents the part from starting up if any of the LED pins are shorted. The part stops soft-start from starting while any of the LED pins are determined to be shorted. Once the short is removed, soft-start is allowed to start.	OFF	ON	OFF
LEDx Pin Open	Auto-restart	Normal operation	NO	When an LED pin is open, the device will determine which LED pin is open by increasing the output voltage until OVP is reached. Any LED string not in regulation will be turned OFF. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	ON	ON	OFF for open pins, ON for all others
ISET Short Protection	Auto-restart	Always	NO	Fault occurs when the ISET current goes above 150% of max current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed, the IC will try to regulate to the preset LED current.	OFF	ON	OFF
Overvoltage Protection	Auto-restart	Always	NO	Fault occurs when OVP pin exceeds $V_{OVP(th)}$ threshold. The IC will immediately stop switching to try to reduce the output voltage. If the output voltage decreases, then the IC will restart switching to regulate the output voltage.	STOP during OVP event	ON	ON
Undervoltage Protection	Auto-restart	Always	YES	Device immediately shuts off boost and current sinks if the voltage at OVP pin is below $V_{UVP(th)}$. It will auto-restart once the fault is removed.	OFF	ON	OFF
LED String Short Detection	Auto-restart	Always	NO	Fault occurs when the LED pin voltage exceeds 5.2 V. Once the LED string short fault is detected, the LED string above the threshold will be removed from operation.	ON	ON	OFF for shorted pins, ON for all others
Overtemperature Protection	Auto-restart	Always	NO	Fault occurs when the die temperature exceeds the overtemperature threshold, typically 170°C.	OFF	OFF	OFF
V_{IN} UVLO	Auto-restart	Always	NO	Fault occurs when V_{IN} drops below $V_{UVLOfall}$, typically 3.9 V. This fault resets all latched faults.	OFF	OFF	OFF

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APPLICATION INFORMATION

Design Example

This section provides a method for selecting component values when designing an application using the A8518.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{IN}: 10 to 14 V
- Quantity of LED channels, #CHANNELS: 2
- Quantity of series LEDs per channel, #SERIESLEDS: 10
- LED current per channel, I_{LED}: 120 mA
- V_f at 120 mA: 3.2 V
- f_{SW}: 2 MHz
- PWM dimming frequency 200 Hz 1% Duty cycle

Step 1: Connect LED strings to pins LED1 and LED2.

Step 2: Determine the LED current set resistor R_{ISET}:

$$R_{ISET} = \frac{(V_{ISET} \times A_{ISET})}{I_{LED}}$$

$$R_{ISET} = \frac{(1.017 \times 1419)}{0.120} = 12\ k\Omega$$

$$R_{ISET} = 11.8\ k\Omega$$

Step 3a: Determining the OVP resistor.

The OVP resistor is connected between the OVP pin and the output voltage of the converter. The first step is to determine the maximum voltage based on the LED requirements. The regulation voltage for an LED pin (V_{LEDx}) of the A8518 is 0.85 mV. A 5 V headroom is added to give margin to the design due to noise and output voltage ripple.

$$V_{OUT(ovp)} = \#SERIESLEDS \times V_f + V_{LED} + 5\ V$$

$$V_{OUT(ovp)} = 10 \times 3.2\ V + 0.85\ V + 5\ V$$

$$V_{OUT} = 37.85\ V$$

The OVP resistor is:

$$R_{OVP} = \frac{(V_{OUT(ovp)} - V_{OVP(th)})}{I_{OVP(th)}}$$

where both $I_{OVP(th)}$ and $V_{OVP(th)}$ values are taken from the datasheet's Electrical Characteristics table.

$$R_{OVP} = \frac{37.85\ V - 8.3\ V}{0.200\ mA} = 147.75\ k\Omega$$

Chose a value of resistor that is a higher value than the calculated R_{OVP}. In this case, a value of 158 kΩ was selected. Below is the actual value of the minimum OVP trip level with the selected resistor.

$$V_{OUT(ovp)} = 158\ k\Omega \times 0.200\ mA + 8.3\ V$$

$$V_{OUT(ovp)} = 39.9\ V$$

Step 3b: At this point, a quick check needs to be done to see if the conversion ratio is adequate for the running switching frequency. Where V_D is the diode forward voltage, minimum off-time ($t_{SW(off)}$) is found in the datasheet:

$$D_{MAX(boost)} = 1 - t_{SW(off)} \times f_{SW(max)}$$

$$D_{MAX(boost)} = 1 - (0.085\ \mu s \times 2.2\ MHz) = 0.813$$

$$Theoretical\ Max\ V_{OUT} = \left[\frac{V_{IN(min)}}{1 - D_{MAX(boost)}}\right] - V_D$$

V_D is the voltage drop of the boost diode.

$$Theoretical\ Max\ V_{OUT} = \left[\frac{10\ V}{1 - .813}\right] - 0.4 = 53.1\ V$$

Theoretical Max V_{OUT} value needs to greater than the value $V_{OUT(ovp)}$. If this is not the case, then either the minimum input voltage needs to be increased, or the number of series LEDs and $V_{OUT(ovp)}$ need to be reduced.

Step 4: Inductor selection.

The inductor needs to be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the system needs to operate in continuous conduction mode throughout the whole input voltage range.

Step 4a: Determine the Duty Cycle.

$$D_{MAX} = 1 - \left[\frac{V_{IN(min)}}{(V_{OUT(ovp)} + V_D)}\right]$$

$$D_{MAX} = 1 - \left[\frac{10}{(39.9 + 0.4)}\right] = 0.75$$

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A good approximation of efficiency η can be taken from the efficiency curves located on page 10. A value of 90% is a good starting approximation.

Step 4b: Determine the maximum and minimum input current to the system. The minimum input current will dictate the inductor value. The maximum current rating will dictate the current rating of the inductor.

$$I_{IN(max)} = \frac{V_{OUT(ovp)} \times I_{OUT}}{V_{IN(min)} \times \eta}$$

$$I_{OUT} = \#Channels \times I_{LED}$$

$$I_{OUT} = 2 \times 0.120\ A = 0.240\ A$$

$$I_{IN(max)} = \frac{39.9\ V \times 0.24\ A}{10\ V \times 0.90} = 1.06\ A$$

$$I_{IN(min)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN(max)} \times \eta}$$

$$V_{OUT} = 10 \times 3.2 + 0.85 = 32.85\ V$$

$$I_{IN(min)} = \frac{32.85\ V \times 240\ mA}{14\ V \times 0.90} = 0.625\ A$$

Step 4c: Determining the inductor value.

To ensure that the inductor operates in continuous conduction mode, the value of inductor needs to be set such that the ½ inductor ripple current is not greater than the average minimum input current. A first pass calculation for K_{ripple} should be 30% of the maximum inductor current.

$$\Delta I_L = I_{IN(max)} \times K_{ripple}$$

$$\Delta I_L = 1.06\ A \times 0.3 = 0.318\ A$$

$$L = \frac{(V_{IN(min)} \times D_{MAX})}{(\Delta I_L \times f_{SW})}$$

$$L = \frac{10\ V}{0.318\ A \times 2\ MHz} \times 0.75 = 11.79\ \mu H$$

Double-check to make sure that ½ current ripple is less than $I_{IN(min)}$.

$$I_{IN(min)} > ½\ \Delta I_L$$

$$0.626\ A > 0.165\ A$$

10 µH was selected. At 10 µH:

$$\Delta I_L = 0.375\ A \qquad \frac{\Delta I_L}{2} = 0.19\ A$$

$$0.626\ A > 0.19\ A$$

A good inductor value to use would be 10 µH.

Step 4d: This step is used to verify that there is sufficient slope compensation for the inductor chosen. The implemented slope compensation is 6 A/µs.

Next, insert the inductor value used in the design:

$$\Delta I_{L(used)} = \frac{V_{IN(min)} \times D_{MAX}}{L(used) \times f_{SW}}$$

$$\Delta I_{L(used)} = \frac{10\ V \times 0.75}{10\ \mu H \times 2.0\ MHz} = 0.375\ A$$

$$Required\ Min\ Slope = \frac{\Delta I_{L(used)} \times \Delta S \times 10^{-6}}{\frac{1}{f_{SW}} \times (1 - D_{MAX})}$$

where ΔS is taken from the following formula:

$$\Delta S = 1 - \frac{0.18}{D_{MAX}}$$

$$\Delta S = 0.76$$

$$Required\ Min\ Slope = \frac{0.375 \times (0.76 \times 10^{-6})}{\frac{1}{2.0\ MHz} \times (1 - 0.75)} = 2.28\ A/\mu s$$

If the required minimum slope is larger than the calculated slope compensation, the inductor value needs to be increased.

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Step 4e: Determining the inductor current rating.

$$I_{L(min)} = I_{IN(max)} + \tfrac{1}{2}\,\Delta I_L$$

$$I_{L(min)} = 1.06 + \frac{0.375\ A}{2} = 1.25\ A$$

Step 5: Choosing the proper output Schottky diode.

The diode needs to be chosen for three characteristics when it is used in LED lighting circuitry. The most obvious two are the current rating of the diode and the reverse voltage rating. The reverse voltage rating should be larger than the maximum output voltage V_{OVP}. The peak current through the diode is:

$$I_{D(pk)} = I_{IN(max)} + \frac{\Delta I_{L(used)}}{2}$$

$$I_{D(pk)} = 1.06 + \frac{0.375\ A}{2} = 1.25\ A$$

The other major factor in deciding the boost diode is the reverse current characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time, the boost converter is not switching. This results in a slow bleeding off of the output voltage due to leakage currents. I_R or reverse current can be a large contributor, especially at high temperatures. The reverse current of the selected diode varies between 1 and 100 µA. For higher efficiency, use a low forward voltage drop Schottky diode. For better EMI performance, use a small junction capacitor Schottky diode.

Step 6: Choosing the output capacitors.

The output capacitors need to be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factors that contribute to the size of the output capacitor are PWM dimming frequency and the PWM duty cycle. Another major contributor is leakage current (I_{LK}). This current is the combination of the OVP current sense as well as the reverse current of the boost diode. In this design, the PWM dimming frequency is 200 Hz and the minimum duty cycle is 0.02%. Typically, the voltage variation on the output during PWM dimming needs to be less than 250 mV (V_{COUT}) so there is no audible hum.

$$C_{OUT} = I_{LK} \times \frac{(1 - \text{minimum dimming duty cycles})}{\text{PWM dimming frequency} \times V_{COUT}}$$

The selected diode leakage current at a 150°C junction temperature and 30 V output is 100 µA, and the maximum leakage current through OVP pin is 1 µA. The total leakage current can be calculated as follows:

$$I_{LK} = I_{LKG(diode)} + I_{LKG(ovp)}$$

$$= 100\ \mu A + 1\ \mu A$$

$$= 101\ \mu A$$

$$C_{OUT} = 101\ \mu A \times \frac{(1 - 0.02)}{200\ Hz \times 0.250\ V} = 2\ \mu F$$

A capacitor larger than 2 µF should be selected. Due to degradation of capacitance at dc voltages, a 4.7 µF / 50 V capacitor is a good choice.

Vendor	Value	Part Number
Murata	4.7 µF / 50 V	GRM21BC81H475KE11K

It is also necessary to note that if a high dimming ratio of 5000:1 must be maintained at lower input voltages, then larger output capacitors will be needed. 4 × 4.7 µF / 50 V / X6S / 0805 capacitors are chosen; 0805 size is selected to minimize possible audible noise.

The RMS current through the capacitor is given by:

$$C_{OUT(rms)} = I_{OUT} \times \sqrt{\frac{D_{MAX} + \frac{\Delta I_{L(used)}}{I_{IN(max)} \times 12}}{1 - D_{MAX}}}$$

$$C_{OUT(rms)} = 0.240 \times \sqrt{\frac{0.75 + \frac{0.375}{1.06 \times 12}}{1 - 0.75}} = 0.424\ A$$

The output capacitor needs to have a current rating of at least 0.424 A. The capacitors selected in this design, 4 × 4.7 µF / 50 V, have a combined current rating of 3 A.

Step 7: Selection of input capacitor.

The input capacitor needs to be selected such that it provides good filtering of the input voltage waveform. A good rule of thumb is to set the input voltage ripple ΔV_{IN} to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

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$$C_{IN} = \frac{\Delta I_{L(used)}}{8 \times f_{SW} \times \Delta V_{IN}}$$

$$C_{IN} = \frac{0.375\ A}{8 \times 2\ MHz \times 0.1\ V} = 0.234\ \mu F$$

$$C_{IN(rms)} = \frac{I_{OUT} \times \frac{\Delta I_{L(used)}}{I_{IN(max)}}}{(1 - D_{MAX}) \times \sqrt{12}} = 0.1\ A$$

$$C_{IN(rms)} = \frac{0.240\ A \times \frac{0.375\ A}{1.06\ A}}{(1 - 0.75) \times \sqrt{12}} = 0.1\ A$$

A good ceramic input capacitor with ratings of 50 V / 2.2 µF or 50 V / 4.7 µF will suffice for this application.

Vendor	Value	Part Number
Murata	4.7 µF / 50 V	GRM32ER71H475KA88L
Murata	2.2 µF / 50 V	GRM31CR71H225KA88L

If long wires are used for the input, it is necessary to use a much larger input capacitor. A larger input capacitor is also required to have stable input voltage during line transients. Combinations of aluminum electrolytic and ceramic capacitors can be used.

Step 8: Choosing the input disconnect switch components.

Set the input disconnect current limit to 4.25 A.

$$R_{SC} = \frac{0.11\ V}{4.25\ A} = 0.0259\ \Omega$$

The chosen R_{SC} is 0.024 Ω. The trip point voltage needs to be:

$$V_{SC} = 4.25\ A \times 0.024\ \Omega = 0.102\ V$$

$$R_{adj} = \frac{V_{VSENSE(trip)} - V_{SC}}{I_{adj}}$$

$$R_{adj} = \frac{0.11\ V - 0.102\ V}{21.5\ \mu A} = 372\ \Omega$$

A value of 383 Ω was chosen for this design. The disconnect switch Q1 works as on or off. Therefore, the R_{adj} value is not critical.

For the input disconnect switch, an AO4421 6.2 A / 60 V P-channel MOSFET is selected.

To achieve proper operation at low dimming ratios, connect an RC filter to the VOUT pin. Use R = 10 kΩ and C = 47 pF.

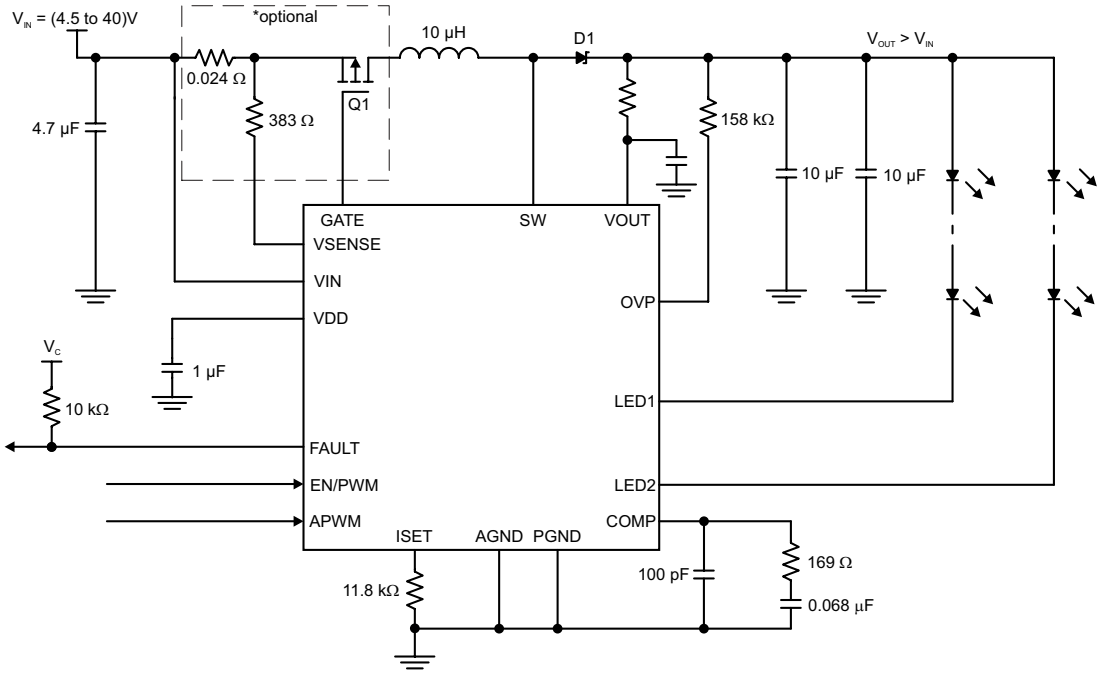

Figure 35: Schematic Showing Calculated Values from the Design Example Above

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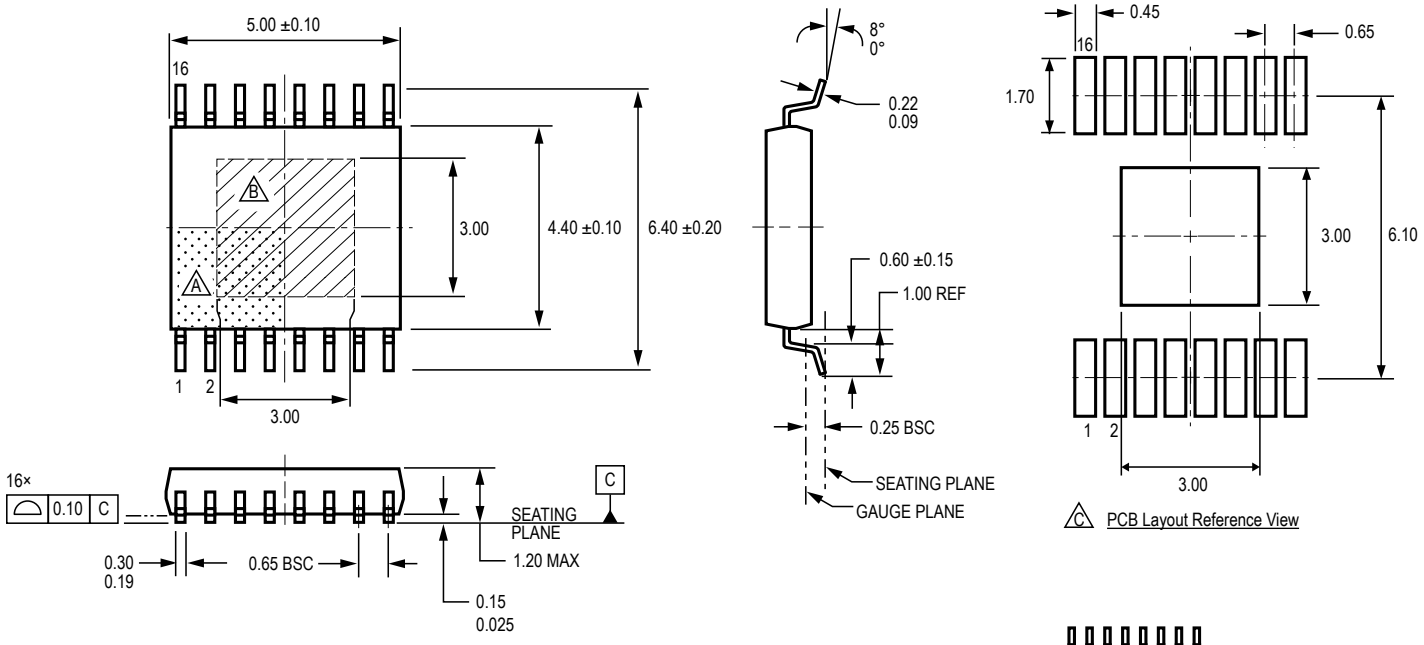
PACKAGE OUTLINE DIAGRAM

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Package LP, 16-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	September 29, 2014	Initial Release
1	March 18, 2015	Revised OVP Thresholds
2	November 4, 2015	Amended “Enabling the IC” (page 12) and “Synchronization” (page 15) of Functional Description; inserted Figures 13 and 14; updated Selection Guide table (page 2); corrected 2nd Typical Application Drawing (page 9)
3	January 8, 2016	Amended “Powering Up: Boost Output Undervoltage Protection” (page 13)
4	October 24, 2016	Revised Input Overcurrent Protection and Disconnect Switch section (page 20-21)
5	May 12, 2020	Minor editorial updates
6	May 16, 2022	Updated package drawing (page 29) and minor editorial updates

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