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Advanced Power MOSFET

IRLM120A

FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μA (Max.) @ $V_{DS} = 100V$
- Lower $R_{DS(ON)}$: 0.176 Ω (Typ.)

BV_{DSS} = 100 V

$R_{DS(on)}$ = 0.22 Ω

I_D = 2.3 A

SOT-223

1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic		Value	Units
V_{DSS}	Drain-to-Source Voltage		100	V
I_D	Continuous Drain Current (T_C=25°C)		2.3	A
	Continuous Drain Current (T_C=70°C)		1.85	
I_{DM}	Drain Current-Pulsed	(1)	18	A
V_{GS}	Gate-to-Source Voltage		$\pm$20	V
E_{AS}	Single Pulsed Avalanche Energy	(2)	105	mJ
I_{AR}	Avalanche Current	(1)	2.3	A
E_{AR}	Repetitive Avalanche Energy	(1)	0.27	mJ
dv/dt	Peak Diode Recovery dv/dt	(3)	6.5	V/ns
P_D	Total Power Dissipation (T_C=25°C) *		2.7	W
	Linear Derating Factor *		0.022	W/^{o}C
T_J, T_{STG}	Operating Junction and Storage Temperature Range		- 55 to +150	^{o}C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds		300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *	--	46.3	^{o}C/W

* When mounted on the minimum pad size recommended (PCB Mount).

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Electrical Characteristics (T_C=25 ^{o}C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV$_{DSS}$	Drain-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V,I_D=250μA
ΔBV/ΔT$_J$	Breakdown Voltage Temp. Coeff.	--	0.09	--	V/^{o}C	I_D=250μA **See Fig 7**
V$_{GS(th)}$	Gate Threshold Voltage	1.0	--	2.0	V	V_{DS}=5V,I_D=250μA
I$_{GSS}$	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-20V
I$_{DSS}$	Drain-to-Source Leakage Current	--	--	10	μA	V_{DS}=100V
		--	--	100		V_{DS}=80V,T_C=125 ^{o}C
R$_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.22	Ω	V_{GS}=5V,I_D=1.15A (4)
g$_{fs}$	Forward Transconductance	--	4.6	--	℧	V_{DS}=40V,I_D=1.15A (4)
C$_{iss}$	Input Capacitance	--	340	440	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz
C$_{oss}$	Output Capacitance	--	90	115		**See Fig 5**
C$_{rss}$	Reverse Transfer Capacitance	--	39	50		
t$_{d(on)}$	Turn-On Delay Time	--	5	20	ns	V_{DD}=50V,I_D=9.2A, R$_G$=9 Ω
t$_r$	Rise Time	--	10	30		
t$_{d(off)}$	Turn-Off Delay Time	--	19	50		**See Fig 13** (4)(5)
t$_f$	Fall Time	--	9	30		
Q$_g$	Total Gate Charge	--	10.2	15	nC	V_{DS}=80V,V_{GS}=5V, I_D=9.2A
Q$_{gs}$	Gate-Source Charge	--	1.7	--		
Q$_{gd}$	Gate-Drain ("Miller") Charge	--	6.0	--		**See Fig 6 & Fig 12** (4)(5)

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic		Min.	Typ.	Max.	Units	Test Condition
I$_S$	Continuous Source Current		--	--	2.3	A	Integral reverse pn-diode in the MOSFET
I$_{SM}$	Pulsed-Source Current	(1)	--	--	18		
V$_{SD}$	Diode Forward Voltage	(4)	--	--	1.5	V	T_J=25 ^{o}C,I_S=2.3A,V_{GS}=0V
t$_{rr}$	Reverse Recovery Time		--	98	--	ns	T_J=25 ^{o}C,I_F=9.2A
Q$_{rr}$	Reverse Recovery Charge		--	0.34	--	μC	di$_F$/dt=100A/μs (4)

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=30mH, I_{AS}=2.3A, V_{DD}=25V, R$_G$=27Ω, Starting T$_J$=25 ^{o}C

③ $I_{SD} \leq$ 9.2A, di/dt $\leq$ 300A/μs, $V_{DD} \leq$ BV$_{DSS}$, Starting T$_J$ =25 ^{o}C

④ Pulse Test : Pulse Width = 250μs, Duty Cycle $\leq$ 2%

⑤ Essentially Independent of Operating Temperature

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IRLM120A

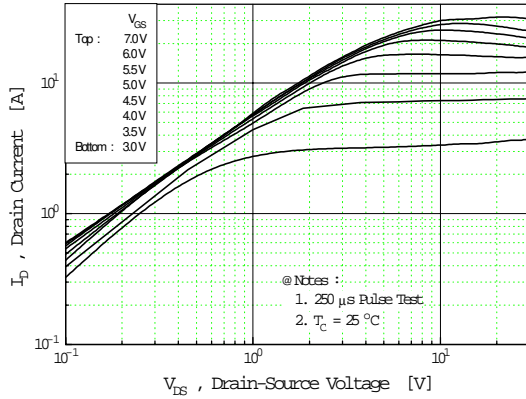### Fig 1. Output Characteristics
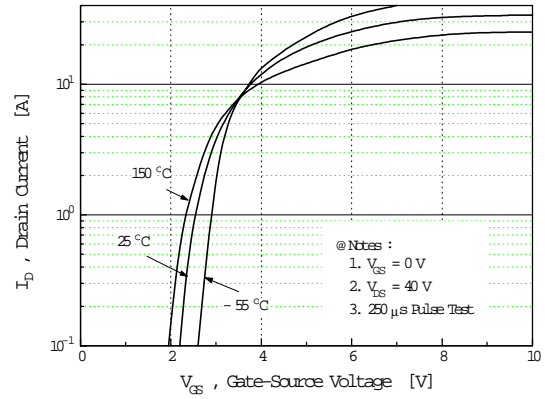

Fig 2. Transfer Characteristics

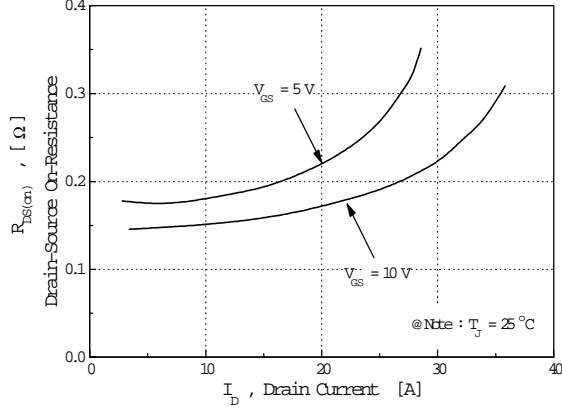### Fig 3. On-Resistance vs. Drain Current

Fig 4. Source-Drain Diode Forward Voltage
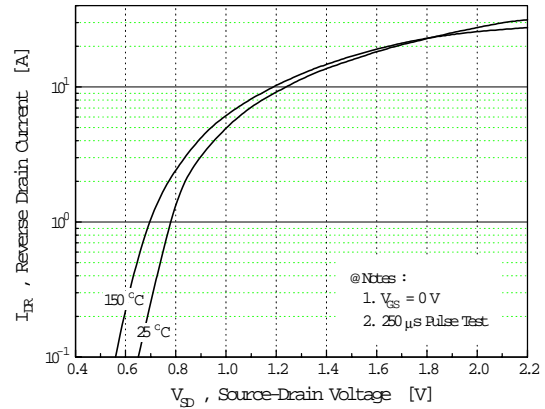
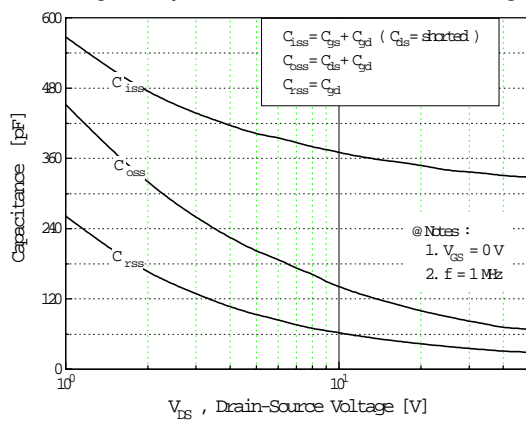### Fig 5. Capacitance vs. Drain-Source Voltage

Fig 6. Gate Charge vs. Gate-Source Voltage

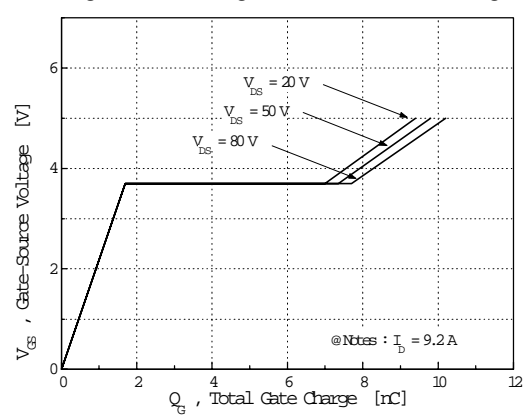**FAIRCHILD**

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Fig 7. Breakdown Voltage vs. Temperature

BV_{DSS} , (Normalized)
Drain-Source Breakdown Voltage

T_J , Junction Temperature [$^{\circ}$C]

@Notes :
1. V_{GS} = 0 V
2. I_D = 250 μA
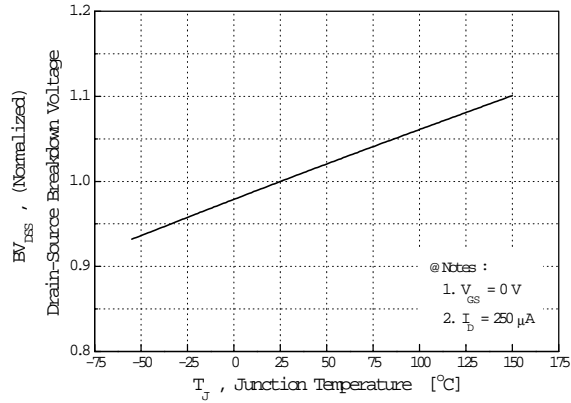
Fig 8. On-Resistance vs. Temperature

$R_{DS(on)}$, (Normalized)
Drain-Source On-Resistance

T_J , Junction Temperature [$^{\circ}$C]

@Notes :
1. V_{GS} = 5 V
2. I_D = 4.6 A
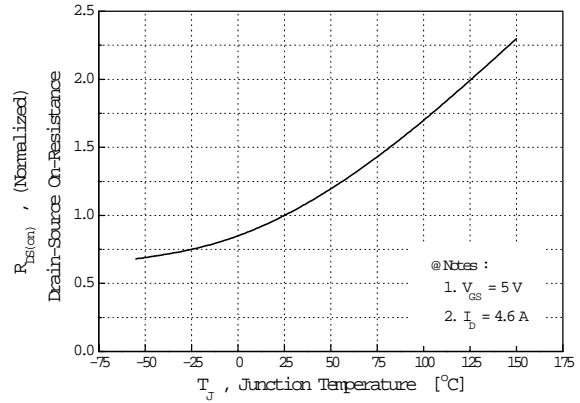
Fig 9. Max. Safe Operating Area

I_D , Drain Current [A]

Operation in This Area
is Limited by $R_{DS(on)}$

100 μs
1 ms
10 ms
DC

@Notes :
1. T_C = 25 $^{\circ}$C
2. T_J = 150 $^{\circ}$C
3. Single Pulse

V_{DS} , Drain-Source Voltage [V]
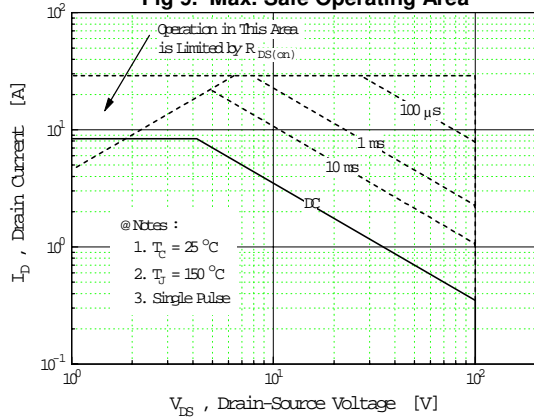
Fig 10. Max. Drain Current vs. Case Temperature

I_D , Drain Current [A]

T_C , Case Temperature [$^{\circ}$C]

Fig 11. Thermal Response

$Z_{\theta JC}(t)$, Thermal Response

D=0.5
0.2
0.1
0.05
0.02
0.01

single pulse

@ Notes :
1. $Z_{\theta JC}(t)$=3.5 $^{\circ}$C/W Max.
2. Duty Factor, D=t_1/t_2
3. T_{JM}−T_C=P_{DM}*$Z_{\theta JC}(t)$

P_{DM}
t_1
t_2

t_1 , Square Wave Pulse Duration [sec]

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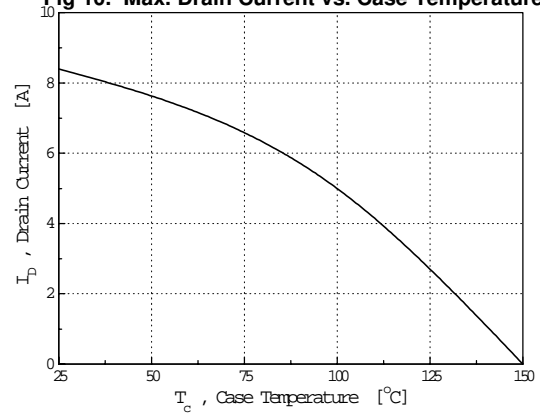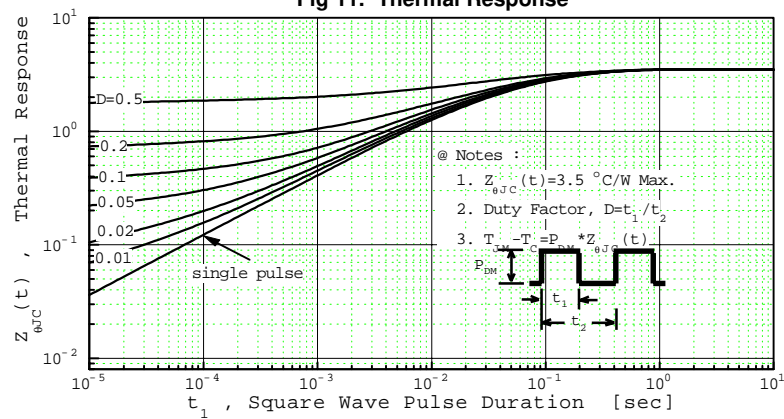
Fig 12. Gate Charge Test Circuit & Waveform

* Current Regulator "

12V
200nF
50KΩ
300nF
Same Type
as DUT

V_{DS}

V_{GS}

DUT

3mA

R_1

R_2

Current Sampling (I_G)
Resistor

Current Sampling (I_D)
Resistor

V_{GS}

10V

Q_g

Q_{gs}

Q_{gd}

Charge
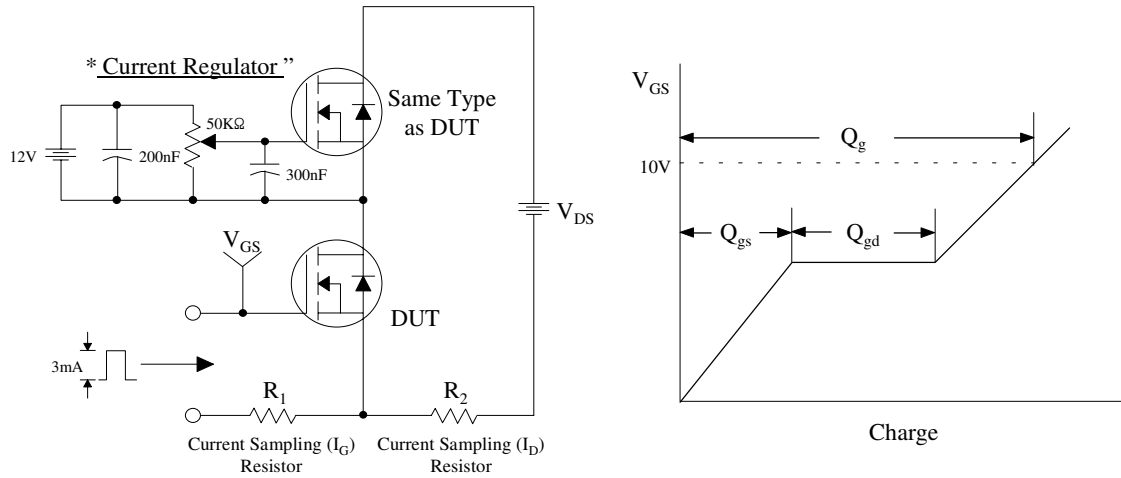
Fig 13. Resistive Switching Test Circuit & Waveforms

R_L

V_{out}

V_{in}

R_G

DUT

V_{DD}
(0.5 rated V_{DS})

10V

V_{out}

90%

V_{in}

10%

$t_{d(on)}$ t_r

t_{on}

$t_{d(off)}$ t_f

t_{off}
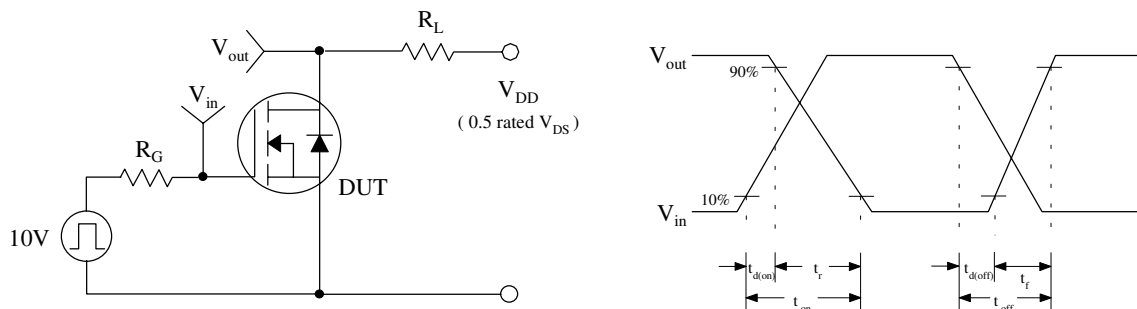
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

L_L

V_{DS}

I_D

Vary t_p to obtain
required peak I_D

R_G

DUT

C

V_{DD}

5V

t_p

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD}

$V_{DS}(t)$

t_p

Time

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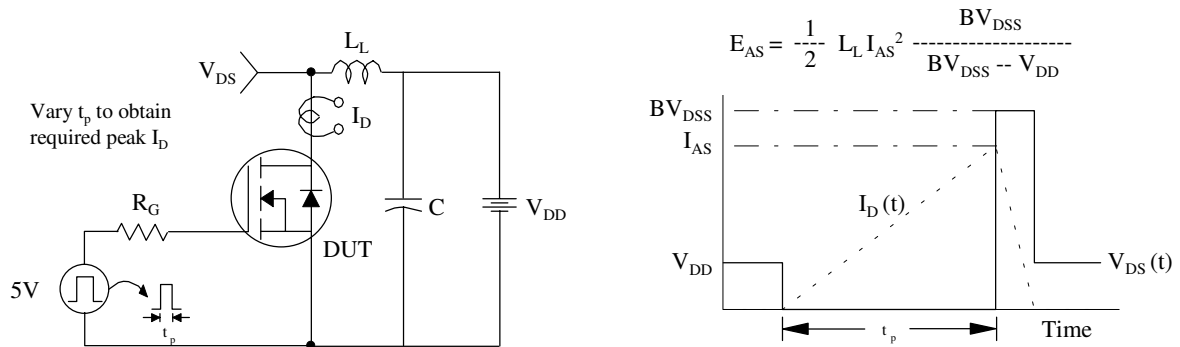
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

+

--

I_S

L

Driver

V_{GS}

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by " R_G "
• I_S controlled by Duty Factor " D "

V_{GS}
(**Driver**)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_S
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_f

V_{DD}

Body Diode
Forward Voltage Drop

6
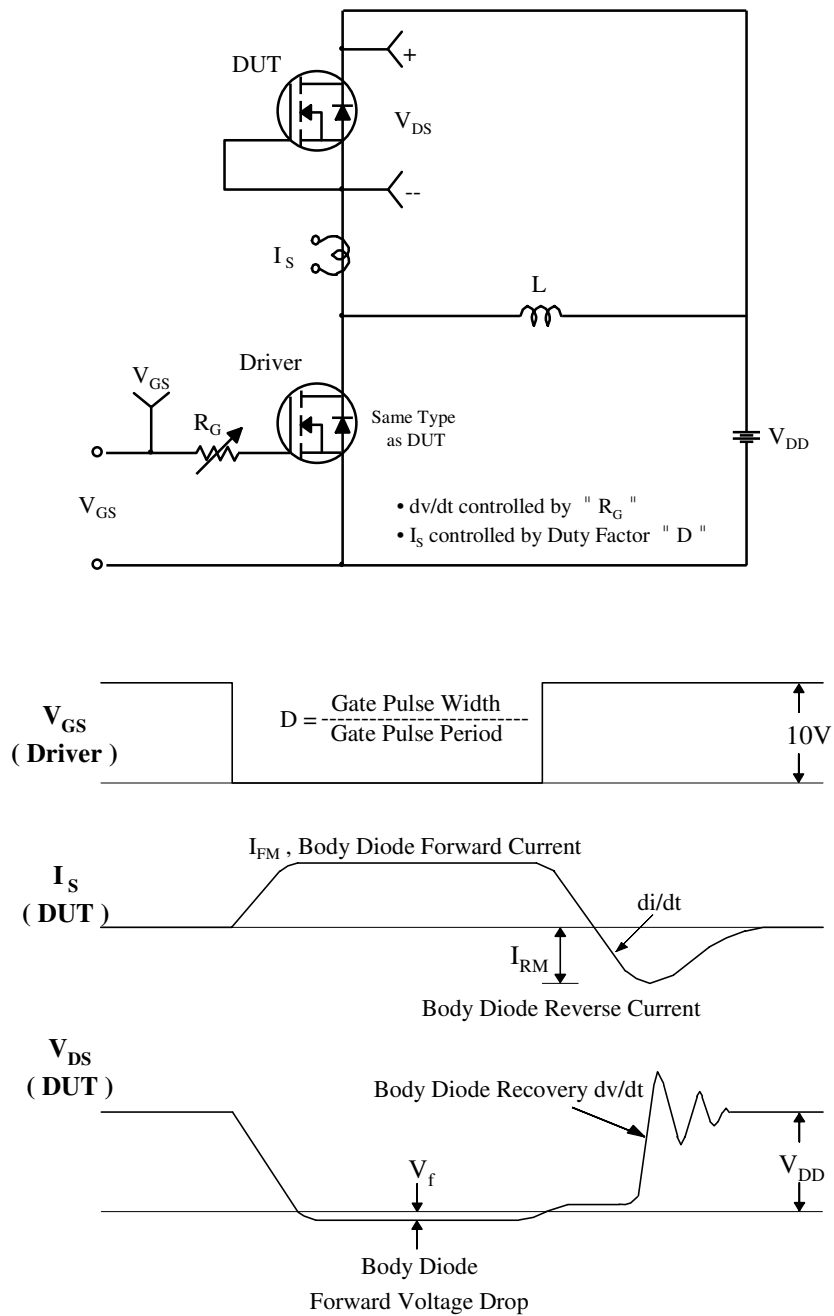
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