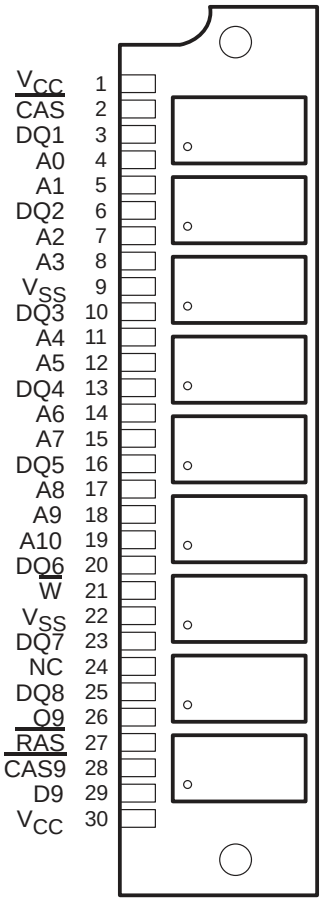
- **Organization . . . 4194304 × 9**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **Utilizes Nine 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period 16 ms (1024 Cycles)**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'4100EAD9-60	60 ns	15 ns	30 ns	110 ns
'4100EAD9-70	70 ns	18 ns	35 ns	130 ns
'4100EAD9-80	80 ns	20 ns	40 ns	150 ns

- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines**
- **Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines**
- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE
(TOP VIEW)



description

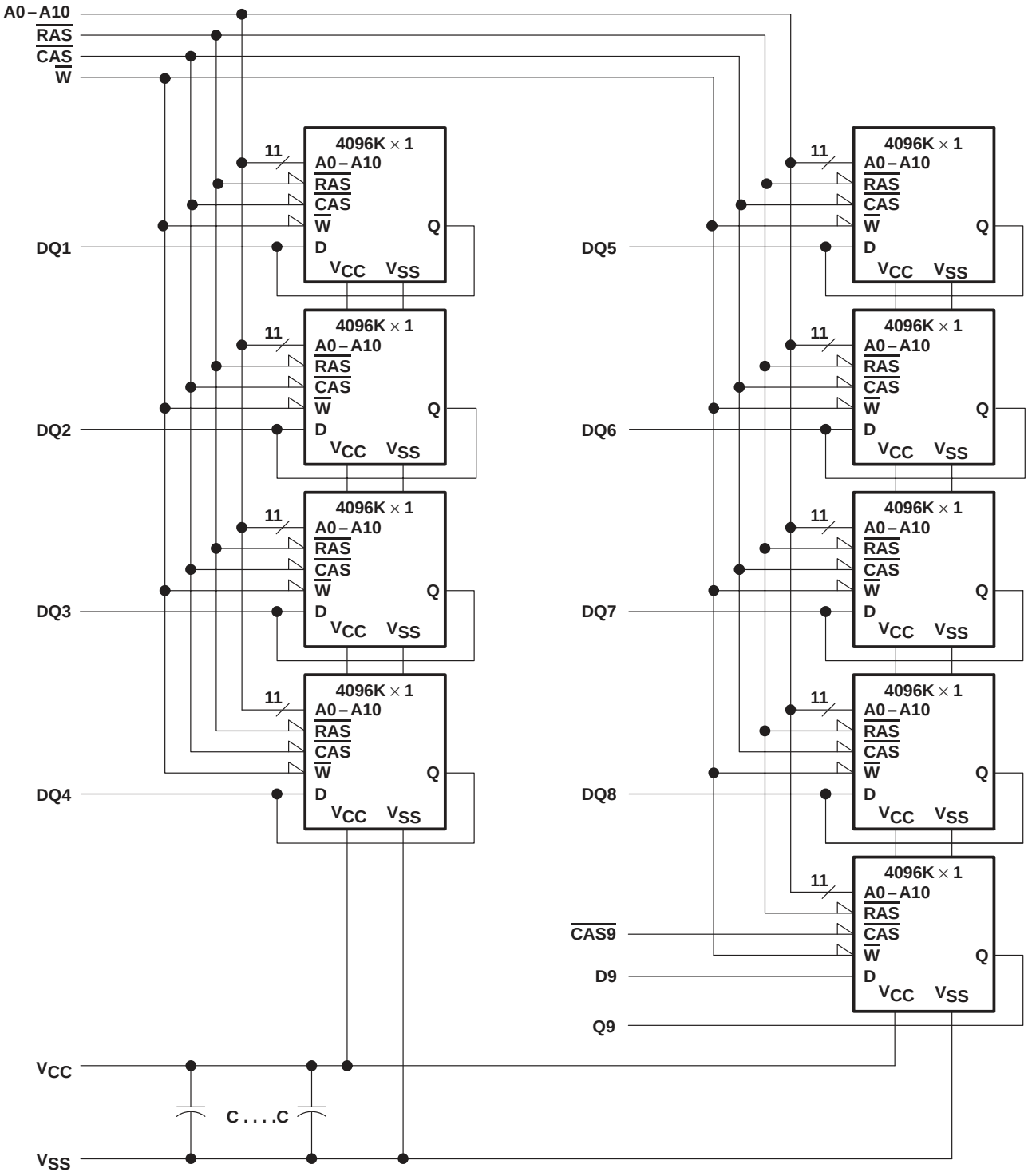
The TM4100EAD9 is a dynamic random-access memory module organized as 4194304 × 9 [bit nine (D9, Q9) is generally used for parity and is controlled by $\overline{CAS9}$] in a 30-pin leadless single in-line memory module (SIMM).

This module is composed of nine TMS44100DJ, 4194304 × 1-bit dynamic RAMs (DRAMs) each in a 20/26-lead plastic small-outline J-lead package (SOJ) mounted on a substrate with decoupling capacitors.

The TM4100EAD9 is characterized for operation from 0°C to 70°C and is available in the AD single-sided, leadless module for use with sockets.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$, $\overline{CAS9}$	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
D9	Data In
NC	No Internal Connection
Q9	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

functional block diagram



operation

The TM4100EAD9 operates as nine TMS44100DJs connected as shown in the functional block diagram. Refer to the TMS44100 data sheet for details of its operation. The common I/O feature of the TM4100EAD9 dictates the use of early-write cycles to prevent contention on D and Q.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 9 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	’4100EAD9-60		’4100EAD9-70		’4100EAD9-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		945		810		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	mA
I_{CC3}	Average refresh current (RAS only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		945		810		720	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0 – A10		45	pF
$C_{i(D)}$	Input capacitance, data input (pin D9)		5	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		63	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		63	pF
$C_{o(DQ)}$	Output capacitance, DQ1 – Q8		12	pF
C_O	Output capacitance, Q9		7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'4100EAD9-60		'4100EAD9-70		'4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’4100EAD9-60		’4100EAD9-70		’4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data (see Note 11)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTS}	Setup time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{DH}	Hold time, data (see Note 10)	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 13)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 13)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 12)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (CBR refresh only)	10		10		10		ns
t_{WTH}	Hold time, $\overline{W}$ low (test mode only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

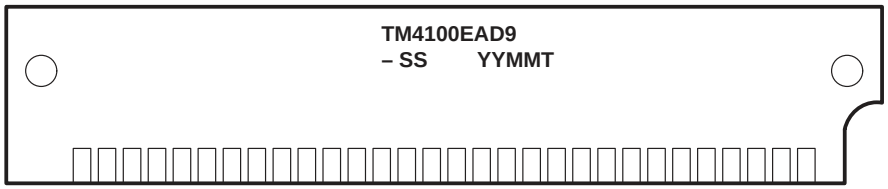
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
12. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		’4100EAD9-60		’4100EAD9-70		’4100EAD9-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTE 14: The maximum value is specified only to assure access time.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of symbolization may vary.

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