CS5374

Dual High-performance Amplifier & ΔΣ Modulator

Features

- High Input Impedance Differential Amplifier
  - Ultra-low input bias: < 1 pA
  - Max signal amplitude: 5 Vpp differential
- Fourth Order Delta-Sigma (ΔΣ) Modulator
  - Signal Bandwidth: DC to 2 kHz
  - Common mode rejection: 110 dB CMRR
- Differential Analog Input, Digital ΔΣ Output
  - Multiplexed inputs: INA, INB, 800Ω termination
  - Selectable Gain: 1x, 2x, 4x, 8x, 16x, 32x, 64x
- Excellent Amplifier Noise Performance
  - 1.5 µVpp between 0.1 Hz and 10 Hz
  - 11 nV / √Hz from 200 Hz to 2 kHz
- High Modulator Dynamic Range
  - 126 dB SNR @ 215 Hz BW (2 ms sampling)
  - 123 dB SNR @ 430 Hz BW (1 ms sampling)
- Low Total Harmonic Distortion
  - –118 dB THD typical (0.000126%)
  - –108 dB THD maximum (0.0004%)
- Low Power Consumption
  - Normal operation: 6.5 mA per channel
  - Power down: 15 µA per channel max
- Dual Power Supply Configuration
  - VA+ = +2.5 V; VA– = –2.5 V; VD = +3.3 V

Description

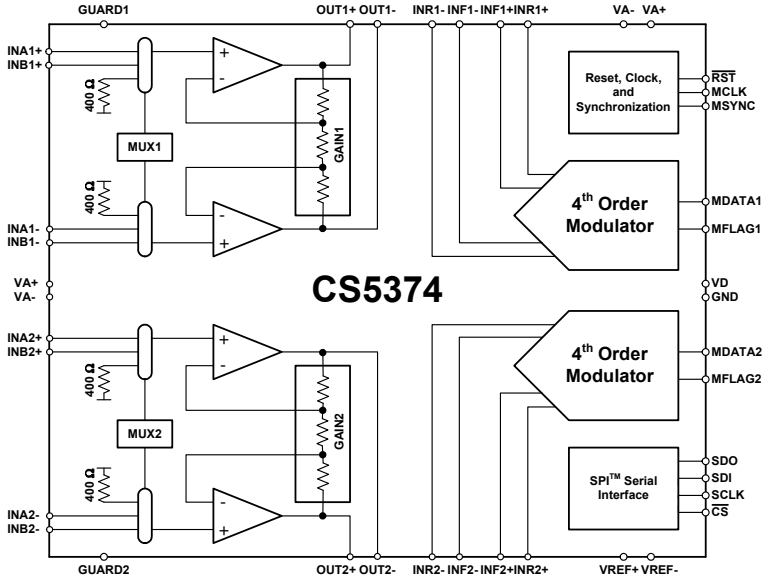
The CS5374 combines two marine seismic analog measurement channels into one 7 mm x 7 mm QFN package. Each measurement channel consists of a high input impedance programmable gain differential amplifier that buffers analog signals into a high-performance, fourth-order ΔΣ modulator. The low-noise ΔΣ modulator converts the analog signal into a one-bit serial bit stream suitable for the CS5376A digital filter.

Each amplifier has two sets of external inputs, INA and INB, to simplify system design as inputs from a hydrophone sensor or the CS4373A test DAC. An internal 800Ω termination can also be selected for noise tests. Gain settings are binary weighted (1x, 2x, 4x, 8x, 16x, 32x, 64x) and match the CS4373A test DAC output attenuation settings for full-scale testing at all gain ranges. Both the input multiplexer and gain are set by registers accessed through a standard SPI™ port.

Each fourth-order ΔΣ modulator has very high dynamic range combined with low total harmonic distortion and low power consumption. It converts differential analog signals from the amplifier to an oversampled ΔΣ serial bit stream which is decimated by the CS5376A digital filter to a 24-bit output at the final output word rate.

ORDERING INFORMATION

See page 43.



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

- Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.
- GND = 0 V, all voltages with respect to 0 V.
- Device connected as shown in Figure 11 and Figure 12 unless otherwise noted.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Bipolar Power Supplies						
Positive Analog	±2%	VA+	2.45	2.50	2.55	V
Negative Analog	(Note 1) ±2%	VA-	-2.45	-2.50	-2.55	V
Positive Digital	±3%	VD	3.20	3.30	3.40	V
Voltage Reference						
[VREF+] - [VREF-]	(Note 2, 3)	VREF	-	2.500	-	V
VREF-	(Note 4)	VREF-	-	VA -	-	V
Thermal						
Ambient Operating Temperature	-CNZ	T_A	-10	25	70	°C

Notes: 1. VA- must always be the most-negative input voltage to avoid potential SCR latch-up conditions.
2. By design, a 2.500 V voltage reference input results in the best signal-to-noise performance.
3. Channel-to-channel gain accuracy is directly proportional to the voltage reference absolute accuracy.
4. VREF inputs must satisfy: VA- ≤ VREF- < VREF+ ≤ VA+.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
DC Power Supplies	Positive Analog	VA+	-0.3	6.8	V
	Negative Analog	VA-	-6.8	0.3	V
	Digital	VD	-0.3	6.8	V
Analog Supply Differential	[(VA+) - (VA-)]	VA_{DIFF}	-	6.8	V
Digital Supply Differential	[(VD) - (VA-)]	VD_{DIFF}	-	6.8	V
Input Current, Any Pin Except Supplies	(Note 5, 6)	I_{IN}	-	±10	mA
Input Current, Power Supplies	(Note 5)	I_{PWR}	-	±50	mA
Output Current	(Note 5)	I_{OUT}	-	±25	mA
Power Dissipation		PD	-	500	mW
Analog Input Voltages		V_{INA}	(VA-)-0.5	(VA+)+0.5	V
Digital Input Voltages		V_{IND}	-0.5	(VD)+0.5	V
Storage Temperature Range		T_{STG}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 5. Transient currents up to 100mA will not cause SCR latch-up.
6. Includes continuous over-voltage conditions on the analog input pins.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	-10	-	70	°C
Storage Temperature Range	T_{STR}	-65	-	150	°C
Allowable Junction Temperature	T_{JCT}	-	-	125	°C
Junction to Ambient Thermal Impedance (4-layer PCB)	θ_{JA}	-	26	-	°C / W

ANALOG CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Amplifier Inputs						
Signal Frequencies		BW	DC	-	2000	Hz
Differential Gain		GAIN	x1	-	x64	
Common Mode Gain	(Note 7)	$GAIN_{CM}$	-	x1	-	
Common Mode Voltage		V_{cm}	-	(VA-)+2.5	-	V
Voltage Range (Signal + Vcm)	x1	V_{IN}	(VA-)+0.7	-	(VA+)-1.25	V
	x2 - x64		(VA-)+0.7	-	(VA+)-1.75	
Full Scale Differential Input	x1	V_{INFS}	-	-	5	V_{pp}
	x2		-	-	2.5	V_{pp}
	x4		-	-	1.25	V_{pp}
	x8		-	-	625	mV_{pp}
	x16		-	-	312.5	mV_{pp}
	x32		-	-	156.25	mV_{pp}
	x64		-	-	78.125	mV_{pp}
Differential Input Impedance		Z_{INDIFF}	-	1, 20	-	TΩ, pF
Common Mode Input Impedance		Z_{INCM}	-	0.5, 40	-	TΩ, pF
Input Bias Current		I_{IN}	-	1	40	pA
Amplifier Outputs						
Full Scale Output, Differential		V_{OUT}	-	-	5	V_{pp}
Output Voltage Range (Signal + Vcm)		V_{RNG}	(VA-)+0.5	-	(VA+)-0.5	V
Output Impedance	(Note 8)	Z_{OUT}	-	40	-	Ω
Output Impedance Drift	(Note 8)	Z_{TC}	-	0.38	-	Ω/°C
Output Current		I_{OUT}	-	-	±25	mA
Load Capacitance		C_L	-	-	100	nF
Guard Outputs						
Guard Output Voltage		V_{GUARD}	-	V_{cm}	-	V
Guard Output Impedance	(Note 8)	ZG_{OUT}	-	500	-	Ω
Guard Output Current		IG_{OUT}	-	-	40	µA
Guard Load Capacitance		CG_L	-	-	100	pF

Notes: 7. Common mode signals pass through the differential amplifier architecture and are rejected by the modulator CMRR.

8. Output impedance characteristics are approximate and can vary up to ±30% depending on process parameters.

ANALOG CHARACTERISTICS (CONT.)

Parameter		Symbol	Min	Typ	Max	Unit
Modulator Inputs						
Input Signal Frequencies (Note 9)		V_{BW}	DC	-	2000	Hz
Full-scale Differential AC Input		V_{AC}	-	-	5	V_{pp}
Full-scale Differential DC Input		V_{DC}	-2.5	-	2.5	V_{DC}
Input Common Mode Voltage		V_{CM}	-	(VA-)+2.5	-	V
Input Voltage Range (V_{cm} ± Signal)		V_{RNG}	(VA-)+0.7	-	(VA+)-1.25	V
Differential Input Impedance	INR± INF±	$ZDIF_{INR}$ $ZDIF_{INF}$	- -	20 1	- -	kΩ MΩ
Single-ended Input Impedance	INR± INF±	ZSE_{INR} ZSE_{INF}	- -	40 2	- -	kΩ MΩ
External Anti-alias Filter (Note 10)	Series Resistance Differential Capacitance	R_{AA} C_{DIFF}	- -	680 20	- -	Ω nF
VREF Inputs						
[VREF+] - [VREF-] (Note 2, 3)		VREF	-	2.500	-	V
VREF- (Note 4)		VREF-	-	VA -	-	V
VREF Input Current		$VREF_{II}$	-	120	-	µA
VREF Input Noise (Note 11)		$VREF_{IN}$	-	-	1	$µV_{rms}$

Notes: 9. The upper bandwidth limit is determined by the selected digital filter cut-off frequency.

10. Anti-alias capacitors are discrete external components and must be of good quality (C0G, NPO, poly). Poor-quality capacitors will degrade total harmonic distortion (THD) performance. See Figure 1 for external anti-alias filter connections.

11. Maximum integrated noise over the measurement bandwidth for the voltage reference device attached to the VREF inputs.

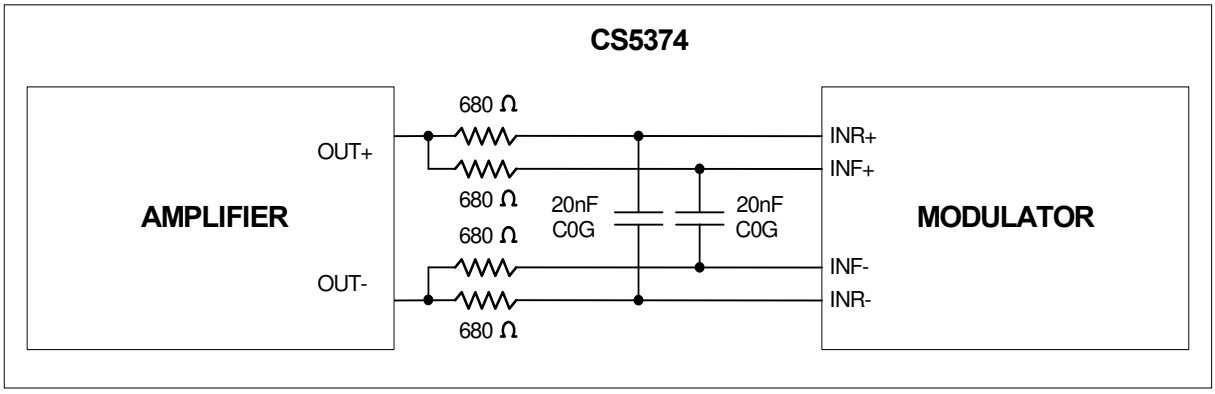


Figure 1. External Anti-alias Filter Components

PERFORMANCE SPECIFICATIONS

Parameter		Symbol	Min	Typ	Max	Unit
Amplifier Noise						
Voltage Noise	f_0 = 0.1 Hz to 10 Hz	VN_{PP}	-	1.5	3	μV_{pp}
Voltage Noise Density	f_0 = 200 Hz to 2 kHz	VN_D	-	11	14	$nV/\sqrt{Hz}$
Current Noise Density		IN_D	-	20	-	$fA/\sqrt{Hz}$
Channel Dynamic Range						
Dynamic Range	(1/4 ms) DC to 1720 Hz	SNR	-	105	-	dB
(1x Gain, Multiple OWRs)	(1/2 ms) DC to 860 Hz		-	120	-	dB
(Note 9, 12)	(1 ms) DC to 430 Hz		121	123	-	dB
	(2 ms) DC to 215 Hz		-	126	-	dB
	(4 ms) DC to 108 Hz		-	129	-	dB
	(8 ms) DC to 54 Hz		-	131	-	dB
	(16 ms) DC to 27 Hz		-	135	-	dB
Dynamic Range	1x	SNR	121	123	-	dB
(Multiple Gains, 1 ms OWR)	2x		-	122	-	dB
(Note 9, 12)	3x		-	120	-	dB
	8x		-	116	-	dB
	16x		-	111	-	dB
	32x		-	105	-	dB
	64x		-	98	-	dB
Channel Distortion						
Total Harmonic Distortion	1x		-	-118	-108	dB
(Note 13)	2x		-	-119	-	dB
	4x		-	-119	-	dB
	8x	THD	-	-119	-	dB
	16x		-	-118	-	dB
	32x		-	-115	-	dB
	64x		-	-112	-	dB

Notes: 12. Dynamic Range defined as 20 log [(RMS full scale) / (RMS idle noise)] where idle noise is measured with the amplifier input terminated. Dynamic Range is dominated by high-frequency quantization noise at the 1/4 ms rate and amplifier noise at high gain.

13. Tested with a 31.25 Hz sine wave at 1 ms sampling rate and -1 dB amplitude.

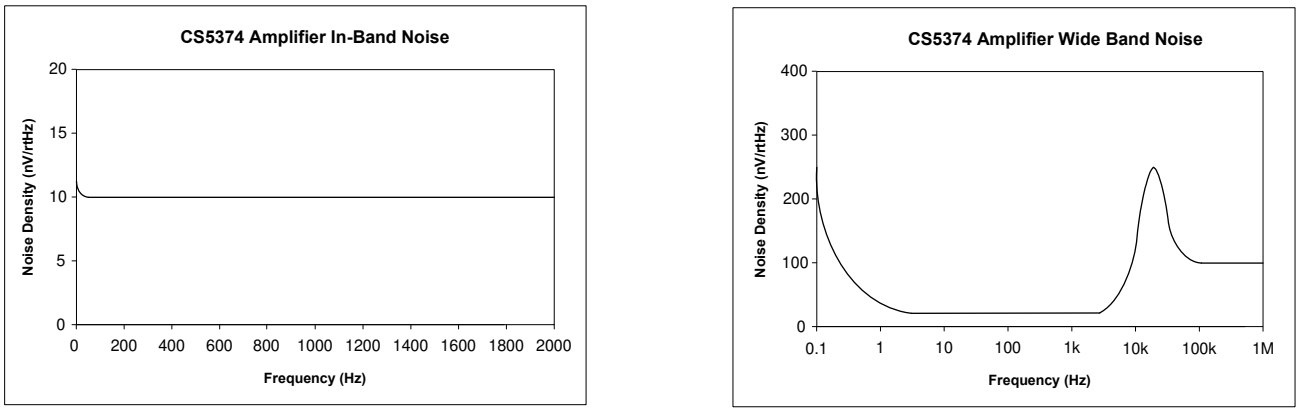


Figure 2. CS5374 Amplifier Noise Performance

PERFORMANCE SPECIFICATIONS (CONT.)

Parameter		Symbol	CS5374 Min	CS5374 Typ	CS5374 Max	Unit
Channel Gain Accuracy						
Channel Gain, Offset Corrected	(Note 3, 14)	$GAIN_{LSB}$	-6101194 0xA2E736	- -	6101194 0x5D18CA	LSB LSB
Absolute Gain Accuracy	(Note 3, 15)	$GAIN_{ABS}$	-	±1	±2	%
Relative Gain Accuracy (Note 16)	2x	$GAIN_{REL}$	-0.3	-0.1	0.1	%
	4x		-	-0.1	-	%
	8x		-	0.1	-	%
	16x		-	0.4	-	%
	32x		-	0.4	-	%
	64x		-	0.3	-	%
Gain Drift	(Note 17)	$GAIN_{TC}$	-	25	-	ppm / °C
Channel Offset Accuracy						
Amplifier Offset Voltage, Input Referred	(Note 18)	$OFST_{AMP}$	-	±250	±750	µV
Amplifier Offset Drift, Input Referred	(Note 17)	$OFST_{ATC}$	-	0.3	-	µV / °C
Modulator Offset Voltage, Differential	($\overline{OFST}$ = 1)	$OFST_{MOD}$	-	±1	-	mV
Modulator Offset Voltage, Channel 1	($\overline{OFST}$ = 0)	$OFST_{MOD1}$	-	-60	-	mV
Modulator Offset Voltage, Channel 2	($\overline{OFST}$ = 0)	$OFST_{MOD2}$	-	-35	-	mV
Modulator Offset Drift	(Note 17)	$OFST_{MTC}$	-	1	-	µV / °C
Offset After Calibration	(Note 19)	$OFST_{CAL}$	-	±1	-	µV
Offset Calibration Range	(Note 20)	$OFST_{RNG}$	-	100	-	%FS
Channel CMRR and Crosstalk						
Common Mode Rejection Ratio		CMRR	-	110	-	dB
Crosstalk, Amplifier Multiplexed Inputs		CXT_{MI}	-	-130	-	dB
Crosstalk, Channel-to-Channel		CXT_{CC}	-	-130	-	dB

Notes: 14. Channel Gain is the nominal full-scale 24-bit output code from the CS5376A digital filter for a 5 V_{PP} differential signal into the CS5374 analog inputs at 1x gain. Value is offset corrected.

15. Absolute gain accuracy tests the matching of 1x gain across multiple CS5374 channels in a system.

16. Relative gain accuracy tests the tracking of 2x, 4x, 8x, 16x, 32x, 64x gain relative to 1x gain on a single CS5374 channel.

17. Specification is for the parameter over the specified temperature range and is for the CS5374 device only. It does not include the effects of external components.

18. Offset voltage is tested with the amplifier inputs connected to the internal 800 Ω termination.

19. The offset after calibration specification is measured from the digitally calibrated output codes of the CS5376A digital filter.

20. Offset calibration is performed in the CS5376A digital filter and includes the full-scale signal range.

CHANNEL PERFORMANCE PLOTS

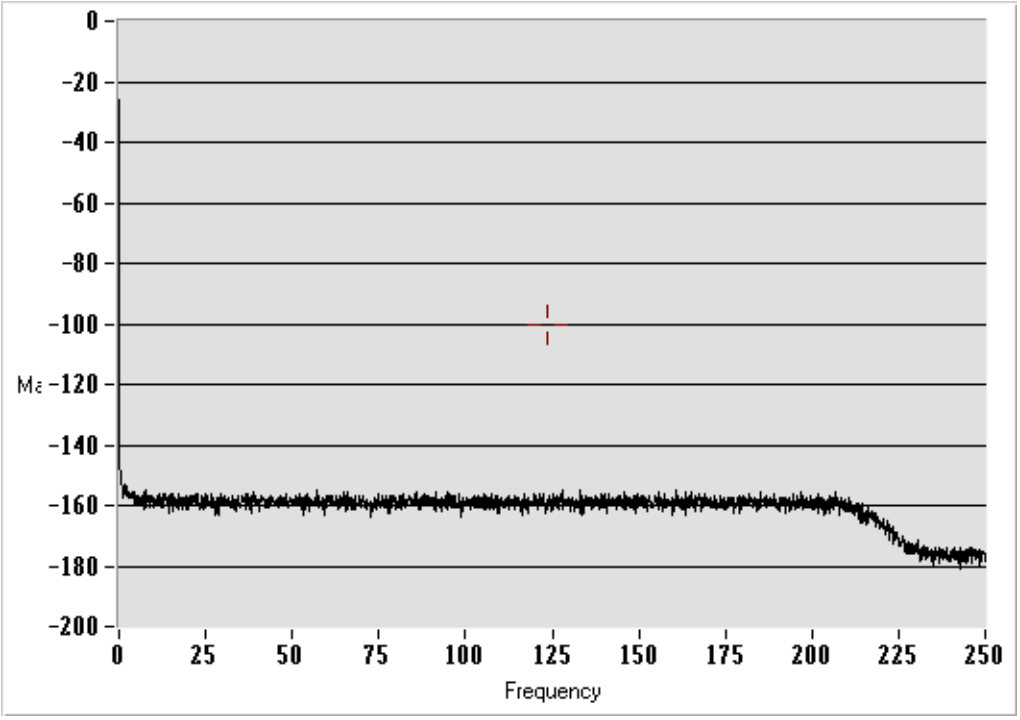


Figure 3. CS5374 Noise Performance (1x Gain)

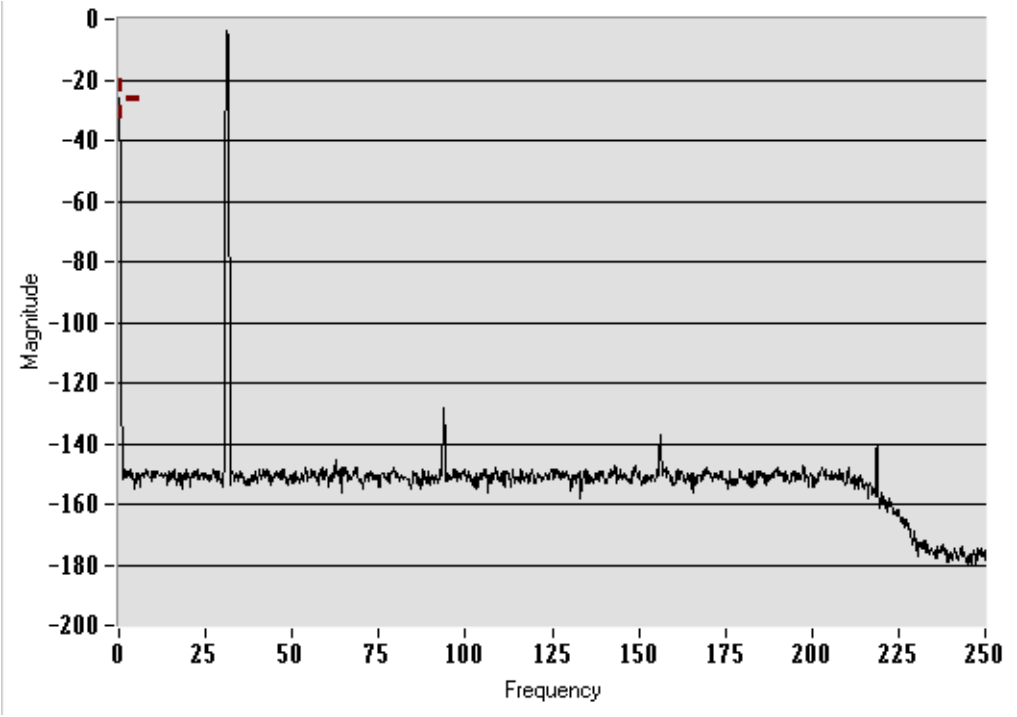


Figure 4. CS5374 + CS4373A Test DAC Dynamic Performance

DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs					
High-level Input Voltage (Note 21)	V_{IH}	0.6*VD	-	VD	V
Low-level Input Voltage (Note 21)	V_{IL}	0.0	-	0.8	V
Input Leakage Current	I_{IN}	-	±1	±10	µA
Digital Input Capacitance	C_{IN}	-	9	-	pF
Input Rise Times Except MCLK	t_{RISE}	-	-	100	ns
Input Fall Times Except MCLK	t_{FALL}	-	-	100	ns
Digital Outputs					
High-level Output Voltage, I_{out} = -40 µA	V_{OH}	VD - 0.3	-	-	V
Low-level Output Voltage, I_{out} = 40 µA	V_{OL}	-	-	0.3	V
High-Z Leakage Current	I_{OZ}	-	±1	±10	µA
Digital Output Capacitance	C_{OUT}	-	9	-	pF
Output Rise Times (Note 22)	t_{RISE}	-	-	100	ns
Output Fall Times (Note 22)	t_{FALL}	-	-	100	ns

Notes: 21. Device is intended to be driven with CMOS logic levels.

22. Guaranteed by design and/or characterization.

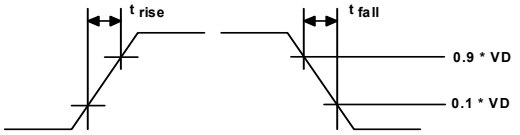


Figure 5. Digital Rise and Fall Times SYNC from external system.

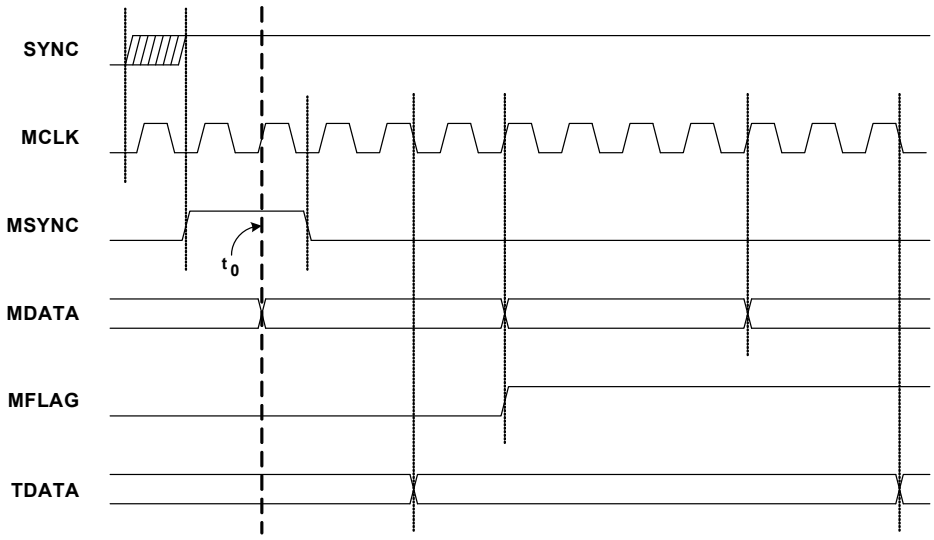


Figure 6. System Synchronization Diagram

SYNC from External. MCLK, MSYNC, TDATA from CS5376A. MDATA, MFLAG from CS5374.

DIGITAL CHARACTERISTICS (CONT.)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Input						
MCLK Frequency	(Note 23)	f_{MCLK}	-	2.048	-	MHz
MCLK Duty Cycle		$MCLK_{DTC}$	40	-	60	%
MCLK Rise Time		t_{RISE}	-	-	50	ns
MCLK Fall Time		t_{FALL}	-	-	50	ns
MCLK Jitter (in-band or aliased in-band)		$MCLK_{IBJ}$	-	-	300	ps
MCLK Jitter (out-of-band)		$MCLK_{OBJ}$	-	-	1	ns
Master Sync Input						
MSYNC Setup Time to MCLK Falling	(Note 24)	t_{MSS}	20	366	-	ns
MSYNC Period	(Note 24)	t_{MSYNC}	40	976	-	ns
MSYNC Hold Time after MCLK Falling	(Note 24)	t_{MSH}	20	610	-	ns
MDATA Output						
MDATA Output Bit Rate		f_{MDATA}	-	512	-	kbits/s
MDATA Output One's Density Range	(Note 22)	$MDAT_{1D}$	14	-	86	%
Full-scale Output Code, Offset Corrected	(Note 25)	$MDAT_{FS}$	0xA2E736	-	0x5D18CA	

Notes: 23. MCLK is generated by the CS5376A digital filter. If MCLK is disabled, the CS5374 device automatically enters a power-down state. See Power Supply Characteristics for typical power-down timing.

24. MSYNC is generated by the CS5376A digital filter and is latched by CS5374 on MCLK falling edge, synchronization instant ($\mathbf{t_0}$) is on the next MCLK rising edge.

25. Decimated, filtered, and offset-corrected 24-bit output word from the CS5376A digital filter.

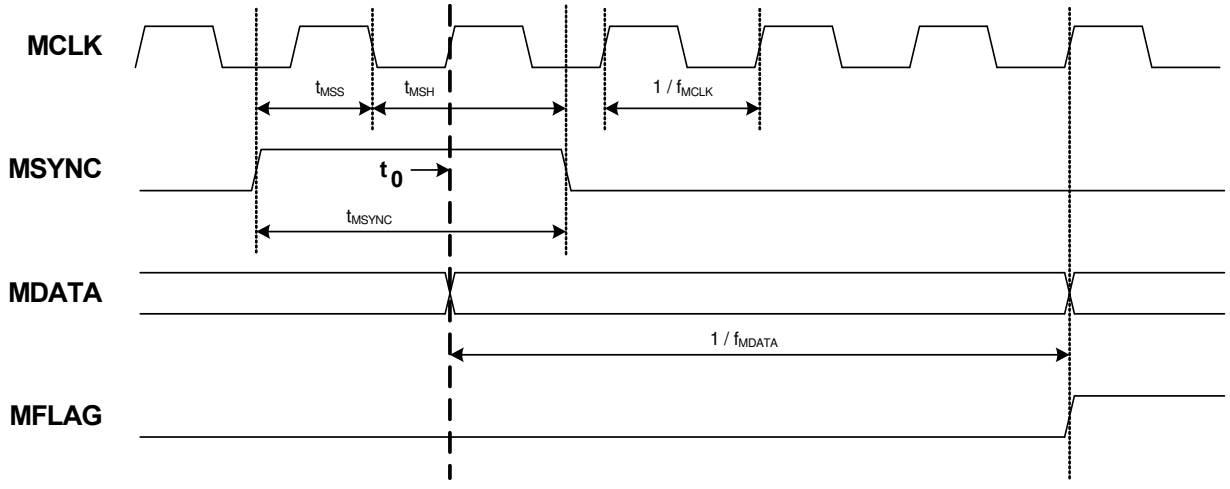


Figure 7. MCLK / MSYNC Timing Detail

SPI™ INTERFACE TIMING (EXTERNAL MASTER)

Parameter	Symbol	Min	Typ	Max	Unit
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_1	60	-	-	ns
Data Set-up Time Prior to SCK Rising	t_2	60	-	-	ns
Data Hold Time After SCK Rising	t_3	60	-	-	ns
SCK High Time	t_4	120	-	-	ns
SCK Low Time	t_5	120	-	-	ns
SCK Falling Prior to $\overline{CS}$ Disable	t_6	60	-	-	ns
SDO Read Timing					
SCK Falling to New Data Bit	t_7	-	-	90	ns
SCK High Time	t_8	120	-	-	ns
SCK Low Time	t_9	120	-	-	ns
SCK Falling Hold Time Prior to $\overline{CS}$ Disable	t_{10}	60	-	-	ns

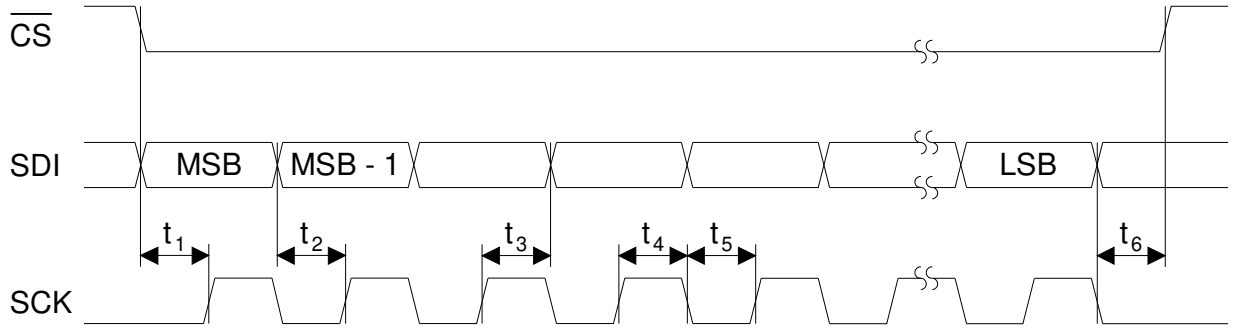


Figure 8. SDI Write Timing in SPI Slave Mode

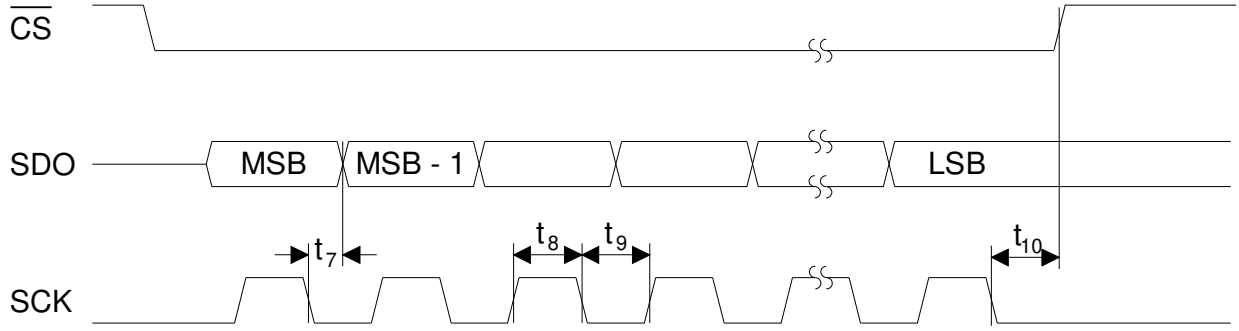


Figure 9. SDO Read Timing in SPI Slave Mode

POWER SUPPLY CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current, ch1 + ch2 combined						
Analog Power Supply Current	(Note 26)	I_A	-	13	16	mA
Digital Power Supply Current	(Note 26)	I_D	-	50	100	µA
Power Supply Current, ch1 or ch2 only						
Analog Power Supply Current	(Note 26)	I_A	-	6.5	8	mA
Digital Power Supply Current	(Note 26)	I_D	-	25	50	µA
Power Down Current, MCLK enabled						
Analog Power Supply Current	(Note 26)	I_A	-	150	250	µA
Digital Power Supply Current	(Note 26)	I_D	-	10	75	µA
Power Down Current, MCLK disabled						
Analog Power Supply Current	(Note 26)	I_A	-	2	15	µA
Digital Power Supply Current	(Note 26)	I_D	-	1	15	µA
Power Down Timing (after MCLK disabled)	(Note 22)	PD_{TC}	-	40	-	µS
Power Supply Rejection						
Power Supply Rejection Ratio	(Note 22)	PSRR	-	100	-	dB

Notes: 26. All outputs unloaded. Digital inputs forced to VD or GND respectively. Amplifier inputs connected to the 800 Ω internal termination.

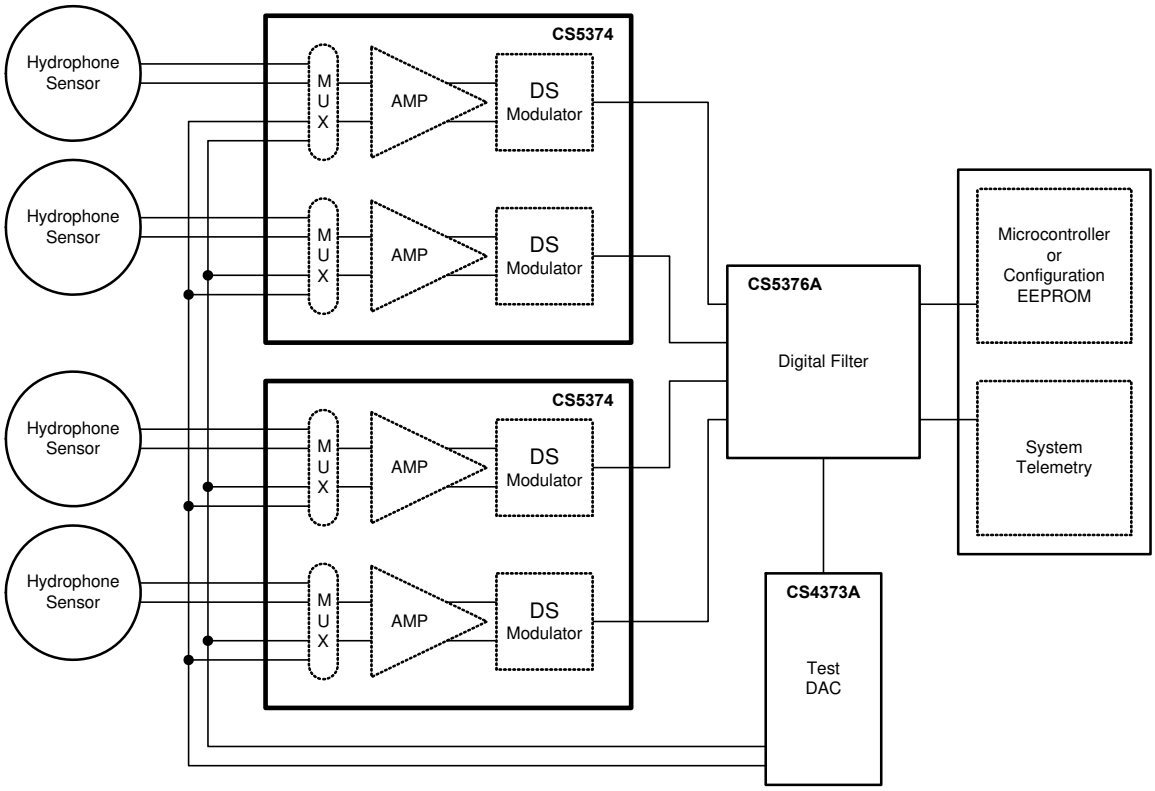


Figure 10. CS5374 System Block Diagram

2. GENERAL DESCRIPTION

The CS5374 combines two marine seismic analog measurement channels into one 7 mm x 7 mm QFN package. Each measurement channel consists of a high input impedance programmable gain differential amplifier that buffers analog signals into a high-performance, fourth-order ΔΣ modulator. The low-noise ΔΣ modulator converts the analog signal into a one-bit serial bit stream suitable for the CS5376A digital filter.

Each amplifier has two sets of external inputs, INA and INB, to simplify system design as inputs from a hydrophone sensor or the CS4373A test DAC. An internal 800 Ω termination can also be selected for noise tests. Gain settings are binary weighted (1x, 2x, 4x, 8x, 16x, 32x, 64x) and match the CS4373A test DAC output attenuation settings for full-scale testing at all gain ranges. Both the input multiplexer and gain are set by registers accessed through a standard SPI™ port.

Each fourth-order ΔΣ modulator has very high dynamic range combined with low total harmonic distortion and low power consumption. It converts differential analog signals from the amplifier to an oversampled ΔΣ serial bit stream which is decimated by the CS5376A digital filter to a 24-bit output at the final output word rate.

Figure 10 shows the system-level architecture of a 4-channel acquisition system using two CS5374, one CS5376A digital filter and one CS4373A test DAC.

Figure 11 and Figure 12 shows connection diagrams for the CS5374 device when connected to the CS5376A digital filter.

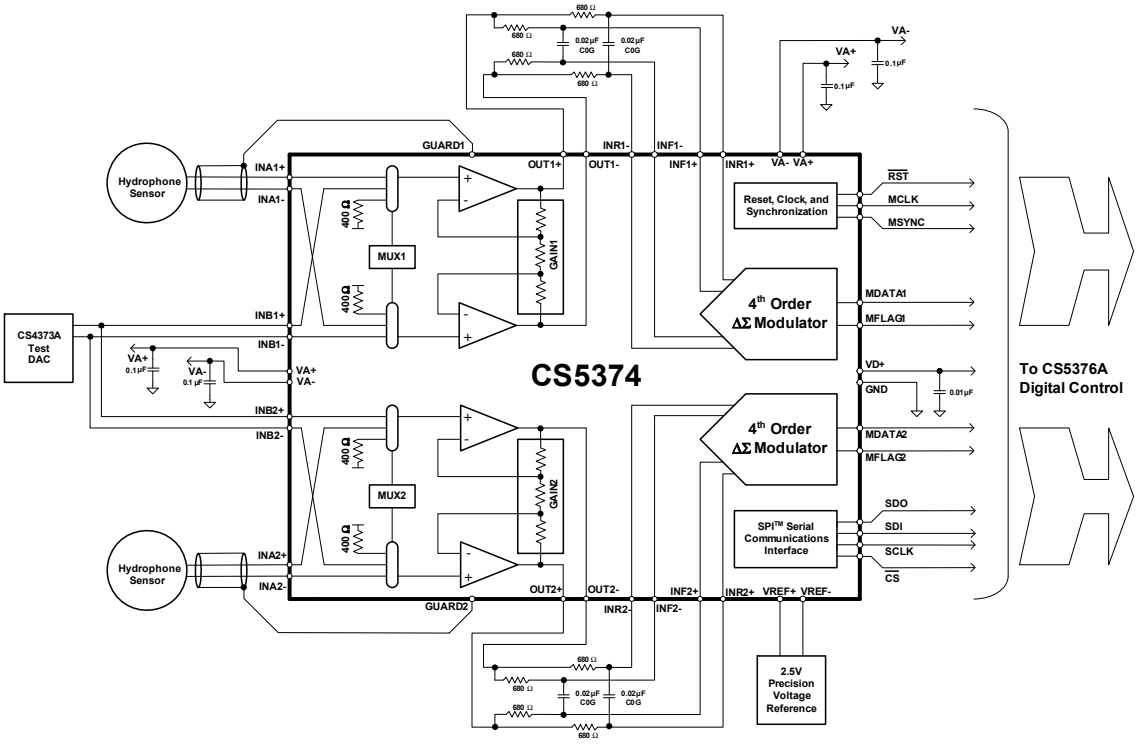


Figure 11. CS5374 Connection Diagram

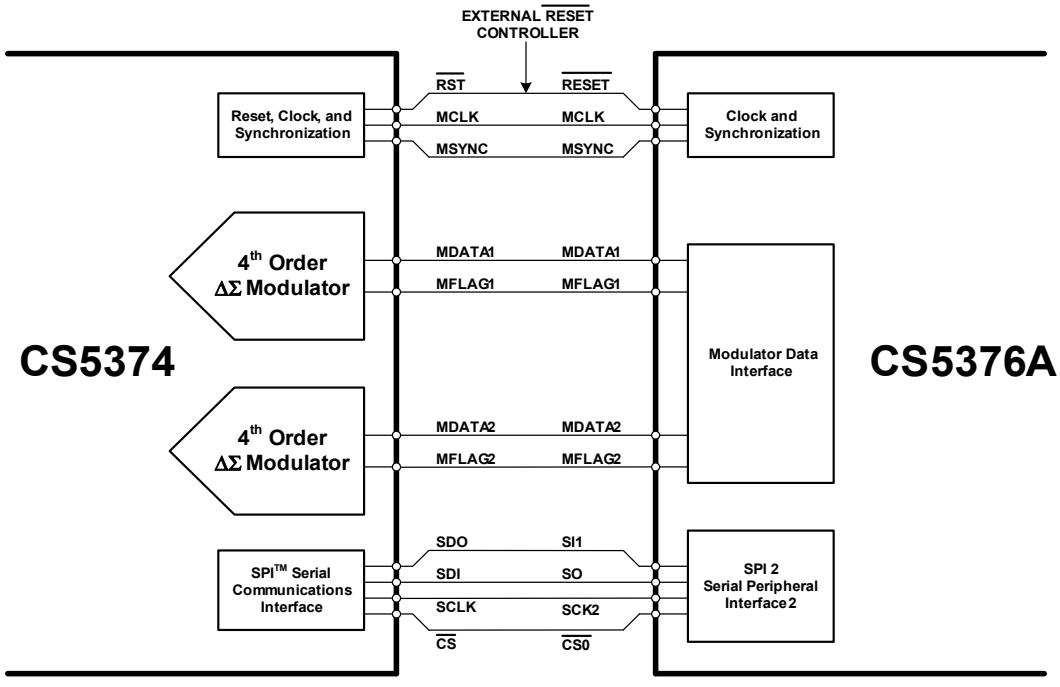


Figure 12. CS5374 to CS5376A Digital Interface

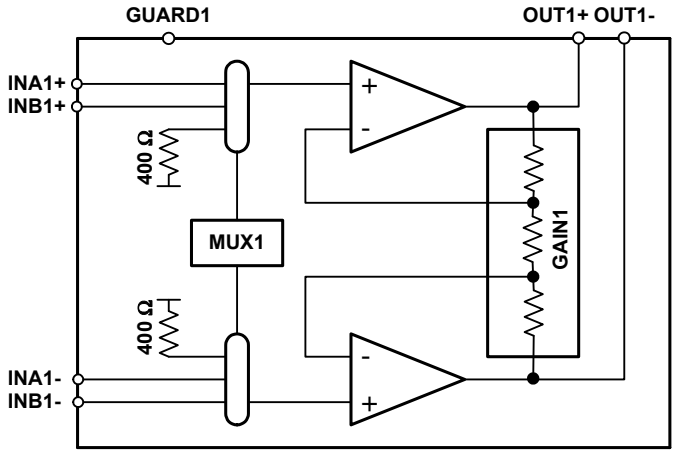


Figure 13. CS5374 Amplifier Block Diagram

3. AMPLIFIER OPERATION

The CS5374 high-impedance, low-noise CMOS differential input, differential output amplifiers are optimized for precision analog signals between DC and 2 kHz. They have multiplexed inputs and programmable gains of 1x, 2x, 4x, 8x, 16x, 32x, and 64x. The performance of this amplifier makes it ideal for low-frequency, high-dynamic-range applications requiring low distortion and minimal power consumption.

3.1 Amplifier Inputs — INA, INB

The amplifier analog inputs are designed for high-impedance differential hydrophone sensors and so have very low input bias below 1 pA.

3.1.1 Multiplexer Settings — MUX

Input multiplexing simplifies system connections by providing separate inputs for a sensor and test DAC (INA, INB) as well as an internal termination for noise tests. The multiplexer determines which input is connected to the amplifier, and is set through internal configuration registers accessed through the SPI port, see the "SPI™ Register Summary" on page 34 for more information.

Although a mux selection is provided to enable the INA and INB switches simultaneously, significant current should not be driven through them in this mode. The CS5374 mux switches will maintain good linearity only with minimal signal current.

3.1.2 Gain Settings — GAIN

The CS5374 supports gain ranges of 1x, 2x, 4,x 8x, 16x, 32x, and 64x. Amplifier gain is selected using internal configuration registers accessed through the SPI port, see the "SPI™ Register Summary" on page 34 for more information.

3.2 Amplifier Outputs — OUTR, OUTF

The amplifier analog outputs are externally separated into rough / fine charge signals to connect into the modulator inputs. Each differential output requires two series resistors and a differential capacitor to create the modulator anti-alias RC filter.

3.2.1 Guard Output — GUARD

The GUARD pin outputs the common mode voltage of the selected analog signal input. It can be used to drive the cable shield between a high-impedance sensor and the amplifier inputs. Driving the cable shield with the analog signal common mode voltage minimizes leakage and improves signal integrity from high-impedance sensors.

The GUARD output is defined as the midpoint voltage between the + and – halves of the currently

selected differential input signal, and will vary as the signal common mode varies. The GUARD output will not drive a significant load, as it can only provide a shielding voltage.

3.3 Differential Signals

Analog signals into and out of the amplifiers are differential, consisting of two halves with equal but opposite magnitude varying about a common mode voltage.

A full-scale 5 V_{pp} differential signal centered on a –0.15 V common mode can have:

SIG+ = –0.15 V + 1.25 V = 1.1 V

SIG– = –0.15 V – 1.25 V = –1.4 V

SIG+ is +2.5 V relative to SIG-

For the reverse case:

SIG+ = –0.15 V – 1.25 V = –1.4 V

SIG– = –0.15 V + 1.25 V = 1.1 V

SIG+ is –2.5 V relative to SIG-

The total swing for SIG+ relative to SIG– is (+2.5 V) – (–2.5 V) = 5 V_{pp}. A similar calculation can be done for SIG– relative to SIG+. Note that a 5 V_{pp} differential signal centered on a –0.15 V common mode voltage never exceeds 1.1 V and never drops below –1.4 V on either half of the signal.

By definition, differential voltages are to be measured with respect to the opposite half, not relative to ground. A multi-meter differentially measuring between SIG+ and SIG– in the above example would properly read 1.767 V_{rms}, or 5 V_{pp}.

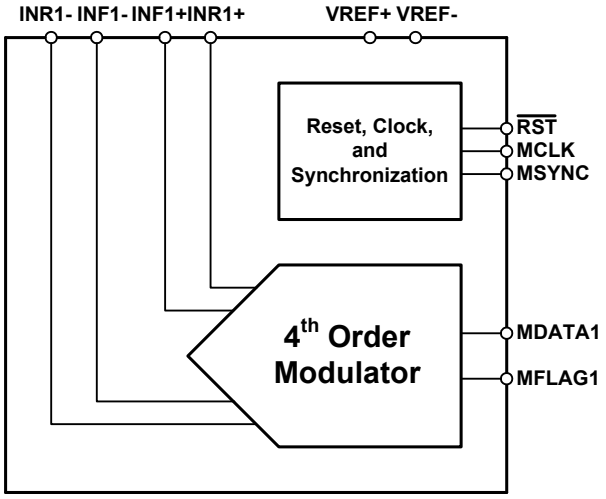


Figure 14. CS5374 Modulator Block Diagram

4. MODULATOR OPERATION

The CS5374 modulators are fourth-order ΔΣ type optimized for extremely high-resolution measurement of signals between DC and 2000 Hz. When combined with the internal differential amplifiers, the CS4373A test DAC and CS5376A digital filter, a small, low-power, self-testing, high-accuracy, multi-channel measurement system results.

The modulators have high dynamic range and low total harmonic distortion with very low power consumption. They are optimized for extremely high-resolution measurement of 5 V_{p-p} or smaller differential signals. They convert analog input signals from the differential amplifiers to an oversampled serial bit stream which is then passed to the digital filter.

The companion CS5376A digital filter generates the clock and synchronization inputs for the modulators while receiving the one-bit data and over-range flag outputs. The digital filter decimates the modulator's oversampled output bit stream to a high-resolution, 24-bit output at the final selected output word rate.

4.1 Modulator Anti-Alias Filter

The modulator inputs are required to be bandwidth limited to ensure modulator loop stability and prevent high-frequency signals from aliasing into the measurement bandwidth. The use of simple, single-pole, differential, low-pass RC filters across the INR± and INF± inputs ensures high-frequency signals are rejected before they can alias into the measurement bandwidth.

The approximate –3 dB corner of the input anti-alias filter is nominally set to the internal analog sampling rate divided by 64, which itself is a division by 4 of the MCLK rate.

- MCLK Frequency = 2.048 MHz
- Sampling Frequency = MCLK / 4 = 512 kHz
- –3 dB Filter Corner = Sampling Freq / 64 = 8 kHz
- RC filter = $1 / [2\pi \times (2 \times R_{series}) \times C_{diff}] \sim 8$ kHz

Figure 1 on page 6 illustrates the CS5374 amplifier-to-modulator analog connections with input anti-alias filter components. Filter components on the rough and fine pins should be identical values for optimum performance, with the capacitor values a minimum of 0.02 µF. The rough input can use either X7R or C0G-type capacitors, while the fine input requires C0G-type capacitors for optimal linearity. Using X7R-type capacitors on the fine analog inputs will significantly degrade total harmonic distortion performance.

4.2 Modulator Inputs — INR, INF

The modulator analog inputs are separated into differential rough and fine signals (INR±, INF±) to maximize sampling accuracy. The positive half of the differential input signal is connected to INR+ and INF+, while the negative half is attached to INF– and INR–. The INR± pins are switched-capacitor 'rough charge' inputs that pre-charge the internal analog sampling capacitor before it is connected to the INF± fine input pins.

4.2.1 Modulator Input Impedance

The modulator inputs have a dynamic switched-capacitor architecture and so have a rough charge input impedance that is inversely proportional to the input master clock frequency and the input capacitor size, [1 / (f · C)].

- MCLK = 2.048 MHz
- INR± Internal Input Capacitor = 20 pF
- Impedance = [1 / (2.048 MHz * 20 pF)] = 24 kΩ

Internal to the modulator, the rough inputs (INR±) pre-charge the sampling capacitor used by the fine inputs (INF±), therefore the input current to the fine inputs is typically very low and the effective input impedance is an order of magnitude above the impedance of the rough inputs.

4.2.2 Modulator Idle Tones — OFST

The modulators are delta-sigma-type and so can produce "idle tones" in the measurement bandwidth when the differential input signal is a steady-state DC signal near mid-scale. Idle tones result from low-frequency patterns in the output data stream and appear in the measurement spectrum as small tones about -135 dB down from full scale.

By default the $\overline{\text{OFST}}$ bit in the ADCCFG register is low and idle tones are eliminated within the modulator by adding –60 mV (channel 1) and –35 mV (channel 2) of internal differential offset during conversion to push idle tones out of the measurement bandwidth. Care should be taken to ensure external offset voltages do not negate the internally added differential offset, or idle tones will reappear.

4.3 Modulator Output — MDATA

The CS5374 modulators are designed to operate with the CS5376A digital filter. The digital filter generates the modulator clock and synchronization signals (MCLK and MSYNC) while receiving back the modulator one-bit ΔΣ conversion data and over-range flag (MDATA and MFLAG).

4.3.1 Modulator One's Density

During normal operation the CS5374 modulators output a ΔΣ serial bit stream to the MDATA pin, with a one's density proportional to the differential amplitude of the analog input signal. The output bit rate from the MDATA output is a divide-by-four of the input MCLK, and so is nominally 512 kHz.

The MDATA output has a 50% one's density for a mid-scale analog input, approximately 86% one's density for a positive full-scale analog input, and approximately 14% one's density for a negative full-scale analog input. One's density of the MDATA output is defined as the ratio of '1' bits to total bits in the serial bit stream output; i.e. an 86% one's density has, on average, a '1' value in 86 of every 100 output data bits.

4.3.2 Decimated 24-bit Output

When the CS5374 modulators operate with the CS5376A digital filter, the final decimated, 24-bit, full-scale output code range depends if digital offset correction is enabled. With digital offset correction enabled within the digital filter, amplifier

offset and the modulator internal offset are removed from the final conversion result.

Modulator Differential Analog Input Signal	CS5376A Digital Filter 24-Bit Output Code		
	Offset Corrected	CH1 –60 mV Offset	CH2 –35 mV Offset
> + (VREF+5%)	Error Flag Possible		
+ VREF	5D18CA	5ADCCE	5BCB22
0 V	000000	FDC404	FEB258
– VREF	A2E736	A0AB3A	A1998E
> – (VREF+5%)	Error Flag Possible		

Table 1. 24-bit Output Coding for the CS5374 Modulator and CS5376A Digital Filter Combination

4.4 Modulator Stability — MFLAG

The CS5374 ΔΣ modulators have a fourth-order architecture which is conditionally stable and may go into an oscillatory condition if the analog inputs are over-ranged more than 5% past either positive or negative full scale.

If an unstable condition is detected, the modulator collapses to a first-order system to regain stability and transitions the MFLAG output low-to-high to signal an error condition to the CS5376A digital filter. The MFLAG output connects to a dedicated input on the digital filter, causing an error flag to be set in the status byte of the next output data word.

The analog input signal must be reduced to within the full-scale range for at least 32 MCLK cycles for the modulator to recover from an oscillatory condition. If the analog input remains over-ranged for an extended period, the modulator will cycle between fourth-order and first- order operation and the MFLAG output will be seen to pulse.

4.5 Modulator Clock Input — MCLK

The CS5376A digital filter generates the master clock for the CS5374, typically 2.048 MHz, from a synchronous clock input from the external system. If MCLK is disabled during operation, the CS5374 will enter a power down state after approximately 40 µS. By default, MCLK is disabled at reset and is enabled by writing the digital filter CONFIG register.

MCLK must have low jitter to guarantee full analog performance, requiring a crystal- or VCXO-based system clock input to the digital filter. Clock jitter on the digital filter CLK input directly translates to jitter on MCLK.

4.6 Modulator Synchronization — MSYNC

The CS5374 modulators are designed to operate synchronously with other modulators in a distributed measurement network, so a rising edge on the MSYNC input resets the internal conversion state machine to synchronize analog sample timing. MSYNC is automatically generated by the CS5376A digital filter after receiving a synchronization signal from the external system, and is chip-to-chip accurate within ± 1 MCLK period. The input SYNC signal to the CS5376A digital filter sets a common reference time t_0 for measurement events, thereby synchronizing analog sampling across a measurement network. By default, MSYNC generation is disabled at reset and is enabled by writing the digital filter CONFIG register.

The CS5374 MSYNC input is rising-edge triggered and resets the internal MCLK counter/divider to guarantee synchronous operation with other system devices. While the MSYNC signal synchronizes the internal operation of the modulators, by default, it does not synchronize the phase of the sine wave from the CS4373A test DAC unless enabled in the digital filter TBSCFG register.

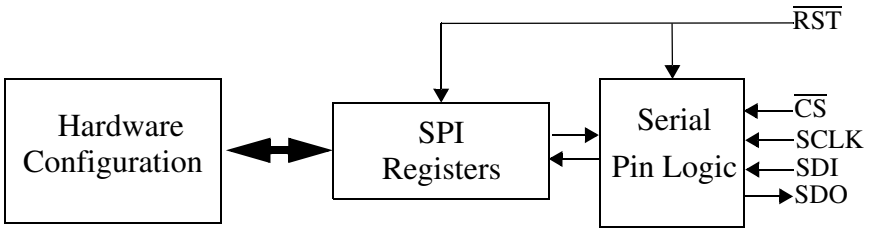


Figure 15. SPI Interface Block Diagram

5. SPI™ SERIAL PORT

The CS5374 SPI interface is a slave serial port designed to interface with the CS5376A SPI 2 port. SPI commands from the CS5376A write and read the CS5374 configuration registers to control hardware operation.

A block diagram of the CS5374 SPI serial interface is shown in Figure 15, and connections to the CS5376A SPI 2 port are shown in Figure 12 on page 15.

5.1 SPI Pin Descriptions

$\overline{\text{RST}}$ — Pin 37

Hardware reset input pin, active low. Defaults the configuration registers and SPI state machine.

$\overline{\text{CS}}$ — Pin 25

Chip select input pin, active low.

SCLK — Pin 26

Serial clock input pin. Maximum 4.096 MHz.

SDI — Pin 27

Serial data input pin. Data expected valid on rising edge of SCLK, transition on falling edge.

SDO — Pin 28

Serial data output pin. Data valid on rising edge of SCLK, transition on falling edge.

5.2 SPI Serial Transactions

Following reset, master mode serial transactions to CS5374 assert $\overline{\text{CS}}$ and write serial clocks to SCLK while writing serial data into SDI or reading serial data out from SDO.

The CS5374 serial port operates in SPI mode 0 (0,0) and reads or writes configuration registers using standard 8-bit SPI opcodes. Each individual serial transaction is 24-bits long and is generated by concatenating an 8-bit SPI command opcode, an 8-bit register address, and an 8-bit data byte as shown in Figure 16 on page 22.

The CS5374 SPI state machine requires 24 clocks with $\overline{\text{CS}}$ asserted to fully shift out the SPI data or else SPI clock synchronization can be lost. The CS5376A SPI 2 hardware generates 24 clocks per transaction and will keep the CS5374 serial port synchronized at all times. However, if another SPI master is used and clock synchronization is lost, two methods are available to recover:

1. Hold $\overline{\text{CS}}$ high (inactive) and apply 24 clocks to shift out any cached SPI data bits. This method retains the existing CS5374 register configuration.

... or ...

2. Apply a hardware reset (toggle $\overline{\text{RST}}$) and then rewrite all CS5374 register configuration values.

Instruction	Opcode	Address	Definition
Write	0x02	ADDR[7:0]	Write SPI register specified by the address in ADDR.
Read	0x03	ADDR[7:0]	Read SPI register specified by the address in ADDR.

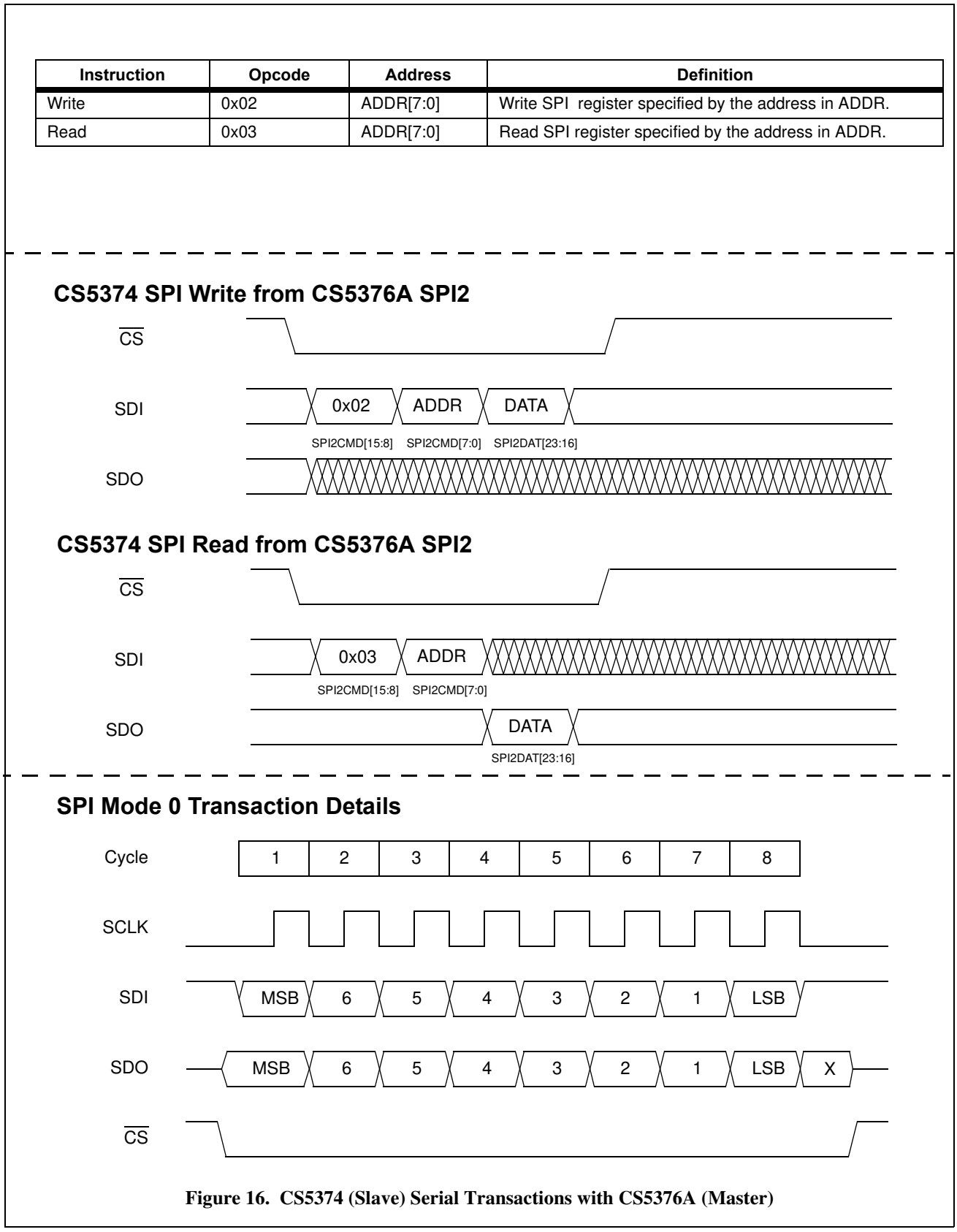


Figure 16. CS5374 (Slave) Serial Transactions with CS5376A (Master)

Name	Addr.	Type	# Bits	Description
VERSION	0x00	R	8	Device Version ID
AMP1CFG	0x01	R/W	8	Amplifier 1 configuration
AMP2CFG	0x02	R/W	8	Amplifier 2 configuration
ADCCFG	0x03	R/W	8	Modulator 1 & 2 configuration
PWRCFG	0x04	R/W	8	Power configuration

Table 2. SPI Configuration Registers

5.3 SPI Registers

The CS5374 SPI registers are 8-bit registers that control the CS5374 hardware configuration. See "SPI™ Register Summary" on page 34 for detailed bit definitions of the SPI registers listed in Table 2.

5.3.1 VERSION — 0x00

The VERSION register indicates the hardware revision of the CS5374 device. Read only.

- Reset Condition : 0100_0001 (0x41)
- Normal Operation : 0100_0001 (0x41)
- Power Down Operation : 0100_0001 (0x41)

5.3.2 AMP1CFG — 0x01

The AMP1CFG register controls the amplifier MUX and GAIN settings for channel 1. It also enables PWDN mode for the channel 1 amplifier plus enables the GUARD output for channels 1 & 2.

- Reset Condition : 0000_0000
- Normal Operation : 00MM_0GGG
- Power Down Operation : 1000_0000

5.3.3 AMP2CFG — 0x02

The AMP2CFG register controls the amplifier MUX and GAIN settings for channel 2. It also enables PWDN mode for the channel 2 amplifier.

- Reset Condition : 0000_0000
- Normal Operation : 00MM_0GGG
- Power Down Operation : 1000_0000

Input Selection	MUX1	MUX0
800 Ω termination	0	0
INA only	1	0
INB only	0	1
INA + INB	1	1

Gain Selection	GAIN2	GAIN1	GAIN0
1x	0	0	0
2x	0	0	1
4x	0	1	0
8x	0	1	1
16x	1	0	0
32x	1	0	1
64x	1	1	0
reserved	1	1	1

Table 3. Digital Selections for Gain and Input Mux Control

5.3.4 ADCCFG — 0x03

The ADCCFG register can disable modulator OFST and enable HP mode. It also enables PWDN mode for the channel 1 & 2 modulators.

- Reset Condition : 0000_0000
- Normal Operation : 0100_0000
- Power Down Operation : 0011_0000

5.3.5 PWRCFG — 0x04

The PWRCFG register can vary bias currents for the amplifier and modulator to minimize power consumption.

- Reset Condition : 0000_0000
- Normal Operation : 1000_1111
- Power Down Operation : 0000_0000

5.4 Example: CS5374 Configuration by an External SPI Master

Any SPI master that supports mode 0 (0,0) communication can write and read the configuration registers and control CS5374.

The following example SPI read and write transactions show how to configure the CS5374 for normal operation.

SPI Write Transactions

Transaction	CS5374 SPI Write	Description
01	SI: 02 | 01 | 20 SO: ----------	Write AMP1CFG register (0x01). CH1 INA enabled, 1x gain (0x20).
02	SI: 02 | 02 | 20 SO: ----------	Write AMP2CFG register (0x02). CH2 INA enabled, 1x gain (0x20).
03	SI: 02 | 03 | 40 SO: ----------	Write ADCCFG register (0x03). Normal operation (0x40).
04	SI: 02 | 04 | 8F SO: ----------	Write PWRCFG register (0x04). Normal operation (0x8F).

SPI Read Transactions

Transaction	CS5374 SPI Read	Description
01	SI: 03 | 00 | 00 SO: ---------- | 41	Read VERSION register (0x00). Returned data byte on the SO pin.
02	SI: 03 | 01 | 00 SO: ---------- | 20	Read AMP1CFG register (0x01). Returned data byte on the SO pin.
03	SI: 03 | 02 | 00 SO: ---------- | 20	Read AMP2CFG register (0x02). Returned data byte on the SO pin.
04	SI: 03 | 03 | 00 SO: ---------- | 40	Read ADCCFG register (0x03). Returned data byte on the SO pin.
05	SI: 03 | 04 | 00 SO: ---------- | 8F	Read PWRCFG register (0x04). Returned data byte on the SO pin.

Table 4. Example SPI Transactions to Write and Read the CS5374 Configuration Registers

5.5 Example: CS5374 Configuration by the CS5376A SPI 2 Port

The CS5374 SPI port was designed to connect to the CS5376A secondary SPI 2 port as shown in Figure 12 on page 15.

The CS5376A SPI 2 hardware is controlled by writing internal digital filter registers SPI2CTRL, SPI2CMD, and SPI2DAT through a primary SPI 1 port. Chip selects are enabled by writing the GPCFG0 digital filter register prior to initiating SPI 2 transactions.

Configuring CS5374 using SPI 2 is more complex than using an external SPI master, but has the advantage of a single standardized hardware interface (the primary SPI 1 port on CS5376A) to control the entire chipset.

5.5.1 CS5376A SPI 1 Transactions

The CS5376A primary SPI 1 port is controlled by an external SPI master writing commands and data into the SPI 1 registers (SPICMD, SPIDAT1, and SPIDAT2). Serial transactions into the CS5376A primary SPI 1 port start with an SPI opcode, followed by an SPI address, and then data bytes written starting at that SPI address. These data bytes contain internal commands to write the CS5376A digital filter registers that control the SPI 2 hardware and enable the chip selects.

A full description of how to write the CS5376A internal digital filter registers using the primary SPI 1 port is described in the CS5376A data sheet.

GPIO Register

Certain GPIO pins on the CS5376A have dual-use as chip selects for the SPI 2 port. The GPIO0:CS0 and GPIO1:CS1 pins are recommended as dedicated chip selects when connecting two CS5374 devices to the CS5376A SPI 2 port. To operate the CS0 and CS1 pins as SPI 2 chip selects they must be programmed as outputs in the GPCFG0 digital filter register, as shown in Table 5.

SPI2 Registers

Three digital filter registers control the CS5376A SPI 2 hardware. The SPI2CMD register is 16-bits wide and contains the first two bytes of the SPI 2 transaction, the SPI opcode and SPI address, in the lower two bytes (i.e. 0x000204).

Transaction	CS5376A Primary SPI 1 Write	Description
01	MOSI: 02 | 03 | 00 00 01 | 00 00 0E | 03 FF FF MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001 : Write Register SPIDAT1 : 0x00000E : GPCFG0 SPIDAT2 : 0x03FFFF : CS as Output
02	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
03	MOSI: 02 | 03 | 00 00 02 | 00 00 0E | 00 00 00 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000002: Read Register SPIDAT1 : 0x00000E : GPCFG0 SPIDAT2 : 0x000000 : Dummy
04	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
05	MOSI: 03 | 06 |----------| MISO: ----------| 03 FF FF |	SPI Command : 0x03 : Read SPI Address : 0x06 : SPIDAT1 SPIDAT1 : 0x03FFFF : GPCFG0

Table 5. Example CS5376A SPI 1 Transactions to Write and Read the GPCFG0 Register

The SPI2DAT register is 24-bits wide and can contain up to three bytes of data to follow the SPI opcode and address. For configuring the CS5374, however, only one data byte per register address is required and is written aligned with the upper byte (i.e. 0x8F0000).

The SPI2CTRL register is 24-bits wide and configures/controls the SPI 2 hardware, with bit assignments detailed in the CS5376A data sheet. If the GPIO:CS0 and GPIO1:CS1 pins are used as chip selects, separate SPI2CTRL values can initiate serial transactions to each device (i.e. 0x3F0161, 0x3F4162).

Tables 6, 7, and 8 show the CS5376A primary SPI 1 transactions required to write the SPI 2 digital filter registers and configure two CS5374 devices for normal operation using the CS0 and CS1 chip selects.

Transaction	CS5376A Primary SPI 1 Write	Description
01	MOSI: 02 | 03 | 00 00 01 | 00 00 11 | 00 02 01 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001 : Write Register SPIDAT1 : 0x000011 : SPI2CMD SPIDAT2 : 0x000201 : Write AMP1CFG
02	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
03	MOSI: 02 | 03 | 00 00 01 | 00 00 12 | 20 00 00 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000012 : SPI2DAT SPIDAT2 : 0x200000 : INA, x1 Gain
04	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
05	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 01 61 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F0161 : CS0 Transaction
06	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
07	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 41 62 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F4162 : CS1 Transaction

Table 6. Example CS5376A SPI 1 Transactions to Write the CS5374 AMP1CFG Register

Transaction	CS5376A Primary SPI 1 Write	Description
01	MOSI: 02 | 03 | 00 00 01 | 00 00 11 | 00 02 02 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001 : Write Register SPIDAT1 : 0x000011 : SPI2CMD SPIDAT2 : 0x000202 : Write AMP2CFG
02	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
03	MOSI: 02 | 03 | 00 00 01 | 00 00 12 | 20 00 00 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000012 : SPI2DAT SPIDAT2 : 0x200000 : INA, x1 Gain
04	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
05	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 01 61 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F0161 : CS0 Transaction
06	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
07	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 41 62 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F4162 : CS1 Transaction

Transaction	CS5376A Primary SPI 1 Write	Description
01	MOSI: 02 | 03 | 00 00 01 | 00 00 11 | 00 02 03 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001 : Write Register SPIDAT1 : 0x000011 : SPI2CMD SPIDAT2 : 0x000203 : Write ADCCFG
02	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
03	MOSI: 02 | 03 | 00 00 01 | 00 00 12 | 40 00 00 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000012 : SPI2DAT SPIDAT2 : 0x400000 : Normal Operation
04	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
05	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 01 61 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F0161 : CS0 Transaction
06	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
07	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 41 62 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F4162 : CS1 Transaction

Table 7. Example CS5376A SPI 1 Transactions to Write AMP2CFG and ADCCFG

Transaction	CS5376A Primary SPI 1 Write	Description
01	MOSI: 02 | 03 | 00 00 01 | 00 00 11 | 00 02 04 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001 : Write Register SPIDAT1 : 0x000011 : SPI2CMD SPIDAT2 : 0x000204 : Write PWRCFG
02	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
03	MOSI: 02 | 03 | 00 00 01 | 00 00 12 | 8F 00 00 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000012 : SPI2DAT SPIDAT2 : 0x8F0000 : Normal Operation
04	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
05	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 01 61 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F0161 : CS0 Transaction
06	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	See the CS5376A data sheet.
07	MOSI: 02 | 03 | 00 00 01 | 00 00 10 | 3F 41 62 MISO: ----------	SPI Command : 0x02 : Write SPI Address : 0x03 : SPICMD SPICMD : 0x000001: Write Register SPIDAT1 : 0x000010 : SPI2CTRL SPIDAT2 : 0x3F4162 : CS1 Transaction

Table 8. Example CS5376A SPI 1 Transactions to Write the CS5374 PWRCFG Register

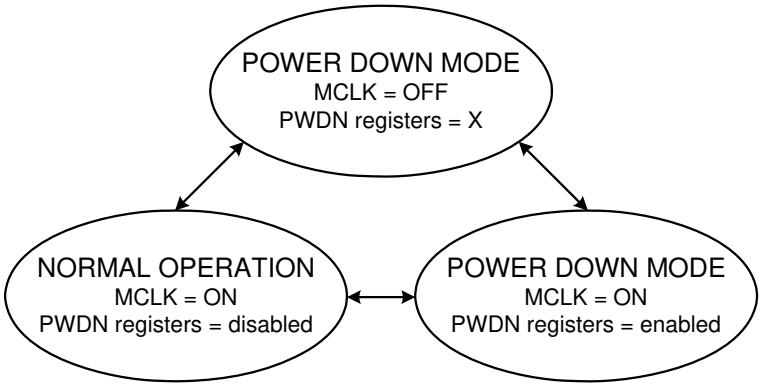


Figure 17. Power Mode Diagram

6. POWER MODES

The CS5374 amplifiers and modulators have three power modes. Normal operation, power down with MCLK enabled, and power down with MCLK disabled.

Power down mode is controlled by PWDN bits in the SPI registers, and are active high. When PWDN is enabled, internal circuitry is disabled, the analog inputs and outputs go high-impedance, and the device enters a micro-power state.

6.1 Normal Operation

With MCLK active and the amplifiers and modulators enabled (PWDN = 0) the CS5374 performs normal data acquisition. A differential analog input signal is converted to an oversampled 1-bit ΔΣ bit stream at 512 kHz. This ΔΣ bit stream is then digitally filtered and decimated by the CS5376A device to a high-precision 24-bit output.

6.2 Power Down, MCLK Enabled

With MCLK active and all amplifiers and modulators disabled (PWDN = 1) the CS5374 is placed into a power-down state. During this power-down state the amplifiers and modulators are disabled and all outputs are high impedance. In this mode power consumption is reduced, but not reduced as low as with MCLK inactive, as sections of the digital state machine are kept awake to support SPI communications. Any unused amplifier/modulator channels can be turned off individually through the configuration registers.

6.3 Power Down, MCLK Disabled

If MCLK is stopped, an internal loss-of-clock detection circuit automatically places the CS5374 into a power-down state. This power-down state is independent of the amplifier and modulator internal configuration registers, and is automatically invoked after approximately 40 µs without receiving an incoming MCLK edge.

During this power-down state, the amplifiers and modulators are disabled and all outputs are high impedance. The entire digital state machine goes inactive but configuration register values are retained, with a reset required to clear them. When used with the CS5376A digital filter, the CS5374 is in this lowest power-down state immediately after reset since MCLK is disabled by default.

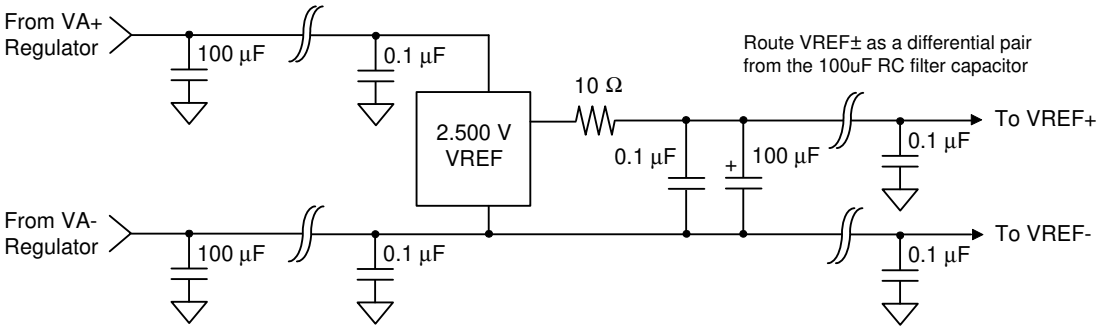


Figure 18. Voltage Reference Circuit

7. VOLTAGE REFERENCE

The CS5374 modulators require a 2.500 V precision voltage reference to be supplied to the VREF± pins.

7.1 VREF Power Supply

To guarantee proper regulation headroom for the voltage reference device, the voltage reference GND pin should be connected to VA– instead of system ground, as shown in Figure 18. This connection results in a VREF– voltage equal to VA– and a VREF+ voltage very near ground potential [(VA–) + 2.500 VREF].

Power supply inputs to the voltage reference device should be bypassed to system ground with 0.1 µF capacitors placed as close as possible to the power and ground pins. In addition to 0.1 µF local bypass capacitors, at least 100 µF of bulk capacitance to system ground should be placed on each power supply near the voltage regulator outputs. Bypass capacitors should be X7R, C0G, tantalum, or other high-quality dielectric type.

7.2 VREF RC Filter

A primary concern in selecting a precision voltage reference device is noise performance in the measurement bandwidth. The Linear Technology LT1019AIS8-2.5 voltage reference yields acceptable noise levels if the output is filtered with a low-pass RC filter.

A separate RC filter is required for each device connected to the voltage reference output. Signal-dependent sampling of the voltage reference by one system device could cause unwanted tones to appear in the measurement bandwidth of another system device if a single VREF RC filter is common to both.

7.3 VREF PCB Routing

To minimize the possibility of outside noise coupling into the CS5374 voltage reference input, the VREF± traces should be routed as a differential pair from the large capacitor of the voltage reference RC filter. Careful control of the voltage reference source and return currents by routing VREF± as a differential pair will significantly improve immunity from external noise.

To further improve noise rejection of the VREF± differential route, include 0.1 µF bypass capacitors to system ground as close as possible to the VREF+ and VREF– pins of the CS5374.

7.4 VREF Input Impedance

The switched-capacitor input architecture of the VREF± inputs results in an input impedance that depends on the internal capacitor size and the MCLK frequency. With a 15 pF internal capacitor and a 2.048 MHz MCLK, the VREF input impedance is approximately

1 / [(2.048 MHz) x (15 pF)] = 32 kΩ. While the size of the internal capacitor is fixed, the voltage reference input impedance can vary with MCLK.

The voltage reference external RC filter series resistor creates a voltage divider with the VREF input impedance to reduce the effective applied input voltage. To minimize gain error resulting from this voltage divider effect, the RC filter series resistor should be the minimum size recommended in the voltage reference device data sheet.

7.5 VREF Accuracy

The nominal voltage reference input is specified as 2.500 V across the VREF± pins, and all CS5374 gain accuracy specifications are measured using a nominal voltage reference input. Any variation from a nominal VREF input will proportionally vary the analog full-scale gain accuracy.

Since temperature drift of the voltage reference results in gain drift of the analog full-scale amplitude, care should be taken to minimize temperature drift effects through careful selection of passive components and the voltage reference device itself. Gain drift specifications of the CS5374 do not include the temperature drift effects of external passive components or of the voltage reference device itself.

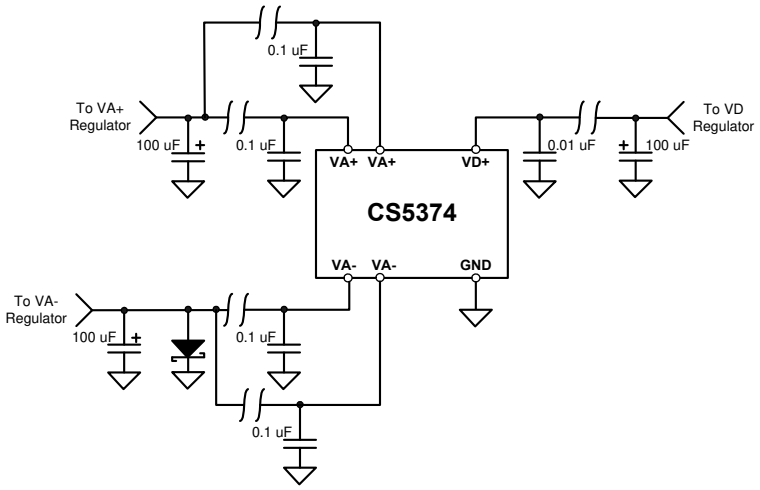


Figure 19. Power Supply Diagram

8. POWER SUPPLIES

The CS5374 has two positive analog power supply pins (VA+), two negative analog power supply pins (VA–), a digital power supply pin (VD+), and a ground pin (GND).

For proper operation, power must be supplied to all power supply pins, and the ground pin must be connected to system ground. The CS5374 digital power supply (VD+) and the CS5376A digital power supply (VD) must share a common voltage.

8.1 Analog Power Supplies

The analog power pins of the CS5374 are to be supplied with a total of 5 V between VA+ and VA– from a bipolar ±2.5 V supply. When using bipolar supplies the analog signal common mode voltage should be biased to 0 V. The analog power supplies are recommended to be bypassed to system ground using 0.1 µF X7R type capacitors.

The VA– supply is connected to the CMOS substrate and as such must remain the most negative applied voltage to prevent potential latch-up conditions. It is recommended to clamp the VA– supply to system ground using a reverse biased Schottky diode to prevent possible latch-up conditions related to mismatched supply rail initialization.

Care should be taken to connect the CS5374 thermal pad on the bottom of the package to VA–, not system ground (GND), since it internally connects to VA– and is expected to be the most negative applied voltage.

8.2 Digital Power Supply

The digital power supply across the VD and GND pins is specified for a +3.3 V power supply. The digital power supply should be bypassed to system ground using a 0.01 µF X7R type capacitor. The digital power supply across the VD+ and GND pins is specified to be +3.3 V.

8.3 Power Supply Bypassing

The VA+ and VA– power supplies should be bypassed to system ground with 0.1 µF capacitors placed as close as possible to the power pins of the device. The VD+ power supply should be bypassed to system ground with 0.1 µF capacitors placed as close as possible to the power pins of the device. Bypass capacitors should be X7R, C0G, tantalum, or other high-quality dielectric type.

In addition to the local bypass capacitors, at least 100 µF bulk capacitance to system ground should be placed on each power supply near the voltage

regulator output, with additional power supply bulk capacitance placed among the analog component route if space permits.

8.4 PCB Layers and Routing

The CS5374 is a high-performance device, and special care must be taken to ensure power and ground routing is correct. Power can be supplied either through dedicated power planes or routed traces. When routing power traces, it is recommended to use a "star" routing scheme with the star point either at the voltage regulator output or at a local power supply bulk capacitor.

It is also recommended to dedicate a full PCB layer to a solid ground plane, without splits or routing. All bypass capacitors should connect between the power supply circuit and the solid ground plane as near as possible to the device power supply pins.

The CS5374 analog signals are differentially routed and do not normally require connection to a separate analog ground. However, if a separate analog ground is required, it should be routed using a "star" routing scheme on a separate layer from the solid ground plane and connected to the ground plane only at a single point. Be sure all active devices and passive components connected to the separate analog ground are included in the "star" route to ensure sensitive analog currents do not return through the ground plane.

8.5 Power Supply Rejection

Power supply rejection of the CS5374 is frequency dependent. The CS5376A digital filter fully rejects power supply noise for frequencies above the selected digital filter corner frequency. Power supply noise frequencies between DC and the digital filter corner frequency are rejected as specified in the "Power Supply Characteristics" on page 13.

8.6 SCR Latch-up Considerations

It is recommended to connect the VA– power supply to system ground (GND) through a reverse-biased Schottky diode. At power up, if the VA+ power supply ramps up before the VA– supply is established, the VA- pin voltage could be pulled above ground potential through the CS5374 device. If the VA– supply is pulled 0.7 V or more above GND, SCR latch-up can occur. A reverse-biased Schottky diode will clamp the VA– voltage a maximum of 0.3 V above ground to ensure SCR latch-up does not occur at power up.

For similar reasons, care should be taken to connect the CS5374 thermal pad on the bottom of the package to VA–, not system ground (GND), since it internally connects to VA– and is expected to be the most negative applied voltage.

8.7 DC-DC Converters

Many low-frequency measurement systems are battery powered and utilize DC-DC converters to efficiently generate power supply voltages. To minimize interference effects, operate the DC-DC converter at a frequency which is rejected by the digital filter, or operate it synchronous to the MCLK rate.

A synchronous DC-DC converter whose operating frequency is derived from MCLK will theoretically minimize the potential for "beat frequencies" to appear in the measurement bandwidth. However this requires the source clock to remain jitter free within the DC-DC converter circuitry. If clock jitter can occur within the DC-DC converter (as in a PLL-based architecture), it's better to use a non-synchronous DC-DC converter whose switching frequency is rejected by the digital filter.

During PCB layout, do not place high-current DC-DC converters near sensitive analog components. Carefully routing a separate DC-DC "star" ground will help isolate noisy switching currents away from the sensitive analog components.

9. SPI™ REGISTER SUMMARY

The CS5374 Configuration Registers contain the hardware configuration settings.

Name	Addr.	Type	# Bits	Description
VERSION	0x00	R	8	Device Version ID
AMP1CFG	0x01	R/W	8	Amplifier 1 configuration
AMP2CFG	0x02	R/W	8	Amplifier 2 configuration
ADCCFG	0x03	R/W	8	Modulator 1 & 2 configuration
PWRCFG	0x04	R/W	8	Power configuration

9.1 VERSION: 0x00

Figure 20. Hardware Version ID Register VERSION

(MSB)7	6	5	4	3	2	1	(LSB)0
VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0
R	R	R	R	R	R	R	R
0	1	0	0	0	0	0	1

Address: 0x00

-- Not defined (read as 0)
R Readable
W Writable
R/W Readable and Writable

Bits in bottom rows are reset condition

Reset Condition : 0100_0001 (0x41) : Default value

Normal Operation : 0100_0001 (0x41) : Default value

Power Down Operation : 0100_0001 (0x41) : Default value

Bit definitions:

7:0	VERS	Hardware revision ID register 0x41: Revision A

9.2 AMP1CFG: 0x01

Figure 21. Amplifier 1 Configuration Register AMP1CFG

(MSB)7	6	5	4	3	2	1	(LSB)0
PWDN1	HP1	MUX1_1	MUX1_0	GUARD	GAIN1_2	GAIN1_1	GAIN1_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Address: 0x01

-- Not defined (read as 0)
R Readable
W Writable
R/W Readable and Writable

Bits in bottom rows are reset condition

Reset Condition : 0000_0000 (0x00) : Default value

Normal Operation : 00MM_GGGG : MUX, GUARD and GAIN select

Power Down Operation : 1000_0000 (0x80) : PWDN enabled

Bit definitions:

7 PWDN1 Amplifier 1 Power Down
1: enable
0: disable

6 HP1 Amplifier 1 High Precision
1: enable
0: disable

5:4 MUX1[1:0] Input Multiplexer
11: INA1 + INB1
10: INA1 only
01: INB1 only
00: 800 ohm termination

3 GUARD GUARD Output
1: disable
0: enable

2:0 GAIN1[2:0] Amplifier 1 Gain
111: reserved
110: 64x
101: 32x
100: 16x
011: 8x
010: 4x
001: 2x
000: 1x

9.3 AMP2CFG: 0x02

Figure 22. Amplifier 2 Configuration Register AMP2CFG

(MSB)7	6	5	4	3	2	1	(LSB)0
PWDN2	HP2	MUX2_1	MUX2_0	---	GAIN2_2	GAIN2_1	GAIN2_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Address: 0x02

-- Not defined (read as 0)
R Readable
W Writable
R/W Readable and Writable

Bits in bottom rows are reset condition

Reset Condition : 0000_0000 (0x00) : Default value

Normal Operation : 00MM_0GGG : MUX and GAIN select

Power Down Operation : 1000_0000 (0x80) : PWDN enabled

Bit definitions:

7 PWDN2 Amplifier 2 Power Down
1: enable
0: disable

6 HP2 Amplifier 2 High Precision
1: enable
0: disable

5:4 MUX2[1:0] Input Multiplexer
11: INA2 + INB2
10: INA2 only
01: INB2 only
00: 800 ohm termination

3 --- Reserved

2:0 GAIN2[2:0] Amplifier 2 Gain
111: reserved
110: 64x
101: 32x
100: 16x
011: 8x
010: 4x
001: 2x
000: 1x

9.4 ADCCFG: 0x03

Figure 23. Modulator 1 & 2 Configuration Register ADCCFG

(MSB)7	6	5	4	3	2	1	(LSB)0
$\overline{\text{OFST}}$	HP	PWDN2	PWDN1	---	---	---	---
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Address: 0x03

-- Not defined (read as 0)
R Readable
W Writable
R/W Readable and Writable

Bits in bottom rows are reset condition

Reset Condition : 0000_0000 (0x00) : Default value

Normal Operation : 0100_0000 (0x40) : HP mode enabled

Power Down Operation : 0011_0000 (0x30) : PWDN enabled

Bit definitions:

7	$\overline{\text{OFST}}$	Modulator Offset (add -60mV to Channel 1, add -35mV to Channel 2) 1: disable 0: enable
6	HP	Modulator High Precision 1: enable 0: disable
5	PWDN2	Modulator 2 Power Down 1: enable 0: disable
4	PWDN1	Modulator 1 Power Down 1: enable 0: disable
3:0	---	Reserved

9.5 PWRCFG: 0x04

Figure 24. Power Configuration Register PWRCFG

(MSB)7	6	5	4	3	2	1	(LSB)0
adc_lpwr	---	amp_i1_1	amp_i1_0	rough	i1_tail	amp_i5_1	amp_i5_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Address: 0x04

--- Not defined (read as 0)
R Readable
W Writable
R/W Readable and Writable

Bits in bottom rows are reset condition.

Reset Condition : 0000_0000 (0x00) : Default value

Normal Operation : 1000_1111 (0x8F) : Reduced power

Power Down Operation : 0000_0000 (0x00) : Default value

Bit definitions:

7 adc_lpwr Modulator Bias
1: reduced current
0: nominal current

6 --- reserved

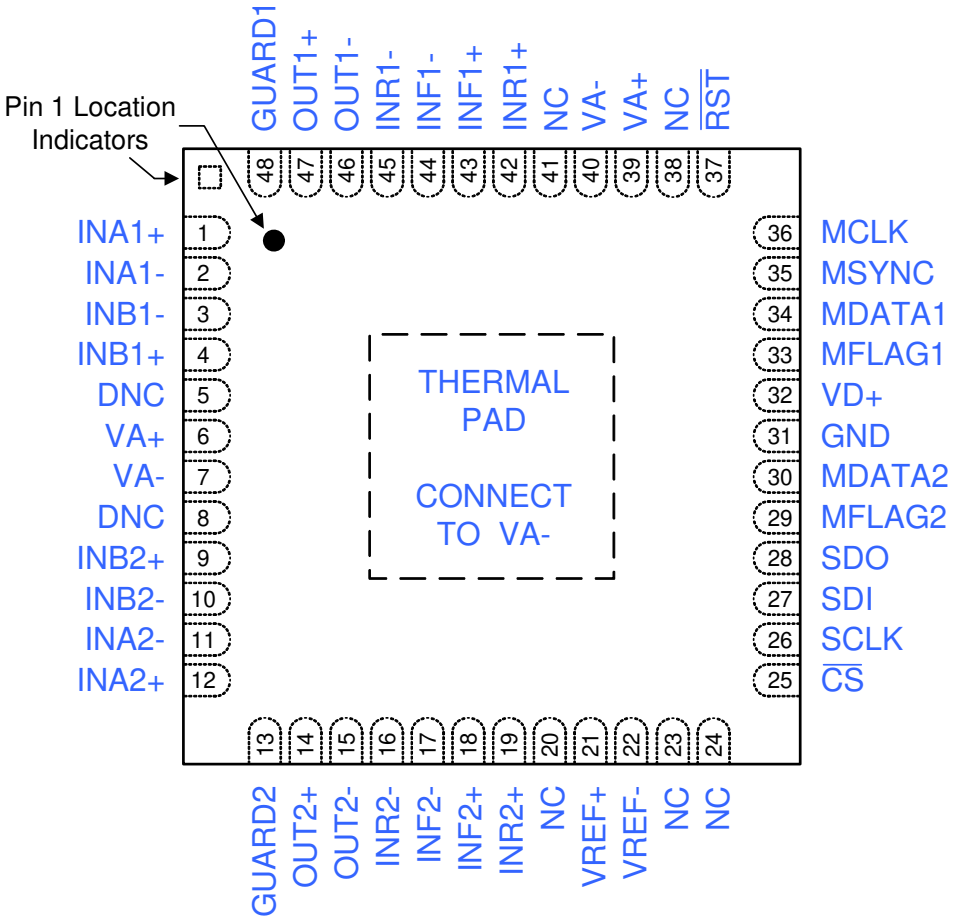
5:4 amp_i1 Amplifier i1 Bias
11: 2/3
10: 1/3
01: 4/3
00: nominal current

3 rough Modulator Rough Phase
1: reduced current
0: nominal current

2 i1_tail Amplifier i1 Tail Current
1: reduced current
0: nominal current

1:0 amp_i5 Amplifier i5 Bias
11: 7/11
10: 9/13
01: 15/13
00: nominal current

10. PIN DESCRIPTIONS



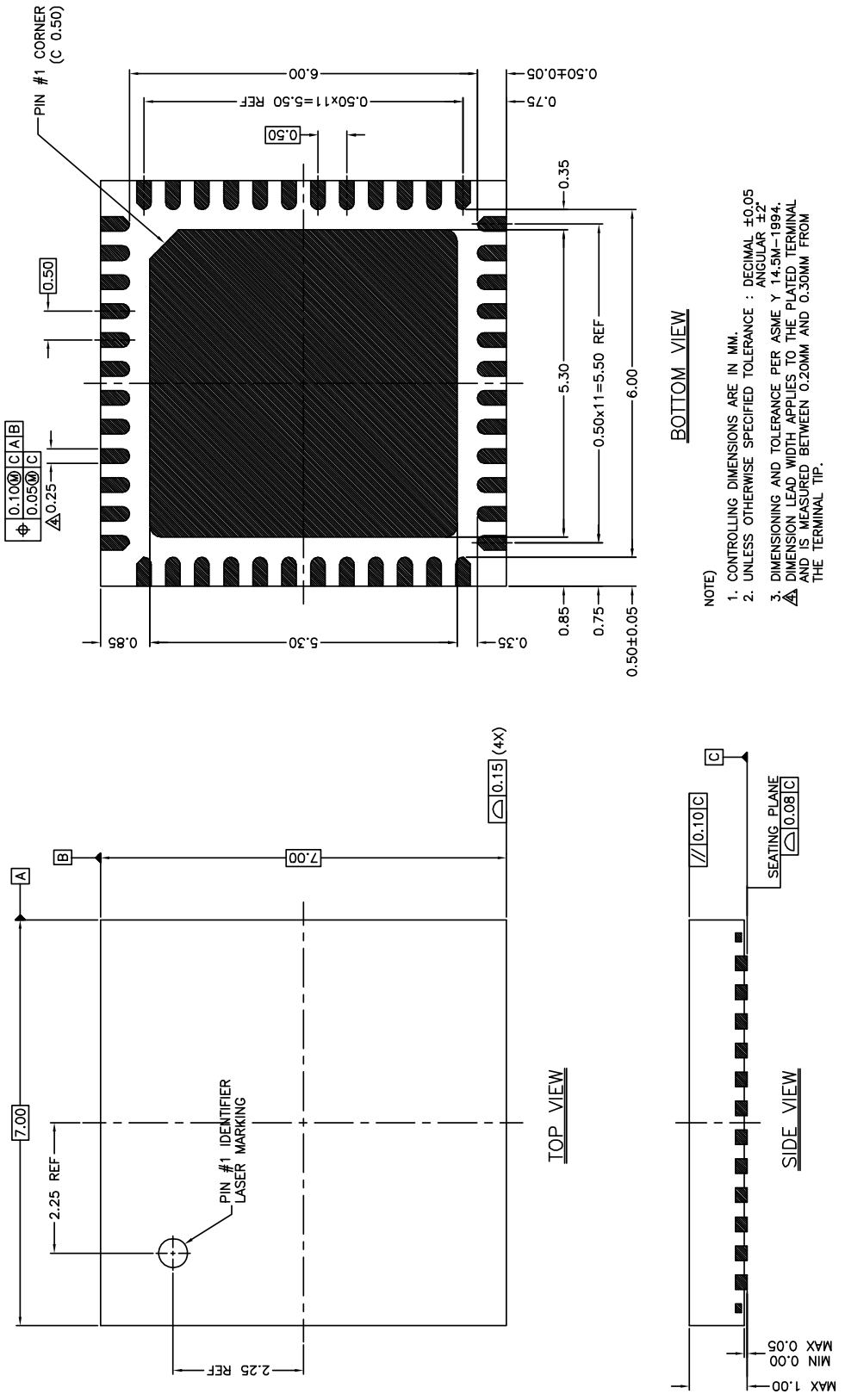
Top-Down
(Though Package)
View

Pin Name	Pin Number	Pin Type	Pin Description
Power Supplies			
VA+ VA–	6, 39 7, 40	I	Analog power supply. Refer to the Specified Operating Conditions.
VD+, GND	32, 31	I	Digital power supply. Refer to the Specified Operating Conditions.
Differential Amplifier Analog Inputs			
INA1+ INA1–	1 2	I	Channel 1 differential analog input A. Selected via Serial Communications Interface.
INB1–, INB1+	3 4	I	Channel 1 differential analog input B. Selected via Serial Communications Interface.
INB2+, INB2–	9 10	I	Channel 2 differential analog input B. Selected via Serial Communications Interface.
INA2–, INA2+	11 12	I	Channel 2 differential analog input A. Selected via Serial Communications Interface.

Differential Amplifier Analog Outputs			
OUT1–, OUT1+	46 47	O	Channel 1 differential analog output.
GUARD1	48	O	Guard output voltage for analog input Channel 1.
GUARD2	13	O	Guard output voltage for analog input Channel 2.
OUT2+, OUT2–	14 15	O	Channel 2 differential analog output.
Modulator Analog Inputs			
INR1+, INF1+, INF1–, INR1–	42 43 44 45	I	Channel 1 analog differential rough and fine inputs. From the Channel 1 differential anti-alias filter.
INR2–, INF2–, INF2+, INR2+	16 17 18 19	I	Channel 2 analog differential rough and fine inputs. From the Channel 2 differential anti-alias filter.
Voltage Reference			
VREF+, VREF–	21 22	I	Voltage reference input. Refer to the Specified Operating Conditions.
Serial Interface			
$\overline{CS}$	25	I	Chip select. Active low.
SCLK	26	I	Serial clock.
SDI	27	I	Serial data in to device.
SDO	28	O	Serial data out of device.
Modulator Interface			
MCLK	36	I	Modulator clock input.
MSYNC	35	I	Modulator sync input.
MFLAG1	33	O	Channel 1 modulator flag output.
MDATA1	34	O	Channel 1 modulator data output.
MFLAG2	29	O	Channel 2 modulator flag output.
MDATA2	30	O	Channel 2 modulator data output.
Device Reset			
$\overline{RST}$	37	I	Reset. Active low.
Other			
NC	20, 23, 24, 38, 41	---	No connect.
DNC	5, 8	---	Do Not Connect.
Thermal Pad	49	I	Connect to VA–. Do not connect to GND.

11. PACKAGE DIMENSIONS

48-PIN QFN (7MM X 7MM)



12. ORDERING INFORMATION

Model Number	Temperature	Package
CS5374-CNZ, lead (Pb) free	-10 to +70 °C	48-Pin QFN

13. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5374-CNZ, lead (Pb) free	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

14. REVISION HISTORY

Revision	Date	Changes
T1	AUG 2008	Initial release of Target data sheet.
A1	DEC 2008	Initial release of Advanced data sheet.
A2	JAN 2009	Update to include more complete characterization data.
PP1	APR 2009	Specify operation for 2.048 MHz MCLK and HP mode. Add PWRCFG register. Update to include more complete characterization data.
F1	OCT 2009	Update to include final characterization data.
F2	SEP 2010	Corrected VERSION register default value to 0100 0001 (0x41) — CS5374, Rev A.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**