Ordering number : ENA1159

LV5050NV

Bi-CMOS IC

DC / DC Converter Controller

ON Semiconductor®

http://onsemi.com

Overview

The LV5050NV is a high efficiency DC/DC converter controller IC adopting a synchronous rectifying system. Incorporating numerous functions on a single chip with easy external setting, it can be used for a wide variety of applications. This device is optimal for use in internal power supply systems which are used in electronic devices, LCD-TVs, DVD recorders, etc.

Functions

- Step-down DC/DC converter controller with 1-channel
- Input UVLO circuit,
- Built-in over current detection function
- Built-in soft-start/soft-stop function
- Built-in start-up delay circuit
- Built-in output voltage monitor function (Under voltage protection with power good and timer latch)
- Synchronized operation is possible between different devices.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Supply voltage		V_{IN}		18	V
Allowable power dissipation		Pd max	Mounted on a specified board *1	800	mW
Junction temperature		Tj		150	°C
Operating temperature		Topr		-20 to 85	°C
Storage temperature		Tstg		-55 to +150	°C
Allowable terminal voltage *2					
1	HDRV,CBOOT			28	V
2	Between HDRV, CBOOT and SW			6.5	V
3	V_{IN}, ILIM, RSNS, SW, PGOOD			18	V
4	VLIN5, V_{DD}, LDRV			6.5	V
5	COMP, FB, SS, UV_DELAY TD, CT, CLKO			VLIN5+0.3	V

*1: Specified board: 114.3mm × 76.1mm ×1.6 mm, glass epoxy board.

*2: The Allowable Terminal Voltage, the SGND+PGND pin becomes a standard except for No.2 of the allowable terminal voltage about No.2 of the allowable terminal voltage, the SW pin becomes a standard.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Condition at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{IN}	V_{IN} and VLIN5 pins opens	7.5 to 16	V
Supply voltage	V_{IN}	V_{IN} and VLIN5 pins shorted	4.5 to 6.0	V

Electrical Characteristics at Ta = 25°C, V_{IN}=12V, Unless especially specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
System						
Reference voltage for comparing	V_{REF}		0.818	0.826	0.834	V
Supply current 1	$I_{CC}1$	TD = 5V (Except for the Ciss charge)		2	4	mA
Supply current 2	$I_{CC}2$	TD = 0V	0.3	0.6	1.2	mA
5V supply voltage	VLIN5	$I_{VIN}5$ = 0 to 10mA	4.75	5.00	5.25	V
Over-current sense comparator offset	$V_{CL}OS$		-5		+5	mV
Over-current sense reference current source	I_{CL}	V_{IN} = 10 to 14V	7.47	8.30	9.13	µA
Leading edge pulse blank time	TLEPB			120	150	
Soft start source current	$I_{SS}SC$	TD = 5V	-2.0	-3.5	-5.0	µA
Soft start sink current	$I_{SS}SK$	TD = 0V	0.5	2.0		mA
Soft start clamp voltage	$V_{SS}T0$	When the voltage of the SS pin operating	1.2	1.6	2.0	V
UV_DELAY source current	$I_{SC}UVD$	UV_DELAY = 2V	-6.1	-8.6	-12.0	µA
UV_DELAY sink current	$I_{SK}UVD$	UV_DELAY = 2V	0.5	2		mA
UV_DELAY threshold voltage	VUVD		1.9	2.4	3.0	V
UV_DELAY operating voltage	VUVP	100% at V_{FB} = V_{REF}	87	92	97	%
VUVP detection hysteresis	ΔVUVP			1.5		%
Output discharge transistor ON resistance	$V_{SW}ON$		5	10	20	Ω
Output part						
CBOOT leakage current	ICBOOT	V_{CBOOT} = VSW + 6.5V			10	µA
HDRV LDRV source current	$I_{SC}DRV$		0.5	1.0		A
HDRV LDRV sink current	$I_{SK}DRV$		0.5	1.0		A
HDRV lower ON resistance	R_HDRV	I_{OUT} = 500mA	0.5	1.5	3.0	Ω
LDRV lower ON resistance	R_LDRV	I_{OUT} = 500mA	0.5	1.5	3.0	Ω
Synchronous ON prevention dead time 1	$T_{dead}1$	LDRV OFF→HDRV ON	50	70	120	ns
Synchronous ON prevention dead time 2	$T_{dead}2$	HDRV OFF→LDRV ON	70	120	280	ns
Oscillator						
Oscillation freaquency	f_{osc}	CT = 130pF	280	330	380	kHz
Oscillation frequency range	f_{osc}op		250		1100	kHz
Maximum ON duty	D_{ON} max	CT = 130pF	83	90	79	%
Minimum ON time	T_{ON} min	CT = 130pF		100		ns
Upper-side voltage saw- tooth wave	$V_{saw}H$	f_{OSC} = 300kHz	1.5	2	2.6	V
Lower-side voltage saw-tooth wave	$V_{saw}L$	f_{OSC} = 300kHz	0.8	1	1.2	V

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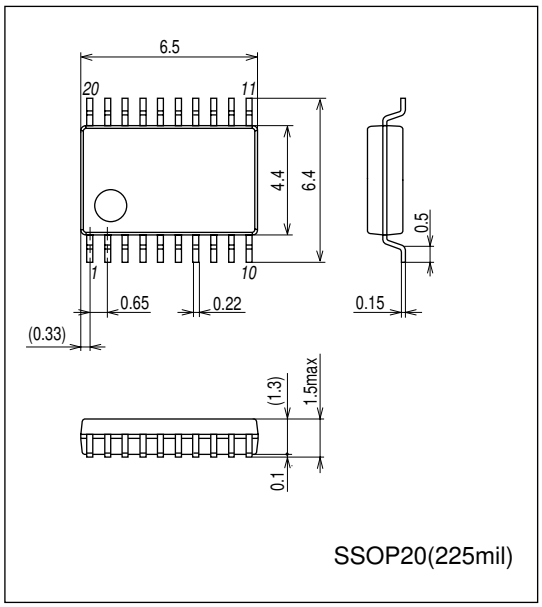
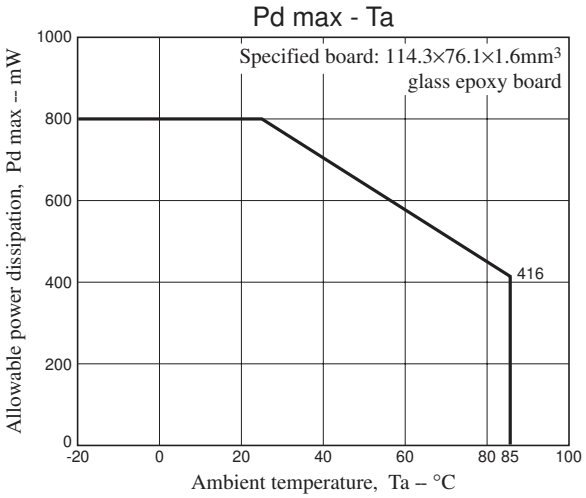
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Error Amplifier						
Error amplifier input current	I_{FB}		-190	-100	-50	nA
COMP pin source current	$I_{COMP}SC$		-150	-100	-50	µA
COMP pin sink current	$I_{COMP}SK$		18	100	150	µA
Error amplifier gm	gm		500	700	900	umho
Logic output						
Power Good low level source current	$I_{pwrgd}L$	V_{PGOOD} = 0.4V	0.5	1.0		mA
Power Good high level leakage current	$I_{pwrgd}H$	V_{PGOOD} = 12V			10	µA
Power Good operation voltage	Vpwrgd	100% at $V_{FB} = V_{REF}$	87	92	97	%
TP pin threshold voltage	$V_{ON}TD$	When the voltage of the TD pin rises	1.5	2.4	3.5	V
TP pin high impedance voltage	$V_{TD}H$	When V_{IN} and VLIN5 pins are set to open	4.5	5.0	5.5	V
TD pin charge source current	$I_{TD}SC$		-2.0	-3.5	-5.0	µA
TD pin discharge sink current	$I_{TD}SK$		0.2	1.0		mA
CLKO high level voltage	$V_{CLKO}H$	I_{CLKO} = 1mA	0.7V5LIN			V
CLKO low level voltage	$V_{CLKO}L$	I_{CLKO} = 1mA			0.3V5LIN	V
Protection function						
V_{IN} UVLO release voltage	V_{UVLO}		3.5	4.1	4.3	mA
UVLO Hysteresis	ΔV_{UVLO}			0.4		µA
UVLO released input voltage	$V_{IN}VUVLO$		4.8	5.5	6.3	V

Package Dimensions

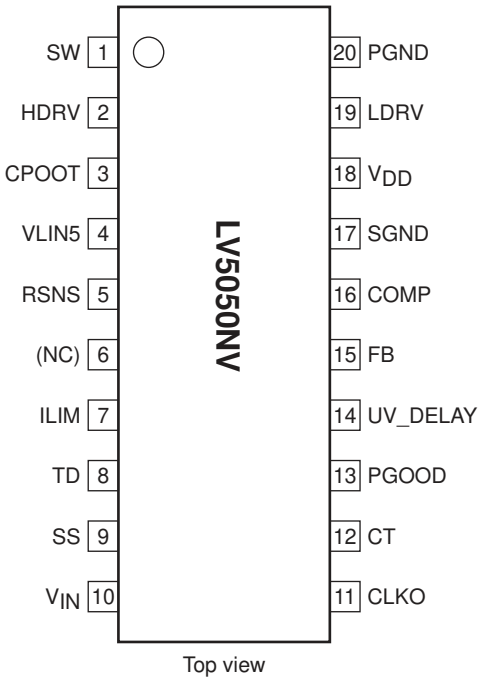
unit : mm (typ)

3179C



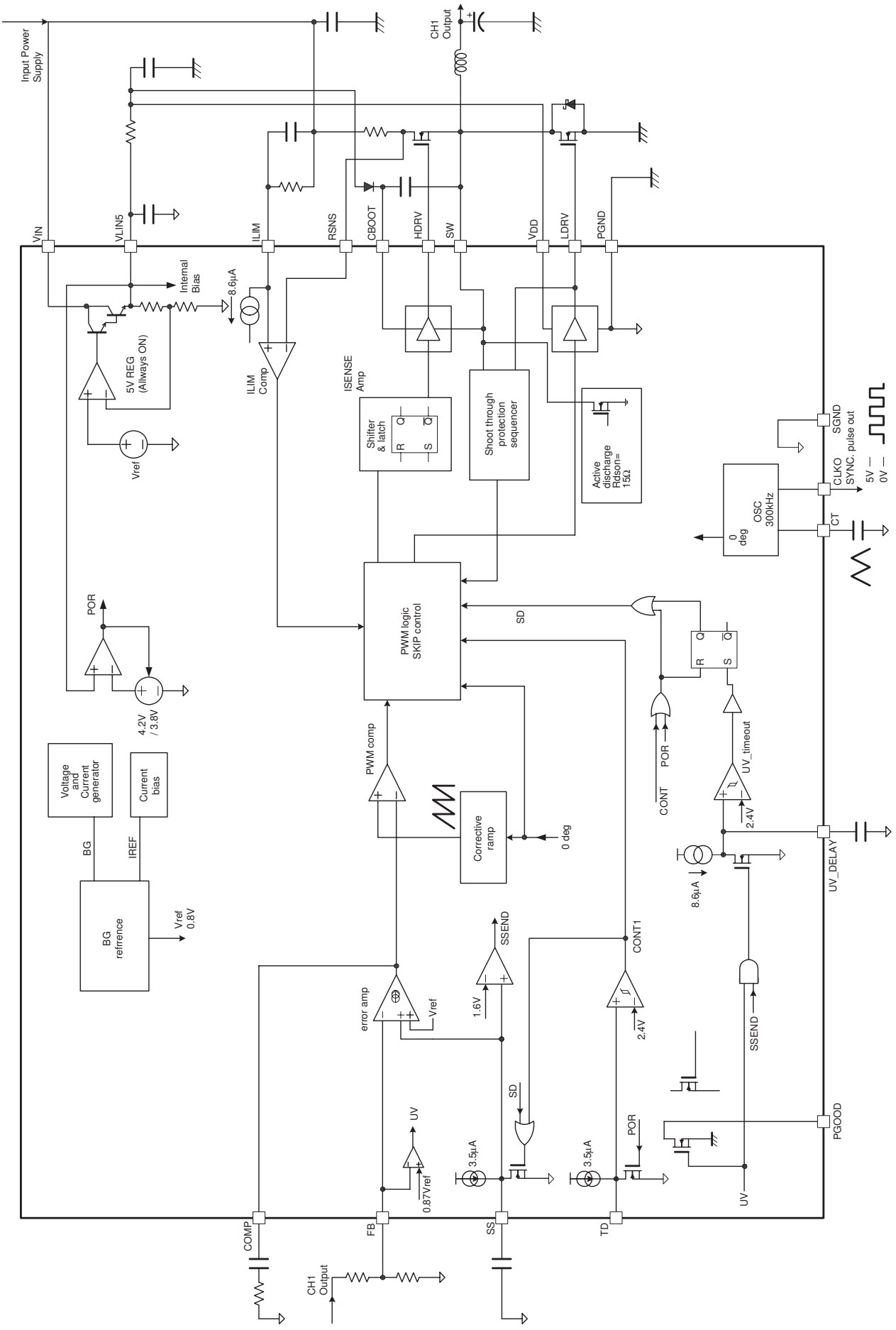


Pin Assignment



Top view

Block Diagram



Pin Functions

Pin No.	Pin name	Description
1	SW	This Pin is connected with the switching node. A source of an external upper side MOS-FET and a drain of an external lower side MOS-FET are connected with this pin. This pin becomes the return current path of the HDRV pin. This pin is connected with a transistor drain of the discharge MOS-FET for SOFT STOP in the IC (typical 15Ω). Also, this pin has the signal output part for the short through prevention of both the upper and lower MOS-FETs. When this terminal voltage becomes 1V or less for PGND, the LDRV pin is turned on.
2	HDRV	The gate drive pin for an external upper side MOS-FET.
3	CBOOT	The bootstrap capacity connection pin. The gate drive power of upper MOS-FET is provided by this pin. This pin is connected to the V_{DD} pin through a diode and is connected to the SW pin through the bootstrap capacity.
4	VLIN5	The output pin of an internal regulator of 5V. the current is provided by the VIN pin. Also, power supply of the control circuit in the IC is provided by this pin. Connect an output capacitor of 4.7μF between this pin and SGND. A regulator of 5V operates, even if the IC is in the standby state. This pin is monitored by an UVLO function and the IC starts by the voltage of 4.0V or more (the IC is off by the voltage of 3.8V or less.)
5	RSNS	The input pin of the over current detection comparator / the current detection amplifier To detect resistance, this pin is connected to the under side of a resistor for the current detection between the V_{IN} pin and the DRAIN of the upper MOS-FET. Also, to use the ON resistance of MOS-FET for the current detection, connect this pin to the SOURCE of the upper MOS-FET. To prevent the common impedance of main current to the detection-voltage, this pin is connected by independent wiring.
6	NC	No connection.
7	ILIM	The pin to set the trip point for over current detection. Since the SINK current source of 8.3μA (ILIM) is connected in the IC, the over-current detection voltage (ILIM × RLIM) is generated by connecting a resistor RLIM between this pin and the V_{IN} pin. The over-current is detected by comparing the voltage between the V_{IN} pin and the ILIM pin to the current detection resistance RSNS or both end voltage of the upper MOS-FET.
8	TD	Start-up delay pin. The time until the IC starts after releasing POR is set by connecting a capacitor between this pin and SGND. After releasing POR, an external capacitor is charged up by the constant current source of 3.5μA in the IC. When this terminal voltage becomes 2.4V or more, The IC starts. Also, when this terminal voltage becomes 2.4V or less, The IC becomes the standby state. If external capacitor is not connected, the IC instantly starts after releasing POR.
9	SS	The pin to connect a capacitor for soft start. After releasing POR, when the voltage of the TD pin becomes 2.4V or more, the SS pin is charged by an internal constant current source of 3.5μA. Since this pin is connected to the positive input of the transformer conductance amplifier, the ramp-up wave form of the SS pin becomes the ramp-up wave form of the output. During POR operations and after the UV_DELAY time-out, the SS pin is discharged
10	VIN	Power supply pin of the IC
11	CLKO	The clock output pin. The clock that synchronized to the oscillation waveform of the CT pin is output. To synchronize two or more LV5050NVs, the CLKO pin of the device that becomes a master is connected to the CT pin of the device that becomes a slave. When two or more the devices are synchronized and the start-up timing is changed by using the Td pin between each device, the earliest start-up device is determined as the master.
12	CT	The pin to connect an external capacitor for the oscillator. Connect a capacitor between this pin and SGND. When a capacitor of 130pF is connected between this pin and GND, the oscillation frequency can be set up by 330kHz. Also, this pin is applied by an external clock signal. The PWM operation is performed by the frequency of applied clock signal. When an external clock signal is applied, the rectangular wave of 0V in low level and from 3.3V to 5V in high level is applied. The rectangular wave source needs the fan-out of 1mA or more.
13	PGOOD	The power good pin. The open drain MOS-FET of the withstand of 28V is connected in the IC. When the output voltage of channel 1 is less than -13% for the setup voltage, the low level is output. This pin has hysteresis of about (V_{REF} × 1.5%).

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Pin No.	Pin name	Description
14	UV_DELAY	UVP DELAY pin By connecting a capacitor between this pin and SGND, the time until the IC latches off after detecting the UVP state can be set. Also, after channel 1 terminated the soft-start function, when the output voltage becomes -80% or less for the setup voltage, an external capacitor is charged by the constant current source of 8.6μA in the IC. When this terminal voltage becomes 2.4V or more, the IC is latched off. If an external capacitor is not connected, the IC is instantly latched off after detecting the UVP state. Also, when this pin is shorted to GND, the UV_DELAY function is not operated.
15	FB	Feed back input pin. The minus terminal (-) of the trans conductance amplifier is connected. The voltage generated when the output voltage was divided by a resistor is input into this pin. The converter operates so that this pin becomes an internal reference voltage (V_{REF}=0.836V). Also, this pin is monitored by the comparators UVP and OVP. When the voltage of this pin becomes less than 87% of the set voltage, the PGOOD pin is low level. A timer of the UV_DELAY function operates. Also, when the voltage of this pin becomes more than 117% of the set voltage, the IC latches off.
16	COMP	The pin to connect a capacitor and a resistor for phase compensation. The output of an internal transformer conductance amplifier is connected. Connect an external phase compensation circuit between this pin and SGND.
17	SGND	The system ground of the IC. The reference voltage is generated based on this pin. This pin is connected to the power supply system ground.
18	V_{DD}	Power supply pin for the gate drive of an external lower-side MOS-FET. This pin is connected to the VLIN5 pin through a filter.
19	LDRV	The gate drive pin of an external lower-side MOS-FET. This pin has the signal input part for prevention of short-through of both the upper and lower MOS-FETs. When the voltage of this pin becomes less than 1V, the HDRV pin is turned on.
20	PGND	Power ground pin. This pin becomes the return current path of the LDRV pin.